Hardware User Guide

Zipcores FMC-HPC Mezzanine Card

ZIP-FMC-HPC Rev. A.0
November 2025

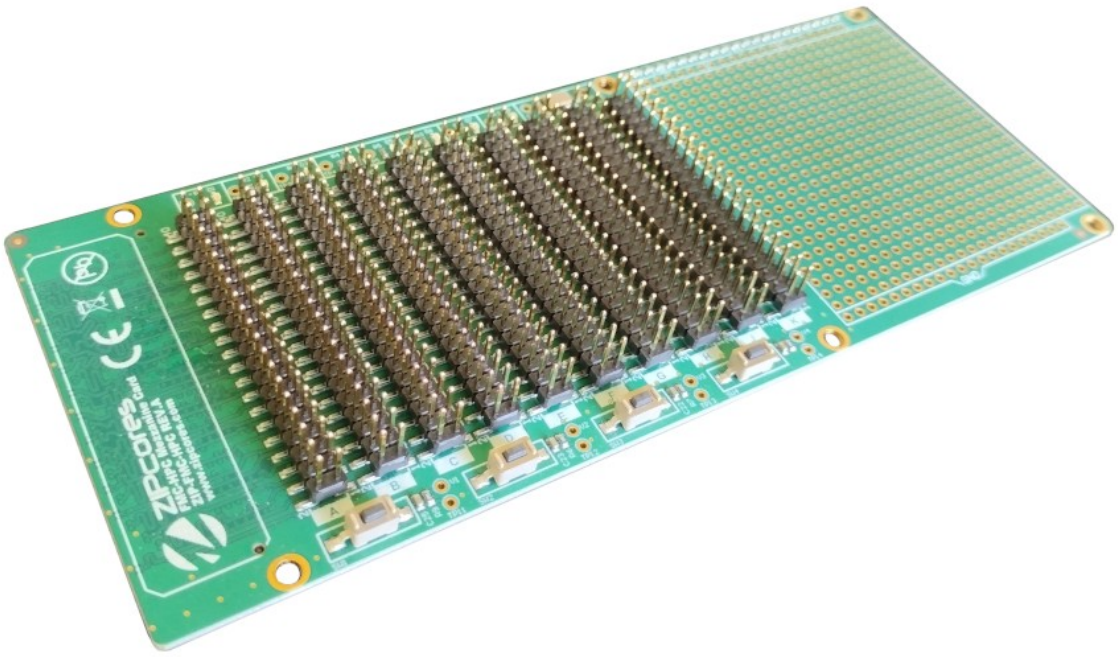

Table of Contents

Overview

Introduction

The Zipcores FMC-HPC Mezzanine card is a versatile FMC breakout-board and prototyping platform that conforms to the ANSI/VITA 57.1 FMC™ mezzanine standard. The card is compatible with a wide range of base-boards and FMC-compliant systems. Examples include evaluation boards from AMD® (Xilinx), Altera® (Intel), Microchip® (Microsemi), Avnet® and Digilent®. The card provides passive connectivity to all 400 signals on the FMC (HPC) connector via 10 x standard 0.100" pitch (2.54 mm) headers. This includes 80 x differential LVDS pairs (LA00:33, HA00:23, HB00:21) or 160 x single-ended signals or a mixture of both. All differential pairs are balanced for track length and impedance-matched for 100Ω LVDS termination. The ground pins of the FMC are also connected to an independent ground plane to offer the best possible signal integrity and noise immunity.

The card is ideal for the development high-speed LVDS and other high-speed differential interfaces such as those required in displays, cameras, image sensors, ADCs, DACs and general purpose serial connectivity. The FMC card also provides access to all 10 x Multi-Gigabit (MGT) transceiver pairs (DP0:9) and transceiver clocks permitting typical serial data rates from 3 to 5 Gbps per channel on even the most basic FPGA or SoC development boards. As such, this allows for potential data rates of up to 50 Gbps if all 10 channels are used.

Other features on the card include: I^2C, JTAG, power supplies, ground pins, 8 x indicator LEDs, 4 x push-button switches (with RC de-bouncing) and a 100 MHz clock oscillator. The LEDs, buttons and oscillator may be powered by either the VADJ or the 3.3V supply on the card. In this way, the components can be made compatible with the desired I/O voltage of the FPGA or SoC on the base-board. FMC power supplies are accessible as separate PCB through-hole vias on the card. All power pins are independently de-coupled with a 100nF capacitor to the ground plane.

Finally, the FMC-HPC card provides a standard pitch 0.100" (2.54 mm) prototyping area of 24 x 22 through-holes. This area is ideal for implementing custom circuitry and extending the functionality of the card for different user applications. Figures (1) and (2) show the general board layout and the distribution of main board components.

Board layout

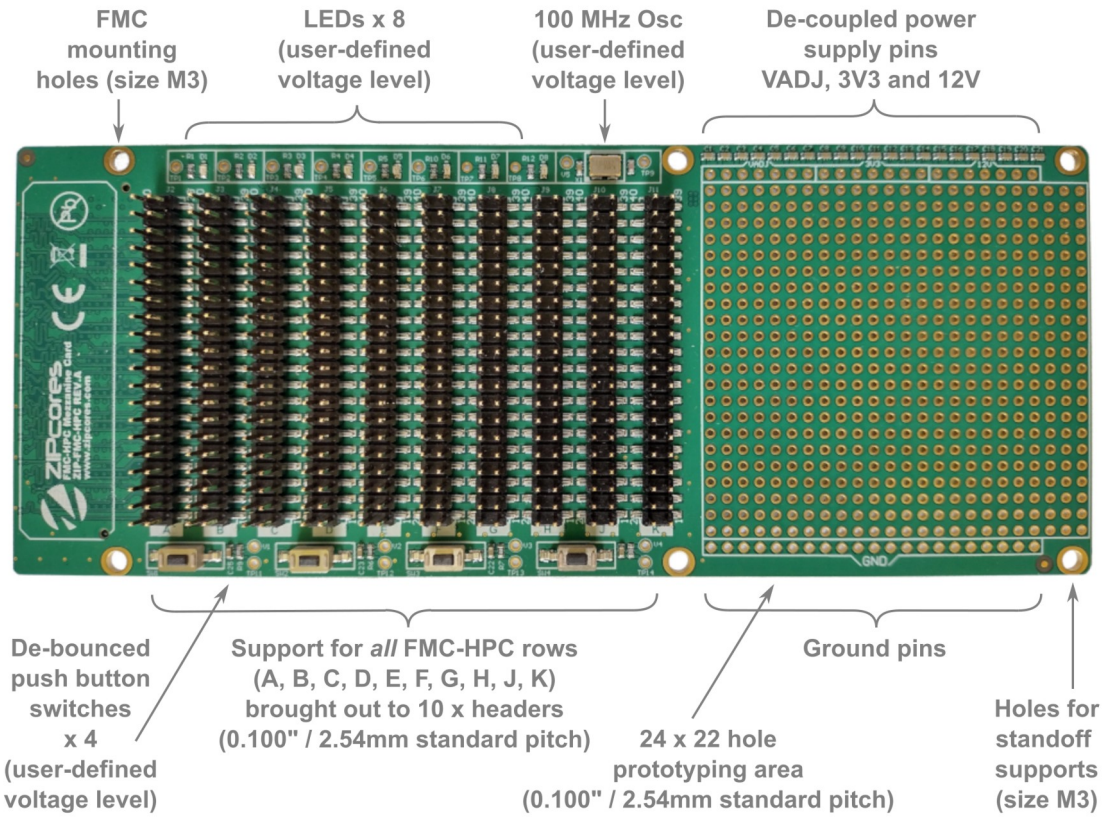

Figure 1: ZIP-FMC-HPC Rev. A board (top view)

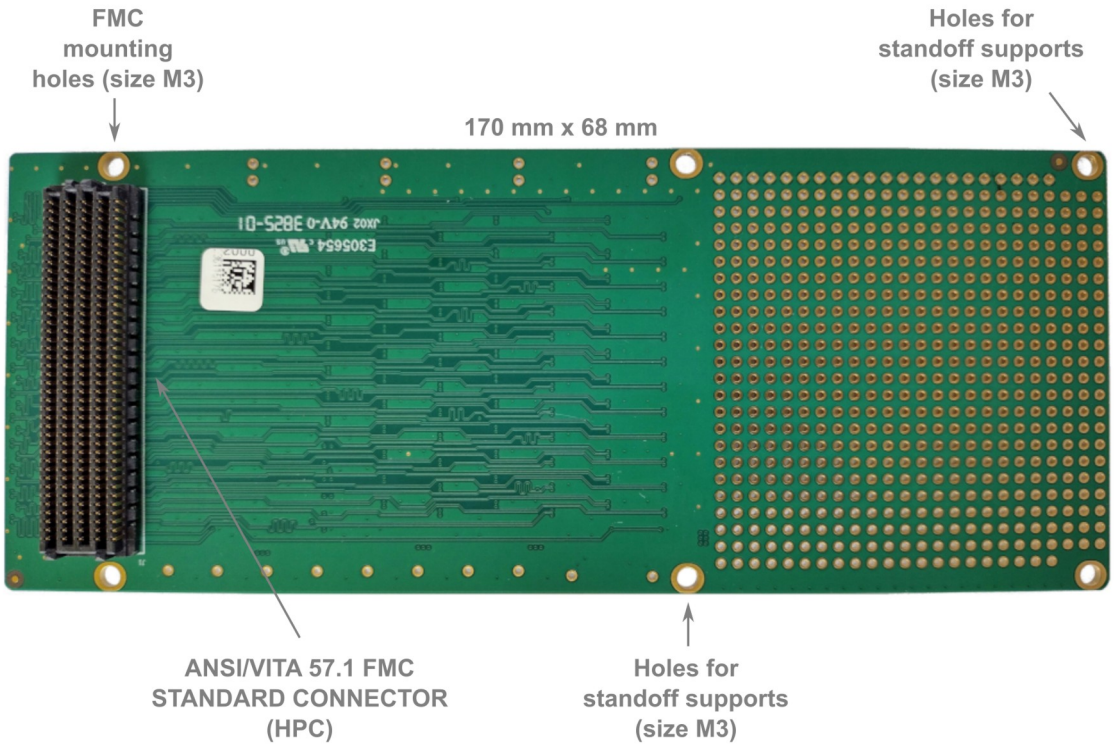

Figure 2: ZIP-FMC-HPC Rev. A board (bottom view)

Key features

- Standard ANSI/VITA 57.1 FMC™ HPC connector
- Also compatible with ANSI/VITA 57.4 FMC+ connector (but only HPC pins used and sits centrally in the FMC+)
- 10 x headers provide passive connectivity to all 400 pins on the FMC connector (rows A/B, C/D, E/F, G/H, J/K)
- All pin and through-hole spacings are standard 0.100” pitch or 2.54 mm
- Access to 34 x differential pairs LA[00:33] or 68 x single-ended signals or a mixture of both
- Access to 24 x differential pairs HA[00:23] or 48 x single-ended signals or a mixture of both
- Access to 22 x differential pairs HB[00:21] or 44 x single-ended signals or a mixture of both
- Access to all 10 x MGT transceiver pairs DP[0:9] including both MGT clocks (GBTCLK0 and GBTCLK1)
- All differential pairs routed with the same track lengths
- All differential signals impedance-matched for LVDS 100Ω termination
- Access to the I2C, JTAG and all other special-purpose signals on the HPC connector
- Access to the VADJ, 3.3V and 12V FMC power supplies
- Dimensions: 170 x 68 mm
- Separate VADJ, 3.3V, 12V and GND through-hole vias for powering custom circuitry
- All power pins (VADJ, 3.3V, and 12V) de-coupled to ground with 100 nF capacitors
- Separate PCB ground-plane for improved signal integrity and noise immunity
- Features large 24 x 22 prototyping area for custom circuitry and user-defined functions
- 8 x user LEDs with 332Ω series resistors to ground (with user-defined voltage input)
- 4 x user push-buttons with RC de-bouncing circuit (with user-defined voltage input)
- 100 MHz low-jitter single-ended clock oscillator (also with user-defined voltage supply)
- 2 x M3 mounting holes for securing the FMC connector
- 4 x M3 mounting holes for inserting standoff supports or spacers – ideal for stacking layers of custom circuitry
- Compatible with a wide range of FMC base-boards and FMC-compliant systems from many different manufacturers

Detailed description

FMC header connectors

The 400 x FMC (HPC) signals are routed to 10 (2 x 20) header connectors as shown in Figure (3) below. A separate 40-pin header is allocated to each row of the FMC connector such that row A maps to J2, row B maps to J3, row C maps to J4 etc. A full list of the FMC (HPC) connector pinouts are also given in Appendix B at the end of this document.

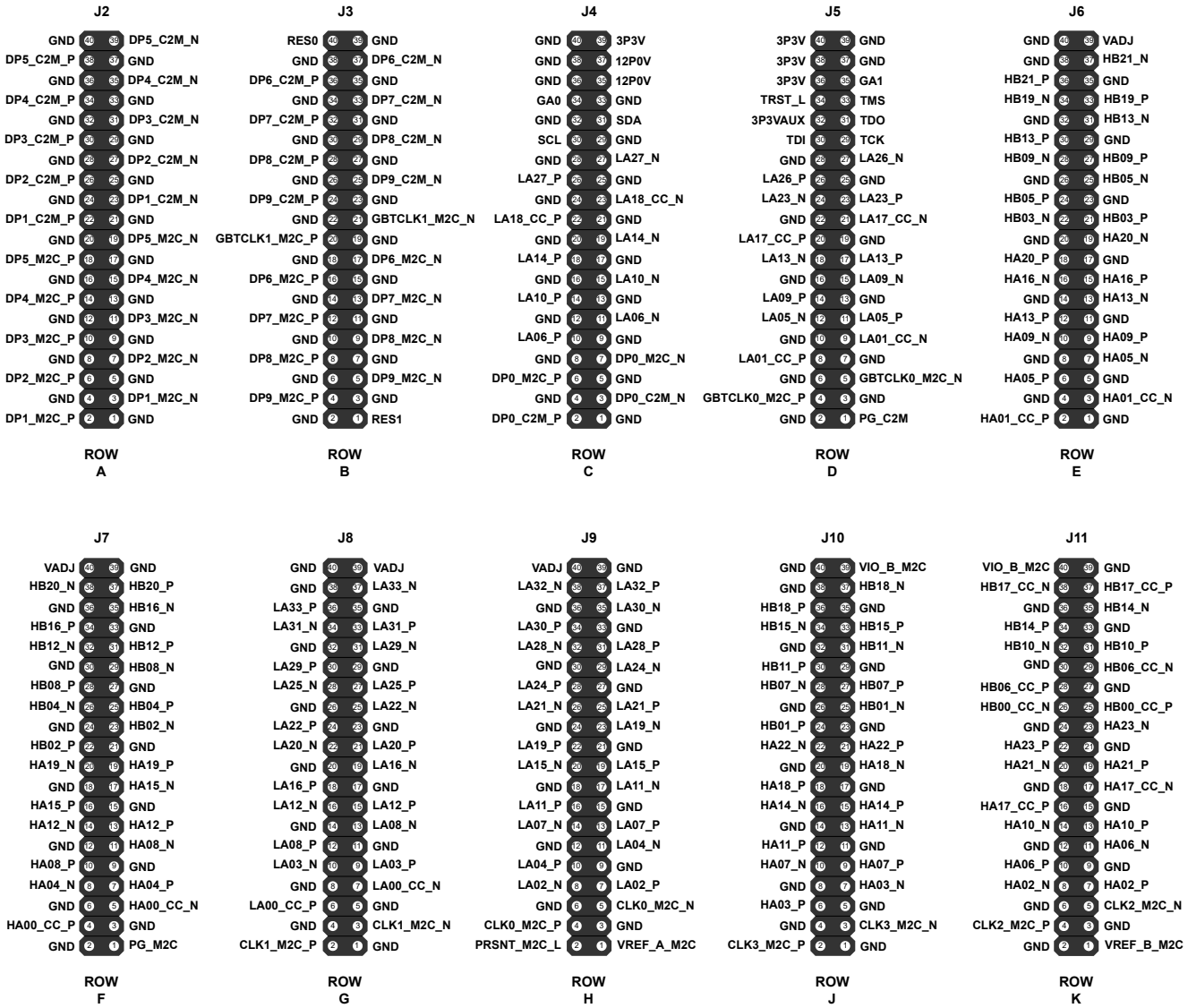

Figure 3: FMC signals mapped to 10 x 40-pin header connectors

User LEDs

The FMC card provides 8 x general purpose indicator LEDs. Each LED is in series with a 332Ω resistor to ground. The input to the LED circuit is a through-hole on the card that allows the LED to be driven using a simple hook-up wire or soldered connection (labelled TP1 to TP8). For instance, the LEDs may be driven by any of the general purpose I/O on the FMC headers. The maximum recommended driving voltage is 3.3V. Figure (4) below shows the LED circuit of which there are 8 in total.

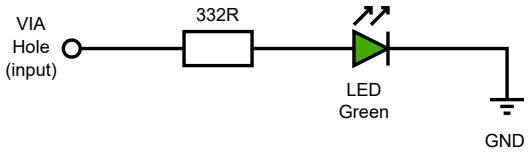

Figure 4: General purpose LED indicator circuit (active high LED on)

User push-button switches

The card features 4 x push-button switches for general purpose use. Each switch is de-bounced with a passive RC circuit. The switches are designed as active-low switches with a button press driving the output low. As with the LED circuits, the switch outputs must be connected using hook-up wire or a soldered connection.

The switches may be powered by either the VADJ or 3.3V supply on the card. Again, the switch power supply must be provided by a hook-up wire or soldered connection to the power vias. The power vias for each switch are labelled V1, V2, V3 and V4 on the FMC card. The switch outputs are labelled TP11, TP12, TP13 and TP14. Figure (5) shows the push-button circuit of which there are 4 in total.

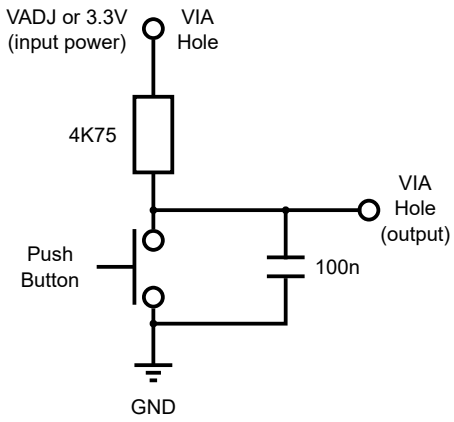

Figure 5: Push-button switches (active low button press)

User 100 MHz clock oscillator

A precision single-ended clock oscillator is provided on the board part number: SG-8018CB from EPSON. As with the other user circuits on the card, the IC power supply and output are connected using a through-hole via. The 100 MHz oscillator power supply voltage can be anything from 1.5 V to 3.3 V. This means that either the VADJ or 3.3V supply on the FMC card may be used to power the device. Figure (6) shows the circuit diagram of the oscillator.

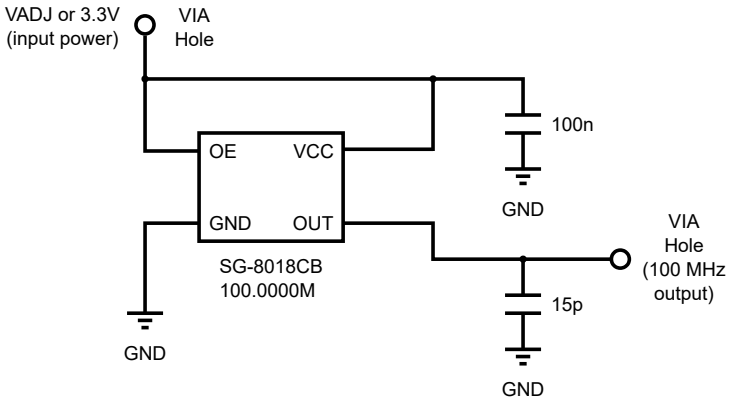

Figure 6: 100 MHz precision clock oscillator circuit

FMC power supplies

All the FMC standard power pins are made available on the FMC-HPC mezzanine card. As well as routing power to the header connectors, the card provides the VADJ, 3.3V and 12V power supplies as separate through-hole vias. These extra supplies are de-coupled with 100 nF capacitors to the ground plane. In addition to the separate power pins, a row of ground pins are provided on the card to allow for easy prototyping.

User prototyping area

The user prototyping area is a grid of 24 x 22 through-holes on the card. The prototyping area is idea for designing custom circuits and adding extra functionality to the FMC-card or main base-board. The area is large enough to support other small development boards and components, extra connectors or custom connectivity between external peripherals. The holes in the prototyping area are standard 0.100” pitch or 2.54 mm.

In addition, the card features 4 x M3 holes positioned in the four corners of the prototyping area. These may be used for standoff ‘legs’ to add support to the board when resting on the bench. They can also be used to add spacers to stack further boards above the FMC-HPC card if necessary.

ANSI/VITA 57.1 FMC™ connector

The mezzanine card uses a standard ANSI/VITA 57.1 FMC connector. The pinouts of the connector are configured with the High-Pin-Count (HPC) option occupying rows A/B, C/D, E/F, G/H and J/K allowing access to 400 pins. Although the pinouts are designed for the HPC connector, the mezzanine card is also compatible with the Low-Pin-Count connector (LPC) and the ANSI/VITA 57.4 FMC+ (plus) connectors.

Note that in the case of evaluation boards that feature the FMC+ connector, then the FMC-HPC sits centrally in the middle of the FMC+. The FMC+ is keyed such that the FMC-HPC will locate properly in the central position. As a general rule, all connectors that follow the FMC standard are upwardly and downwardly compatible. A detailed specification of the FMC connector may be found on the Samtec® website just here:

www.samtec.com/standards/vita/fmc

www.samtec.com/standards/vita/fmc-plus

The FMC standard connector is used in a wide selection of FPGA development boards from vendors such as AMD®, Altera®, Microchip®, Avnet® and Digilent®. AMD in particular have adopted the FMC standard in all their FPGA and SoC development boards. Appendix A gives some examples of compatible base-boards. More information can be found on the AMD website just here:

www.amd.com/en/search/adaptive-socs-and-fpgas/boards.html

Special design considerations when using the MGT (Multi-Gigabit) pins

The FMC-HPC mezzanine card has been specifically designed to take advantage of all 10 x Gbit transceiver pairs on the FMC connector. In particular, all the DP* differential pairs and GBTCLK* pairs have the exact same track lengths and maintain an inter-pair skew of less than 5ps. Typically, these transceiver pairs are connected to the high-speed SERDES resources on the host FPGA or SoC via the FMC connector. On most FPGAs, these pins are normally labelled as MGTTX* and MGTRX* for the serial transmitter and serial receiver pins respectively.

[***IMPORTANT***: *Given the very high serial rates supported by these pins, then it's important to use robust design techniques to avoid signal integrity issues and potential data loss. Special attention to grounding, impedance matching, signal termination, cable type, crosstalk, noise etc. are essential to achieve the best possible rates. In particular, a stable, low-jitter reference clock connected to the GBTCLK* pins is of critical importance*]

One useful tool when using the AMD devices is to use the Integrated Bit Error Ratio Tester (IBERT) which is available with the Vivado design suite. This is a tool that allows in-system serial I/O validation and debug for all the MGT resources on the FPGA or SoC[1]. As an example, the FMC-HPC card was attached to the Genesys 2 evaluation board from Digilent®. This board features a Kintex 7 FPGA that supports all 10 x DP pairs on the FMC-HPC. In particular, the DP transmit and receive pins were connected in loopback configuration such that:

DP0_C2M_P/N → DP0_M2C_P/N, DP1_C2M_P/N → DP1_M2C_P/N, … DP9_C2M_P/N → DP9_M2C_P/N.

In addition, a 125 MHz low-jitter clock source was used for the GBTCLK0 and GBTCLK1 reference clock inputs. Figure (7) below shows the results of the serial I/O analysis in Vivado with all 10 transceivers working simultaneously with a combined data rate of 31.25 Gbps.

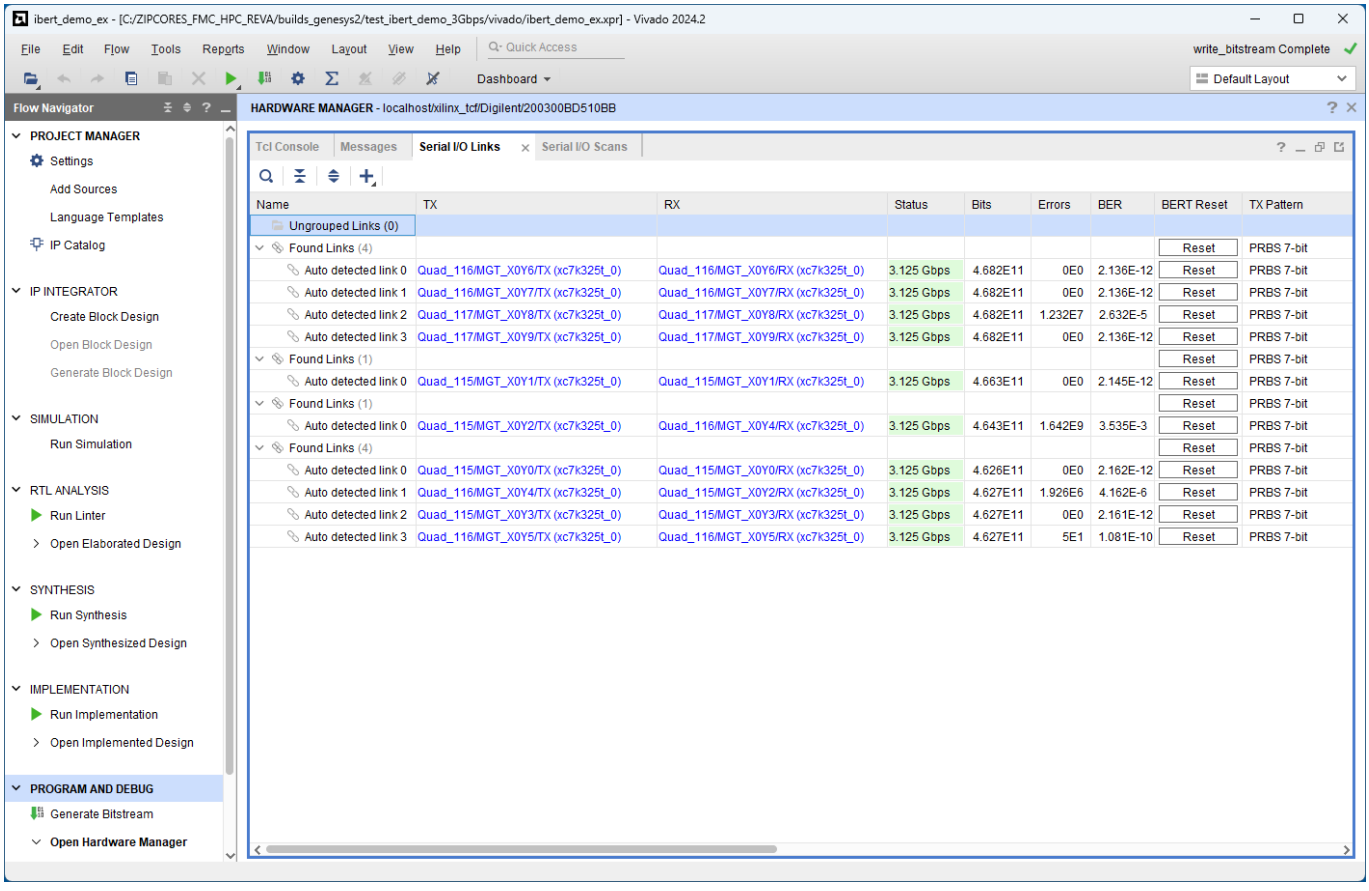

Figure 7: Serial I/O analysis of all 10 MGT links in Vivado using (IBERT)

1 For more information, please refer to the AMD website and search for the IBERT tutorial.

Appendices

Appendix A: Examples of supported base-boards with FMC connectors

[***IMPORTANT**: Please note that this is only an example list of evaluation boards based on AMD® products. Generally, **ANY** evaluation board that features an FMC connector will be compatible with our FMC-HPC mezzanine card. However, the number of FMC user pins available will be determined by the base-board connectivity. As such, please refer to the evaluation board datasheets and schematics for reference*]

ZYNQ-BASED SYSTEMS

Base-board name	***No. of FMC connectors***	***VADJ options***
AMD Zynq™ 7000 SoC ZC702 Evaluation Kit	2 x LPC	1.8V, 2.5V, 3.3V
AMD Zynq™ 7000 SoC ZC706 Evaluation Kit	1 x HPC + 1 x LPC	1.8V, 2.5V, 3.3V

GENERAL FPGA-BASED SYSTEMS

Base-board name	***No. of FMC connectors***	***VADJ options***
AMD Spartan™ 7 FPGA SP701 Evaluation Kit	1 x LPC	1.8V, 2.5V, 3.3V
AMD Artix™ 7 FPGA AC701 Evaluation Kit	1 x HPC	1.8V, 2.5V, 3.3V
AMD Kintex™ 7 FPGA KC705 Evaluation Kit	1 x HPC + 1 x LPC	1.8V, 2.5V, 3.3V
AMD Virtex™ 7 FPGA VC707 Evaluation Kit	2 x HPC	1.2V, 1.5V, 1.8V
AMD Virtex™ 7 FPGA VC709 Connectivity Kit	1 x HPC	1.8V fixed
AMD Virtex™ 7 FPGA VC7203 Characterization Kit	3 x HPC	1.8V fixed
AMD Virtex™ 7 FPGA VC7215 Characterization Kit	2 x HPC	1.8V fixed
AMD Virtex™ 7 FPGA VC7222 Characterization Kit	2 x HPC	1.8V fixed

ULTRASCALE-BASED SYSTEMS

Base-board name	***No. of FMC connectors***	***VADJ options***
AMD Kintex™ UltraScale™ FPGA KCU105 Evaluation Kit	1 x HPC + 1 x LPC	1.2V, 1.5V, 1.8V
AMD Kintex™ UltraScale+™ FPGA KCU116 Evaluation Kit	1 x HPC	1.8V fixed
AMD Virtex™ UltraScale™ FPGA VCU108 Evaluation Kit	2 x HPC	1.2V, 1.5V, 1.8V
AMD Virtex™ UltraScale™ FPGA VCU110 Development Kit	2 x HPC	1.2V, 1.5V, 1.8V
AMD Virtex™ UltraScale+™ FPGA VCU118 Evaluation Kit	1 x HPC	1.2V, 1.5V, 1.8V
AMD Virtex™ UltraScale™ FPGA VCU1287 Characterization Kit	3 x HPC	1.8V fixed

ZYNQ ULTRASCALE-BASED SYSTEMS

Base-board name	***No. of FMC connectors***	***VADJ options***
AMD Zynq™ UltraScale+™ MPSoC ZCU102 Evaluation Kit	2 x HPC	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ MPSoC ZCU104 Evaluation Kit	1 x LPC	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ MPSoC ZCU106 Evaluation Kit	2 x HPC	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ RFSoC ZCU111 Evaluation Kit	1 x FMC+	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ RFSoC ZCU208 Evaluation Kit	1 x FMC+	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ RFSoC ZCU216 Evaluation Kit	1 x FMC+	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ RFSoC ZCU670 Evaluation Kit	1 x FMC+	1.2V, 1.5V, 1.8V
AMD Zynq™ UltraScale+™ RFSoC ZCU1275 Characterization Kit	1 x HPC + 1 x LPC	1.8V fixed

VERSAL-BASED SYSTEMS

Base-board name	***No. of FMC connectors***	***VADJ options***
AMD Versal™ Prime Series VMK180 Evaluation Kit	2 x FMC+	1.2V, 1.5V
AMD Versal™ AI Core Series VCK190 Evaluation Kit	2 x FMC+	1.2V, 1.5V
AMD Versal™ HBM Series VHK158 Evaluation Kit	1 x FMC+	1.0V, 1.2V, 1.5V
AMD Versal™ Premium Series VPK120 Evaluation Kit	1 x FMC+	1.2V, 1.5V
AMD Versal™ Premium Series VPK180 Evaluation Kit	1 x FMC+	1.0V, 1.2V, 1.5V
AMD Versal™ AI Edge Series VEK280 Evaluation Kit	1 x FMC+	1.5V fixed
AMD Versal™ AI Edge Series VEK385 Evaluation Kit	1 x FMC+	1.5V fixed

Appendix B: VITA 57.1 FMC™ (HPC) Connector pinouts

Figure 8 shows the full FMC (HPC) pin connections on the mezzanine card.

[***NOTE**: Unlike the LA and HA I/O pins, the HB I/O pins are not powered by default. If the user wishes to use these pins, then the I/O voltage must be supplied externally via the **VIO_B_M2C pin**. Typically, this may be connected to the VADJ or 3.3V power supply on the mezzanine card. Bear in mind, however, that the VIO_B_M2C voltage must match the voltage of the FPGA or SoC bank that it's connected to. If not, then the user risks damage to the host device]*

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Figure 8: Signal connectivity on the FMC (HPC) connector

Appendix C: List of supporting design files

The FMC-HPC card has a number of supporting design files and documents that may be downloaded from the Zipcores website at: www.zipcores.com/downloads.html. Most of the design files are source-code files that are required for building and running the example demo as described in Appendix D. A list of these files and a brief description is given below:

Folders and important files	***Description***
docs/ zip_fmc_hpc_user_guide.pdf zip_fmc_hpc_safety_info.pdf zip_fmc_hpc_schematic.pdf zip_fmc_hpc_assembly.pdf zip_fmc_hpc_gerber.pdf zip_fmc_hpc_bom.pdf	Folder containing various design documents. FMC-HPC hardware user guide (this document). FMC-HPC regulatory compliance and safety information. FMC-HPC design schematics. FMC-HPC assembly drawings. FMC-HPC gerber summary. FMC-HPC bill of materials.
const/ fmc_hpc_top.xdc	Folder containing the physical constraints for the AMD Vivado project. Example master 'XDC' file that defines all the top-level pinouts and design constrains for the FMC-HPC card when connected to the base-board. This file may be adapted for use with all AMD FPGAs.
vivado/ FMC_HPC_TOP.xpr	This folder contains the Vivado project environment for the demo. Vivado project setup file (double click to invoke project).
vhdl/ fmc_hpc_top.vhd fmc_hpc_top_bench.vhd	This folder contains the top-level VHDL source-code files for the example demo. The main top-level files are: The top-level synthesizable component. The top-level testbench for the VHDL simulation.
modelsim/ FMC_HPC_TOP.mpf	This folder contains the Modelsim® simulation environment in order to run a VHDL hardware simulation of the demo. You will need to obtain a copy of Mentor Graphics Modelsim in order to use these files. Modelsim project setup file (double click to invoke project).
misc/	This folder contains various data sheets, schematics and design notes for the FMC-HPC card.

Zipcores offers a wide range of IP Cores and custom solutions for the ZIP-FMC-HPC mezzanine card. As well as AMD® devices, we can provide IP for other FPGAs or SoCs on request. If you have a specific requirement or simply want to discuss a potential solution then please get in touch. Further details may be found by visiting our website or contacting us at: www.zipcores.com/help.php.

Appendix D: Running the example demo

A simple demo is provided to get started with the ZIP-FMC-HPC mezzanine card. The demo generates a series of pulses on the output pairs of the card. The pulses are at LVCMOS25 levels and are generated such that the LA*_P/N, HA*_P/N and HB*_P/N signals are inverted versions of each other. The period of each pulse is also defined according to the pin-number. For instance, the LA00_P/N has a 1.0us period, LA01_P/N has a 1.1us period, LA02_P/N has a 1.2us period etc. In this way, it's easy to locate each pin on the card by its waveform. In order to run the demo, the following basic lab setup is recommended:

- Suitable oscilloscope for measuring the output pulse waveforms (E.g. 100 MHz B/W and 2 GS/s)
- Hook-up wire to easily connect the scope probe to the header pins
- For testing the HB[00:21] pins then remember to connect the 'VIO_B_M2C' pin to the VADJ supply
- A suitable development board based on an AMD® device to connect the ZIP-FMC-HPC card. For this example we chose the Genesys 2 board from Digilent® which offers full FMC (HPC) connectivity using a Kintex 7 FPGA. (Note: other base boards may be supported on request. Please contact us for more details).
- Spacers (10 mm) and screws (size M2.5) in order to secure the FMC-HPC card to the base-board
- AMD Vivado Software. (Note: the demo was based on Vivado rev. 2024.2, but any version of Vivado would work)
- USB cable for programming the Genesys 2 board

Once the equipment is set up then the user should invoke the Vivado software and load the project environment 'FMC_HPC_TOP.xpr' which is in the 'vivado' folder as described in Appendix C above. The same directory structure should be maintained so that the links and dependencies are correctly resolved. If the project loads correctly, the initial project layout should look something like Figure (9) below:

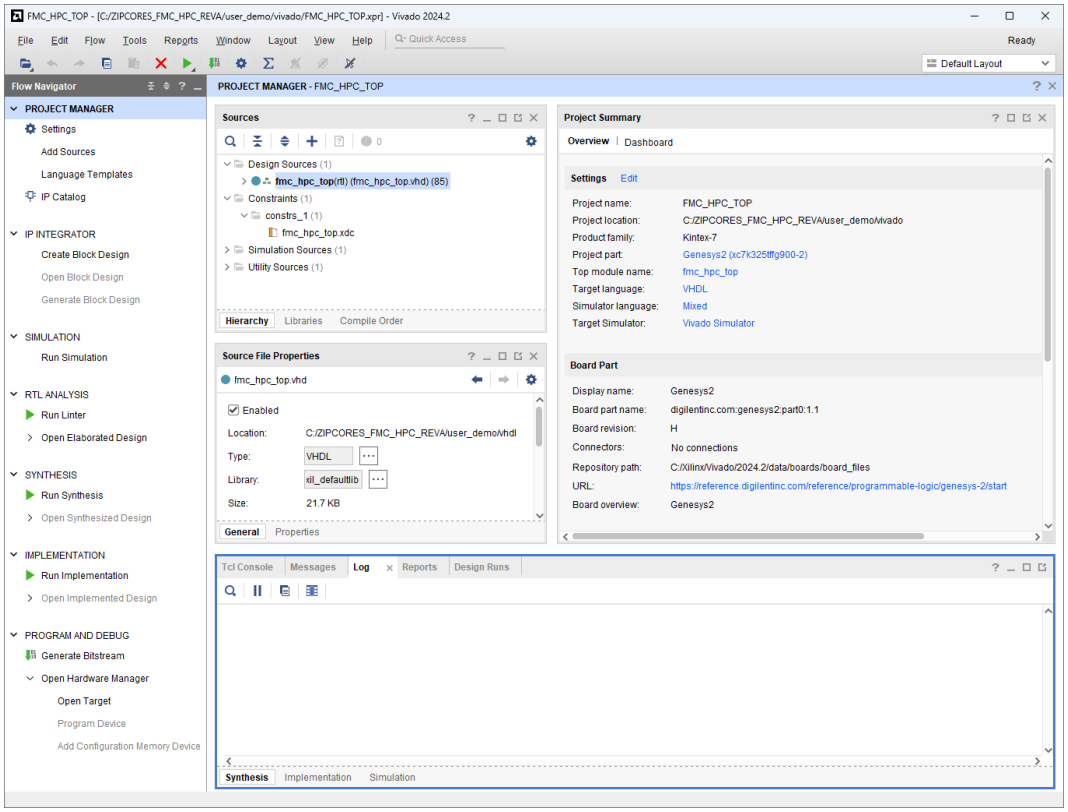

Figure 9: Initial Vivado project startup for demo

Once the project is loaded then the next step is to generate the bitstream for programming the FPGA. Click on 'Generate Bitstream' in the project manager window and wait for the compile process to complete. After the bitstream is generated then open the hardware manager and program the Genesys 2 board.

Figure (10) below shows an example bench setup with the LA32_P and LA32_N pins (H37/H38) being probed on the FMC header connector. Notice that the pulse period is exactly 4.2 us and the pulse trains are inverted versions of each other.

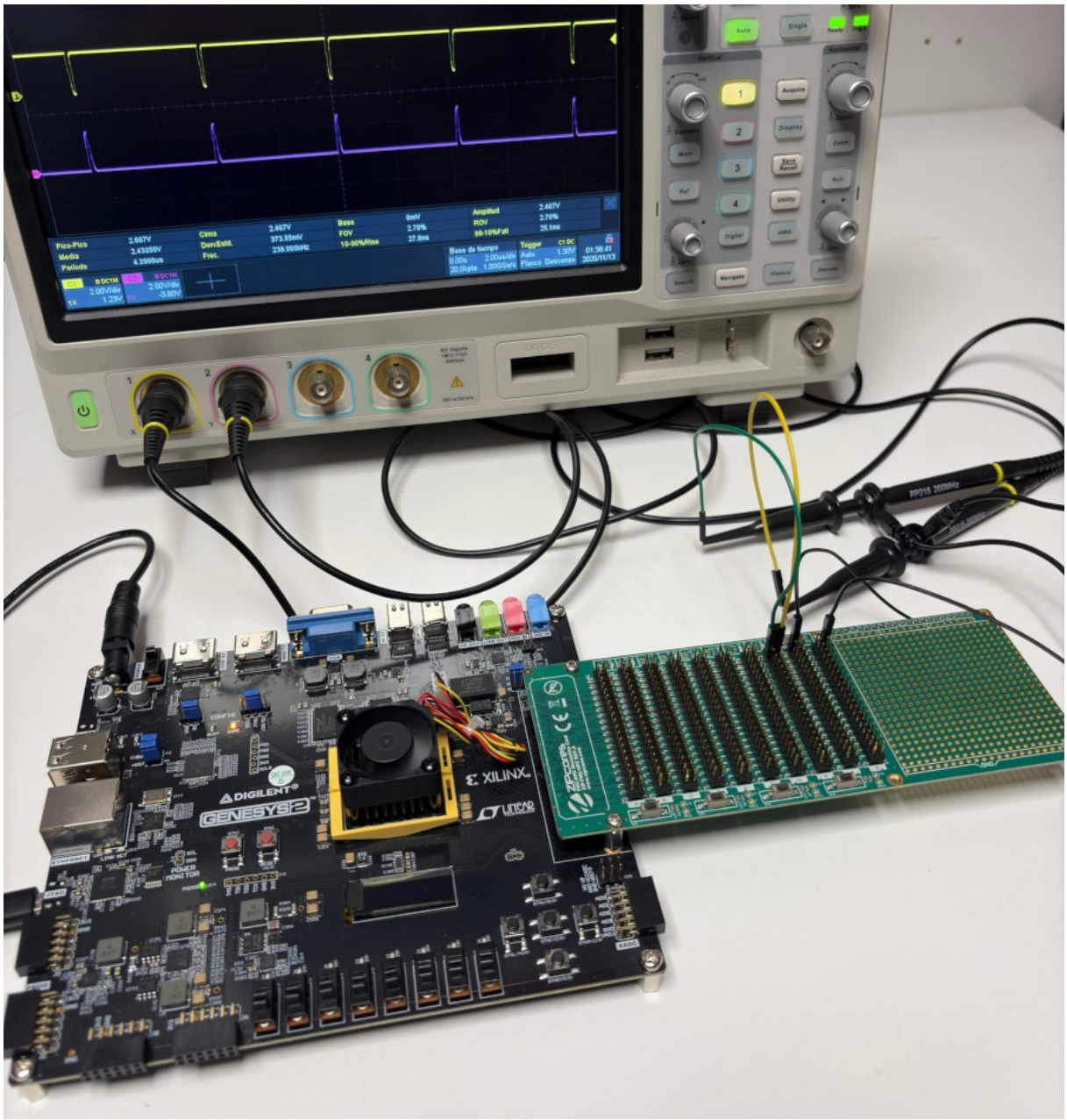

Figure 10: Bench setup showing FMC-HPC card connected to the Genesys 2 board

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