

Description

The TSV61x family of single and dual operational amplifiers offers low voltage, low power operation, and rail-to-rail input and output.

The devices also feature an ultra-low input bias current as well as a low input offset voltage.

The TSV61x have a gain bandwidth product of 120 kHz while consuming only 10 μ A at 5 V.

These features make the TSV61x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

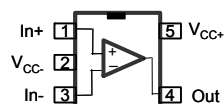
Applications

- Battery-powered applications
- Smoke detectors
- Proximity sensors
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

Features

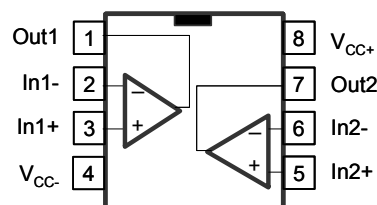
- Rail-to-rail input and output
- Low power consumption: 10 μ A typ at 5 V
- Low supply voltage: 1.5 to 5.5 V
- Gain bandwidth product: 120 kHz typ
- Unity gain stable
- Low input offset voltage: 800 μ V max (A version)
- Low input bias current: 1 pA typ
- Temperature range: -40 to 85 $^{\circ}$ C

**TSV611ILT/TSV611AILT/
TSV611AICT**



SOT23-5/SC70-5

TSV612IDT/TSV612AIDT



SOP-8

Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	
V_{in}	Input voltage ⁽³⁾	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
T_{stg}	Storage temperature	-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient ^{(4) (5)}		°C/W
	SC70-5	205	
	SOT23-5	250	
	SOP8	125	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁶⁾	4	kV
	MM: machine model ⁽⁷⁾	200	V
	CDM: charged device model ⁽⁸⁾	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC} - V_{in} must not exceed 6 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100 pF discharged through a 1.5 k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{oper}	Operating free air temperature range	-40 to 85	°C

Electrical characteristics

Table 3. Electrical characteristics at $V_{CC+} = 1.8$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V _{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV
		T _{min.} < T _{op} < T _{max.} TSV61x T _{min.} < T _{op} < T _{max.} TSV61xA			5 2	
ΔV _{io} /ΔT	Input offset voltage drift			2		μV/°C
I _{io}	Input offset current (V _{out} = V _{cc} /2)			1	10 ⁽¹⁾	pA
		T _{min.} < T _{op} < T _{max.}		1	100	
I _{ib}	Input bias current (V _{out} = V _{cc} /2)			1	10 ⁽¹⁾	pA
		T _{min.} < T _{op} < T _{max.}		1	100	
CMR	Common mode rejection ratio 20 log (ΔV _{ic} /ΔV _{io})	0 V to 1.8 V, V _{out} = 0.9 V	55	71		dB
		T _{min.} < T _{op} < T _{max.}	53			
A _{vd}	Large signal voltage gain	R _L = 10 kΩ, V _{out} = 0.5 V to 1.3 V	78	83		dB
		T _{min.} < T _{op} < T _{max.}	74			
V _{OH}	High level output voltage (V _{OH} = V _{CC} - V _{out})	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		4	35 50	mV
V _{OL}	Low level output voltage	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		7	35 50	
I _{out}	Isink	V _O = 1.8 V T _{min.} < T _{op} < T _{max.}	9 9	13		mA
	Isource	V _O = 0 V T _{min.} < T _{op} < T _{max.}	8 8	10		
I _{CC}	Supply current (per operator)	No load, V _{out} = V _{cc} /2	6.5	9	12	μA
		T _{min.} < T _{op} < T _{max.}	6		12.5	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 20 pF		100		kHz
φ _m	Phase margin			60		Degrees
G _m	Gain margin			9.5		dB
SR	Slew rate	R _L = 10 kΩ, C _L = 20 pF, V _{out} = 0.5 V to 1.3 V		0.03		V/μs

Table 3. Electrical characteristics at $V_{CC+} = 1.8$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, and R_L connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f = 1$ kHz		110		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	$F_{in} = 1$ kHz, $A_v = 1$, $V_{out} = 1$ V _{pp} , $R_L = 100$ k Ω , BW = 22 kHz		0.07		%

1. Guaranteed by design.

Table 4. Electrical characteristics at $V_{CC+} = 3.3$ V, $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
DC performance						
V _{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV
		T _{min} <T _{op} <T _{max} TSV61x T _{min} <T _{op} <T _{max} TSV61xA			5 2	
ΔV _{io} /ΔT	Input offset voltage drift			2		μV/°C
I _{io}	Input offset current			1	10 ⁽¹⁾	pA
		T _{min.} < T _{op} < T _{max.}		1	100	
I _{ib}	Input bias current			1	10 ⁽¹⁾	pA
		T _{min.} < T _{op} < T _{max.}		1	100	
CMR	Common mode rejection ratio 20 log (ΔV _{ic} /ΔV _{io})	0 V to 3.3 V, V _{out} = 1.75 V	61	76		dB
		T _{min.} < T _{op} < T _{max.}	58			
A _{vd}	Large signal voltage gain	R _L = 10 kΩ, V _{out} = 0.5 V to 2.8 V	85	92		dB
		T _{min.} < T _{op} < T _{max.}	83			
V _{OH}	High level output voltage (V _{OH} = V _{CC} - V _{out})	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		5	35 50	mV
V _{OL}	Low level output voltage	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		10	35 50	
I _{out}	Isink	V _o = V _{CC} T _{min.} < T _{op} < T _{max.}	37 35	44		mA
	Isource	V _o = 0 V T _{min.} < T _{op} < T _{max.}	32 30	38		
I _{CC}	Supply current (per operator)	No load, V _{out} = V _{CC} /2	6.5	9.5	12.5	μA
		T _{min.} < T _{op} < T _{max.}	6		13	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 20 pF		110		kHz
φ _m	Phase margin			60		Degrees
G _m	Gain margin			9.5		dB
SR	Slew rate	R _L = 10 kΩ, C _L = 20 pF, V _{out} = 0.5V to 2.8V		0.035		V/μs
e _n	Equivalent input noise voltage	f = 1 kHz		110		$\frac{nV}{\sqrt{Hz}}$

1. Guaranteed by design.

Table 5. Electrical characteristics at $V_{CC+} = 5$ V, $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit	
DC performance							
V _{io}	Offset voltage	TSV61x TSV61xA			4 0.8	mV	
		T _{min} <T _{op} <T _{max} TSV61x T _{min} <T _{op} <T _{max} TSV61xA			5 2		
ΔV _{io} /ΔT	Input offset voltage drift			2		μV/°C	
I _{io}	Input offset current			1	10 ⁽¹⁾	pA	
		T _{min.} < T _{op} < T _{max.}		1	100		
I _{ib}	Input bias current			1	10 ⁽¹⁾		100
		T _{min.} < T _{op} < T _{max.}		1	100		
CMR	Common mode rejection ratio 20 log (ΔV _{ic} /ΔV _{io})	0 V to 5 V, V _{out} = 2.5 V	64	80		dB	
		T _{min.} < T _{op} < T _{max.}	63				
SVR	Supply voltage rejection ratio 20 log (ΔV _{cc} /ΔV _{io})	V _{cc} = 1.8 to 5 V	76	93			
		T _{min.} < T _{op} < T _{max.}	74				
A _{vd}	Large signal voltage gain	R _L = 10 kΩ, V _{out} = 0.5 V to 4.5 V	88	93			
		T _{min} <T _{op} <T _{max}	85				
V _{OH}	High level output voltage (V _{OH} = V _{CC} - V _{out})	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		7	35 50	mV	
V _{OL}	Low level output voltage	R _L = 10 kΩ T _{min.} < T _{op} < T _{max.}		16	35 50		
I _{out}	Isink	V _o = V _{CC} T _{min.} < T _{op} < T _{max.}	52 42	57		mA	
	Isource	V _o = 0 V T _{min.} < T _{op} < T _{max.}	58 49	63			
I _{CC}	Supply current (per operator)	No load, V _{out} = V _{CC} /2	7.5	10.5	14	μA	
		T _{min.} < T _{op} < T _{max.}	7		15		
AC performance							
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 20 pF		120		kHz	
φ _m	Phase margin			62		Degrees	
G _m	Gain margin			10		dB	
SR	Slew rate	R _L = 10 kΩ, C _L = 20 pF, V _{out} = 0.5V to 4.5V		0.04		V/μs	

Table 5. Electrical characteristics at $V_{CC+} = 5$ V, $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, R_L connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f = 1$ kHz		105		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	$F_{in} = 1$ kHz, $A_v = 1$, $V_{out} = 1$ V _{pp} , $R_L = 100$ k Ω , BW = 22kHz		0.02		%

1. Guaranteed by design.

Figure 1. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

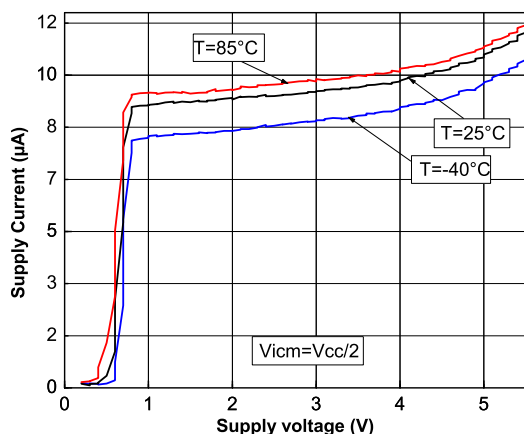


Figure 2. Output current vs. output voltage at $V_{CC} = 1.5$ V

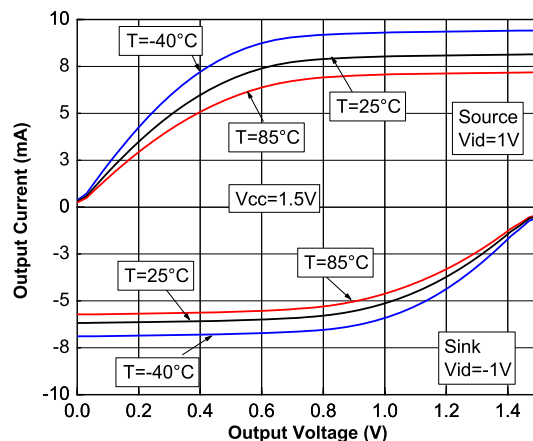


Figure 3. Output current vs. output voltage at $V_{CC} = 5$ V

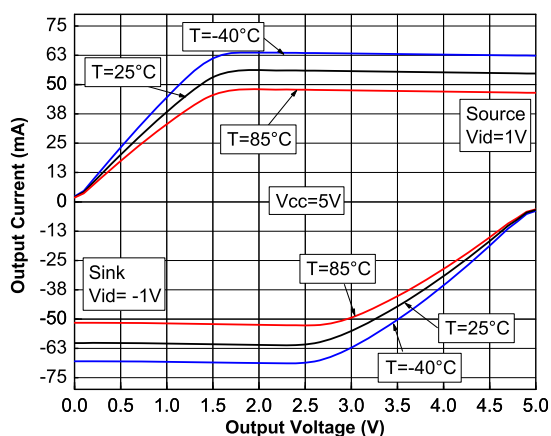


Figure 4. Voltage gain and phase vs. frequency at $V_{CC} = 1.5$ V

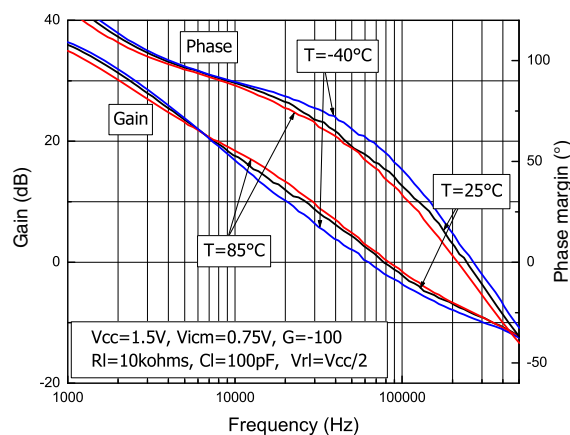


Figure 5. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V

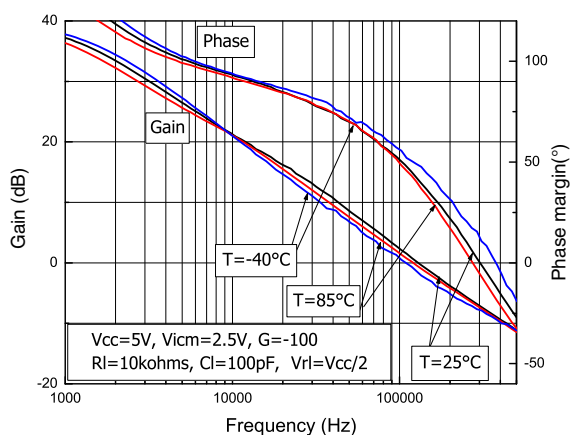


Figure 6. Phase margin vs. output current

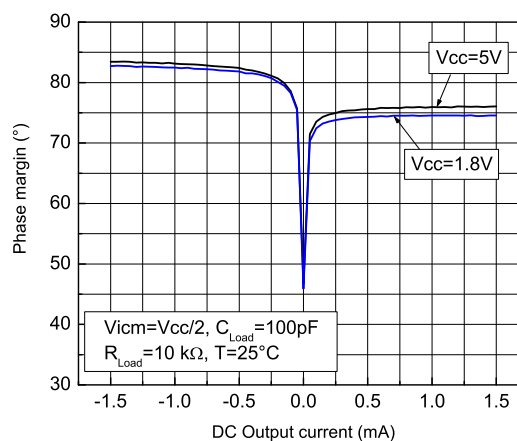


Figure 7. Positive slew rate vs. time, $V_{CC} = 1.5$ V,
 $C_{Load} = 100$ pF, $R_{Load} = 10$ k Ω

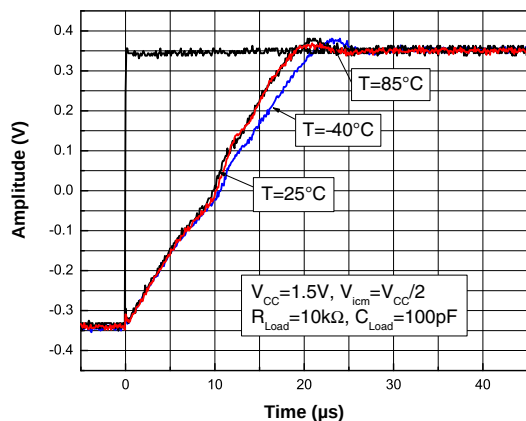


Figure 8. Negative slew rate vs. time, $V_{CC} = 1.5$ V,
 $C_{Load} = 100$ pF, $R_{Load} = 10$ k Ω

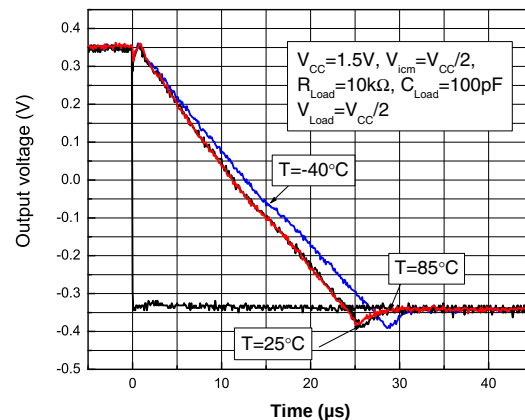


Figure 9. Positive slew rate vs. time, $V_{CC} = 5.5$ V,
 $C_{Load} = 100$ pF, $R_{Load} = 100$ k Ω

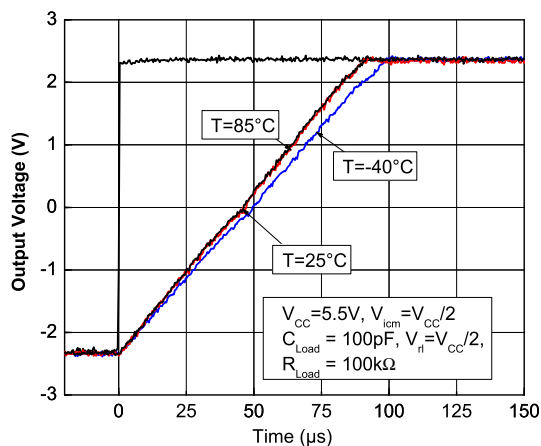


Figure 10. Negative slew rate vs. time, $V_{CC} = 5.5$ V,
 $C_{Load} = 100$ pF, $R_{Load} = 100$ k Ω

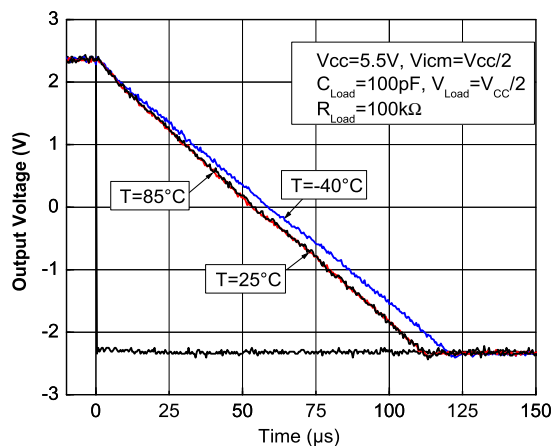


Figure 11. Slew rate vs. supply voltage

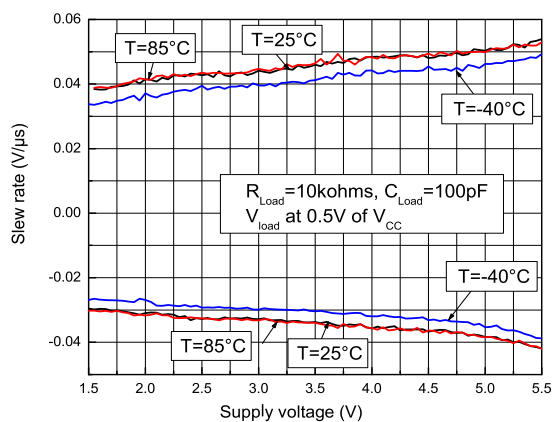


Figure 12. Noise vs. frequency at $V_{CC} = 5$ V

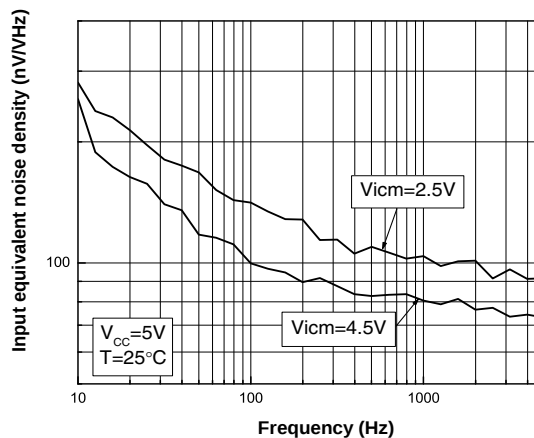


Figure 13. Distortion + noise vs. frequency

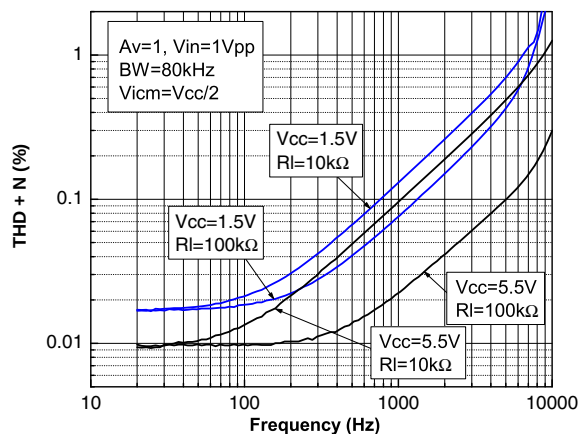


Figure 14. Distortion + noise vs. output voltage

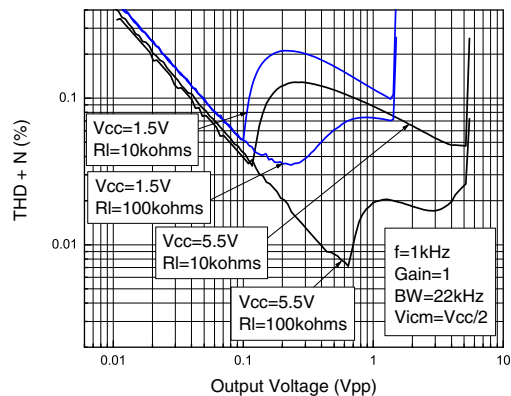


Figure 15. Voltage gain and phase vs. frequency at $V_{CC} = 1.8$ V (based on simulation results)

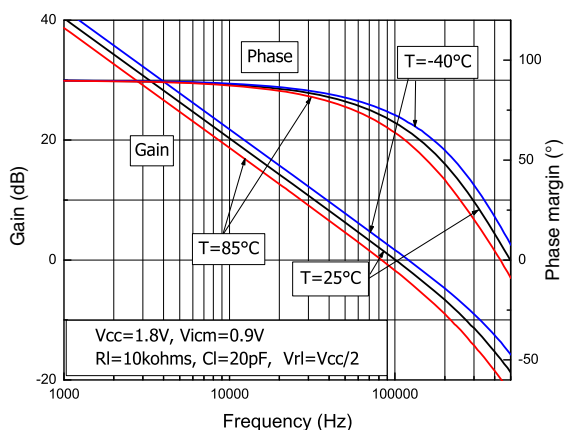


Figure 16. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V (based on simulation results)

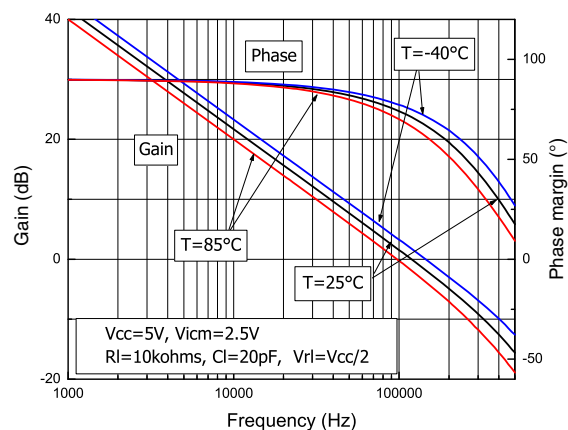


Figure 17. Input offset voltage vs input common mode at $V_{CC} = 1.5$ V

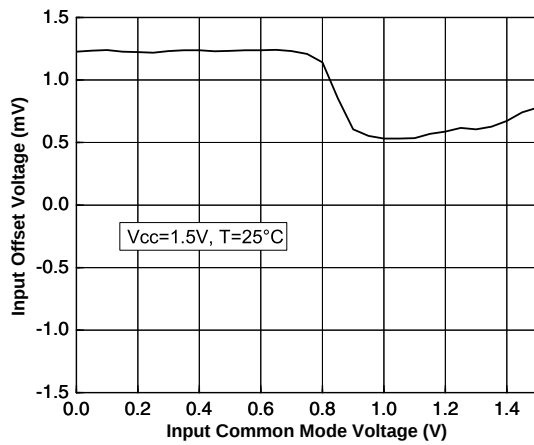
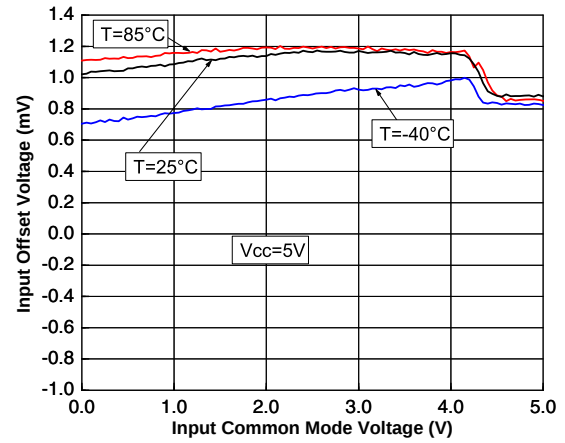


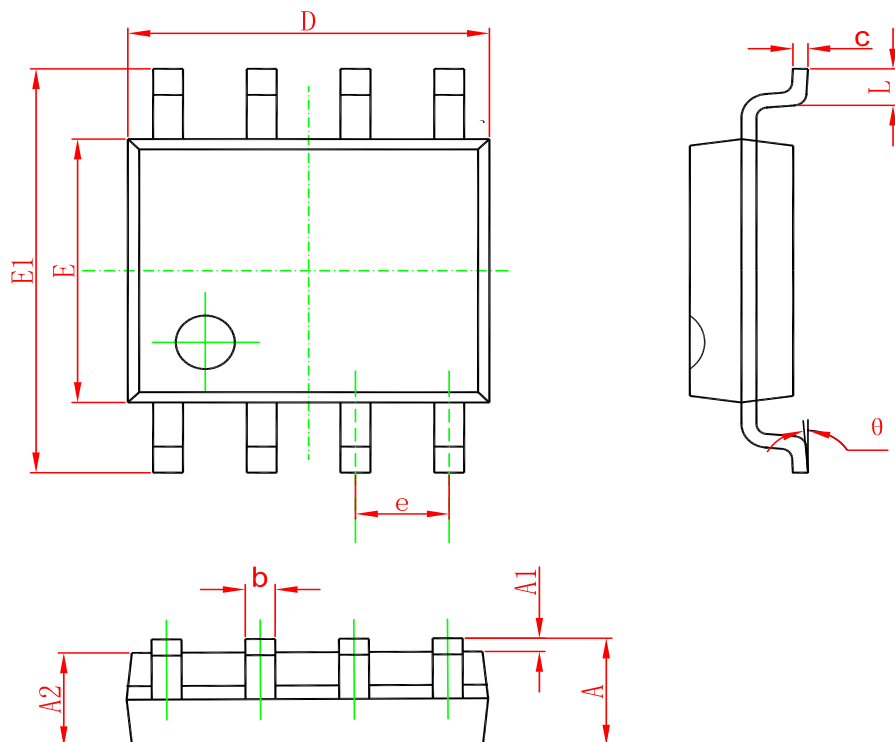
Figure 18. Input offset voltage vs input common mode at $V_{CC} = 5$ V



The device is guaranteed without phase reversal.

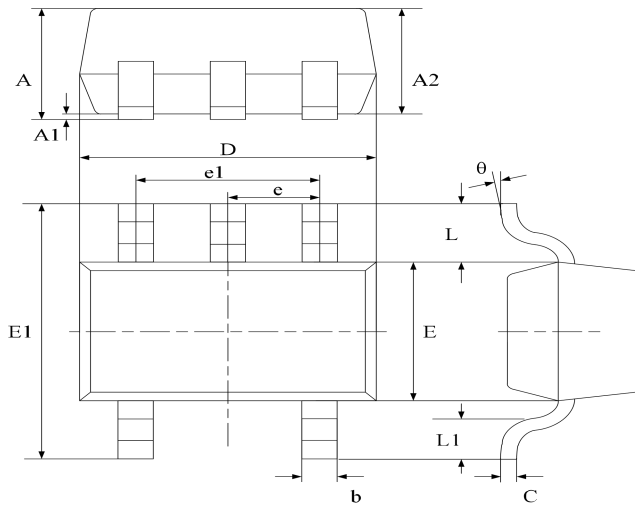
Package Dimension

SOP-8



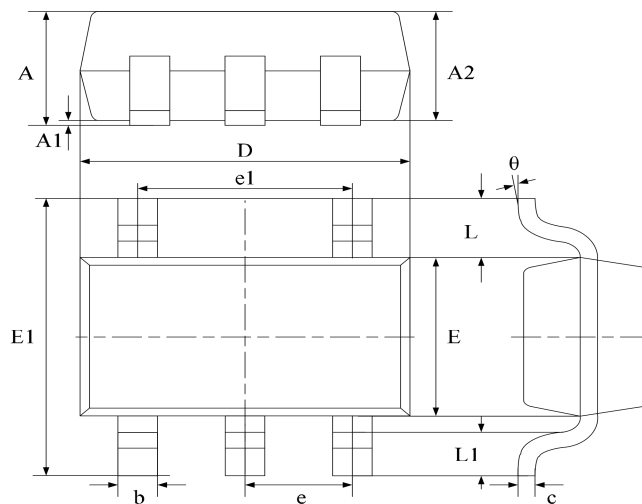
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SC70-5 (SOT353)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	1.8500	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 typ.		0.037 typ.	
e1	1.900 typ.		0.078 typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW TSV611ILT	SOT23-5	3000	Tape and reel	K12 U
UMW TSV611AILT	SOT23-5	3000	Tape and reel	K11 U
UMW TSV611AICT	SC70-5	3000	Tape and reel	K11 U
UMW TSV612IDT	SOP-8	2500	Tape and reel	V612I
UMW TSV612AIDT	SOP-8	2500	Tape and reel	V612AI

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[TP1562AL1-VR](#) [HT324ARQZ](#) [IL324DT](#) [RS724XP-Q1](#) [CLM2543IDWR](#) [RS8424XP](#) [TSV6291AICT\(UMW\)](#) [TLV521DCKR\(UMW\)](#)
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[FMLN16T](#) [LMV321AQDCKRQ1](#)