

Description

The OPAx333 series of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 μ V, maximum) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (± 0.9 V) and up to 5.5 V (± 2.75 V) can be used. These devices are optimized for low-voltage, single-supply operation.

The OPAx333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the 5-pin SOT-23, SOT, and 8-pin SOP packages, while the OPA2333 (dual version) is available in the 8-pin SOP packages. All versions are specified for operation from -40°C to 125°C .

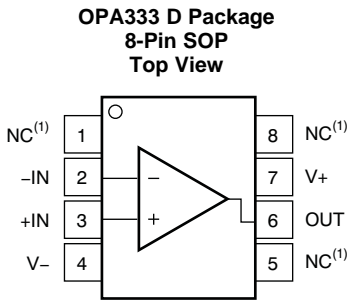
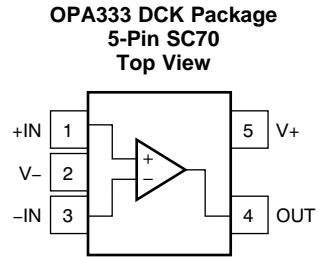
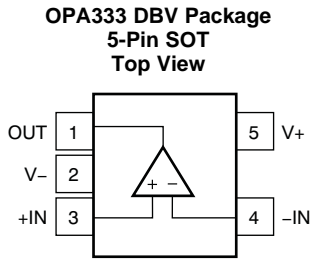
Features

- Low Offset Voltage: 10 μ V (Maximum)
- Zero Drift: 0.05 μ V/ $^{\circ}\text{C}$ (Maximum)
- 0.01-Hz to 10-Hz Noise: 1.1 μ V_{PP}
- Quiescent Current: 17 μ A
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- *microSize* Packages: SC70 and SOT23

Applications

- Transducers
- Temperature Measurements
- Electronic Scales
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

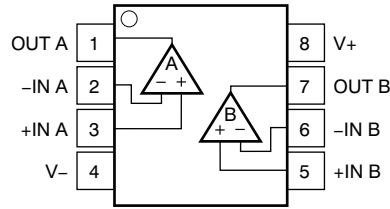
Pin Configuration and Functions



Pin Functions: OPA333

NAME	PIN			I/O	DESCRIPTION
	SOP	SOT	SC70		
+IN	3	3	1	I	Noninverting input
-IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection (can be left floating)
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V-	4	2	2	—	Negative (lowest) power supply

OPA2333 D or DGK Package
8-Pin SOP
Top View



Pin Functions: OPA2333

PIN		I/O	DESCRIPTION
NAME	SOP		
+IN	—	I	Noninverting input
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
-IN	—	I	Inverting input
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
OUT	—	O	Output
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	Supply	7		V
	Signal input terminals ⁽²⁾	-0.3	(V+) + 0.3	
Current	Signal input terminals ⁽²⁾	-1	1	mA
	Output short-circuit ⁽³⁾	Continuous		
Operating junction temperature, T _J			150	°C
Operating temperature, T _A		-40	150	
Storage temperature, T _{stg}		-65	150	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

ESDRatings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage, V _S	1.8	5.5	V
Specified temperature	-40	125	°C

Thermal Information: OPA333

THERMAL METRIC ⁽¹⁾		OPA333			UNIT
		D (SOIC)	DBV (SOT)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	80.6	61.7	97.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

Thermal Information: OPA2333

THERMAL METRIC ⁽¹⁾		OPA2333		UNIT
		D (SOP)		
		8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	124.0		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	73.7		°C/W
R _{θJB}	Junction-to-board thermal resistance	64.4		°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.0		°C/W
ψ _{JB}	Junction-to-board characterization parameter	63.9		°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—		°C/W

Electrical Characteristics

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$V_S = 5\text{ V}$		2	10	μV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to 125°C		0.02	0.05	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 1.8\text{ V}$ to 5.5 V , $T_A = -40^\circ\text{C}$ to 125°C		1	5	$\mu\text{V}/\text{V}$
	Long-term stability ⁽¹⁾			See note ⁽¹⁾		μV
	Channel separation, dc			0.1		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = 25^\circ\text{C}$		± 70	± 200	pA
		$T_A = -40^\circ\text{C}$ to 125°C		± 150		
I_{OS}	Input offset current			± 140	± 400	
NOISE						
	Input voltage noise	$f = 0.01\text{ Hz}$ to 1 Hz		0.3		μV_{PP}
		$f = 0.1\text{ Hz}$ to 10 Hz		1.1		
i_n	Input current noise	$f = 10\text{ Hz}$		100		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		$(V-) - 0.1$		$(V+) + 0.1$	V
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C	106	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V-) + 100\text{ mV} < V_O < (V+) - 100\text{ mV}$, $R_L = 10\text{ k}\Omega$, $T_A = -40^\circ\text{C}$ to 125°C	106	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	$C_L = 100\text{ pF}$		350		kHz
SR	Slew rate	$G = +1$		0.16		$\text{V}/\mu\text{s}$
OUTPUT						
	Voltage output swing from rail	$R_L = 10\text{ k}\Omega$		30	50	mV
		$R_L = 10\text{ k}\Omega$, $T_A = -40^\circ\text{C}$ to 125°C			70	
I_{SC}	Short-circuit current			± 5		mA
C_L	Capacitive load drive		See Typical Characteristics			
	Open-loop output impedance	$f = 350\text{ kHz}$, $I_O = 0\text{ A}$		2		k Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$		17	25	μA
		$T_A = -40^\circ\text{C}$ to 125°C			28	
	Turn-on time	$V_S = +5\text{ V}$		100		μs
TEMPERATURE						
T_A	Specified range		-40		125	$^\circ\text{C}$
	Operating range		-40		150	$^\circ\text{C}$
T_{stg}	Storage range		-65		150	$^\circ\text{C}$

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately $1\text{ }\mu\text{V}$.

Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $C_L = 0\text{ pF}$, unless otherwise noted.

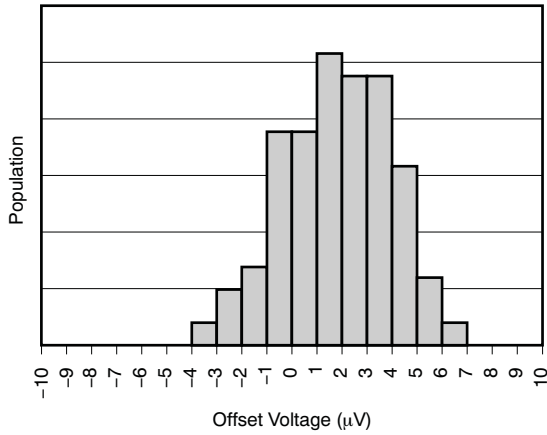


Figure 1. Offset Voltage Production Distribution

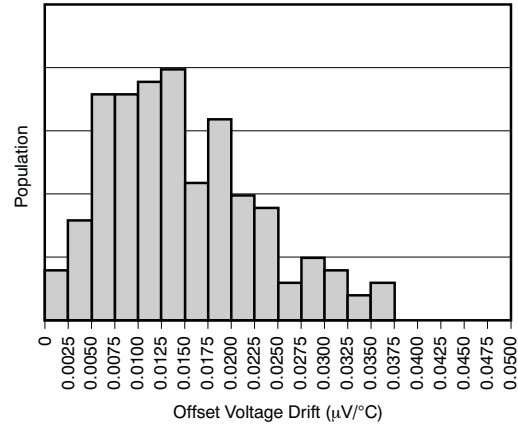


Figure 2. Offset Voltage Drift Production Distribution

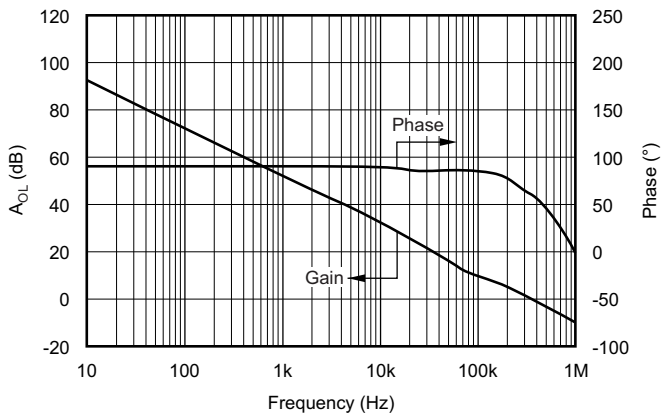


Figure 3. Open-Loop Gain and Phase vs Frequency

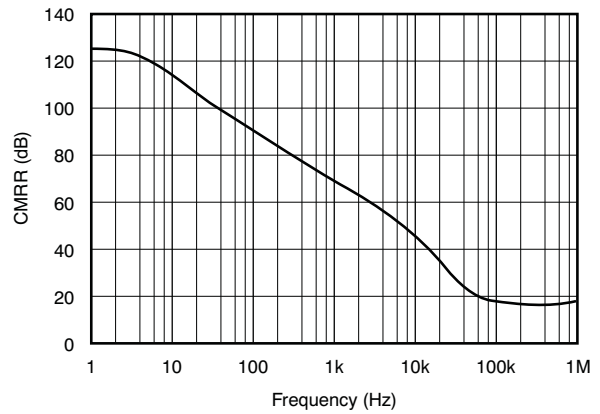


Figure 4. Common-Mode Rejection Ratio vs Frequency

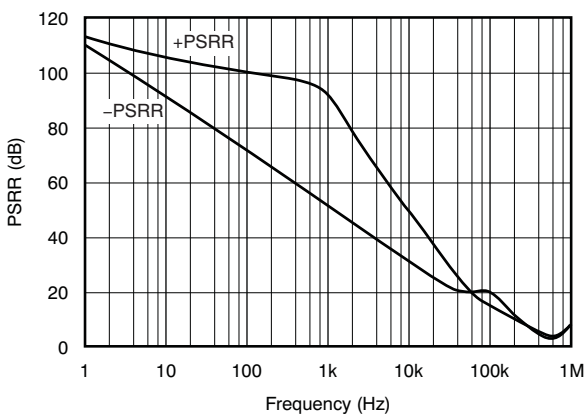


Figure 5. Power-Supply Rejection Ratio vs Frequency

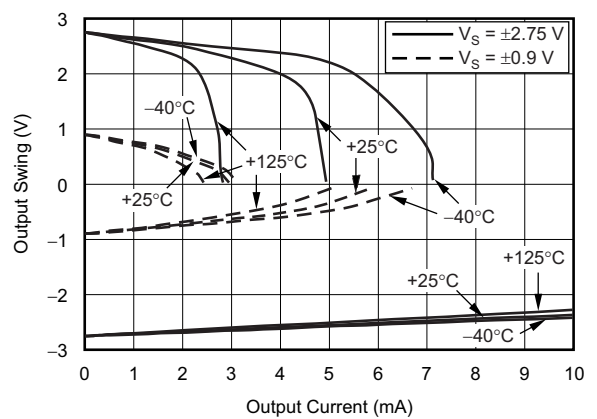


Figure 6. Output Voltage Swing vs Output Current

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $C_L = 0\text{ pF}$, unless otherwise noted.

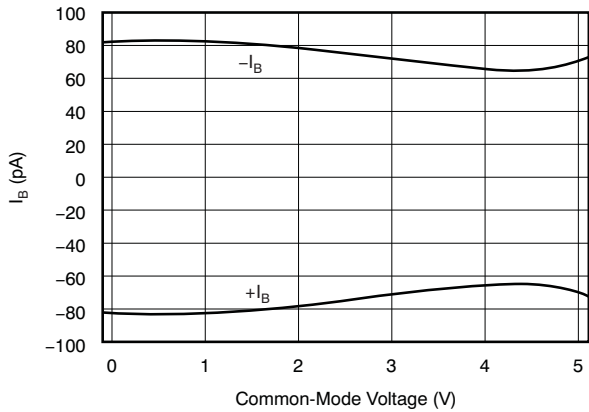


Figure 7. Input Bias Current vs Common-Mode Voltage

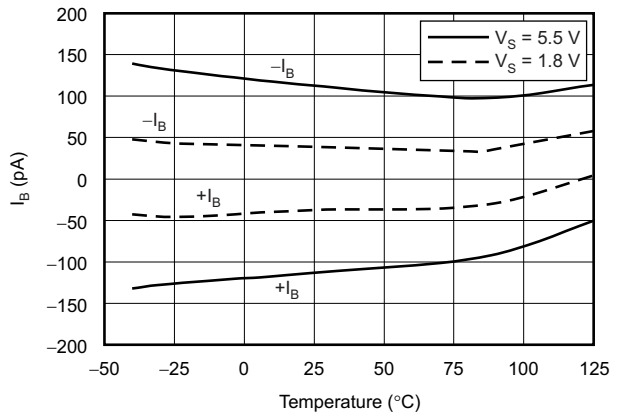


Figure 8. Input Bias Current vs Temperature

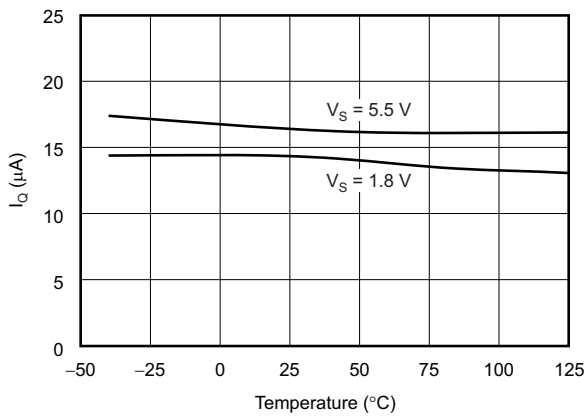


Figure 9. Quiescent Current vs Temperature

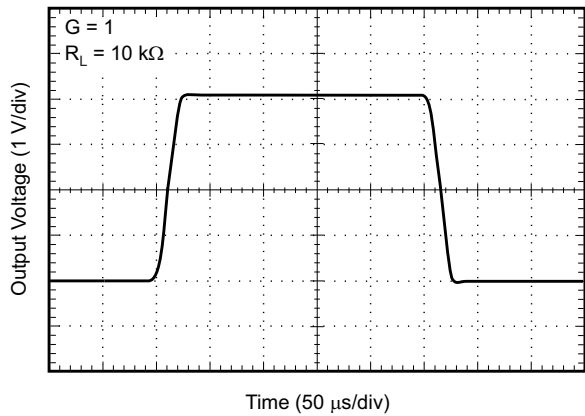


Figure 10. Large-Signal Step Response

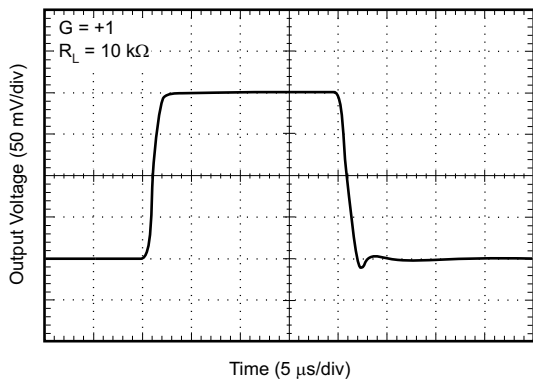


Figure 11. Small-Signal Step Response

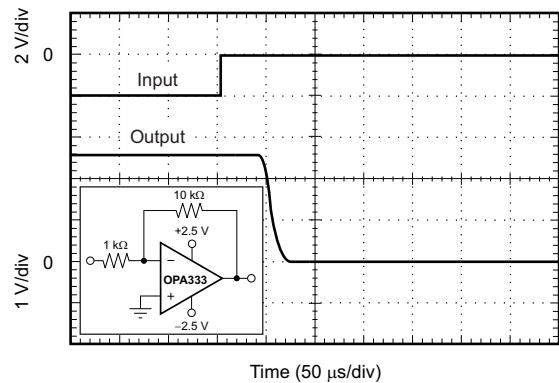


Figure 12. Positive Overtolerance Recovery

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $C_L = 0\text{ pF}$, unless otherwise noted.

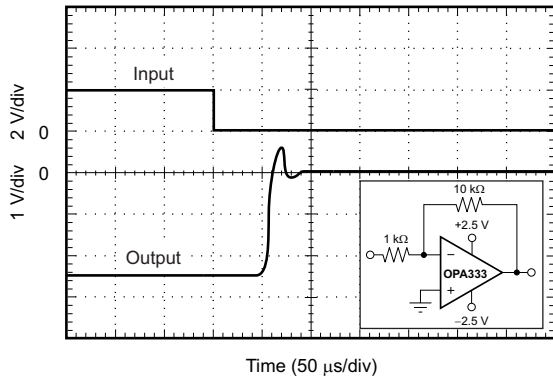


Figure 13. Negative Overvoltage Recovery

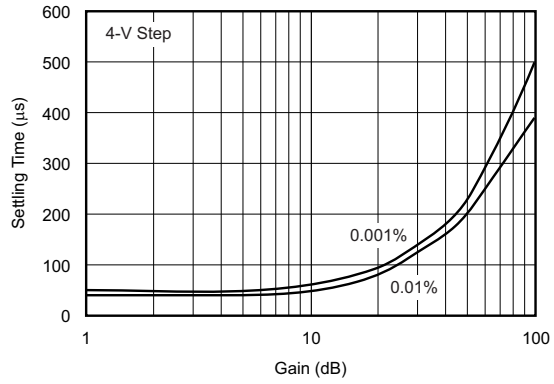


Figure 14. Settling Time vs Closed-Loop Gain

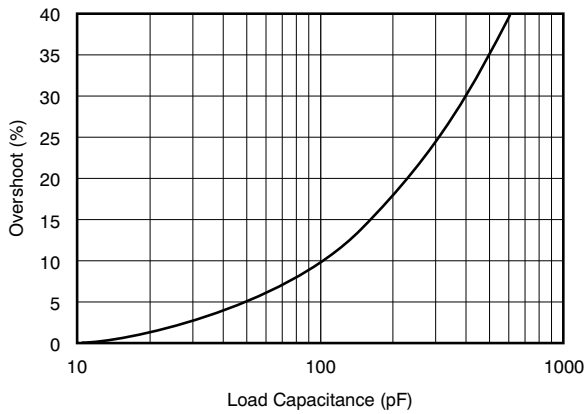


Figure 15. Small-Signal Overshoot vs Load Capacitance

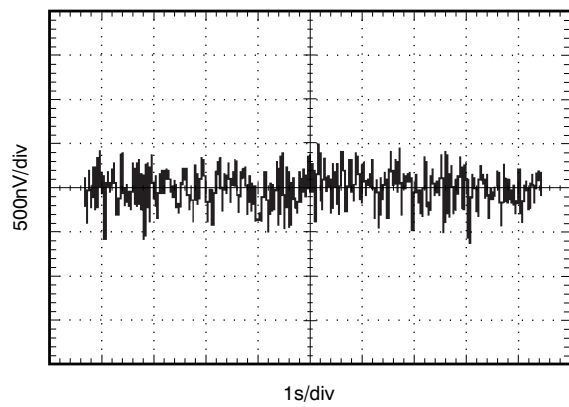


Figure 16. 0.1-Hz to 10-Hz Noise

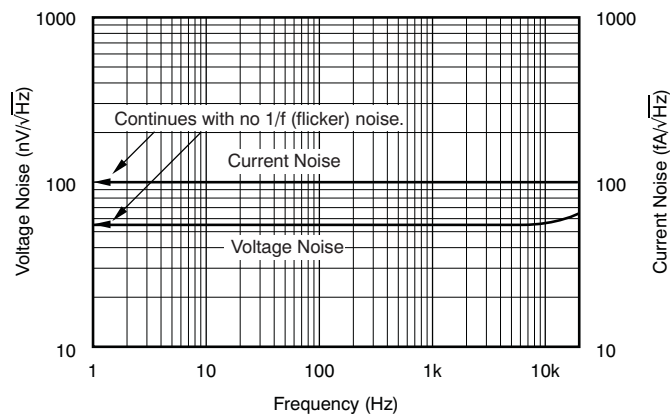


Figure 17. Current and Voltage Noise Spectral Density vs Frequency

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW OPA333AIDBVR	SOT23-5	3000	Tape and reel	OAXQ U
UMW OPA2333AIDR	SOP-8	2500	Tape and reel	O2333A
UMW OPA333AIDR	SOP-8	2500	Tape and reel	O333A
UMW OPA333AIDCKR	SC70-5	3000	Tape and reel	BQY U

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[MCP6V54-E/SL](#) [OP07CP\(LX\)](#) [CBM8606AWS8](#) [MCP6V91UT-E/LTY](#) [LTC2057HS8#TRPBF](#) [AD8662ARZ-REEL](#) [OPA277UA\(UMW\)](#)
[HG8552CMM/TR](#) [TSZ122IYDT\(UMW\)](#) [TSZ122IDT\(UMW\)](#) [LTC8552-TP](#) [OPA2330AIDR-TP](#) [TPV2376S8](#) [OPA2336UA-TP](#)
[OPA2376AIDR-TP](#) [TPSGM8552XS8G](#) [AD8538ARZ\(UMW\)](#) [OPA2333AIDR-TP](#) [OPA2317IDR-TP](#) [OPA2330AIDR\(UMW\)](#)
[OPA2333AIDR\(XBLW\)](#) [AD8552ARZ\(XBLW\)](#) [OP177FN](#) [AD8554ARZ-MS](#) [OP2177ARZ\(UMW\)](#) [AD8630ARZ-MS](#) [SL8582XS8](#)
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