UMW NDT452AP

-30V P-Channel MOSFET

1.Description

Power SOT-223 P-Channel enhancement mode power field effect transistors especially tailored to minimize on state resistance and provide superior switching performance.

2.1Features

- $V_{DS\ (V)}$=-30V
- I_D=-5A(V_{GS}=-10V)
- $R_{DS(ON)}$<65mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<100mΩ(V_{GS}=-4.5V)

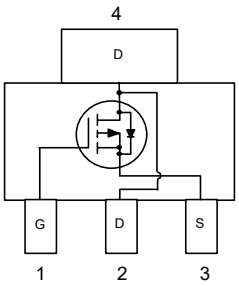
2.2Features

- High power and current handling capability in a widely used surface mount package.
- High density cell design for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2,4	D	DRAIN
3	S	SOURCE

SOT-223 top view



4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current - Continuous	(Note 1a)	I_D	-5	A
-Pulsed			-15	A
Power Dissipation for Single Operation	(Note 1a)	P_D	3	W
	(Note 1b)		1.3	W
	(Note 1c)		1.1	W
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-65 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	42	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	12	°C/W

6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	-30			V
Zero Gate Voltage Drain Curent	I_{DSS}	V_{DS}=-24V, V_{GS}=0V, T_J=55°C			-1	μA
					-10	μA
Gate - Body Leakage, Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	-1	-1.6	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5A		52	65	mΩ
		V_{GS}=-4.5V, I_D=-4.3A		85	100	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-15			A
		V_{GS}=-4.5V, V_{DS}=-5V	-5			A
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-5A		7		S
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz		690		pF
Output Capacitance	C_{oss}			430		pF
Reverse Transfer Capacitance	C_{rss}			160		pF
Turn - On Delay Time	$t_{D(on)}$	V_{DD}=-10V, I_D=-1A V_{GS}=-10V, R_{GEN}=6Ω		9	20	ns
Turn - On Rise Time	t_r			20	30	ns
Turn - Off Delay Time	$t_{D(off)}$			40	50	ns
Turn - Off Fall Time	t_f			19	40	ns
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-5A, V_{GS}=-10V		22	30	nC
Gate-Source Charge	Q_{gs}			3.2		nC
Gate-Drain Charge	Q_{gd}					nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-2.5	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-2.5A (Note 2)		-0.85	-1.2	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_S=-2.5A,dI_F/dt=100 A/μs			100	ns

Notes:

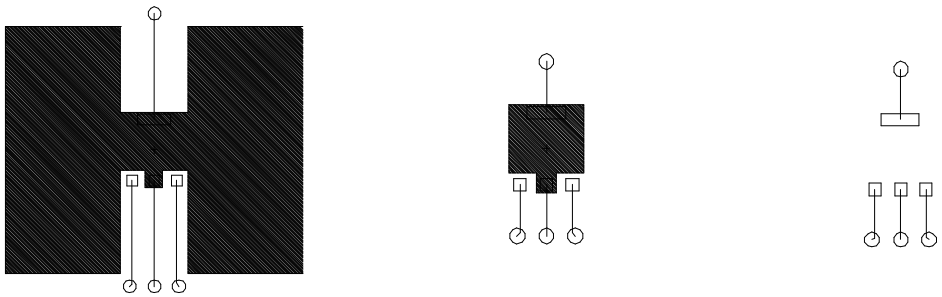
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

7.1Typical characteristic

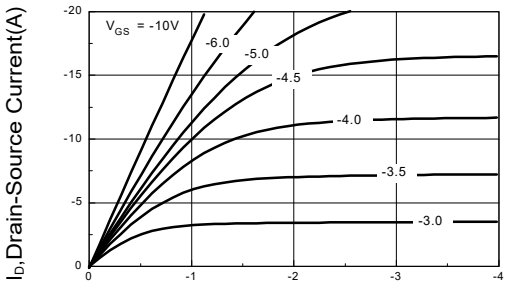


Figure 1: On-Region Characteristics

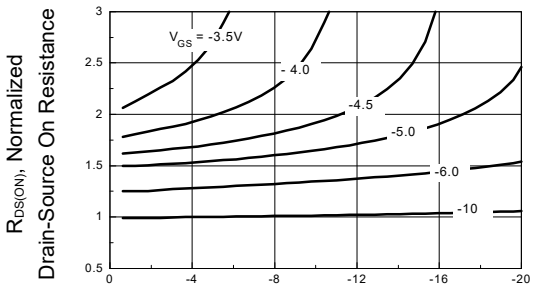


Figure 2: On-Resistance Variation with Gate Voltage and Drain Current

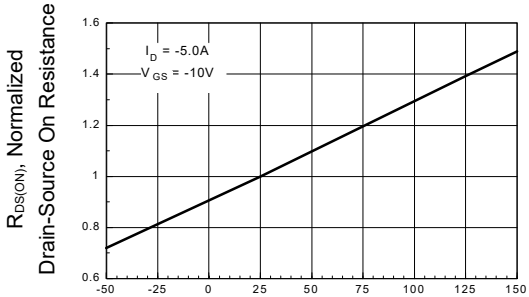


Figure 3: On-Resistance Variation with Temperature

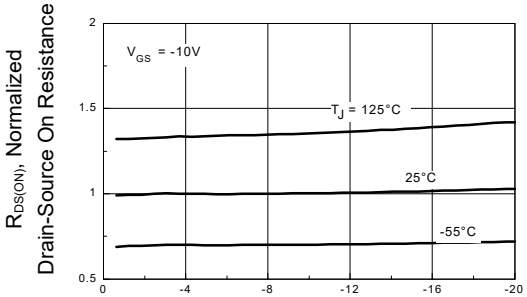


Figure 4: On-Resistance Variation with Drain Current and Temperature.

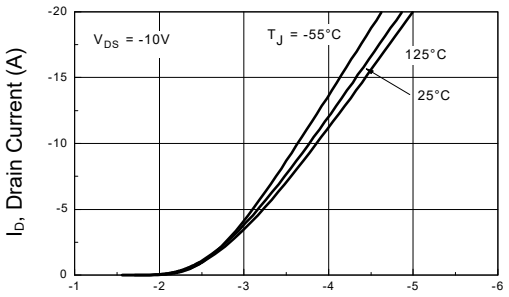


Figure 5: Transfer Characteristics

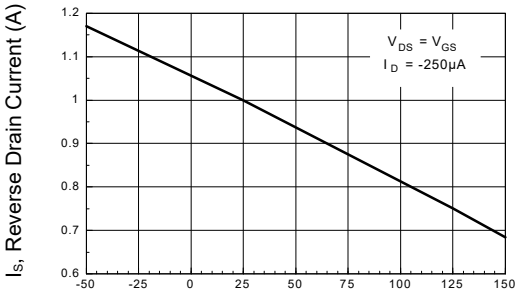
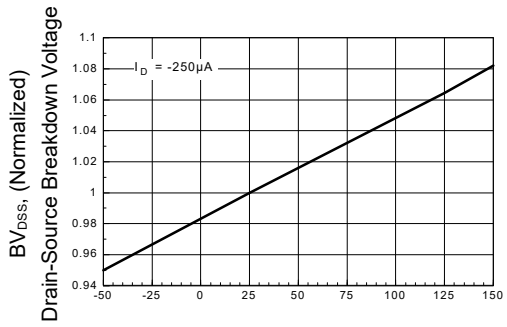


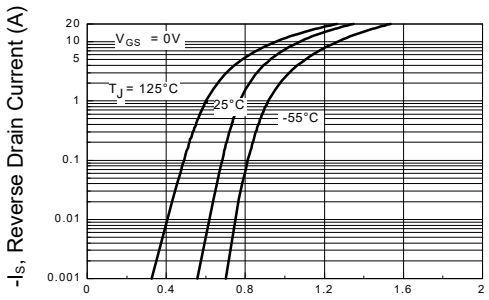
Figure 6: Gate Threshold Variation with Temperature.

7.2Typical characteristic



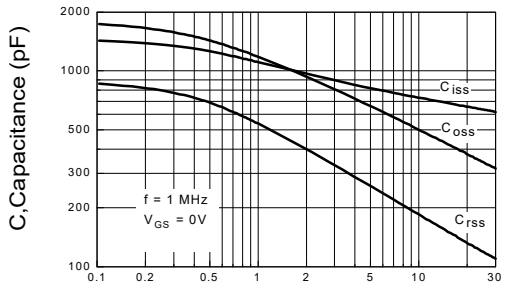
T_J,Junction Temperature (°C)

Figure 7: Breakdown Voltage Variation with Temperature



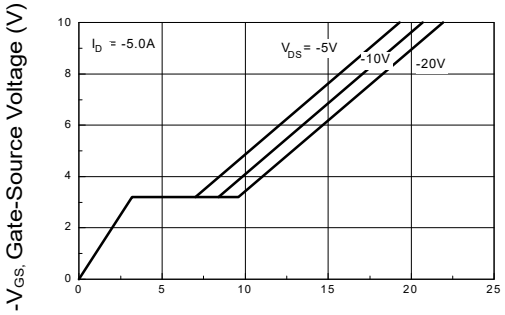
$-V_{SD}$,Body Diode Forward Voltage (V)

Figure 8: Body Diode Forward Voltage Variation with Current and Temperature



$-V_{DS}$, Drain-source Voltage (V)

Figure 9: Capacitance Characteristics



Q_G, Total Gate Charge (nC)

Figure 10: Gate Charge Characteristics

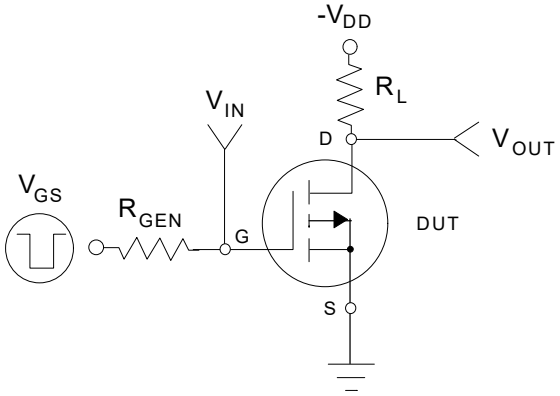


Figure 11: Switching Test Circuit

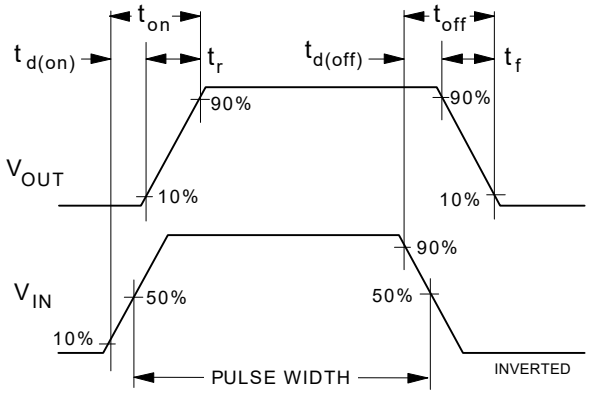


Figure 12: Switching Waveforms

7.3Typical characteristic

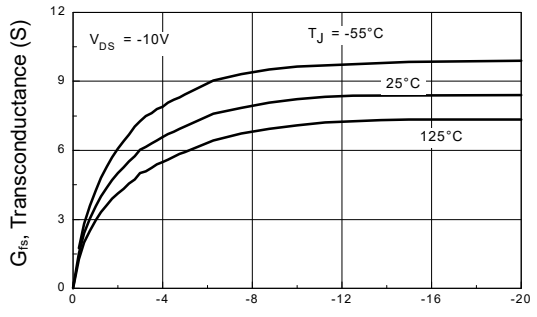


Figure 13: Transconductance Variation with Drain Current and Temperature

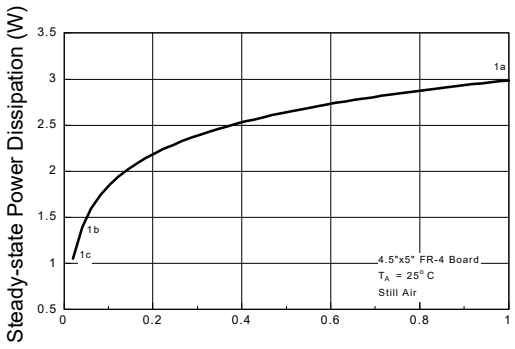


Figure 14: SOT-223 Maximum Steady- tate Power Dissipation versus CopperMounting Pad Area

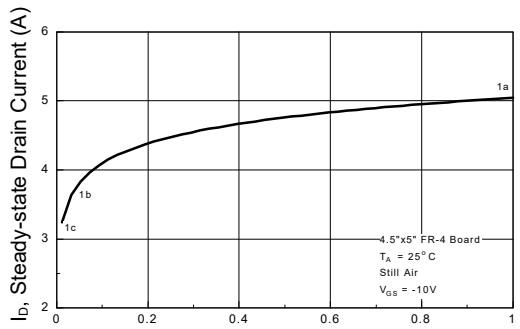


Figure 15:Maximum Steady-State Drain Current versus Copper Mounting PadArea

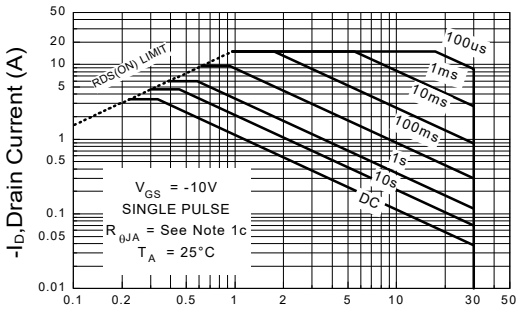


Figure 16: Maximum Safe Operating Area

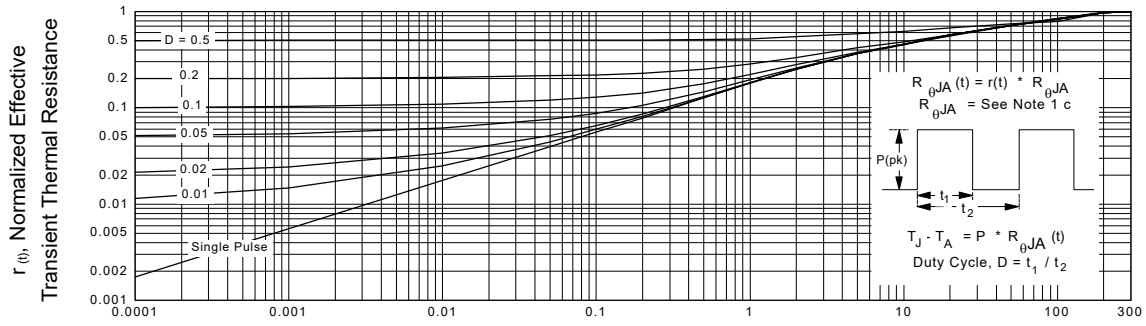
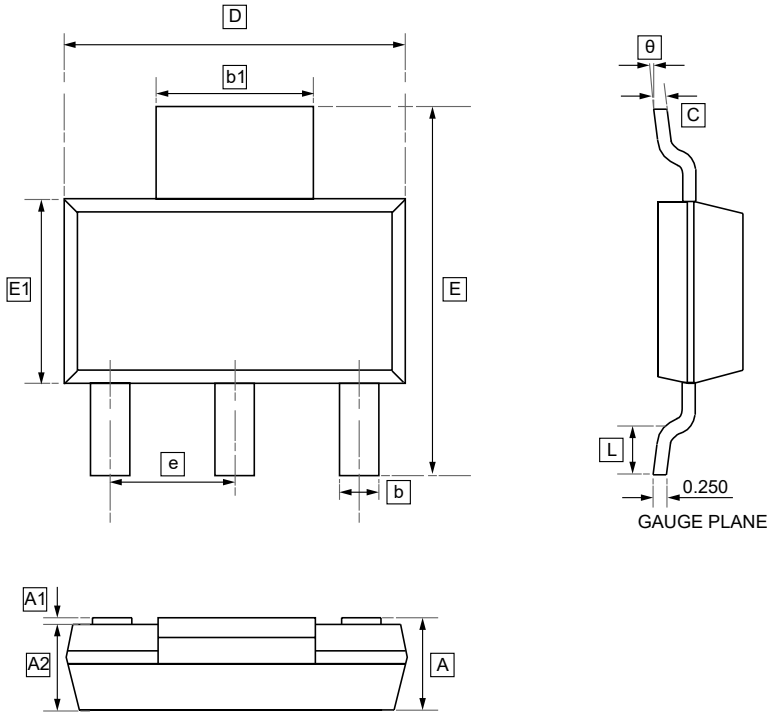


Figure 17: Transient Thermal Response Curve

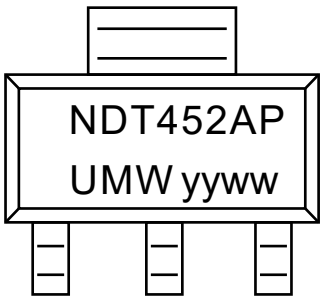
8.SOT-223 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	D	E	E1	e	L	θ
Min	-	0.020	1.500	0.660	2.900	0.230	6.300	6.700	3.300	2.300	0.750	0°
Max	1.800	0.100	1.700	0.840	3.100	0.350	6.700	7.300	3.700	BSC	-	10°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NDT452AP	SOT-223	2500	Tape and reel

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