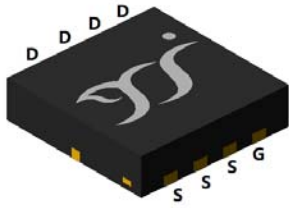
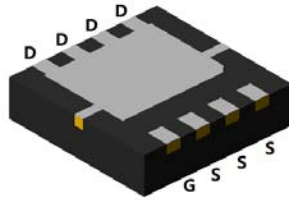




N-Channel Enhancement Mode Field Effect Transistor

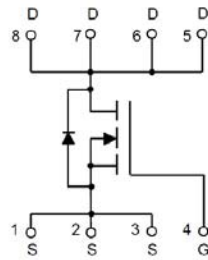


Top View



Bottom View

DFN3333-8L



Product Summary

• V_{DS}	60V
• I_D	53A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	$<8.2m\Omega$
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	$<12m\Omega$
• 100% EAS Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	10	A
	$T_A=100^\circ\text{C}$		6	
	$T_C=25^\circ\text{C}$		53	
	$T_C=100^\circ\text{C}$		33	
Pulsed Drain Current ^A		I_{DM}	160	A
Avalanche energy ^B		EAS	162	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	2.5	W
	$T_A=100^\circ\text{C}$		1	
	$T_C=25^\circ\text{C}$		44	
	$T_C=100^\circ\text{C}$		17	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.2	2.8	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ53G06AQ	F1	Q53G06	5000	10000	100000	13" reel



YJQ53G06AQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
		V _{DS} =60V, V _{GS} =0V, T _j =150℃	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	6	8.2	mΩ
		V _{GS} =4.5V, I _D =10A	-	8	12	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.9	1.2	V
Gate resistance	R _G	f=1MHz	-	1.6	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	53	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz	-	1850	-	pF
Output Capacitance	C _{oss}		-	440	-	
Reverse Transfer Capacitance	C _{rss}		-	20	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	31	-	nC
Gate-Source Charge	Q _{gs}		-	6	-	
Gate-Drain Charge	Q _{gd}		-	5	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=500A/us	-	18	-	nC
Reverse Recovery Time	t _{rr}		-	30	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V,V _{DD} =30V,R _L =2.5Ω R _{GEN} =3Ω	-	10	-	ns
Turn-on Rise Time	t _r		-	34	-	
Turn-off Delay Time	t _{D(off)}		-	26.2	-	
Turn-off fall Time	t _f		-	45	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=40V, V_G=10V, R_G=25Ω, L=1mH, I_{AS}=18A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

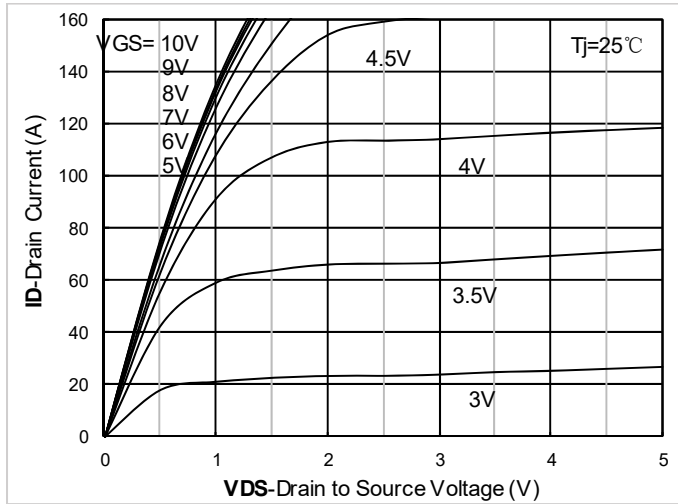


Figure 1. Output Characteristics

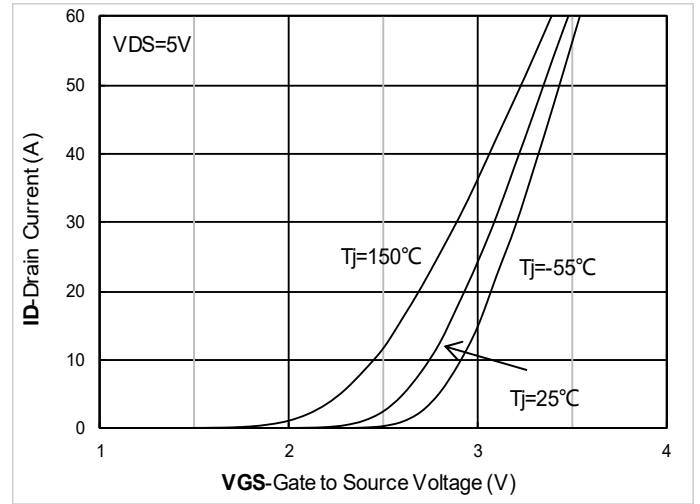


Figure 2. Transfer Characteristics

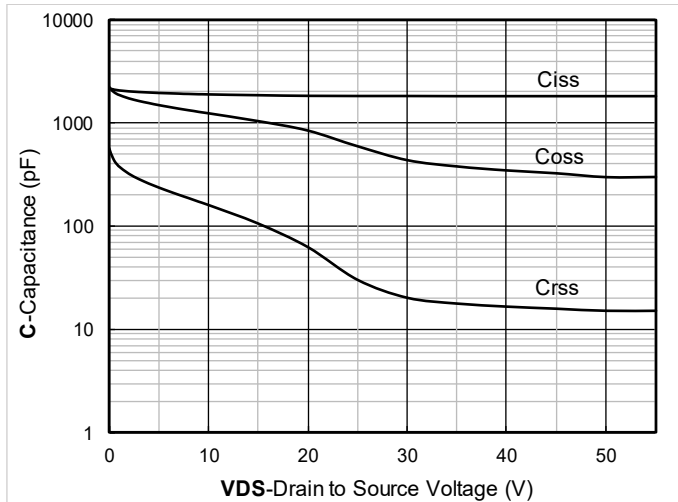


Figure 3. Capacitance Characteristics

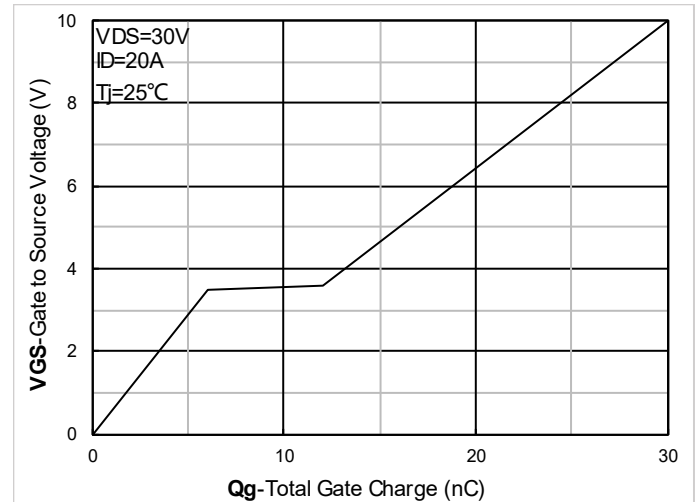


Figure 4. Gate Charge

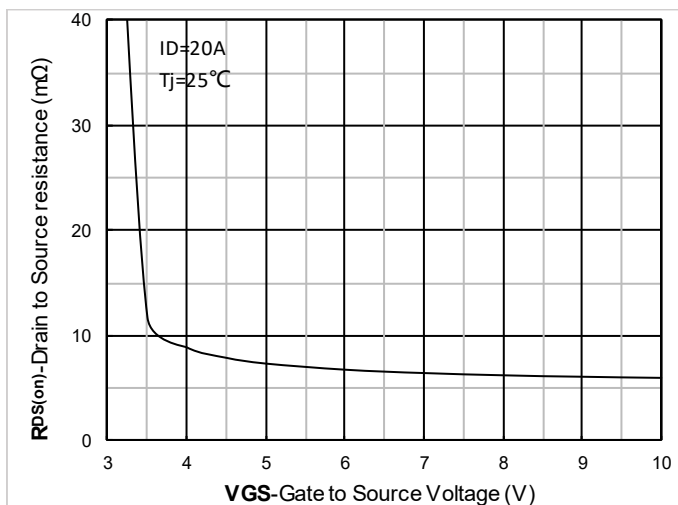


Figure 5. On-Resistance vs Gate to Source Voltage

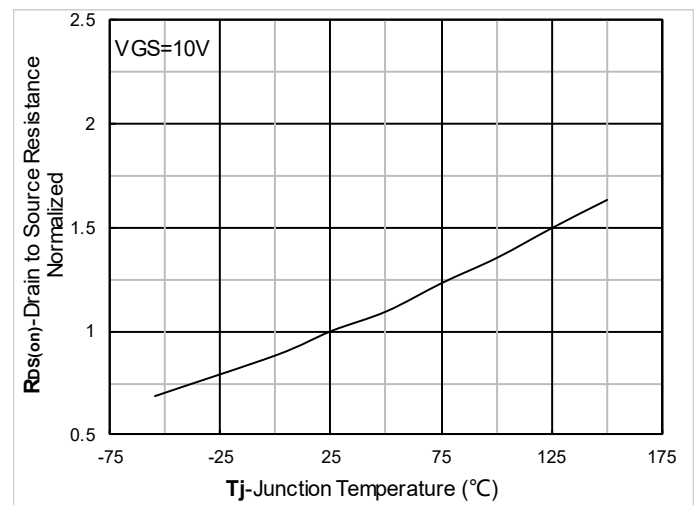


Figure 6. Normalized On-Resistance

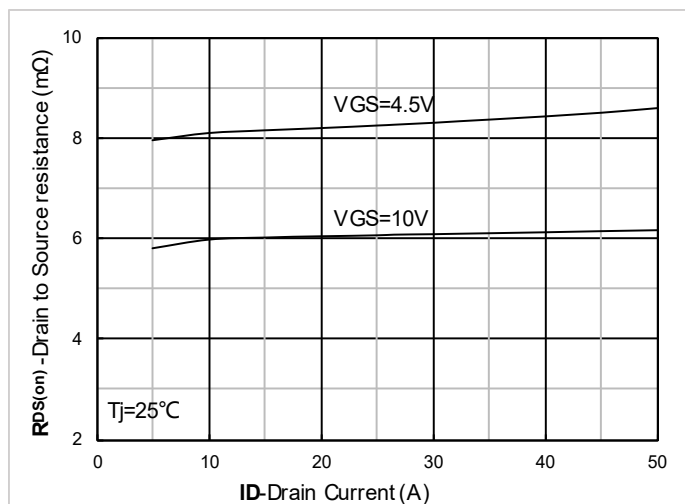


Figure 7. $R_{DS(on)}$ VS Drain Current

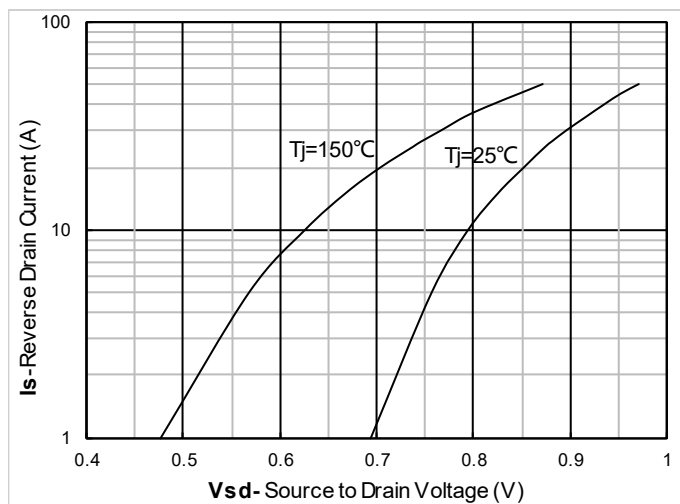


Figure 8. Forward characteristics of reverse diode

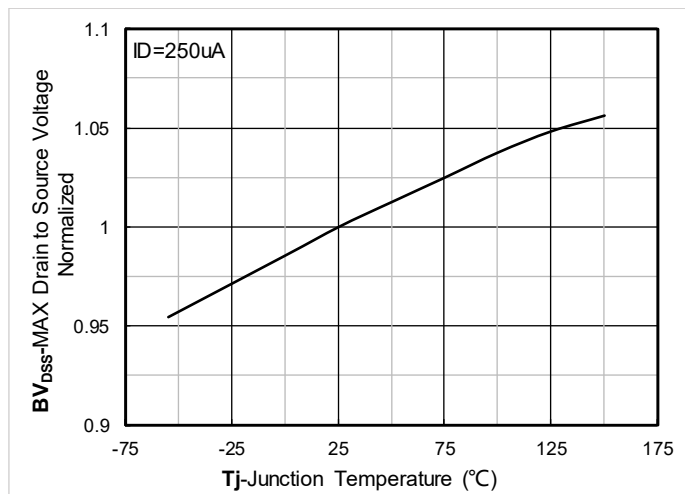


Figure 9. Normalized breakdown voltage

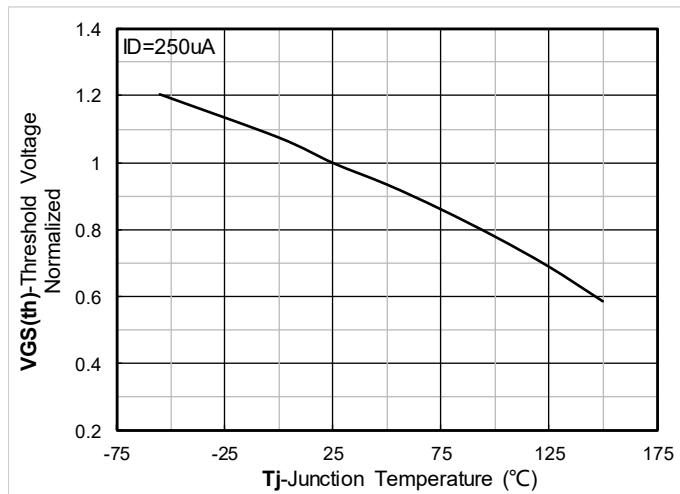


Figure 10. Normalized Threshold voltage

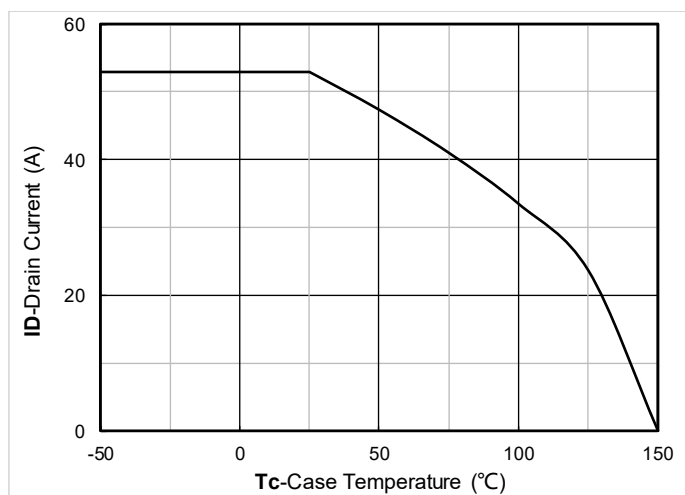


Figure 11. Current dissipation

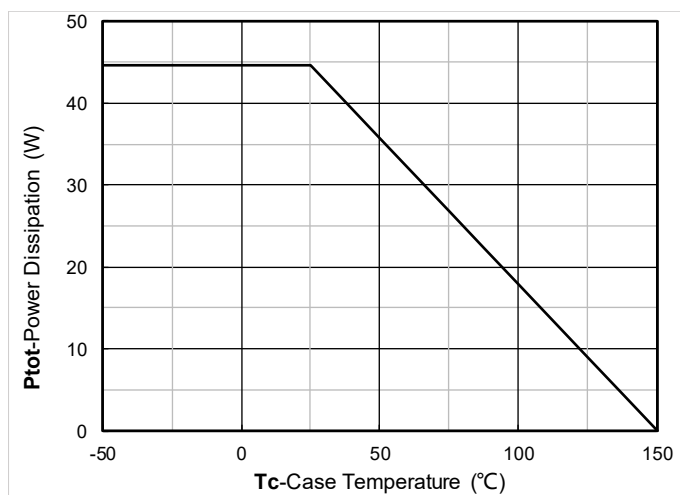


Figure 12. Power dissipation

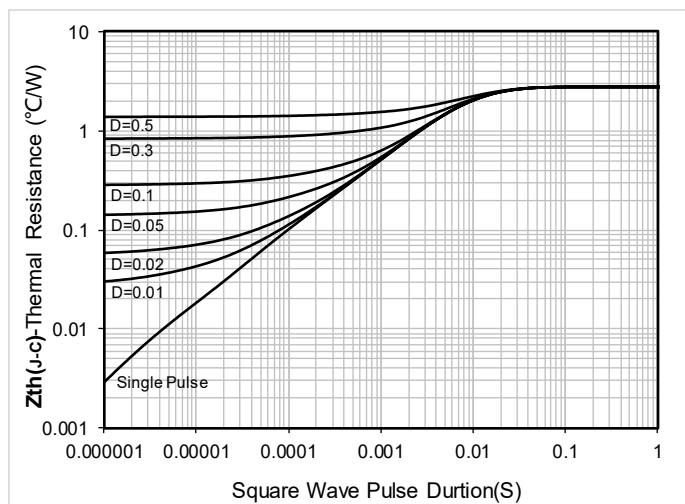


Figure 13. Maximum Transient Thermal Impedance

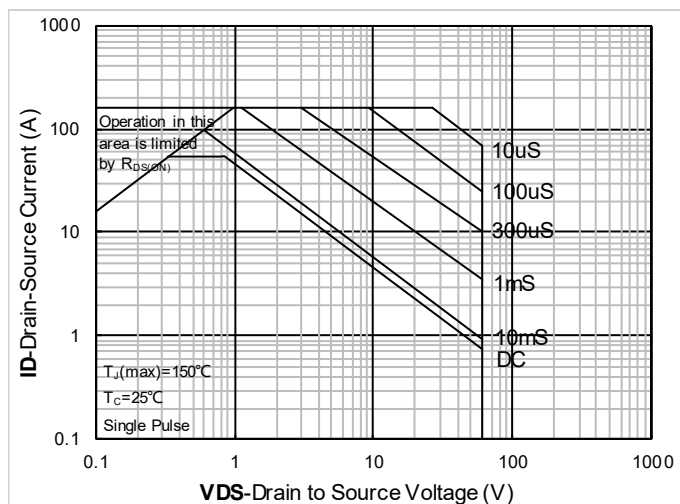


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

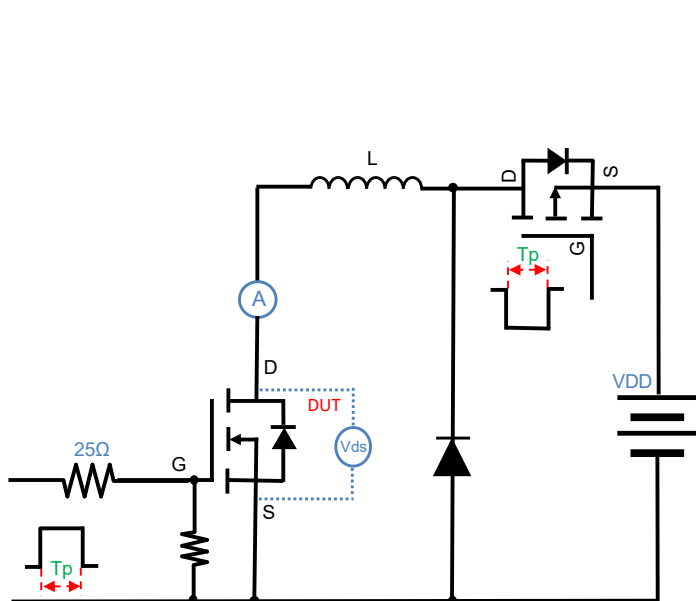
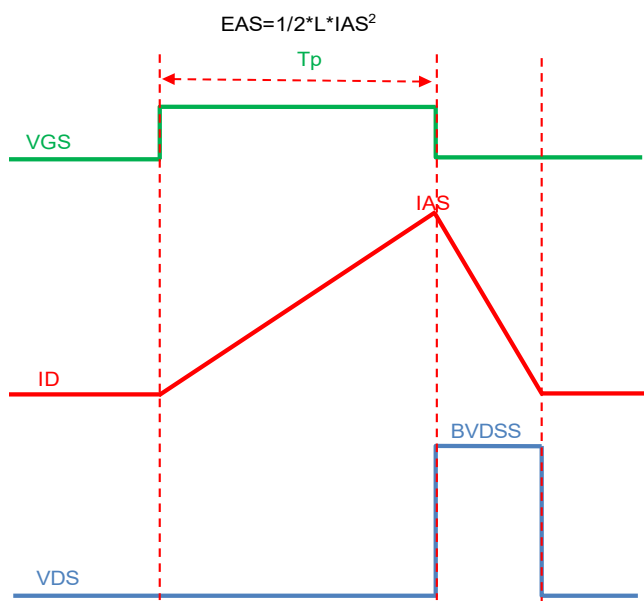


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



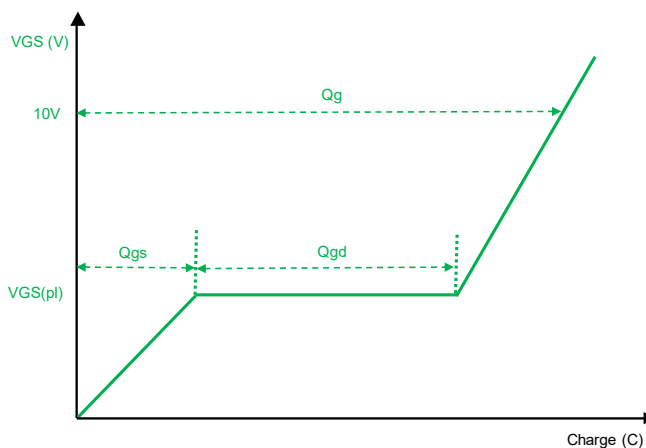
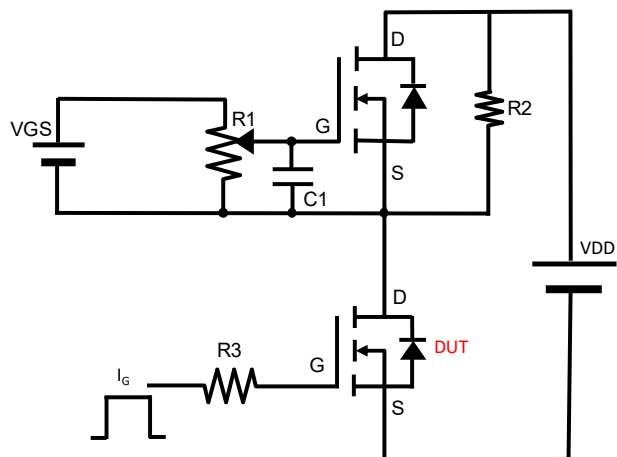


Figure B. Gate Charge Test Circuit & Waveform

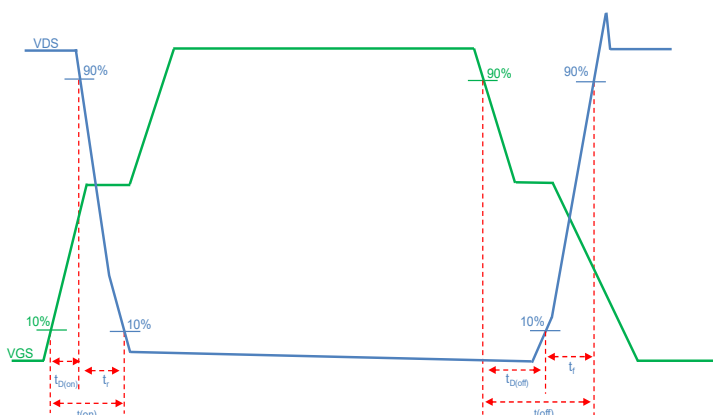
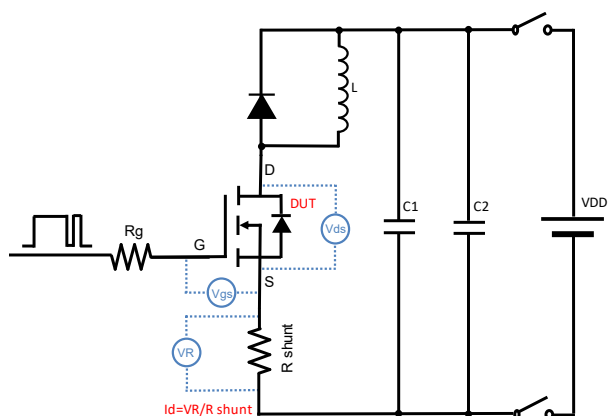


Figure C. Resistive Switching Test Circuit & Waveform

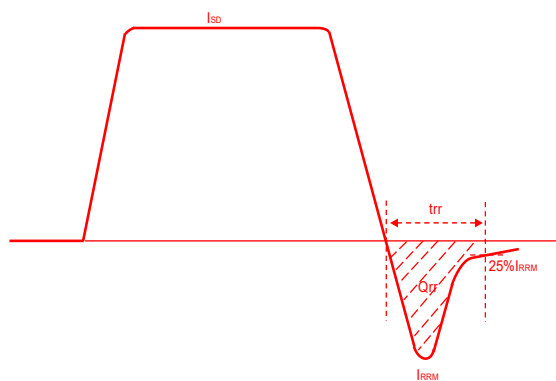
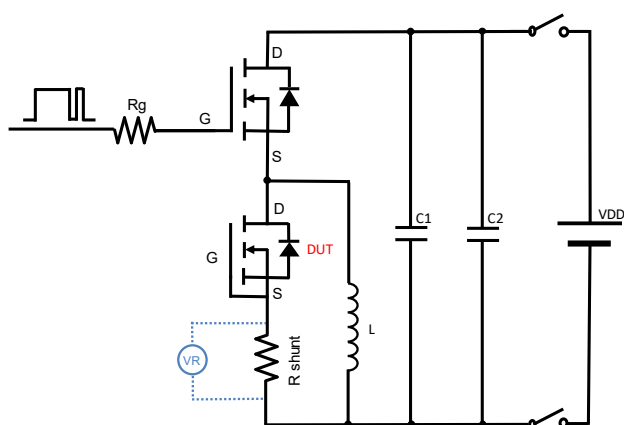
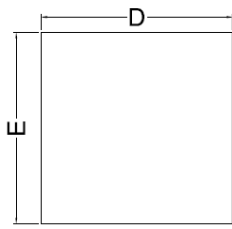


Figure D. Diode Recovery Test Circuit & Waveform

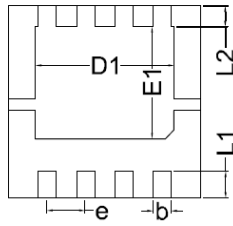


YJQ53G06AQ

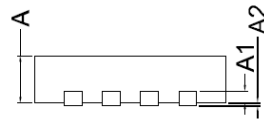
■DFN3333-8L Package information



Top View
正面视图

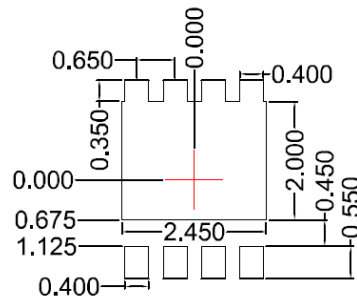


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



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