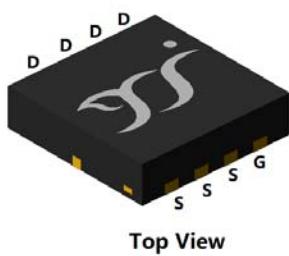
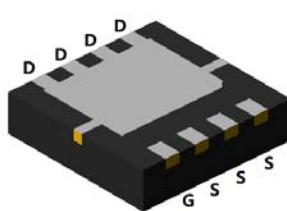


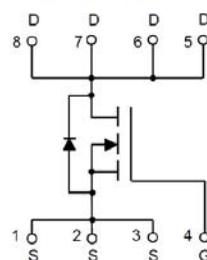
## N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View

**DFN3333-8L**

### Product Summary

- $V_{DS}$  100V
- $I_D$  40A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $<18.5m\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $<22.5m\Omega$
- 100% EAS Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter
- 12V, 24V and 48V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	8	A
	$T_A=100^\circ C$		5	
	$T_c=25^\circ C$		40	
	$T_c=100^\circ C$		25	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	110	A
Avalanche energy <sup>B</sup>		EAS	81	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2	W
	$T_A=100^\circ C$		0.9	
	$T_c=25^\circ C$		43	
	$T_c=100^\circ C$		17.2	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	°C

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	45	55	°C/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ40G10AQ	F1	Q40G10A	5000	10000	100000	13" reel



# YJQ40G10AQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	14	18.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	17	22.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	0.9	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain	-	1.4	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	40	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	1300	-	pF
Output Capacitance	C <sub>oss</sub>		-	750	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	21	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =25A	-	16	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5.6	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	2.4	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us	-	42	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	39.8	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>		-	39.2	-	ns
Turn-on Rise Time	t <sub>r</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>DS</sub> =25A R <sub>GEN</sub> =2.2Ω	-	11	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	53.2	-	
Turn-off fall Time	t <sub>f</sub>		-	15.8	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=40V, V<sub>G</sub>=10V, R<sub>G</sub>=25Ω, L=2mH, IAS=9A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on R<sub>θJA</sub> t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

### ■ Typical Electrical and Thermal Characteristics Diagrams

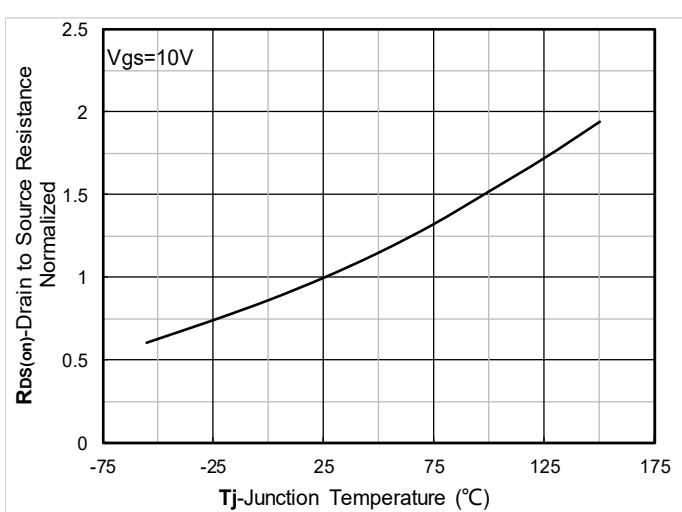
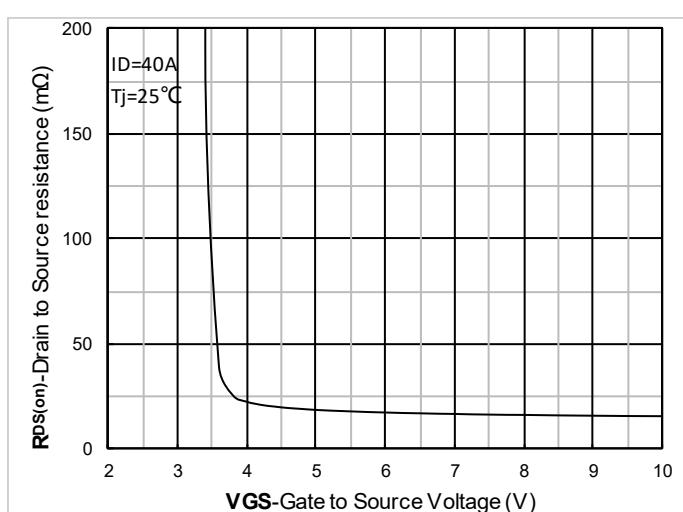
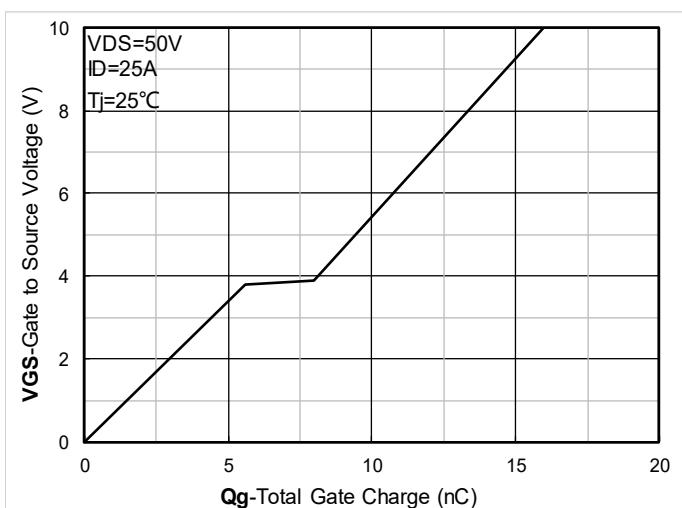
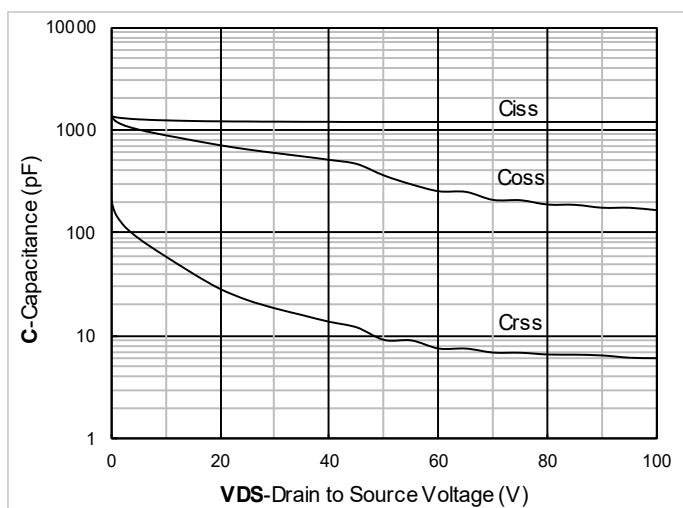
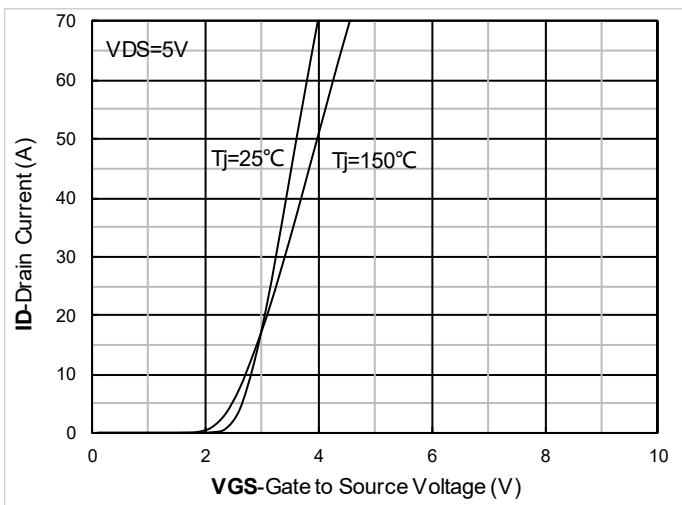
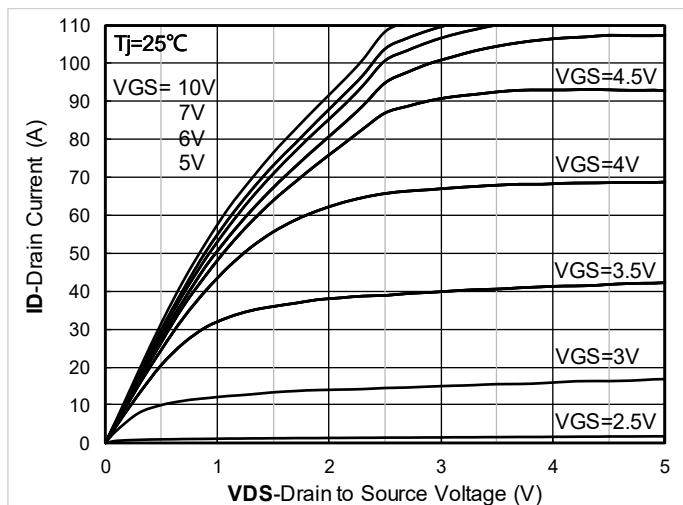


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

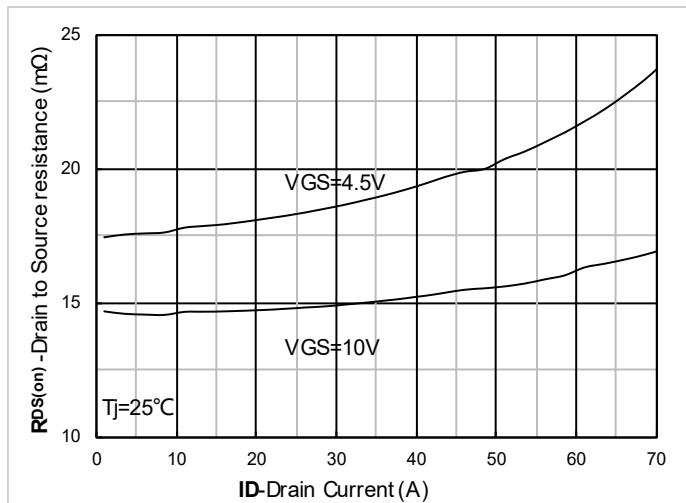


Figure 7. RDS(on) VS Drain Current

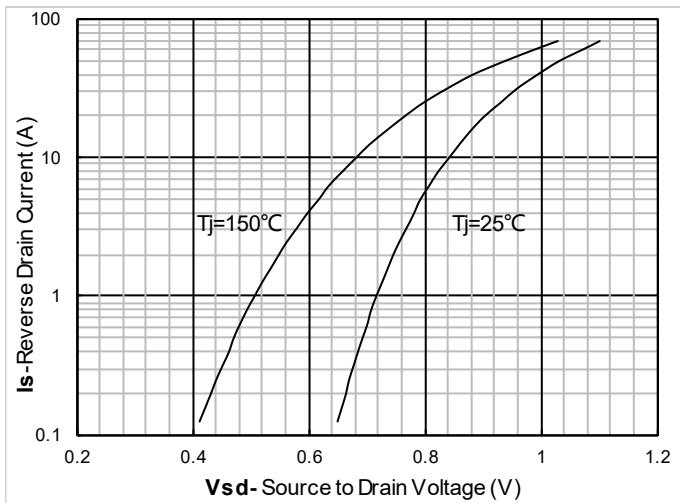


Figure 8. Forward characteristics of reverse diode

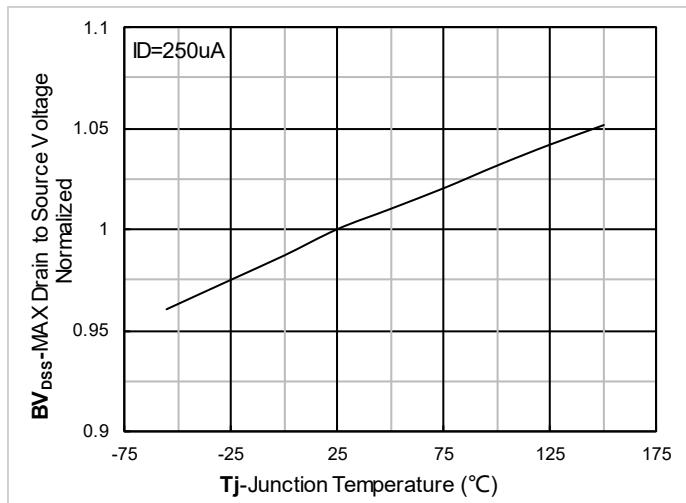


Figure 9. Normalized breakdown voltage

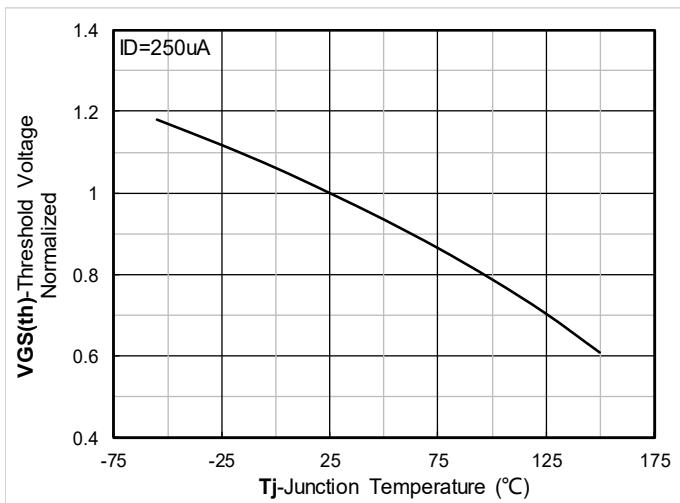


Figure 10. Normalized Threshold voltage

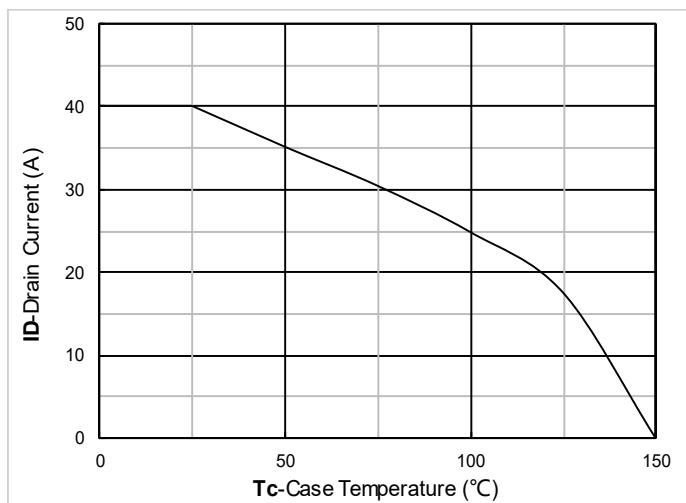


Figure 11. Current dissipation

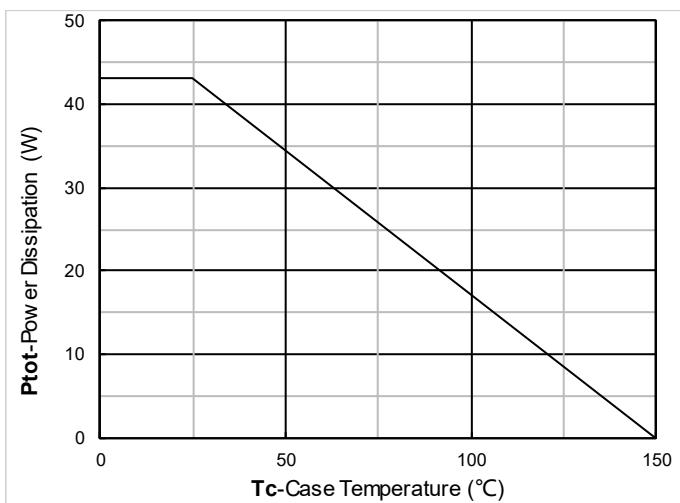


Figure 12. Power dissipation

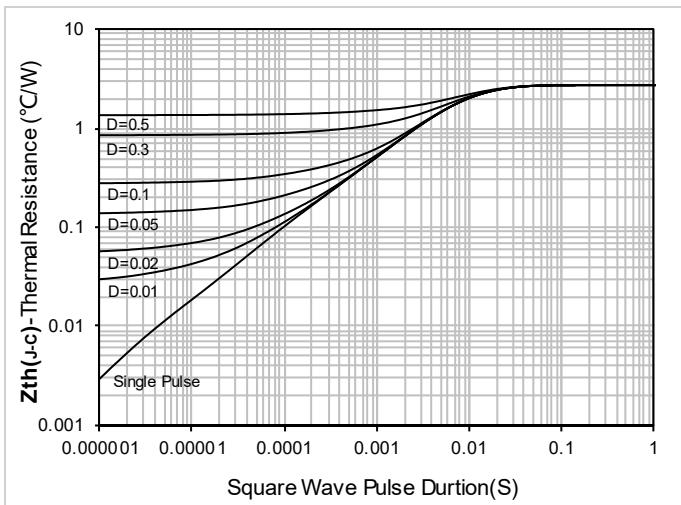


Figure 13. Maximum Transient Thermal Impedance

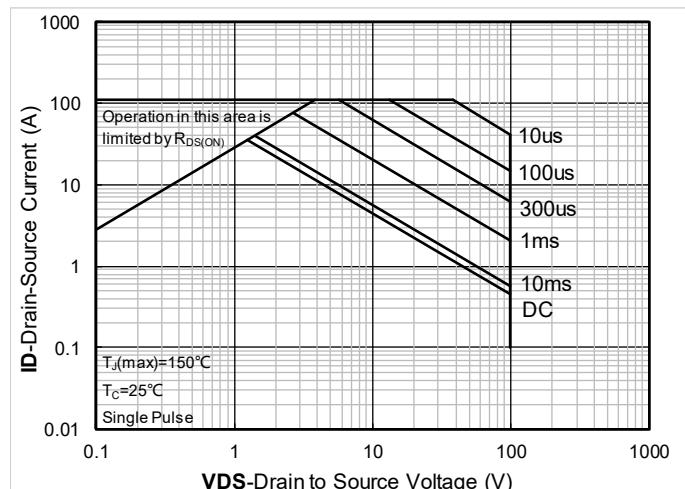


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

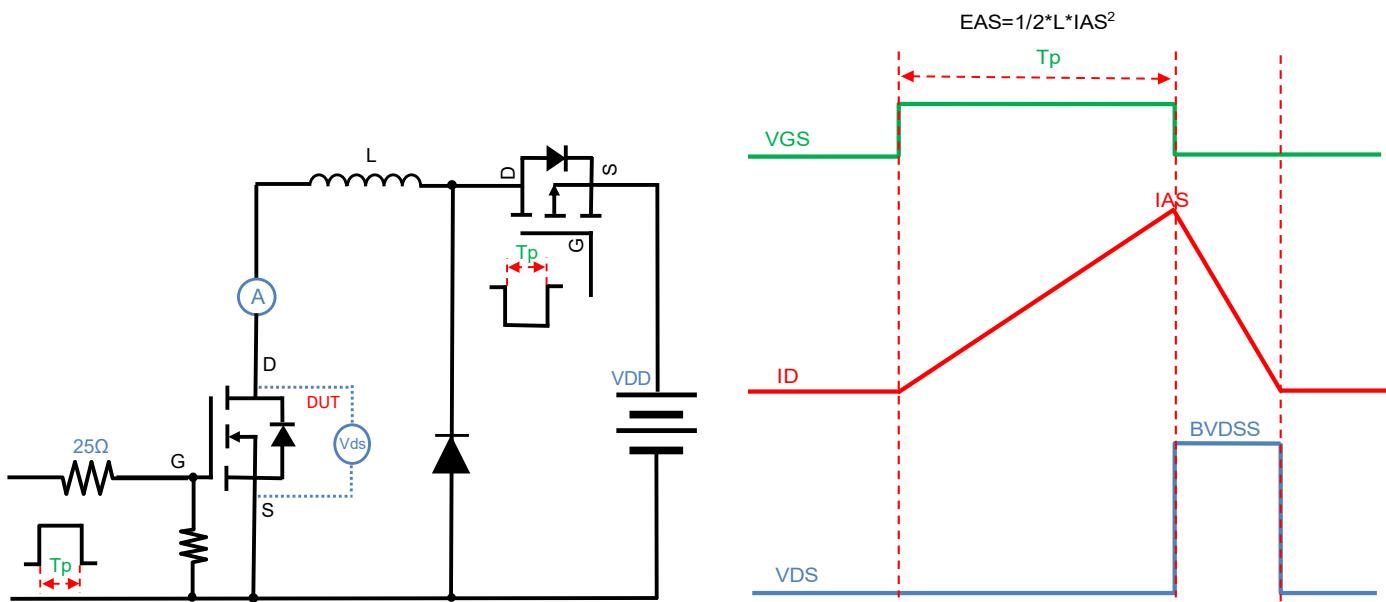


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

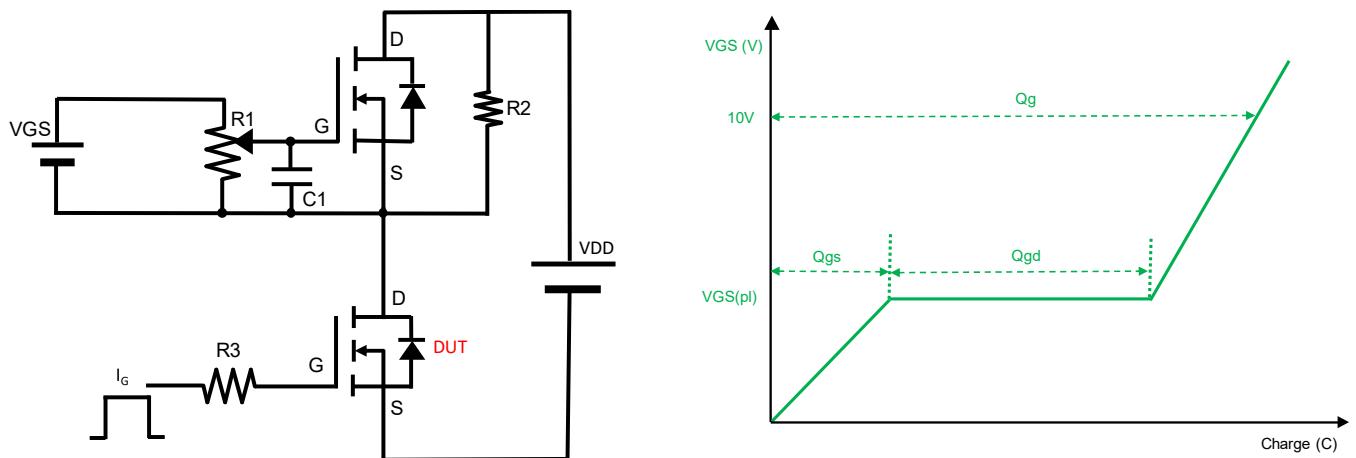


Figure B. Gate Charge Test Circuit & Waveform

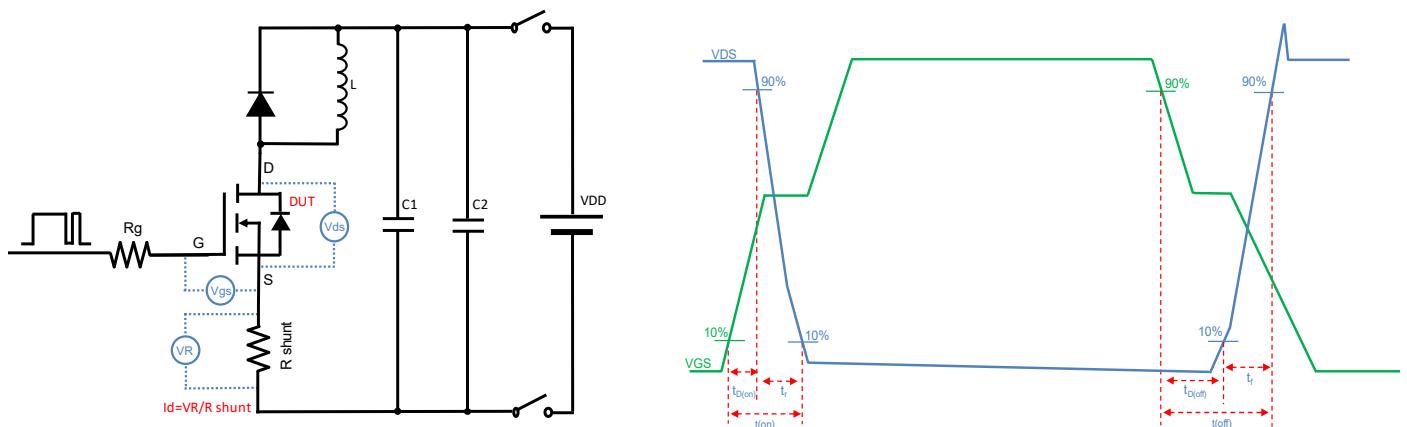


Figure C. Resistive Switching Test Circuit & Waveform

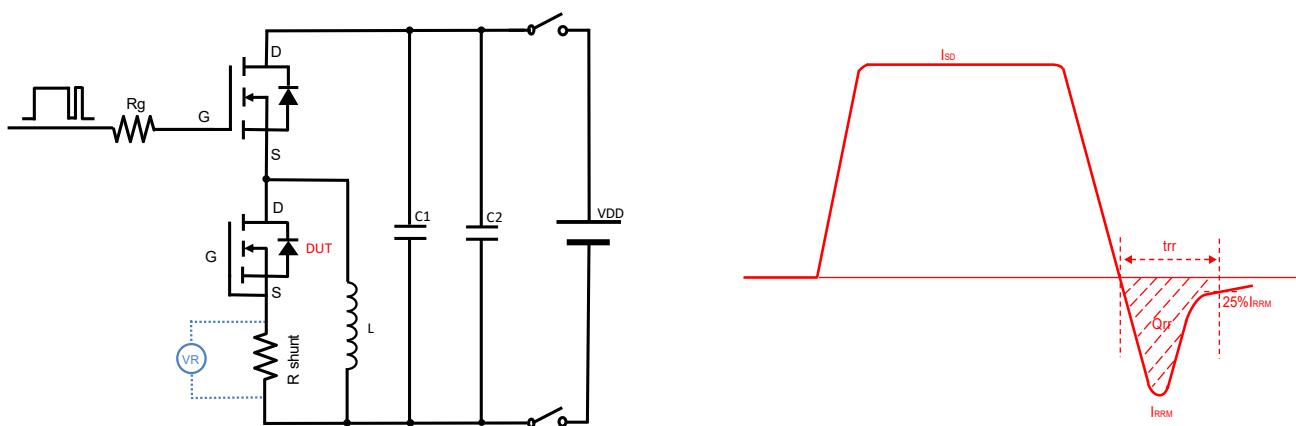
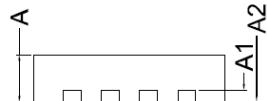
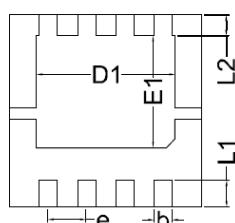
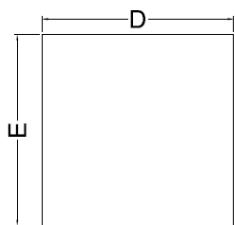


Figure D. Diode Recovery Test Circuit & Waveform



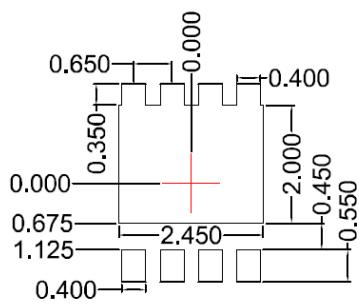
## ■DFN3333-8L Package information

Top View  
正面视图Bottom View  
背面视图Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	

## Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.

Suggested Solder Pad Layout  
Top View



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