

xTAG v3.0 Hardware Manual

IN THIS DOCUMENT

- ▶ Introduction
 - ▶ XS1-U8 device
 - ▶ xSYS Connector (J2)
 - ▶ J3 and J4 connectors
 - ▶ 24MHz Crystal Oscillator
 - ▶ I/O Port-to-Pin Mapping
 - ▶ xTAG v3.0 Schematic
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1 Introduction

The xTAG v3.0 debug adapter converts between an XMOS xSYS connector and USB 2.0, providing pins for JTAG control, system reset, processor debug, one duplex UART link and one duplex serial XMOS Link. The xTAG v3.0 debug adapter can be used to connect XMOS development kits to most PCs, and provide a 5V power supply from a USB 2.0 port.

The diagram below shows the layout of the components on the card.

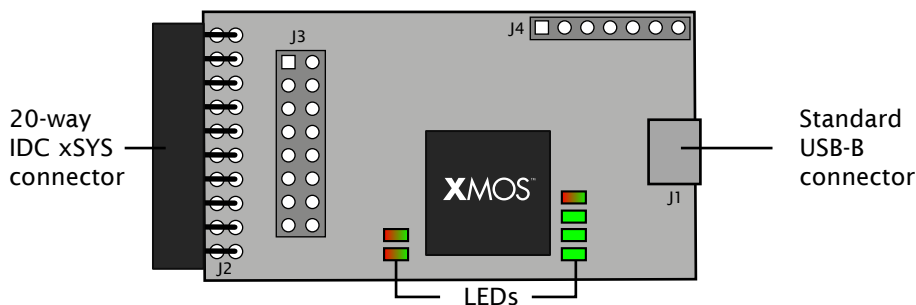


Figure 1:
xTAG v3.0
features

To debug a board with the xTAG v3.0 you must use xTIMEcomposer 13.1 or later, available from the XMOS web site: <http://xmos.com/downloads>.

The board requires an XMOS xSYS connector.

2 XS1-U8 device

The xTAG v3.0 is based on a single XS1-U8 device in a BGA package. The XS1-U8 consists of a single xCORE, which comprises a multicore microcontroller with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins are brought out of the package and connected to the card's components as follows:

- ▶ USB Connector (J1) The xTAG v3.0 uses a Standard B-type micro USB connector to link to a PC. The USB connector is connected to the XS1-U8 device.
- ▶ xSYS 20-way IDC header

The processor has ports that are directly connected to the I/O pins. Six LEDs are driven by the debugger, their function (clockwise, starting from the power button on the bottom right):

Power	Green	The xTAG is powered on
Run	Green	Target is running
	Red	Target is in debug mode and stopped
Status	Green	Target stop reason is expected e.g. breakpoint, print message
	Red	Target stop reason is unexpected e.g. exception
Target	Green	Target device is detected after a Run Configuration or Debug Configuration is used (xrun or xgdb command)
	Red	Target device is not detected after a Run Configuration or Debug Configuration is used (xrun or xgdb command)
xSCOPE	Green Flashing	xSCOPE is enabled
	Off	No xSCOPE
JTAG	Green	There is JTAG activity with the target happening
	Off	No JTAG

3 xSYS Connector (J2)

The xTAG v3.0 includes an xSYS 20-way IDC header, which can be used to connect it to an XMOS development board for debugging programs on the hardware.

The xSYS connector provides pins for JTAG control, system reset, processor debug, a duplex UART link and a 2-bit serial xCONNECT Link.

Pin	Signal	Direction	Description
1	5V	Target to Host	Power
2	NC	N/A	No connection
3	MSEL	Host to Target	Select boot from JTAG - Active Low
4	GND	N/A	Ground
5	TDSRC	Host to Target	JTAG Test Data
6	XL1_UP1	Target to Host	xCONNECT Link
7	TMS	Host to Target	JTAG Test Mode Select
8	GND	N/A	Ground
9	TCK	Host to Target	JTAG Test Clock
10	XL1_UP0	Target to Host	xCONNECT Link
11	DEBUG	Bidirectional	Debug
12	GND	N/A	Ground
13	TDSNK	Target to Host	JTAG Test Data
14	XL1_DN0	Host to Target	xCONNECT Link
15	RST_N	Host to Target	System Reset - Active Low
16	GND	N/A	Ground
17	UART_RX	Host to Target	Serial Port
18	XL1_DN1	Host to Target	xCONNECT Link
19	UART_TX	Target to Host	Serial Port
20	GND	N/A	Ground

The routing of these I/O pins along with the power pins is shown below.

3.1 xCONNECT Link configuration

Some of the I/O pins on the processor are configured as a duplex 2-bit serial xCONNECT Link. The mapping of xCONNECT Link to the pins is shown in the table below:

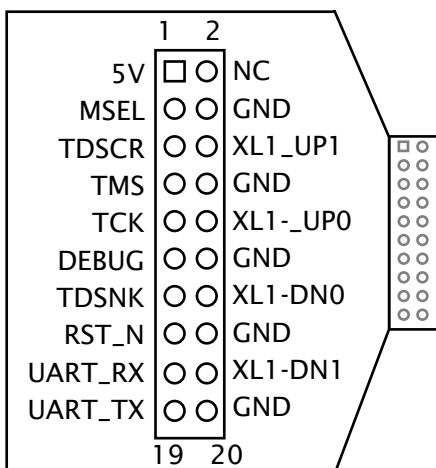


Figure 2:
xTAG v3.0
xSYS pinout

Pin	xCONNECT Link
X0D52	XL1_UP1
X0D53	XL1_UP0
X0D54	XL1_DN0
X0D55	XL1_DN1

3.2 JTAG Configuration

Some of the I/O pins on the microcontroller are driven by the JTAG signals. The mapping of the signals to the pins is shown in the table below:

Pin	Port	Processor
X0D11	P1D0	TDSRC
X0D13	P1F0	TDSNK
X0D22	P1G0	TMS
X0D10	P1C0	TCK
X0D70	P32A19	MSEL

3.3 System Reset

The system reset signal is mapped to a 1-bit port on the processor as described below. It is used as an output to reset the target processor from the debugger

Pin	Port	Processor
X0D50	P32A1	RST_N

4 J3 and J4 connectors

The xTAG v3.0 has two additional connectors. These are reserved for future use.

5 24MHz Crystal Oscillator

The XS1-U8 is clocked at 24MHz by a crystal oscillator on the card. The processor is clocked at 500MHz and the I/O ports at 100MHz, by an on-chip phase locked loop (PLL).

6 I/O Port-to-Pin Mapping

The table below provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port	8b	32b	Processor
X0D0	P1A0			UART_UP
X0D10	P1C0			TCK
X0D11	P1D0			TDSRC
X0D12	P1E0			
X0D13	P1F0			TDSNK
X0D14		P8B0		LED
X0D15		P8B1		LED
X0D16		P8B2		LED
X0D17		P8B3		LED
X0D18		P8B4		LED
X0D19		P8B5		LED
X0D20		P8B6		LED
X0D21		P8B7		LED
X0D22	P1G0			TMS
X0D50			P32A1	RST_N
X0D51			P32A2	DBG
X0D52			P32A3	XL1_UP1
X0D53			P32A4	XL1_UP0
X0D54			P32A5	XL1_DN0
X0D55			P32A6	XL1_DN1
X0D69			P32A19	UART_DN
X0D70			P32A20	MSEL

7 xTAG v3.0 Schematic

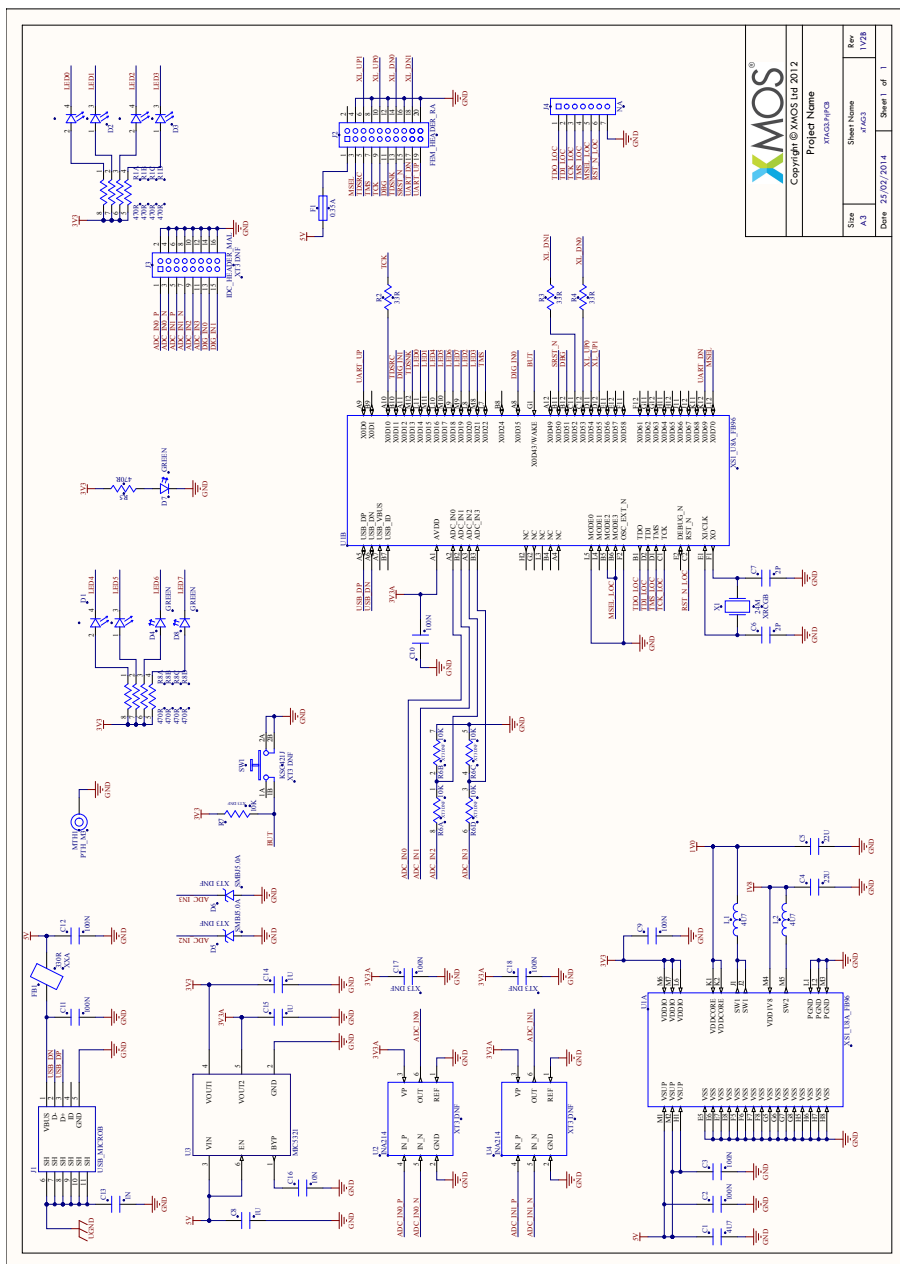


Figure 3:
xTAG v3.0
schematic

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