

## Thyristor/Thyristor (Super MAGN-A-PAK Power Modules), 570 A



Super MAGN-A-PAK


**RoHS**  
COMPLIANT

**FEATURES**

- High current capability
- High surge capability
- Industrial standard package
- 3000 V<sub>RMS</sub> isolating voltage with non-toxic substrate
- Designed and qualified for industrial level
- UL approved file E78996 
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

**TYPICAL APPLICATIONS**

- Motor starters
- DC motor controls - AC motor controls
- Uninterruptible power supplies

**PRIMARY CHARACTERISTICS**

$I_{T(AV)}$	570 A
Type	Modules - thyristor, standard
Package	Super MAGN-A-PAK

**MAJOR RATINGS AND CHARACTERISTICS**

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$	$T_C = 85\text{ }^\circ\text{C}$	570	A
$I_{T(RMS)}$	$T_C = 85\text{ }^\circ\text{C}$	894	
$I_{TSM}$	50 Hz	18 000	
	60 Hz	18 800	
$I^2t$	50 Hz	1620	kA <sup>2</sup> s
	60 Hz	1473	
$I^2\sqrt{t}$		16 200	kA <sup>2</sup> $\sqrt{s}$
$V_{DRM}/V_{RRM}$		1600	V
$T_{Stg}$	Range	-40 to +125	°C
$T_J$	Range	-40 to +135	

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}/I_{DRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-VSKT570-16PbF	16	1600	1700	110



ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			570	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave at $T_C = 85\text{ °C}$			894	A
Maximum peak, one-cycle, non-repetitive on-state surge current	$I_{TSM}, I_{FSM}$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	18.0	kA
		t = 8.3 ms			18.8	
		t = 10 ms	100 % $V_{RRM}$ reapplied		15.1	
		t = 8.3 ms			15.8	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied		1620	kA <sup>2</sup> s
		t = 8.3 ms			1473	
		t = 10 ms	100 % $V_{RRM}$ reapplied		1146	
		t = 8.3 ms			1042	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			16 200	kA <sup>2</sup> √s
Low level value or threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			0.59	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			0.63	
Low level value on-state slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			0.41	mΩ
High level value on-state slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			0.38	
Maximum on-state voltage drop	$V_{TM}$	$I_{pk} = 1500\text{ A}$ , $T_J = 25\text{ °C}$ , $t_p = 10\text{ ms}$ sine pulse			1.36	V
Maximum holding current	$I_H$	$T_J = 25\text{ °C}$ , anode supply 12 V resistive load			500	mA
Maximum latching current	$I_L$				1000	

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum rate of rise of turned-on current	$di/dt$	$T_J = T_J$ maximum, $I_{TM} = 400\text{ A}$ , $V_{DRM}$ applied			1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$ , $T_J = 25\text{ °C}$			2.0	μs
Typical turn-off time	$t_q$	$I_{TM} = 750\text{ A}$ ; $T_J = T_J$ maximum, $di/dt = -60\text{ A}/\mu\text{s}$ , $V_R = 50\text{ V}$ , $dV/dt = 20\text{ V}/\mu\text{s}$ , gate 0 V 100 Ω			65 to 240	

BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum, linear to $V_D = 80\% V_{DRM}$			1000	V/μs
RMS insulation voltage	$V_{INS}$	t = 1 s			3000	V
Maximum peak reverse and off-state leakage current	$I_{RRM}, I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied			110	mA



TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	W
Maximum peak average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0	
Maximum peak positive gate current	$+I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum peak positive gate voltage	$+V_{GM}$		20	
Maximum peak negative gate voltage	$-V_{GM}$		5.0	
Maximum DC gate current required to trigger	$I_{GT}$	$T_J = 25$ °C, $V_{ak} 12$ V	200	mA
DC gate voltage required to trigger	$V_{GT}$		3.0	V
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	10	mA
DC gate voltage not to trigger	$V_{GD}$		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	$T_J$		-40 to +135	°C
Maximum storage temperature range	$T_{Stg}$		-40 to +125	
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	0.06	K/W
Maximum thermal resistance, case to heatsink per module	$R_{thC-hs}$	Mounting surface smooth, flat and greased	0.02	
Mounting torque $\pm 10$ %	Super MAGN-A-PAK to heatsink busbar to super MAGN-A-PAK	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound	6 to 8	Nm
			12 to 15	
Approximate weight			1500	g
Case style		See dimensions (link at the end of datasheet)	Super MAGN-A-PAK	

$\Delta R_{thJC}$ CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006	$T_J = T_J$ maximum	K/W
120°	0.011	0.011		
90°	0.014	0.015		
60°	0.021	0.022		
30°	0.037	0.038		

**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

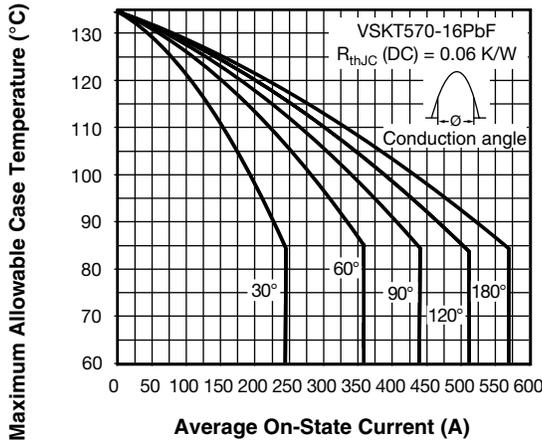


Fig. 1 - Current Ratings Characteristics

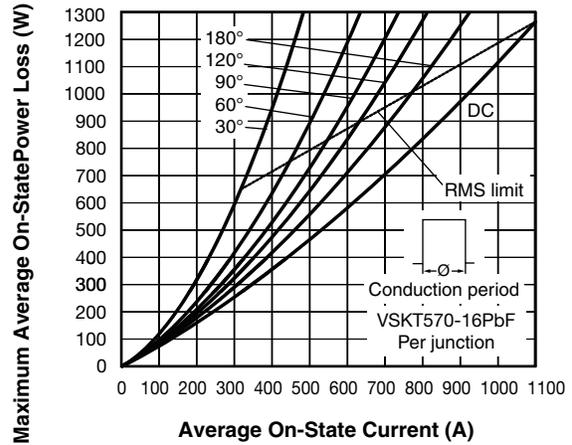


Fig. 4 - On-State Power Loss Characteristics

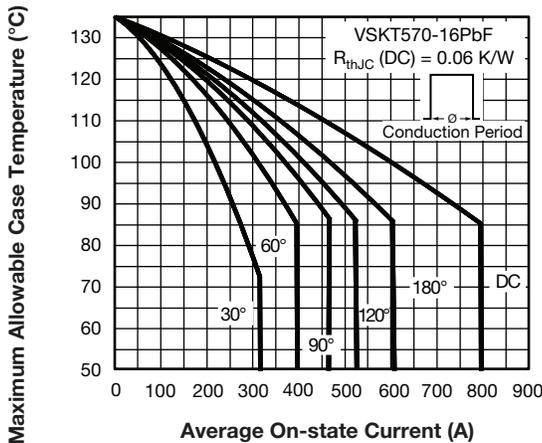


Fig. 2 - Current Ratings Characteristics

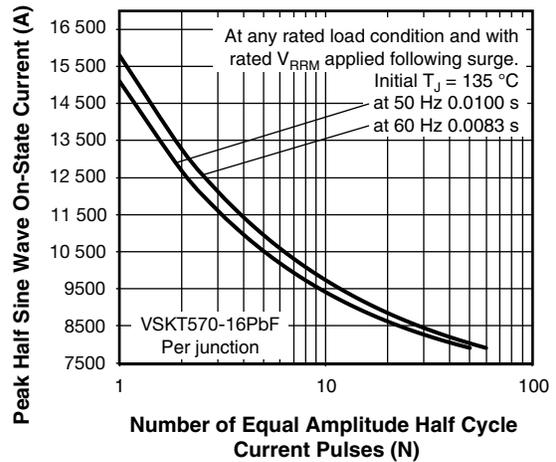


Fig. 5 - Maximum Non-Repetitive Surge Current

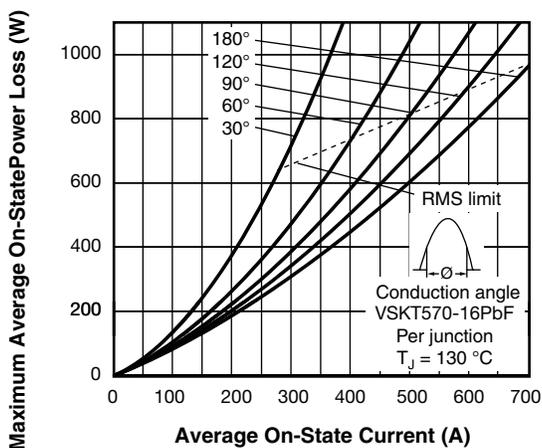


Fig. 3 - On-State Power Loss Characteristics

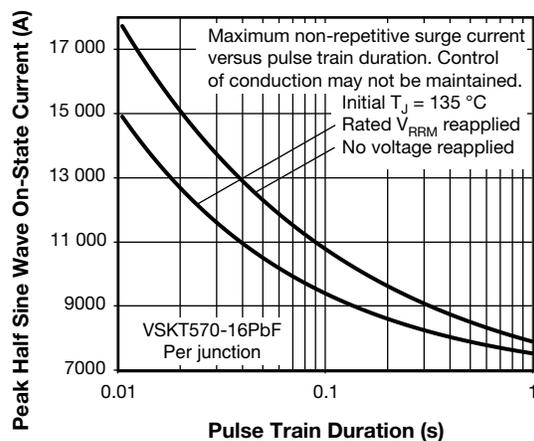


Fig. 6 - Maximum Non-Repetitive Surge Current

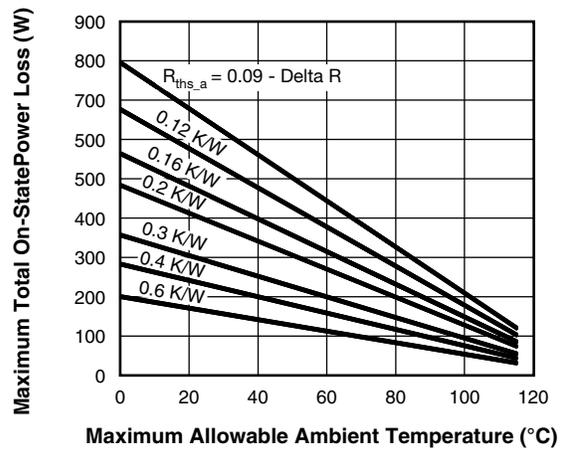
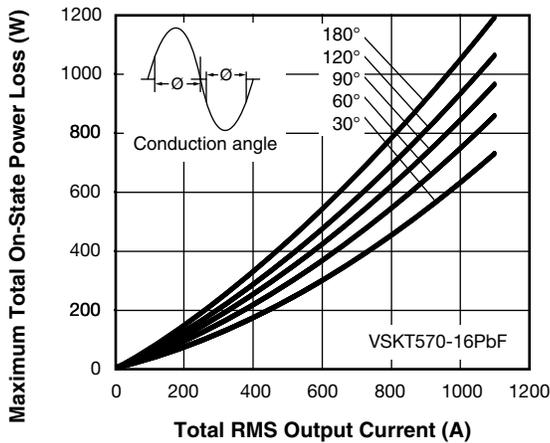


Fig. 7 - On-State Power Loss Characteristics

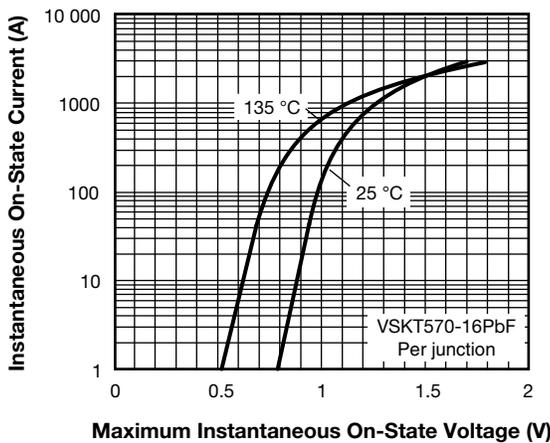


Fig. 8 - On-State Voltage Drop Characteristics

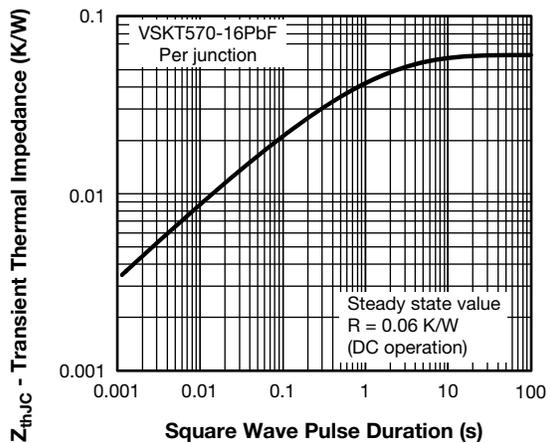


Fig. 9 - Thermal Impedance  $Z_{thJC}$  Characteristics

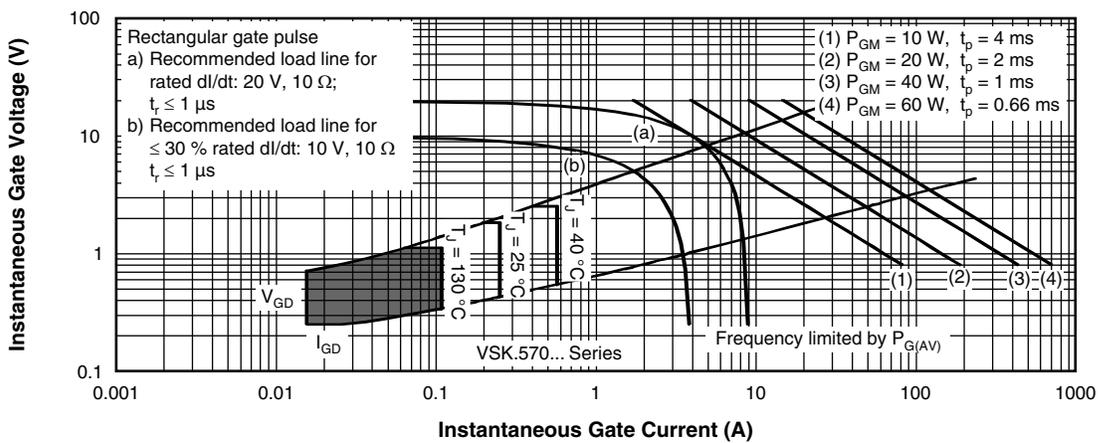


Fig. 10 - Gate Characteristics



**ORDERING INFORMATION TABLE**

Device code	<b>VS-VS</b>	<b>KT</b>	<b>570</b>	<b>-</b>	<b>16</b>	<b>PbF</b>
	①	②	③		④	⑤

- 1** - Vishay Semiconductors product
- 2** - Circuit configuration (see below)
- 3** - Current rating
- 4** - Voltage code x 100 =  $V_{RRM}$
- 5** - Lead (Pb)-free

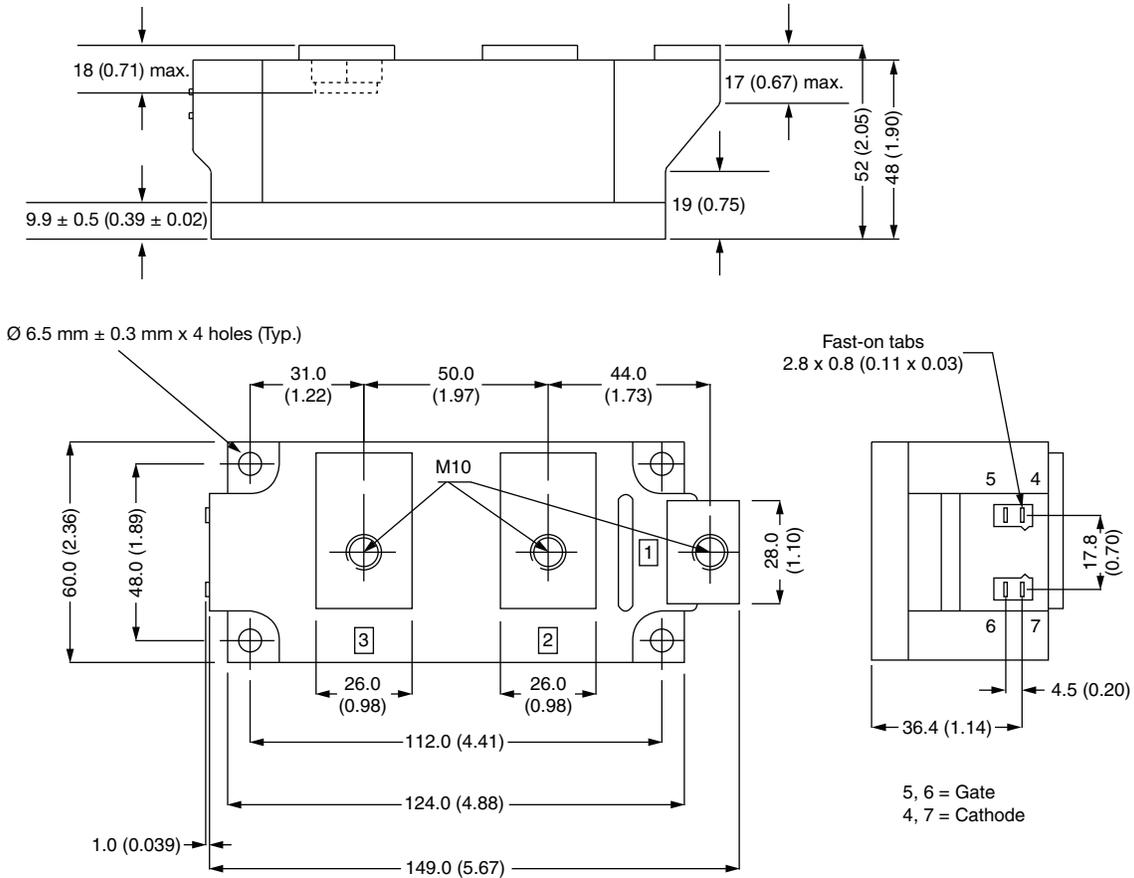
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	KT	

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95283">www.vishay.com/doc?95283</a>



## Super MAGN-A-PAK Thyristor/Diode

**DIMENSIONS** in millimeters (inches)





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