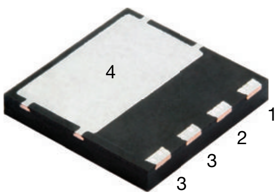
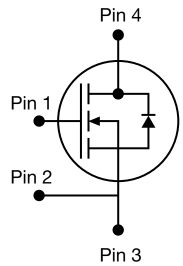
EF Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.310
Q_g max. (nC)	62	
Q_{gs} (nC)	7	
Q_{gd} (nC)	13	
Configuration	Single	

PowerPAK® 8 x 8





N-Channel MOSFET

FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Completely lead (Pb)-free device
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH11N60EF-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	11	A
		T_C = 100 °C		7	
Pulsed Drain Current [a]			I_{DM}	27	
Linear Derating Factor				0.9	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	127	mJ
Maximum Power Dissipation			P_D	114	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse Diode dV/dt [c]				28	

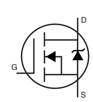
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 3 A.

c. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	42	55	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.76	1.10	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 10 mA	-	0.66	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 480 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	50	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.5 A	-	0.310	0.357	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 5.5 A	-	3.7	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1078	-	pF
Output Capacitance	C_{oss}		-	57	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	35	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$		-	145	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 480 V	-	31	62	nC
Gate-Source Charge	Q_{gs}		-	7	-	
Gate-Drain Charge	Q_{gd}		-	13	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 5.5 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	16	32	ns
Rise Time	t_r		-	21	42	
Turn-Off Delay Time	$t_{d(off)}$		-	39	68	
Fall Time	t_f		-	21	42	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.2	0.7	1.5	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	11	A
Pulsed Diode Forward Current	I_{SM}		-	-	27	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 5.5 A, V_{GS} = 0 V	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 5.5 A, dI/dt = 100 A/μs, V_R = 25 V	-	114	228	ns
Reverse Recovery Charge	Q_{rr}		-	0.56	1.12	μC
Reverse Recovery Current	I_{RRM}		-	9.5	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

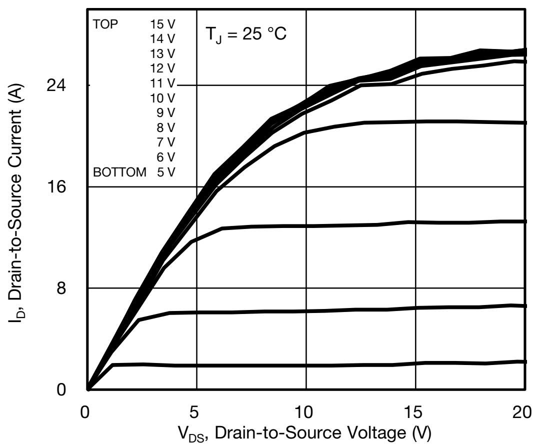


Fig. 1 - Typical Output Characteristics

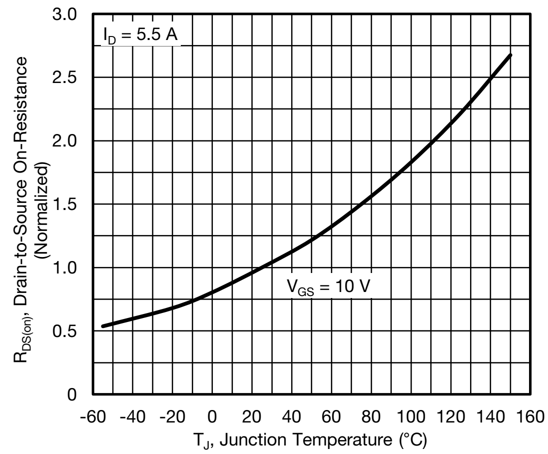


Fig. 4 - Normalized On-Resistance vs. Temperature

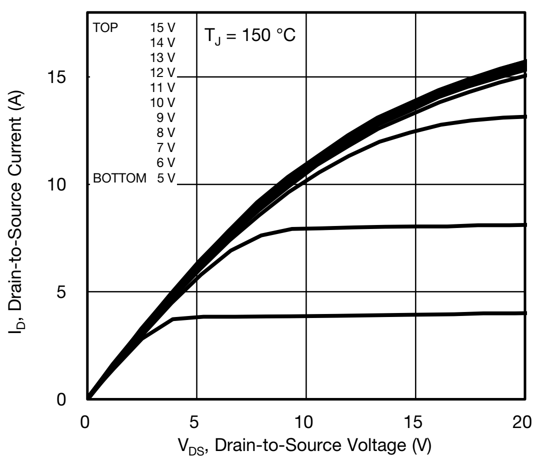


Fig. 2 - Typical Output Characteristics

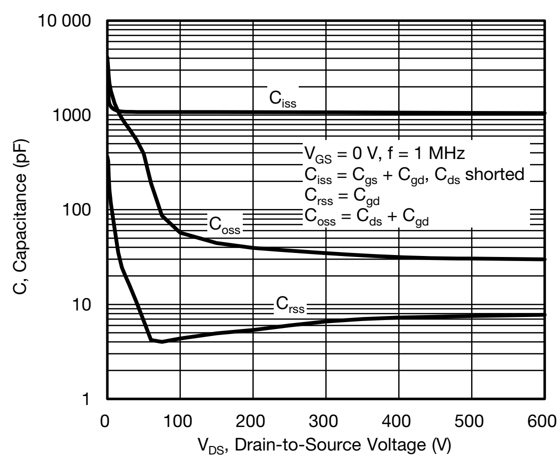


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

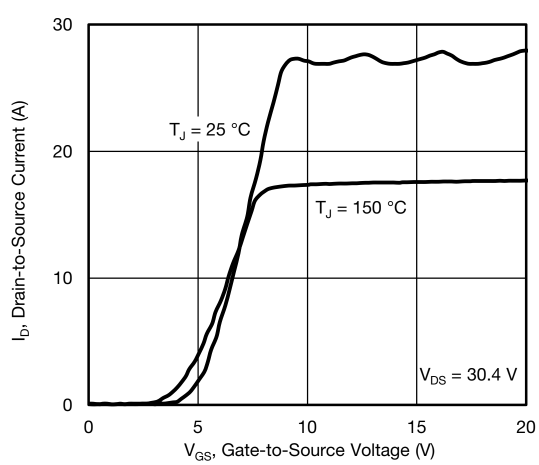


Fig. 3 - Typical Transfer Characteristics

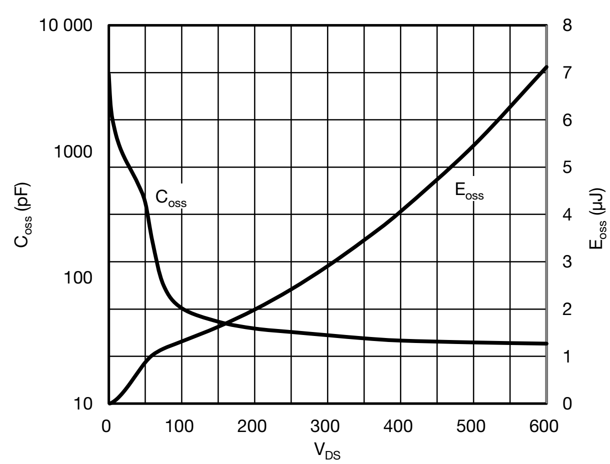


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

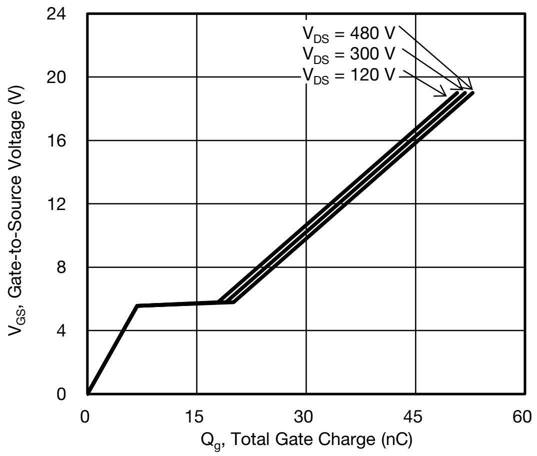


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

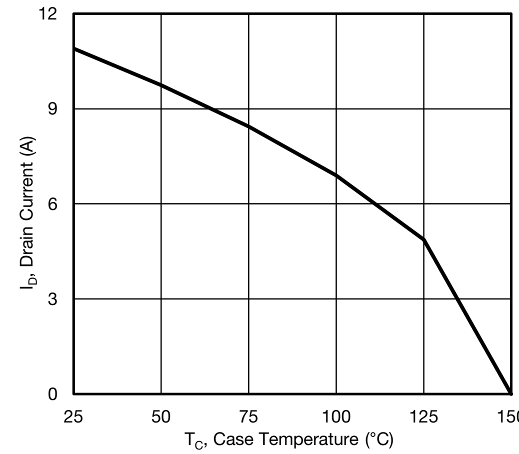


Fig. 10 - Maximum Drain Current vs. Case Temperature

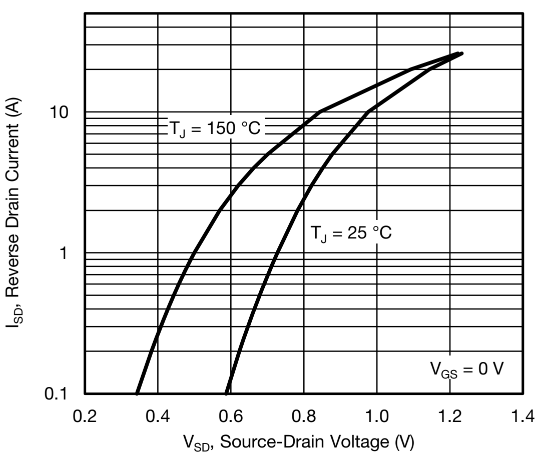


Fig. 8 - Typical Source-Drain Diode Forward Voltage

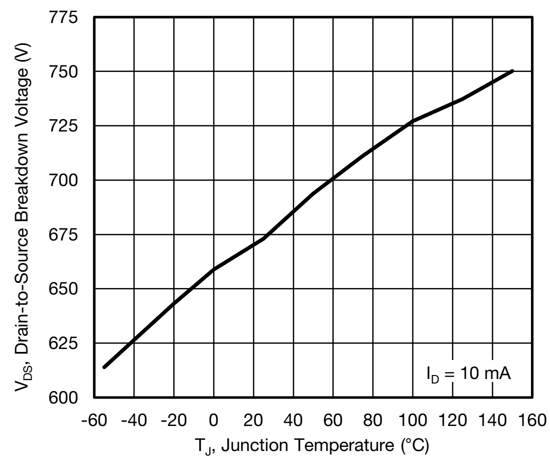
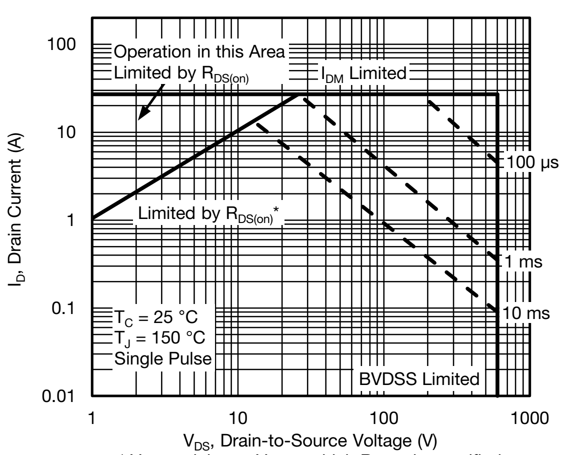


Fig. 11 - Temperature vs. Drain-to-Source Voltage



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

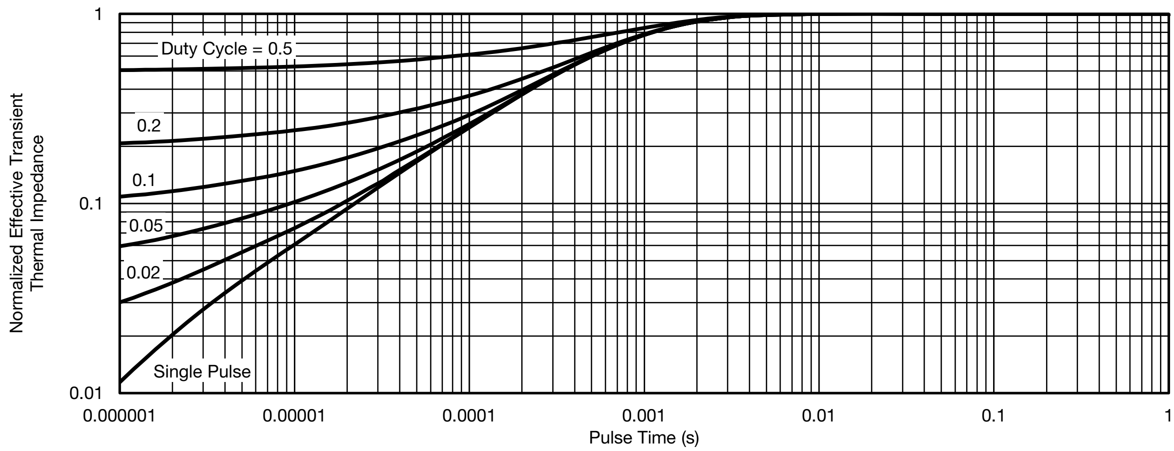


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

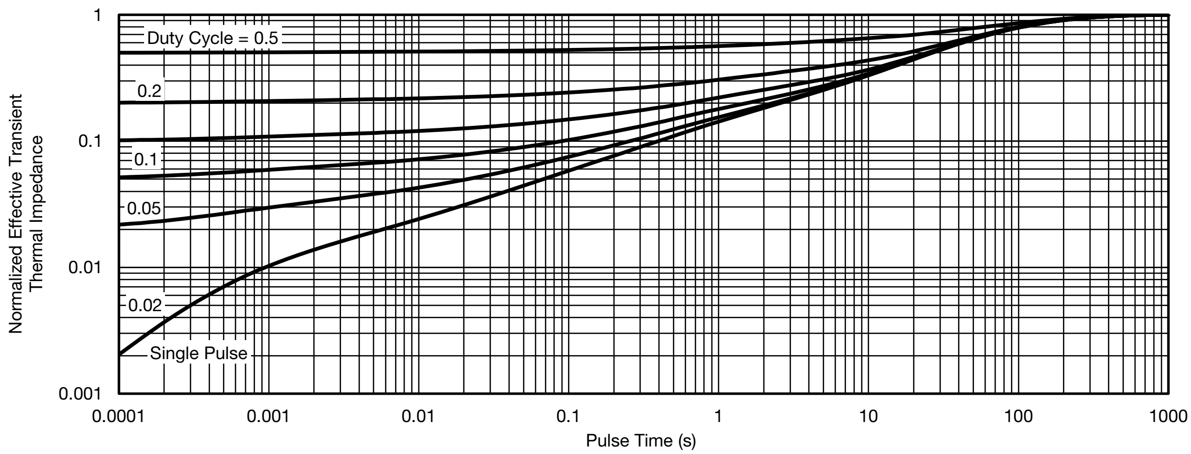


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

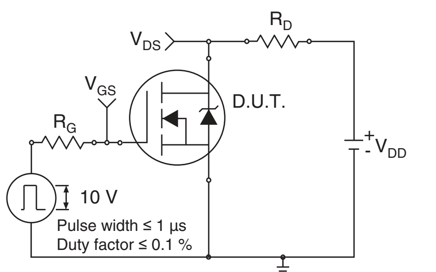


Fig. 14 - Switching Time Test Circuit

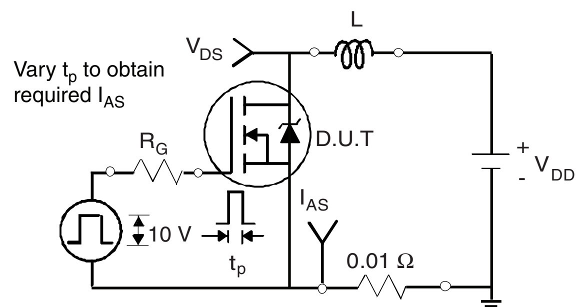


Fig. 16 - Unclamped Inductive Test Circuit

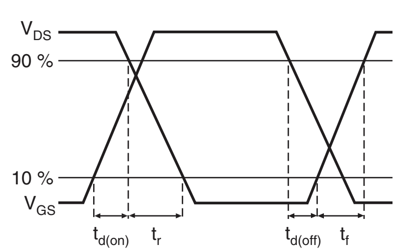


Fig. 15 - Switching Time Waveforms

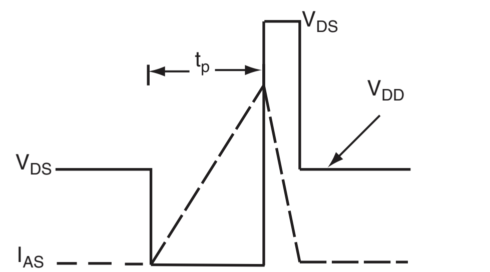


Fig. 17 - Unclamped Inductive Waveforms

For technical questions, contact: hvm@vishay.com

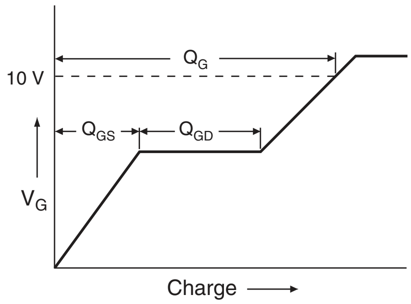


Fig. 18 - Basic Gate Charge Waveform

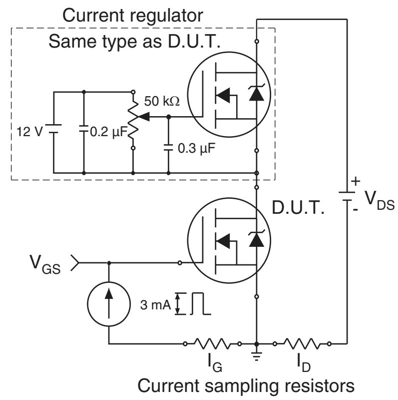
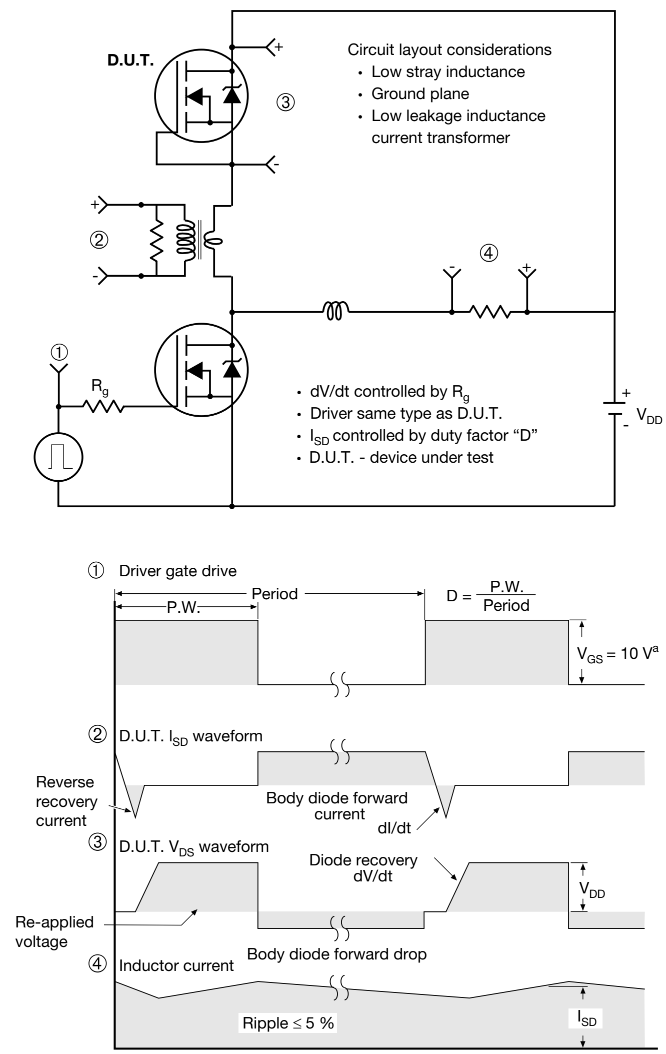


Fig. 19 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



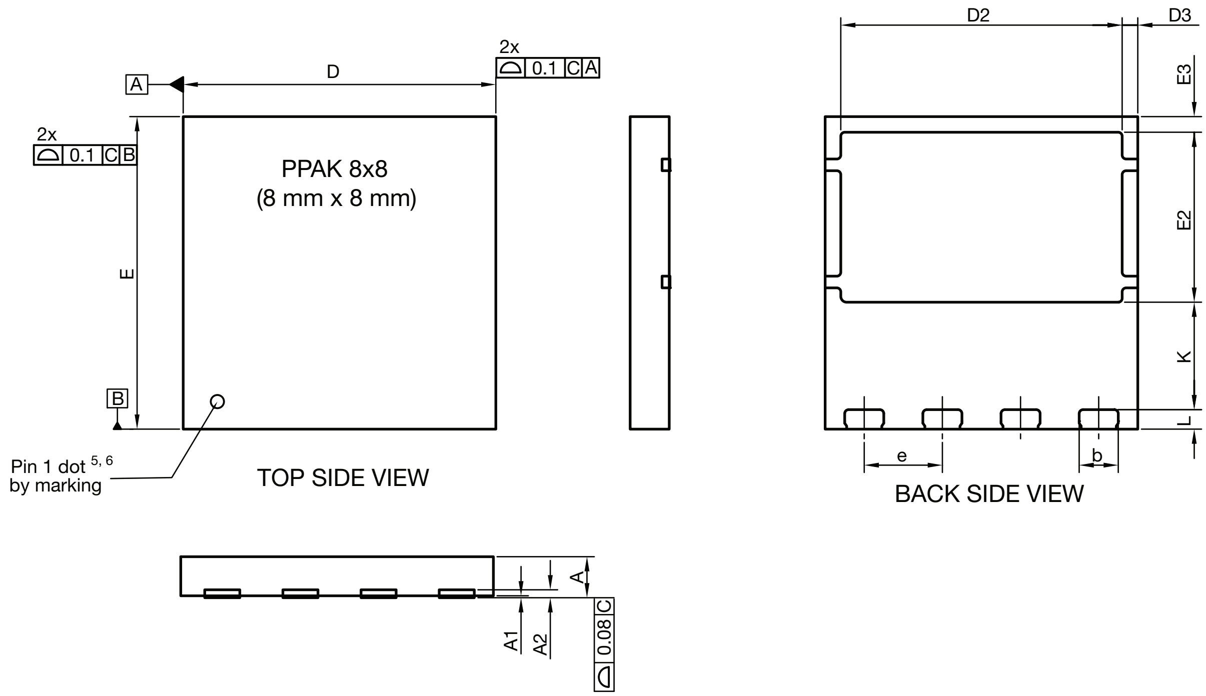
Note

a. V_{GS} = 5 V for logic level devices

Fig. 20 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91726.

PowerPAK® 8 x 8 Case Outline



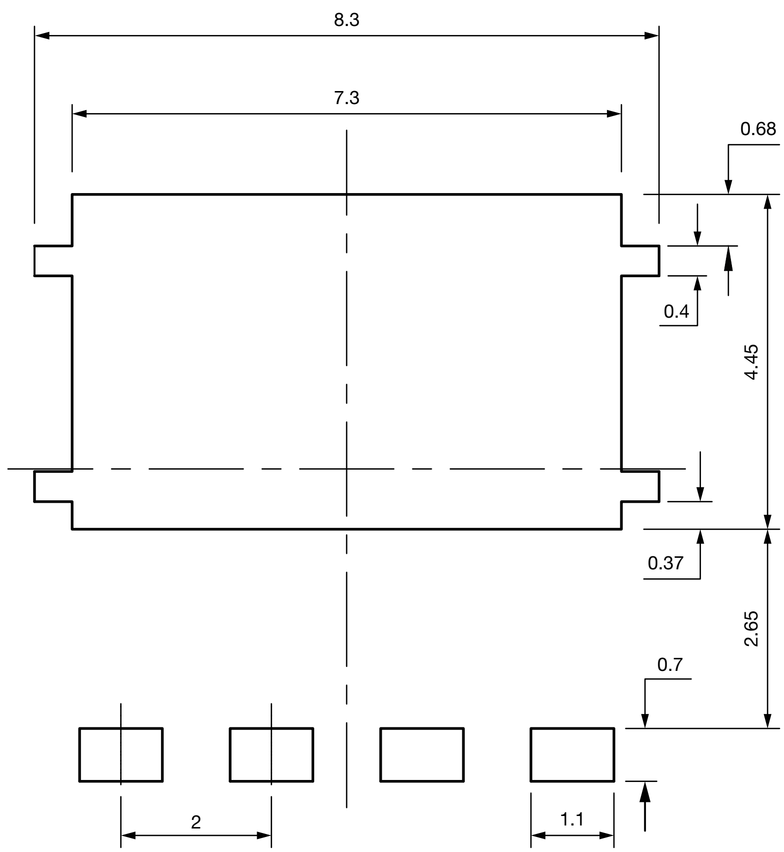
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b [4]	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N [3]	8			8		

Notes

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5 M - 1994.
3. N is the number of terminals.
4. Package warpage max. 0.08 mm.
5. The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.

ECN: T15-0225-Rev. A, 18-May-15
DWG: 6041

Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters

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