

P-Channel 200V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)		-200
$R_{DS(on)}$ (Ω)	$V_{GS} = -10\text{ V}$	2.0
Q_g max. (nC)		29
Q_{gs} (nC)		5.4
Q_{gd} (nC)		15
Configuration		Single

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling



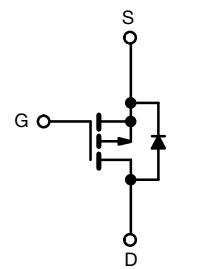
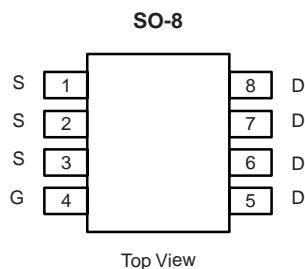
RoHS*

Available

HALOGEN

FREE

Available



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-200	
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	V_{GS} at -10 V	I_D	-3.6	
			-2.5	A
Pulsed Drain Current ^a		I_{DM}	-12	
Linear Derating Factor			0.59	
Linear Derating Factor (PCB mount) ^e			0.025	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b		E_{AS}	500	mJ
Avalanche Current ^a		I_{AR}	-6.4	A
Repetitive Avalanche Energy ^a		E_{AR}	7.4	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	74	
Maximum Power Dissipation (PCB mount) ^e	$T_A = 25\text{ }^\circ\text{C}$		3.0	W
Peak Diode Recovery dV/dt ^c		dV/dt	-5.0	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	
Soldering Recommendations (Peak temperature) ^d	for 10 s		300	$^\circ\text{C}$

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 17\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -6.5\text{ A}$ (see fig. 12).
- $I_{SD} \leq -6.5\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = -250 \mu\text{A}$		-200	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$, $I_D = -1 \text{ mA}$		-	-0.24	-	$\text{V}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$		-1.5	-	-4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 10	μA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	-100	μA	
		$V_{DS} = -160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	-500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10 \text{ V}$	$I_D = -1.0 \text{ A}^b$	-	2.00	-	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = -50 \text{ V}$	$I_D = -1.0 \text{ A}^b$	2.8	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = -25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	700	-	pF	
Output Capacitance	C_{oss}			-	200	-		
Reverse Transfer Capacitance	C_{rss}			-	40	-		
Total Gate Charge	Q_g	$V_{GS} = -10 \text{ V}$	$I_D = -3.5 \text{ A}$, $V_{DS} = -160 \text{ V}$, see fig. 6 and 13 ^b	-	-	29	nC	
Gate-Source Charge	Q_{gs}			-	-	5.4		
Gate-Drain Charge	Q_{gd}			-	-	15		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100 \text{ V}$, $I_D = -3.5 \text{ A}$, $R_g = 12 \Omega$, $R_D = 15 \Omega$, see fig. 10 ^b		-	12	-	ns	
Rise Time	t_r			-	27	-		
Turn-Off Delay Time	$t_{d(off)}$			-	28	-		
Fall Time	t_f			-	24	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		0.6	-	3.7	Ω	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-3 .5	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-6		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = -3.5 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	-6.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = -3.5 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ ^b		-	200	300	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.9	2.9	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

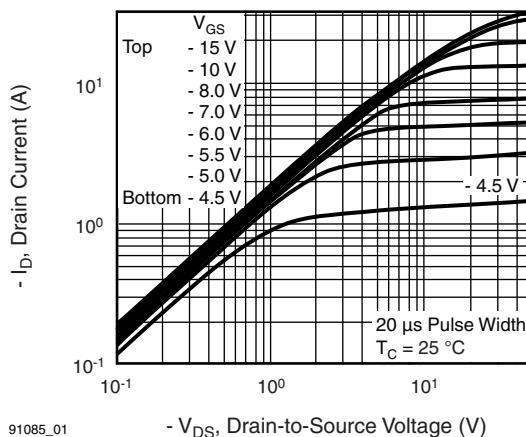
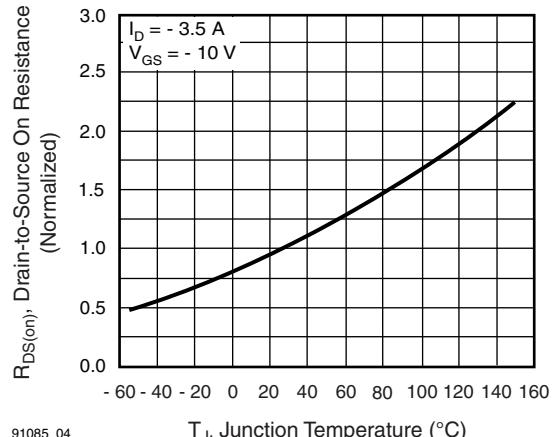
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature

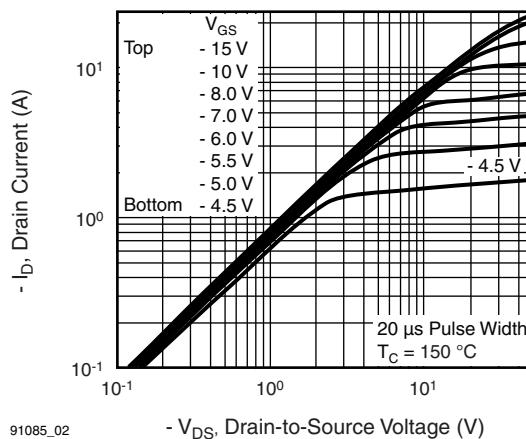
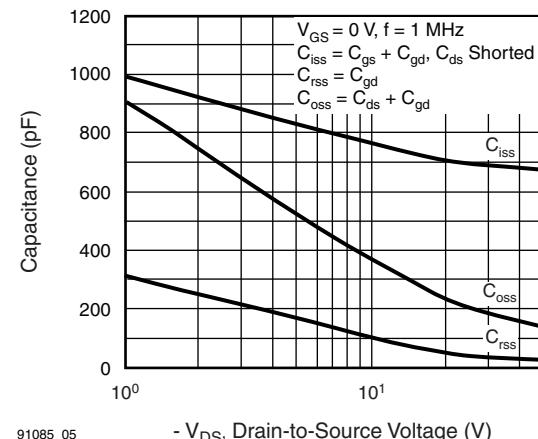
Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$ 

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

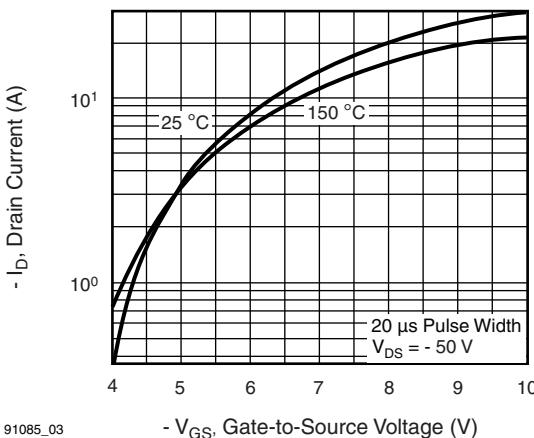


Fig. 3 - Typical Transfer Characteristics

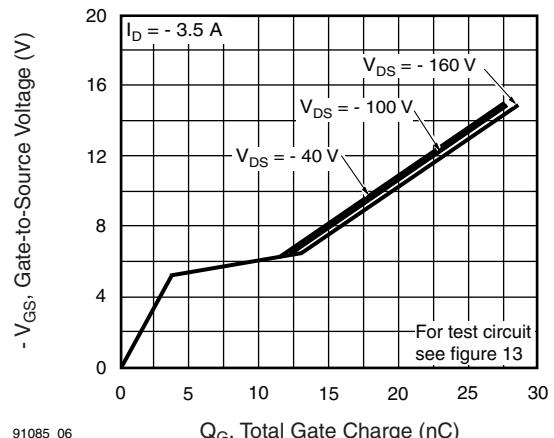
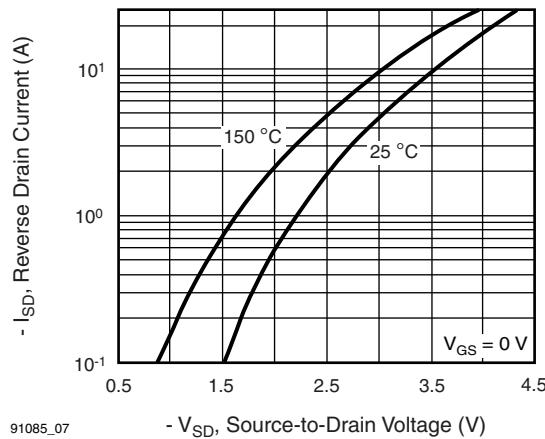
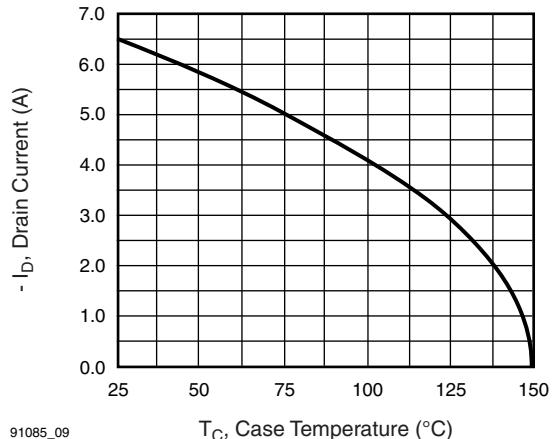


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



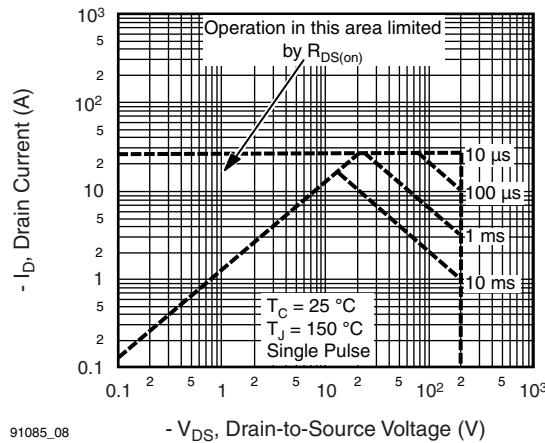
91085_07 - V_{SD} , Source-to-Drain Voltage (V)

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91085_09 - T_C , Case Temperature (°C)

Fig. 9 - Maximum Drain Current vs. Case Temperature



91085_08 - V_{DS} , Drain-to-Source Voltage (V)

Fig. 8 - Maximum Safe Operating Area

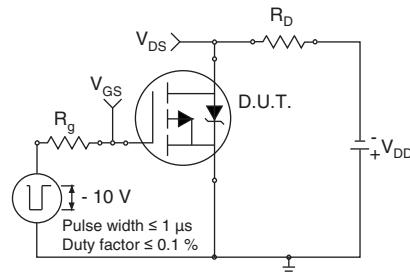


Fig. 10a - Switching Time Test Circuit

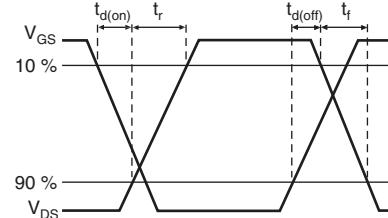
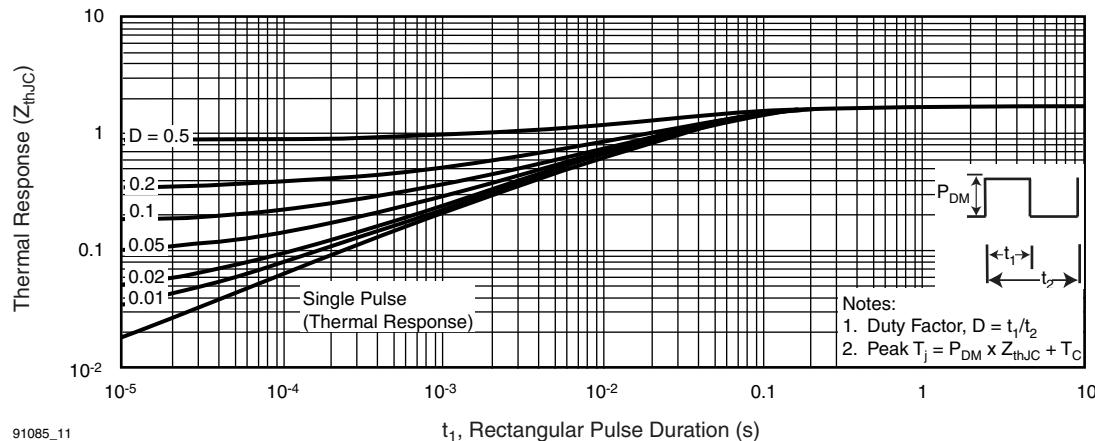


Fig. 10b - Switching Time Waveforms



91085_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

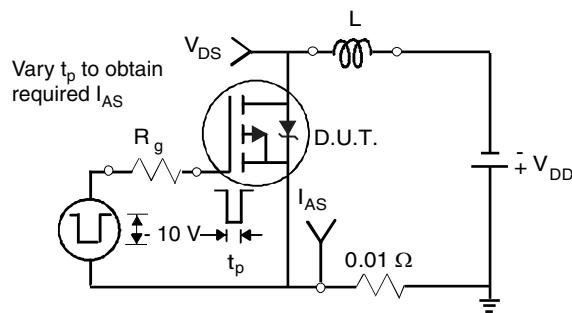


Fig. 12a - Unclamped Inductive Test Circuit

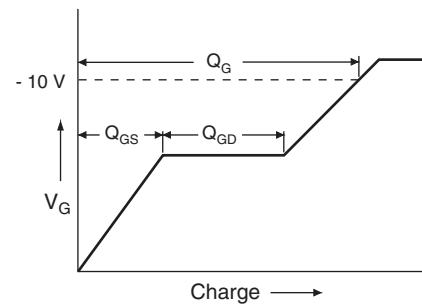


Fig. 13a - Basic Gate Charge Waveform

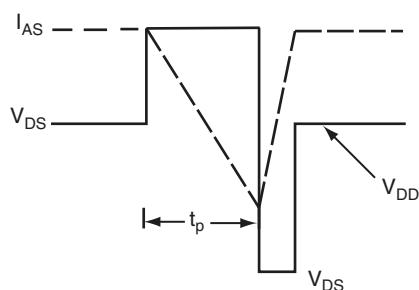


Fig. 12b - Unclamped Inductive Waveforms

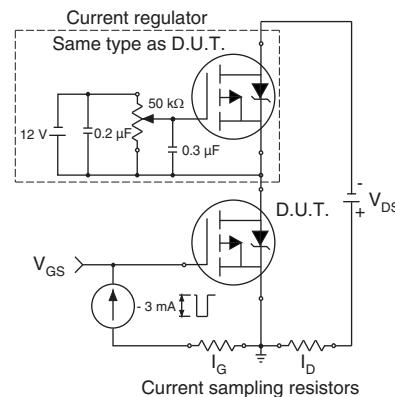


Fig. 13b - Gate Charge Test Circuit

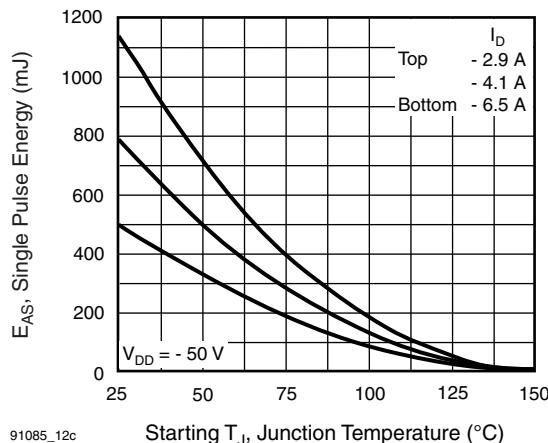
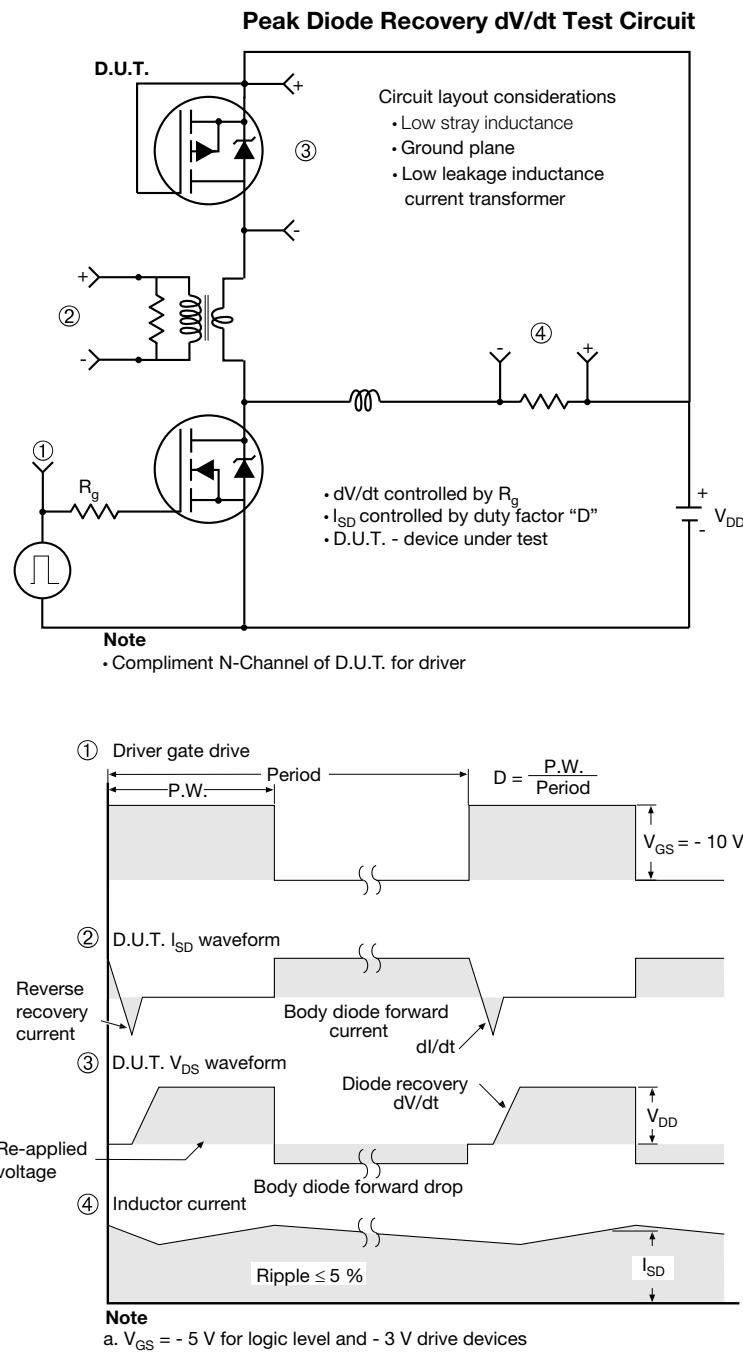
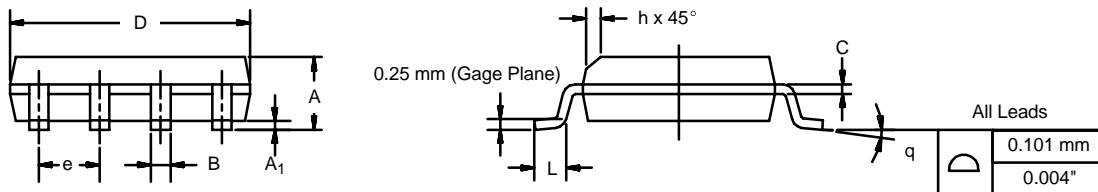
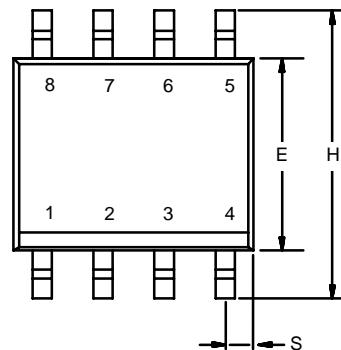


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

**Fig. 14 - For P-Channel**

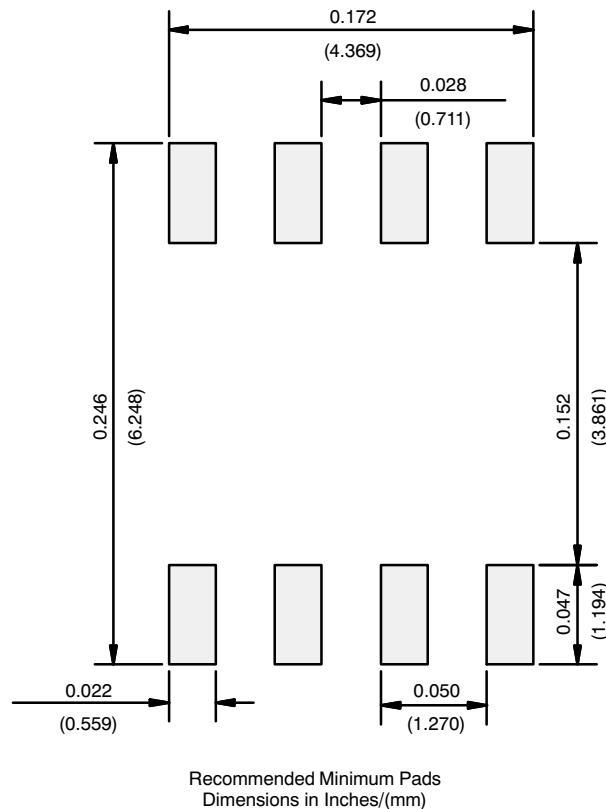
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8

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