

SQM40031EL_GE3-VB Datasheet P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	- 40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.006			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.007			
I _D (A)	-80			
Configuration	Single			

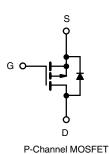
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- SGT technology Power MOSFET
- Package with Low Thermal Resistance
- \bullet 100 % R_{g} and UIS Tested
- Compliant to RoHS Directive 2002/95/EC









ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	d)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	- 40	V	
Gate-Source Voltage	V _{GS}	± 20	V	
Continuous Drain Current	T _C = 25 °C	I-	-80	
	T _C = 125 °C	I _D	-50	
Continuous Source Current (Diode Conducti	I _S	-70	Α	
Pulsed Drain Current ^b	I _{DM}	-240		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	-70	
Single Pulse Avalanche Energy	L = 0.1 MH	E _{AS}	1345	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	250	10/
	T _C = 125 °C		100	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	50	°C/W		
Junction-to-Case (Drain)		R _{thJC}	0.6	C/VV		

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static				L	L	L	l	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		- 40	-	-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = - 250 μA	- 1.0	-	-3.0	V	
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = - 40 V	-	-	- 1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = - 40 V, T _J = 125 °C	-	-	- 50	μA	
		$V_{GS} = 0 V$	$V_{DS} = -40 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	-	-	- 250		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V	$V_{DS} \le -5 V$	- 30	-	-	Α	
		V _{GS} = - 10 V	I _D = - 20 A	-	0.006	-	Ω	
Dunin Course On Chata Basistanas	D	V _{GS} = - 10 V	I _D = - 20 A, T _J = 125 °C	-	0.006	-		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 20 A, T _J = 175 °C	-	0.011	-		
		V _{GS} = - 4.5 V	I _D = -20 A	-	0.005	-		
Forward Transconductance ^b	9 _{fs}	V _{DS} = - 15 V, I _D = -20 A		=.	35		S	
Dynamic ^b								
Input Capacitance	C _{iss}			=.	8000	-		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$	-	301	-	pF	
Reverse Transfer Capacitance	C _{rss}			=.	208	-		
Total Gate Charge ^c	Qg			=.	96	144		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = - 10 V	$V_{DS} = -50V, I_{D} = -9.2 A$	-	8.4	-	nC	
Gate-Drain Charge ^c	Q _{gd}	7		-	23.5	-		
Gate Resistance	R_{g}	f = 1 MHz		1.5	3.13	4.7	Ω	
Turn-On Delay Time ^c	t _{d(on)}				11	17		
Rise Time ^c	t _r	V_{DD} = - 50 V, R_{L} = 6.49 Ω $I_{D} \cong$ - 7.7 A, V_{GEN} = - 10 V, R_{g} = 1.0 Ω		-	11	17	- ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	78	117		
Fall Time ^c	t _f			-	15	23		
Source-Drain Diode Ratings and Chara	acteristics ^b	•						
Pulsed Current ^a	I _{SM}			-	_	- 240	Α	
Forward Voltage	V_{SD}	I _F = - 7.7 A, V _{GS} = 0 V		_	- 0.8	- 1.5	V	

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Typical Electrical and Thermal Characteristics

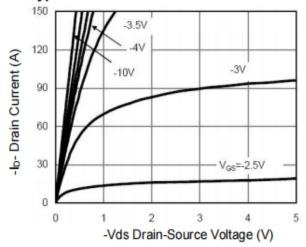


Figure 1 Output Characteristics

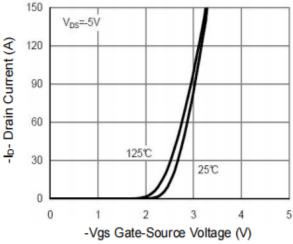
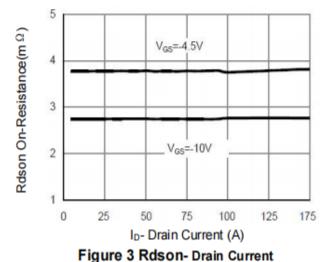


Figure 2 Transfer Characteristics



1.8

1.6

V_{os}=10V
I_p=.75A

1.2

V_{os}=4.5V
I_p=.75A

1.3

V_{os}=4.5V
I_p=.75A

T_J-Junction Temperature(°C)

Figure 4 Rdson-JunctionTemperature

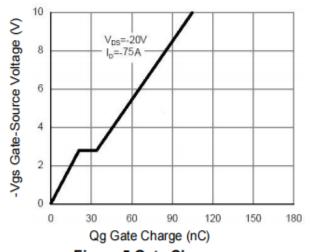


Figure 5 Gate Charge

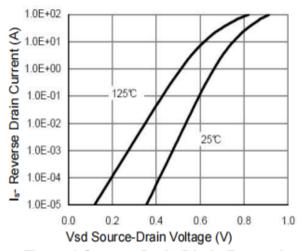


Figure 6 Source- Drain Diode Forward

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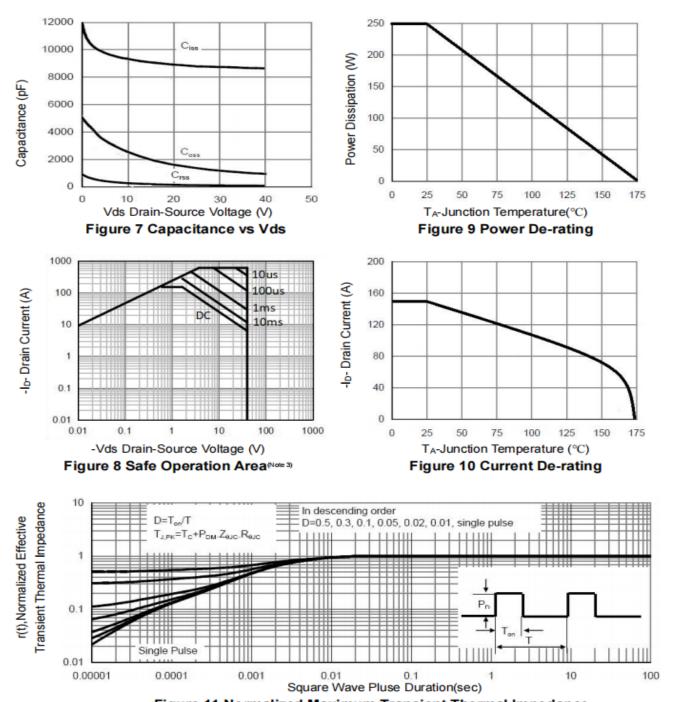
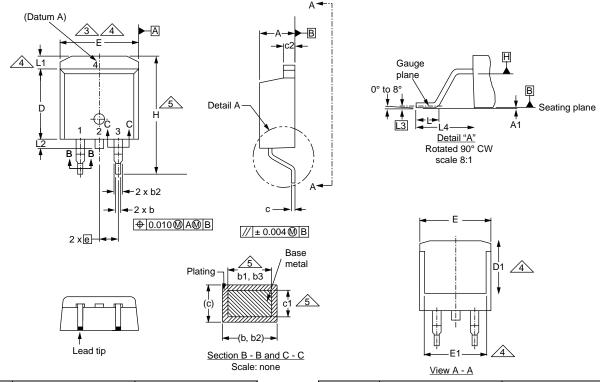


Figure 11 Normalized Maximum Transient Thermal Impedance

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TO-263



	MILLIN	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
Е	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
е	2.54	BSC	0.100 BSC	
Н	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010	BSC
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08 DWG: 5970

- 1. Dimensioning and tolerancing per ASME Y14.5M.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.



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