

Dual N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

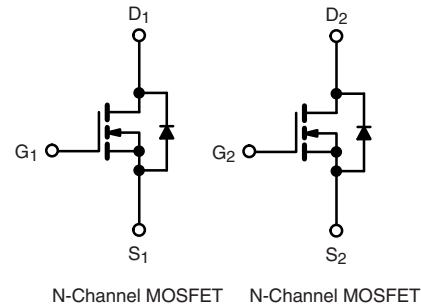
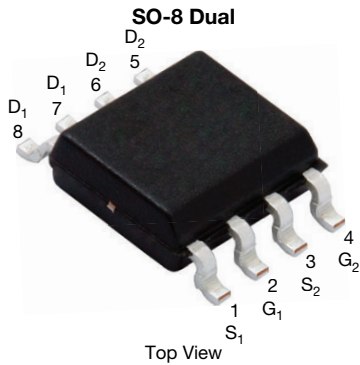
V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.028
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.030
I_D (A) per leg	7
Configuration	Dual

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Continuous Source Current (Diode Conduction) ^a	I_S	3.6	
Pulsed Drain Current ^b	I_{DM}	28	
Single Pulse Avalanche Current	I_{AS}	18	
Single Pulse Avalanche Energy	E_{AS}	16.2	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	W
		$T_C = 125$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	110	°C/W
Junction-to-Foot (Drain)	R_{thJF}	34	

Notes

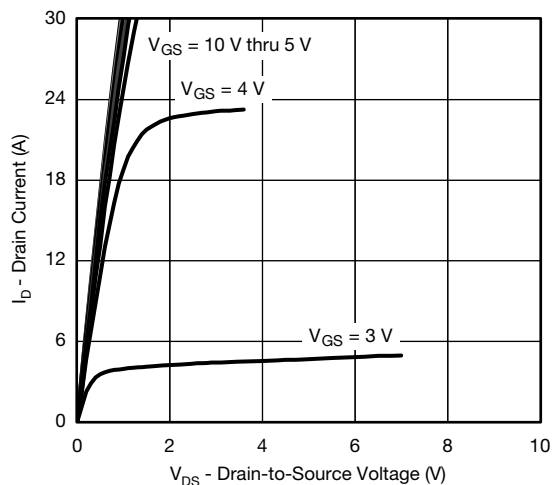
- a. Package limited.
 b. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
 c. When mounted on 1" square PCB (FR4 material).

SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2.0	2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	20	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.5 A-		0.028	-	Ω
		V _{GS} = 10 V	I _D = 4.5 A, T _J = 125 °C	-	0.066	-	
		V _{GS} = 10 V	I _D = 4.5 A, T _J = 175 °C	-	0.081	-	
		V _{GS} = 4.5 V	I _D = 4 A-		0.030	-	
Forward Transconductance ^f	g _{fs}	V _{DS} = 15 V, I _D = 4.5 A		-	15	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	600	750	pF
Output Capacitance	C _{oss}			-	110	140	
Reverse Transfer Capacitance	C _{rss}			-	50	62	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 30 V, I _D = 5.3 A	-	11.7	18	nC
Gate-Source Charge ^c	Q _{gs}			-	1.8	2.7	
Gate-Drain Charge ^c	Q _{gd}			-	2.8	4.2	
Gate Resistance	R _g	f = 1 MHz		1.3	-	6	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 6.8 Ω I _D ≅ 4.4 A, V _{GEN} = 10 V, R _g = 1 Ω		-	7	11	ns
Rise Time ^c	t _r			-	3.3	5	
Turn-Off Delay Time ^c	t _{d(off)}			-	22.4	33.5	
Fall Time ^c	t _f			-	2.1	3.2	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	28	A
Forward Voltage	V _{SD}	I _F = 2 A, V _{GS} = 0 V		-	0.75	1.1	V

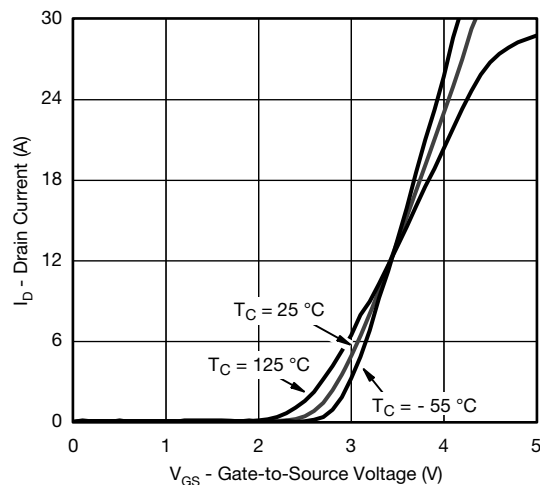
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

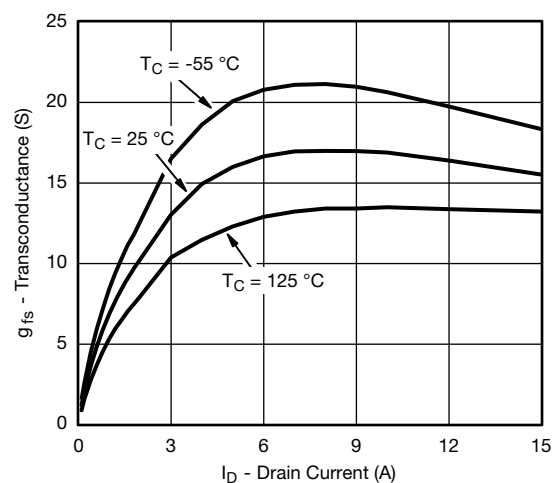
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



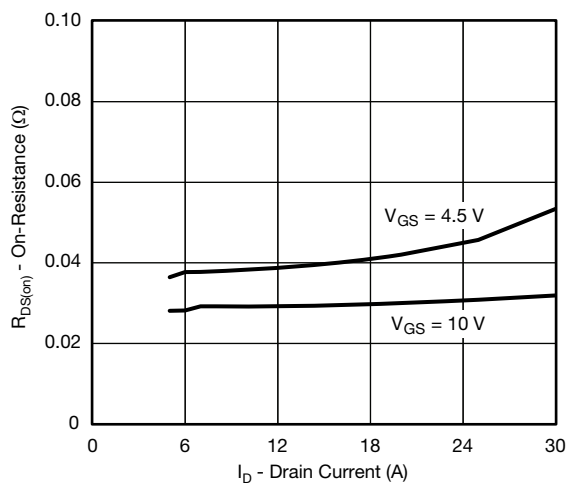
Output Characteristics



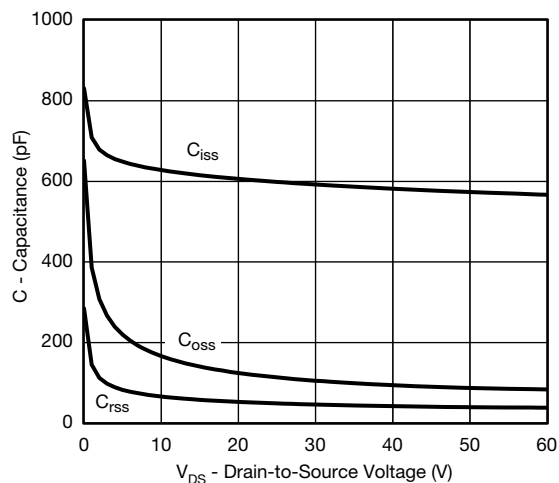
Transfer Characteristics



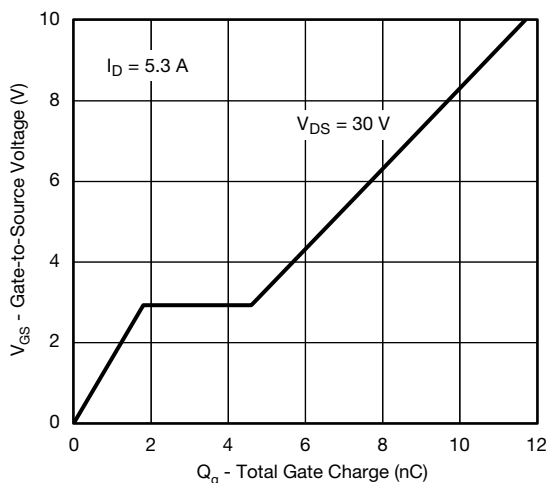
Transconductance



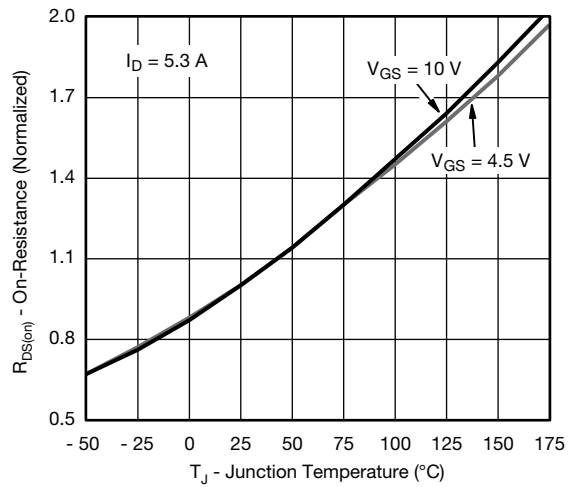
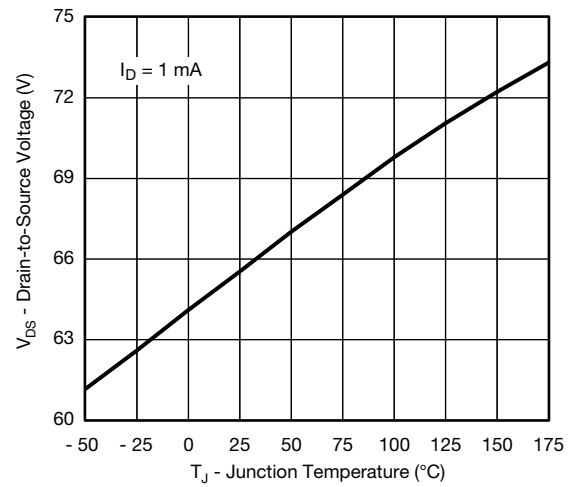
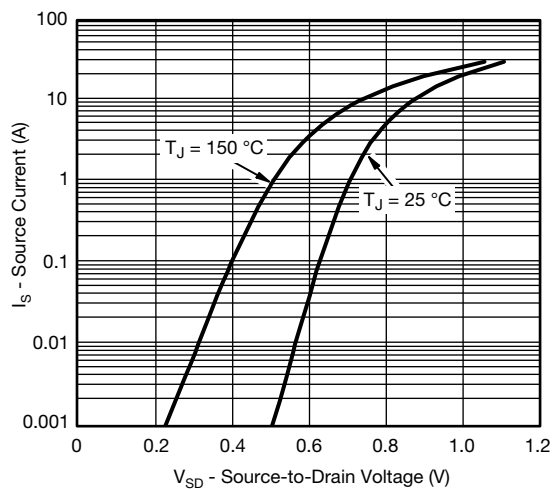
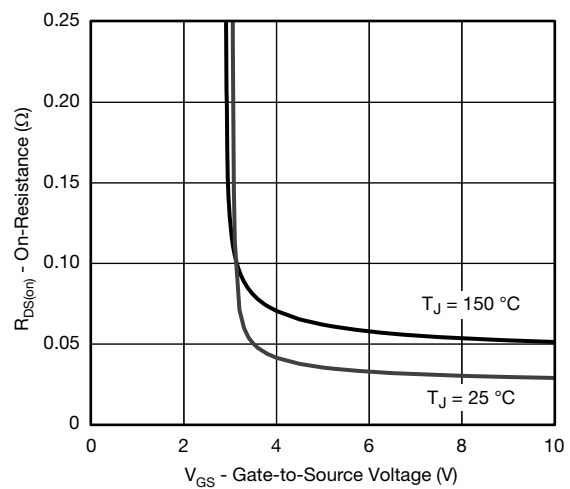
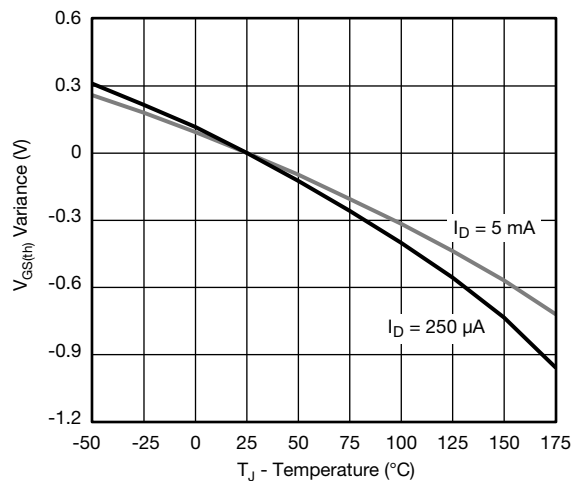
On-Resistance vs. Drain Current



Capacitance



Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Drain Source Breakdown vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Safe Operating Area

Y-axis: I_D - Drain Current (A)

X-axis: V_{DS} - Drain-to-Source Voltage (V)

Conditions: $T_C = 25^\circ\text{C}$, Single Pulse

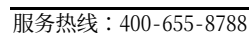
Regions and Limits:

- I_{DM} Limited
- Limited by $R_{DS(on)}$
- BVDSS Limited

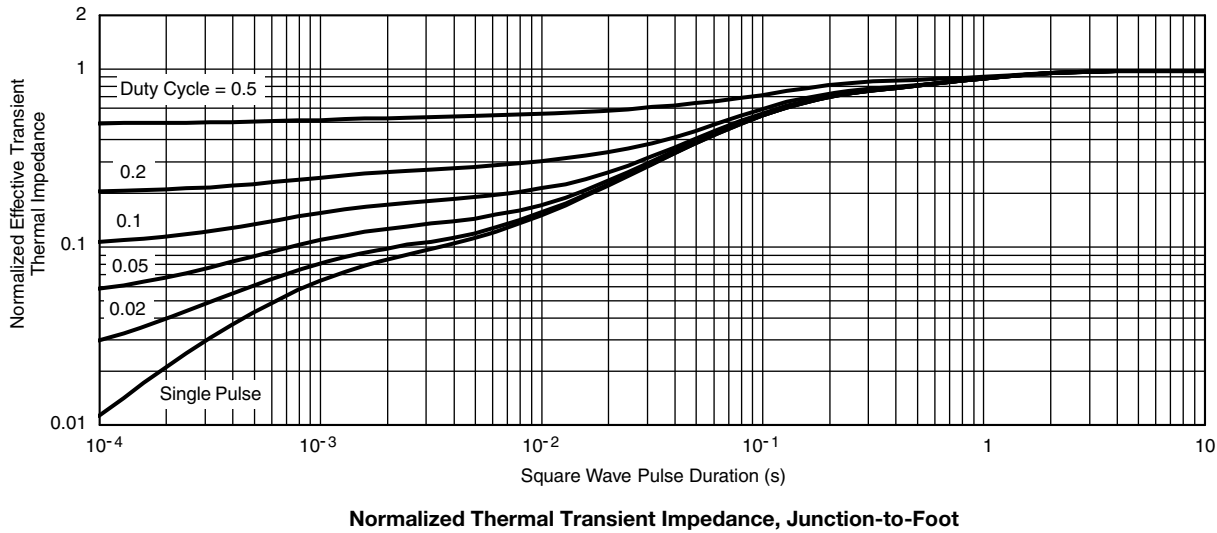
Pulse Widths (dashed lines):

- 100 μs
- 1 ms
- 10 ms
- 100 ms
- 1 s
- 10 s, DC

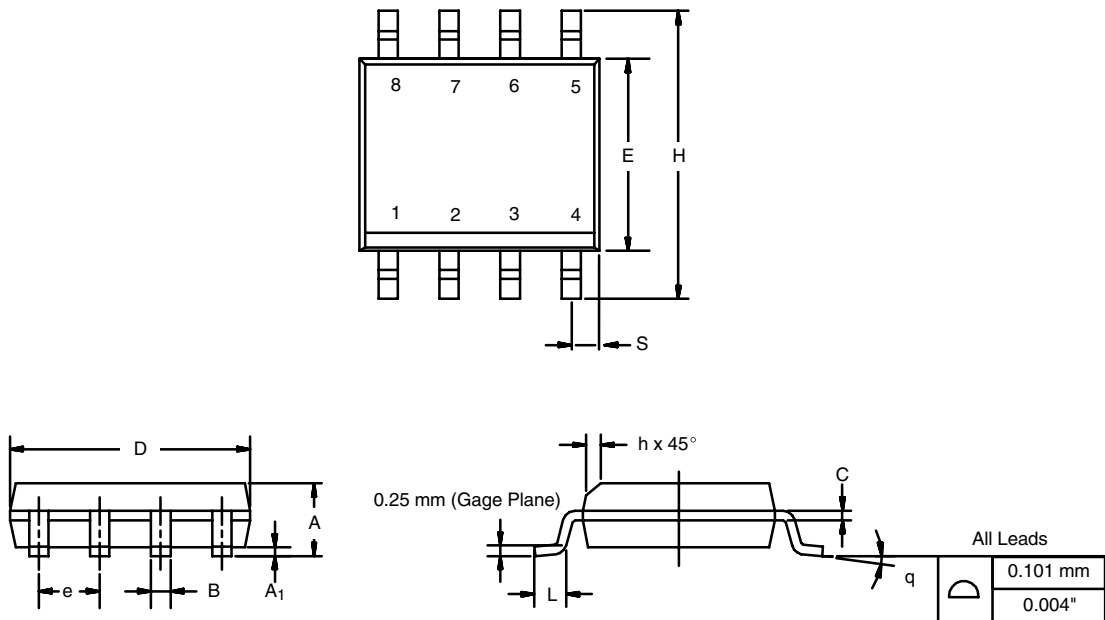
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

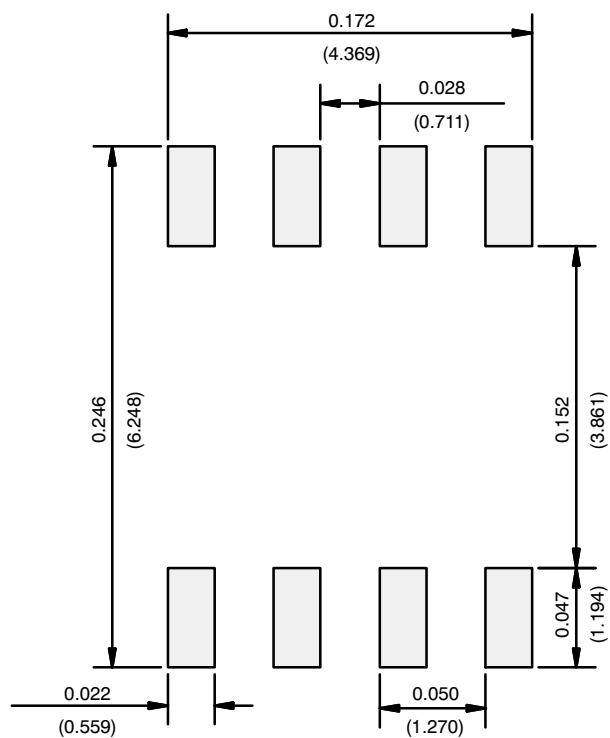


SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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