

TLP719

- Digital logic ground isolation
- Line receivers
- Microprocessor system interfaces
- Switching power supply feedback control
- Industrial invertors

The TOSHIBA TLP719 consists of a high-output infrared emitting diode and a high-speed detector.

This unit is a 6-lead SDIP. The TLP719 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

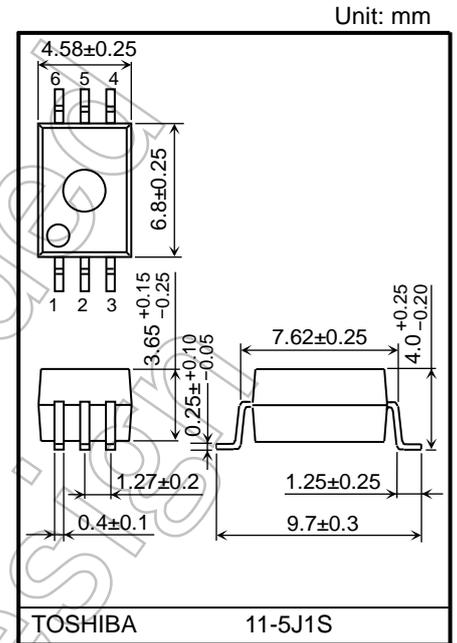
The TLP719 has a Faraday shield integrated on the photodetector chip to provide an effective common mode noise transient immunity. Therefore this product is suitable for application in noisy environmental conditions.

- Open collector
- Package type : SDIP6
- Isolation voltage : 5000 Vrms (min)
- Common mode transient immunity : $\pm 10 \text{ kV}/\mu\text{s}$ (min) @ $V_{CM} = 400 \text{ V}_{p-p}$
- Switching speed : $t_{PHL}/t_{PLH} = 0.8 \mu\text{s}$ (max)
@ $I_F = 16 \text{ mA}$, $V_{CC} = 5 \text{ V}$,
 $R_L = 1.9 \text{ k}\Omega$, $T_a = 25 \text{ }^\circ\text{C}$
- TTL compatible
- Construction mechanical rating

| | 7.62-mm pitch standard type | 10.16-mm pitch TLPXXXF type |
|----------------------|-----------------------------|-----------------------------|
| Creepage Distance | 7.0 mm (min) | 8.0 mm (min) |
| Clearance | 7.0 mm (min) | 8.0 mm (min) |
| Insulation Thickness | 0.4 mm (min) | 0.4 mm (min) |

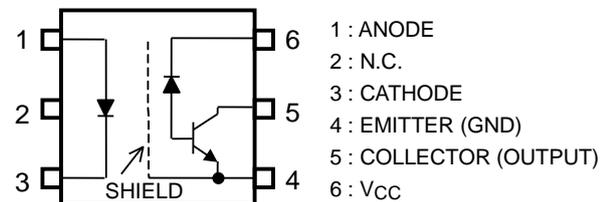
- UL-recognized : UL 1577, File No.E67349
- cUL-recognized : CSA Component Acceptance Service No.5A
File No.E67349
- VDE-approved : EN 60747-5-5 , EN 62368-1 (Note1)

Note 1: When a VDE approved type is needed, please designate the **Option(D4)**.

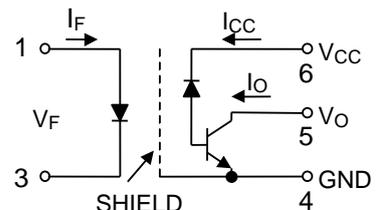


Weight: 0.26 g (typ.)

PIN CONFIGURATION (Top View)



SCHEMATIC



A 0.1- μF bypass capacitor must be connected between pins 4 and 6.

Start of commercial production
2007-09

Absolute Maximum Ratings (Ta = 25 °C)

| Characteristic | | Symbol | Rating | Unit |
|---|--|---------------------|------------|------------------|
| LED | Forward current | I _F | 25 | mA |
| | Forward current derating (Ta ≥ 70 °C) | I _F / Ta | -0.45 | mA / °C |
| | Pulse forward current (Note 1) | I _{FP} | 50 | mA |
| | Peak transient forward current (Note 2) | I _{FPT} | 1 | A |
| | Reverse voltage | V _R | 5 | V |
| | Diode power dissipation (Note 3) | P _D | 45 | mW |
| | Junction temperature | T _J | 125 | °C |
| Detector | Output current | I _O | 8 | mA |
| | Peak output current | I _{OP} | 16 | mA |
| | Output voltage | V _O | -0.5 to 20 | V |
| | Supply voltage | V _{CC} | -0.5 to 30 | V |
| | Output power dissipation | P _O | 100 | mW |
| | Output power dissipation derating (Ta ≥ 70 °C) | P _O / Ta | -1.8 | mW / °C |
| | Junction Temperature | T _J | 125 | °C |
| Operating temperature range | | T _{opr} | -55 to 100 | °C |
| Storage temperature range | | T _{stg} | -55 to 125 | °C |
| Lead soldering temperature (10 s) | | T _{sol} | 260 | °C |
| Isolation voltage (AC, 60 s, R.H. ≤ 60 %) | | BV _S | 5000 | V _{rms} |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note : A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high-gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: 50 % duty cycle, 1 ms pulse width.
Derate 0.9 mA / °C above 70 °C.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: Derate 0.8 mW / °C above 70 °C.

Note 4: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Electrical Characteristics (Ta = 25 °C)

| Characteristic | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|----------------|---|---------------------------|--|-----|------|------|---------------|
| LED | Forward voltage | V_F | $I_F = 16 \text{ mA}$ | — | 1.65 | 1.85 | V |
| | Forward voltage Temperature coefficient | $\Delta V_F / \Delta T_a$ | $I_F = 16 \text{ mA}$ | — | -2 | — | mV / °C |
| | Reverse current | I_R | $V_R = 5 \text{ V}$ | — | — | 10 | μA |
| | Capacitance between terminals | C_T | $V_F = 0 \text{ V}, f = 1 \text{ MHz}$ | — | 45 | — | pF |
| Detector | HIGH-level output current | $I_{OH} (1)$ | $I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$ | — | 3 | 500 | nA |
| | | $I_{OH} (2)$ | $I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$ $V_O = 20 \text{ V}$ | — | — | 5 | μA |
| | | I_{OH} | $I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$ $V_O = 20 \text{ V}, T_a = 70 \text{ }^\circ\text{C}$ | — | — | 50 | |
| | HIGH-level supply current | I_{CCH} | $I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$ | — | 0.01 | 1 | μA |
| | Supply voltage | V_{CC} | $I_{CC} = 0.01 \text{ mA}$ | 30 | — | — | V |
| | Output voltage | V_O | $I_O = 0.5 \text{ mA}$ | 20 | — | — | V |

Coupled Electrical Characteristics (Ta = 25 °C)

| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------|-------------|---|-----|------|-----|------|
| Current transfer ratio | I_O / I_F | $I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $V_O = 0.4 \text{ V}$ | 20 | — | — | % |
| LOW-level output voltage | V_{OL} | $I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $I_O = 2.4 \text{ mA}$ | — | — | 0.4 | V |

Isolation Characteristics (Ta = 25 °C)

| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|-----------------------------|--------|---|--------------------|-----------|-----|-----------|
| Capacitance input to output | C_S | $V = 0 \text{ V}, f = 1 \text{ MHz}$ | — | 0.8 | — | pF |
| Isolation resistance | R_S | R.H. $\leq 60 \%$, $V_S = 500 \text{ V}$ | 1×10^{12} | 10^{14} | — | Ω |
| Isolation voltage | BV_S | AC, 60 s | 5000 | — | — | V_{rms} |

Note : Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Switching Characteristics (Ta = 25 °C, Vcc = 5 V)

| Characteristic | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--|-----------|--------------|---|--------|------|-----|--------------------------|
| Propagation delay time (H→L) | t_{pHL} | Fig1 | $I_F = 0 \rightarrow 16 \text{ mA}$ $R_L = 1.9 \text{ k}\Omega$ | — | — | 0.8 | μs |
| Propagation delay time (L→H) | t_{pLH} | | $I_F = 16 \rightarrow 0 \text{ mA}$ $R_L = 1.9 \text{ k}\Omega$ | — | — | 0.8 | μs |
| Common mode transient immunity at logic HIGH output (Note 1) | CM_H | Fig2 | $I_F = 0 \text{ mA}$ $V_{CM} = 400 \text{ Vp-p}$ $R_L = 1.9 \text{ k}\Omega$ | 10000 | — | — | $\text{V} / \mu\text{s}$ |
| Common mode transient immunity at logic LOW output (Note 1) | CM_L | | $I_F = 16 \text{ mA}$ $V_{CM} = 400 \text{ Vp-p}$ $R_L = 1.9 \text{ k}\Omega$ | -10000 | — | — | $\text{V} / \mu\text{s}$ |

Note 1 : CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic LOW state ($V_O < 0.8 \text{ V}$).

CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic HIGH state ($V_O > 2.0 \text{ V}$).

Figure 1. Switching Time Test Circuit

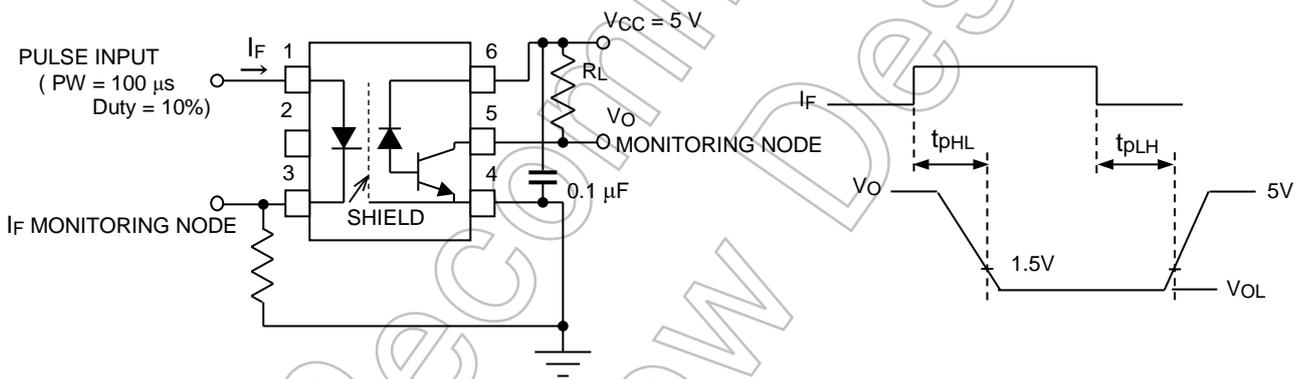
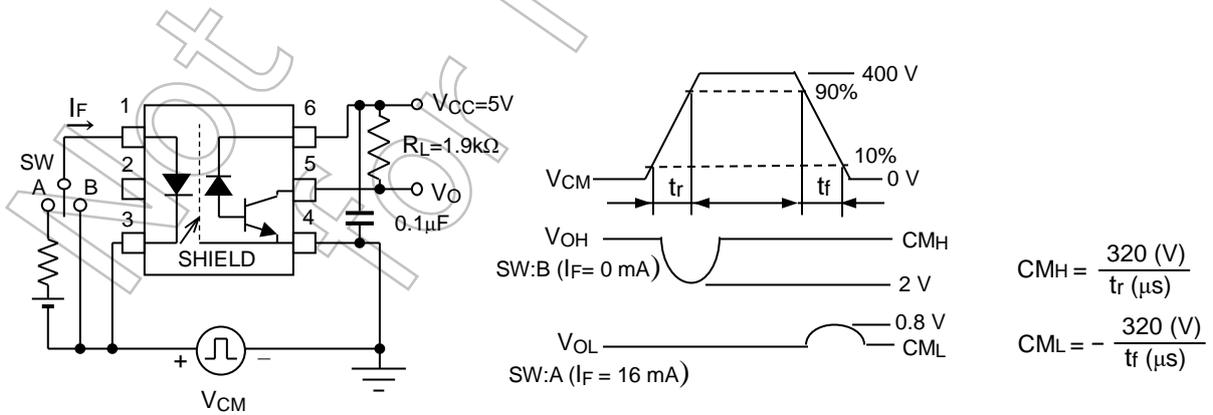
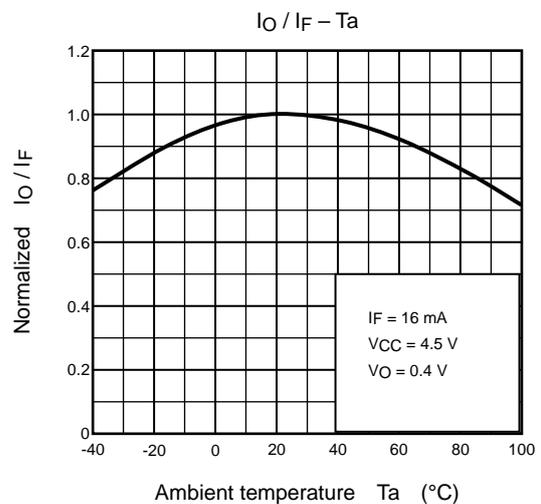
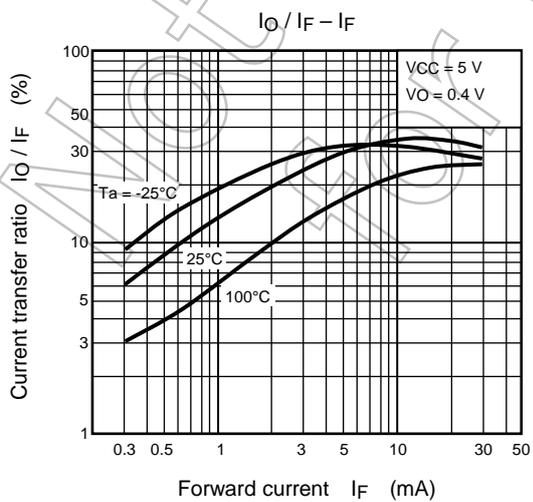
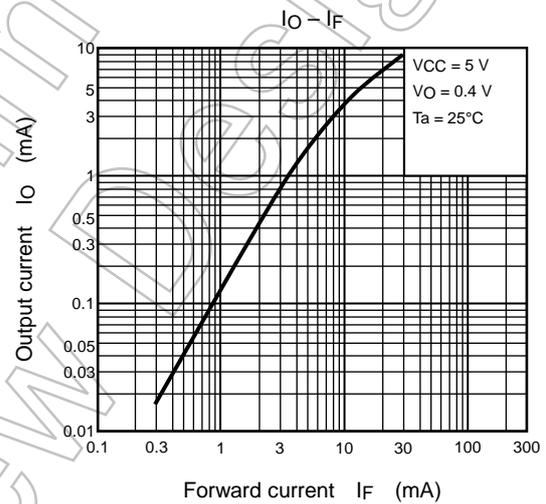
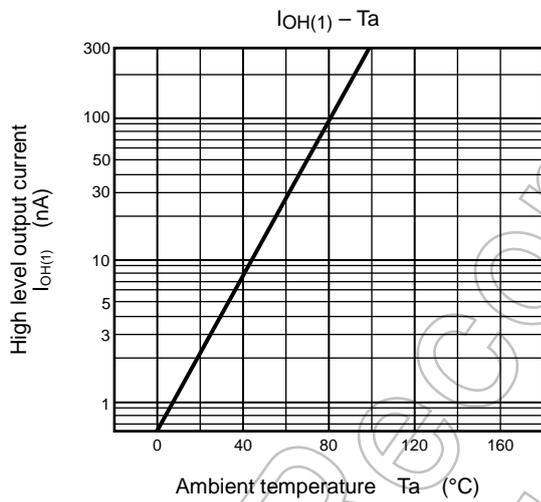
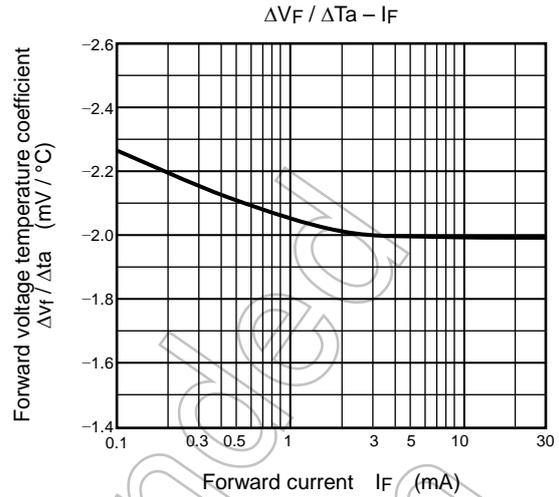
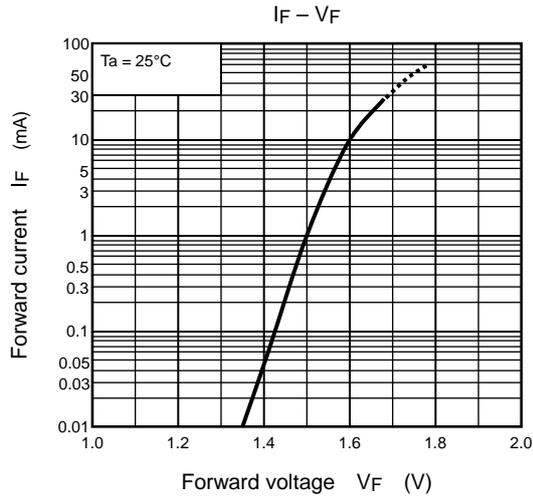
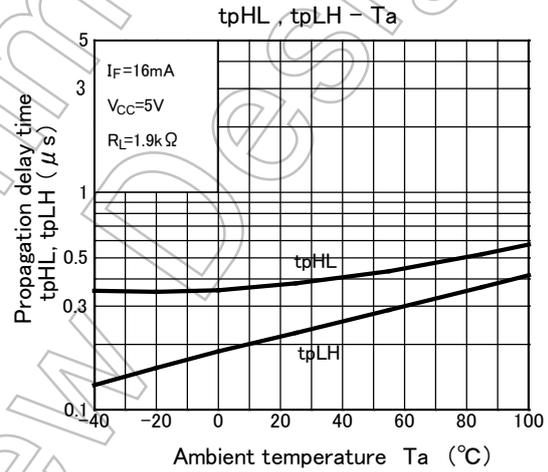
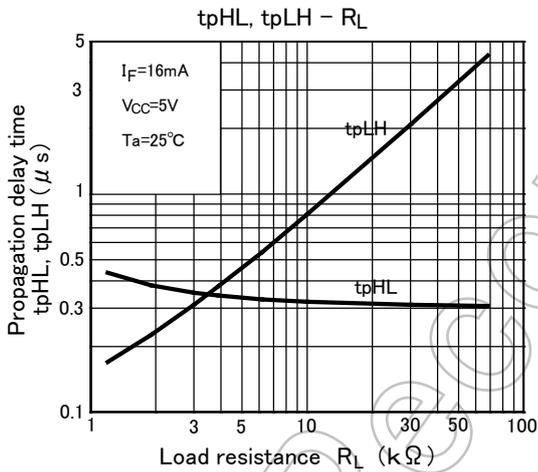
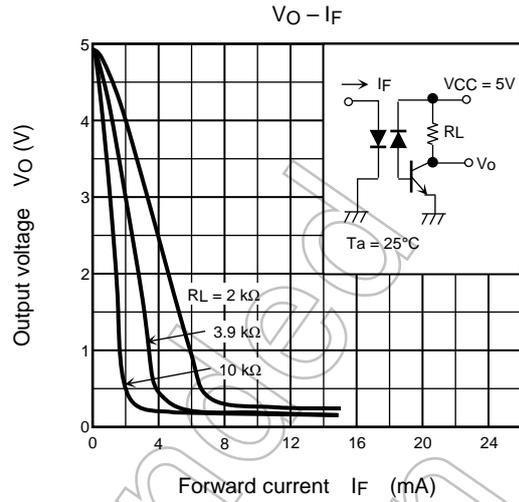
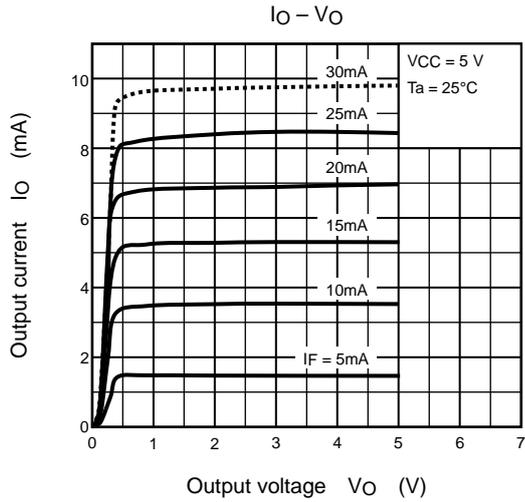


Figure 2. Common Mode Noise Immunity Test Circuit.





NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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