

MOSFETs Silicon N-channel MOS (U-MOS X-H)

TK5R0A15Q5

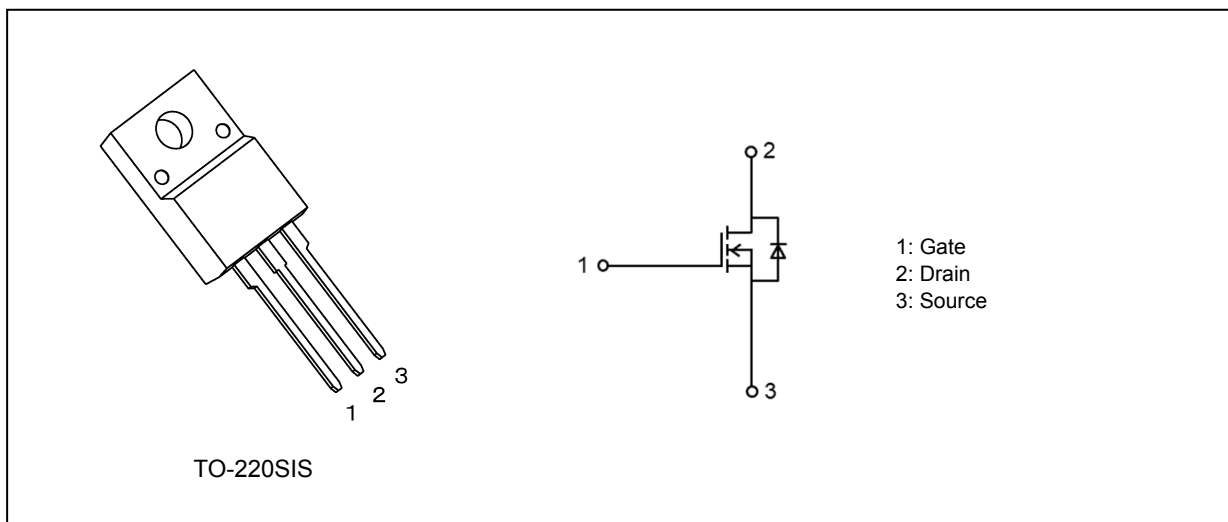
1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

2. Features

- (1) Fast reverse recovery time: $t_{rr} = 52 \text{ ns}$ (typ.)
- (2) Small reverse recovery charge : $Q_{rr} = 55 \text{ nC}$ (typ.)
- (3) Small gate charge: $Q_{SW} = 26 \text{ nC}$ (typ.)
- (4) Low drain-source on-resistance: $R_{DS(ON)} = 4.3 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (5) Low leakage current: $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 150 \text{ V}$)
- (6) Enhancement mode: $V_{th} = 3.1 \text{ to } 4.5 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 2.2 \text{ mA}$)

3. Packaging and Internal Circuit



Start of commercial production
2024-07

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ °C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	150	V
Gate-source voltage	V_{GSS}	± 20	
Drain current (DC) ($T_c = 25\text{ °C}$) (Note 1)	I_D	76	A
Drain current (DC) (Silicon limit) (Note 1), (Note 2)	I_D	76	
Drain current (pulsed) ($t = 100\text{ }\mu\text{s}$) (Note 1)	I_{DP}	480	
Power dissipation ($T_c = 25\text{ °C}$)	P_D	53	W
Single-pulse avalanche energy (Note 3)	E_{AS}	136	mJ
Single-pulse avalanche current (Note 3)	I_{AS}	76	A
Channel temperature	T_{ch}	175	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to 175	
Isolation voltage (RMS) ($t = 1.0\text{ s}$)	$V_{ISO(RMS)}$	2000	V
Mounting torque	TOR	0.6	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance ($T_c = 25\text{ °C}$)	$R_{th(ch-c)}$	2.78	$^{\circ}\text{C/W}$
Channel-to-ambient thermal resistance ($T_a = 25\text{ °C}$)	$R_{th(ch-a)}$	62.5	

Note 1: Ensure that the channel temperature does not exceed 175 °C .

Note 2: Limited by silicon chip capability.

Note 3: $V_{DD} = 100\text{ V}$, $T_{ch} = 25\text{ °C}$ (initial), $L = 23\text{ }\mu\text{H}$, $I_{AS} = 76\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 0.1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 150\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	150	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}$, $V_{GS} = -20\text{ V}$	130	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 2.2\text{ mA}$	3.1	—	4.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 8\text{ V}$, $I_D = 38\text{ A}$	—	4.5	6	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$	—	4.3	5	

Note 4: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 75\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	7820	—	pF
Reverse transfer capacitance	C_{rss}		—	50	—	
Output capacitance	C_{oss}		—	1540	—	
Gate resistance	r_g	—	—	1.9	2.9	Ω
Switching time (rise time)	t_r	See Fig. 6.2.1	—	62	—	ns
Switching time (turn-on time)	t_{on}		—	95	—	
Switching time (fall time)	t_f		—	57	—	
Switching time (turn-off time)	t_{off}		—	130	—	

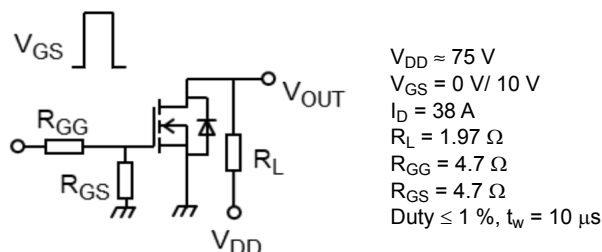


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 75\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$	—	96	—	nC
		$V_{DD} \approx 75\text{ V}$, $V_{GS} = 8\text{ V}$, $I_D = 38\text{ A}$	—	78	—	
Gate-source charge 1	Q_{gs1}	$V_{DD} \approx 75\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$	—	44	—	
Gate-drain charge	Q_{gd}		—	11.6	—	
Gate switch charge	Q_{SW}		—	26	—	
Output charge	Q_{oss}	$V_{DS} = 75\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	190	—	

6.4. Source-Drain Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 5)	I _{DRP}	t = 100 μs	—	—	480	A
Diode forward voltage	V _{DSF}	I _{DR} = 38 A, V _{GS} = 0 V	—	—	-1.2	V
Reverse recovery time (Note 6)	t _{rr}	I _{DR} = 19 A, V _{GS} = 0 V, -dI _{DR} /dt = 100 A/μs	—	52	78	ns
Reverse recovery charge (Note 6)	Q _{rr}		—	55	125	nC

Note 5: Ensure that the channel temperature does not exceed 175 °C.

Note 6: Defined by design.

7. Marking (Note)

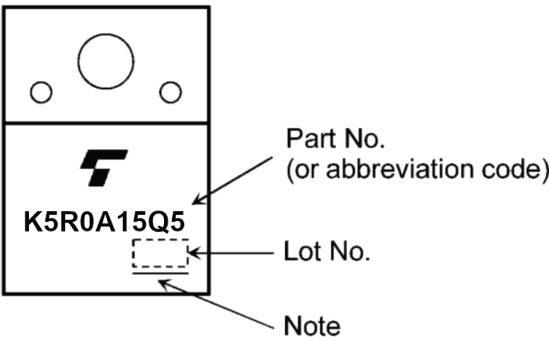


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]
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8. Characteristics Curves (Note)

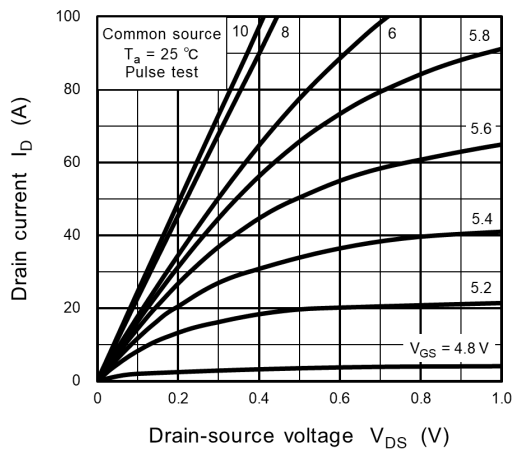


Fig. 8.1 $I_D - V_{DS}$

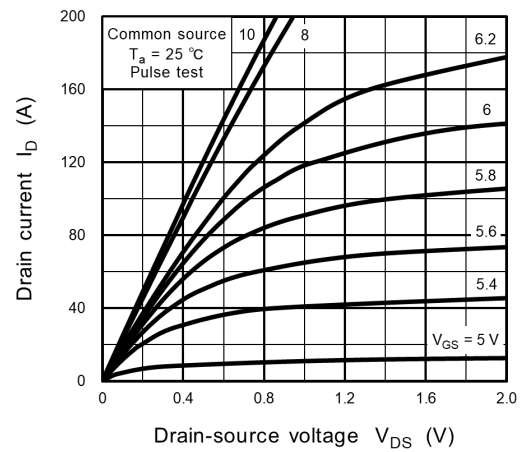


Fig. 8.2 $I_D - V_{DS}$

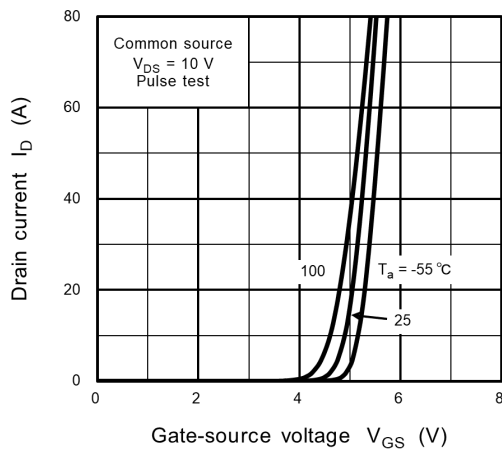


Fig. 8.3 $I_D - V_{GS}$

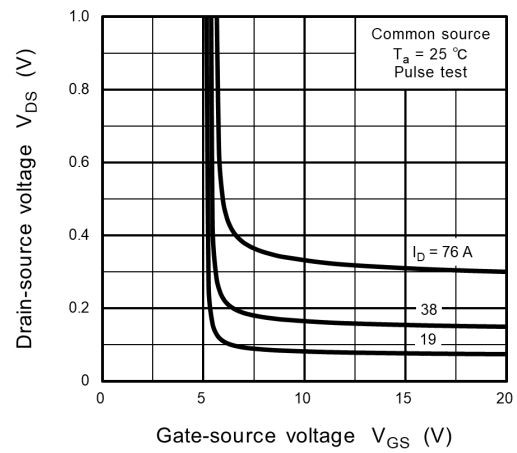


Fig. 8.4 $V_{DS} - V_{GS}$

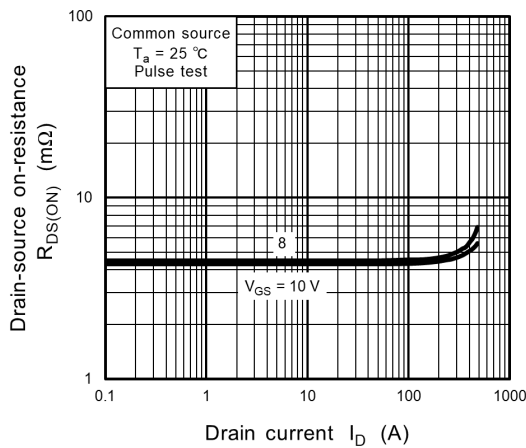


Fig. 8.5 $R_{DS(ON)} - I_D$

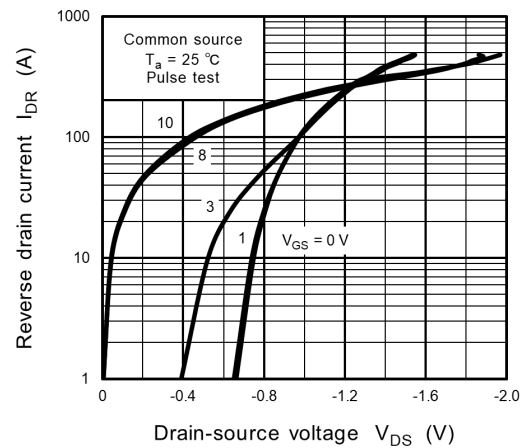


Fig. 8.6 $I_{DR} - V_{DS}$

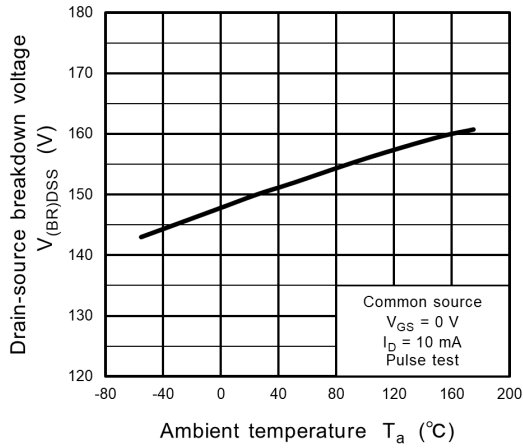


Fig. 8.7 $V_{(BR)DSS} - T_a$

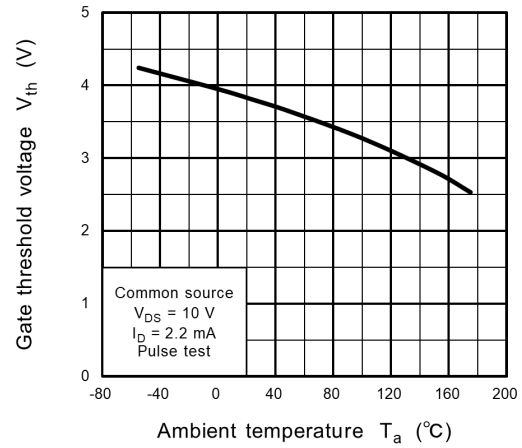


Fig. 8.8 $V_{th} - T_a$

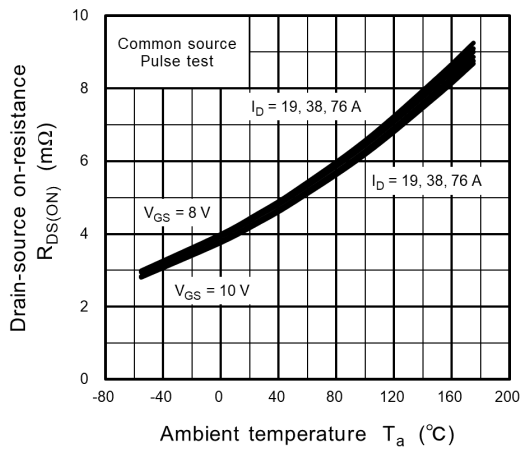


Fig. 8.9 $R_{DS(ON)} - T_a$

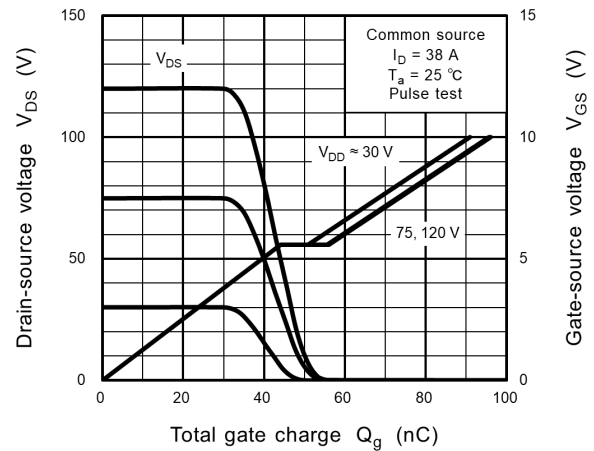


Fig. 8.10 Dynamic Input/Output Characteristics

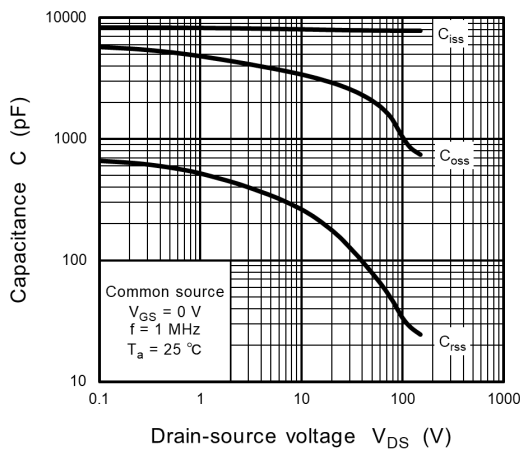


Fig. 8.11 Capacitance - V_{DS}

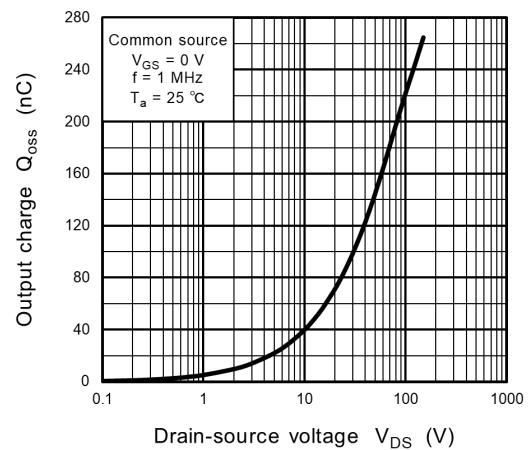


Fig. 8.12 $Q_{oss} - V_{DS}$

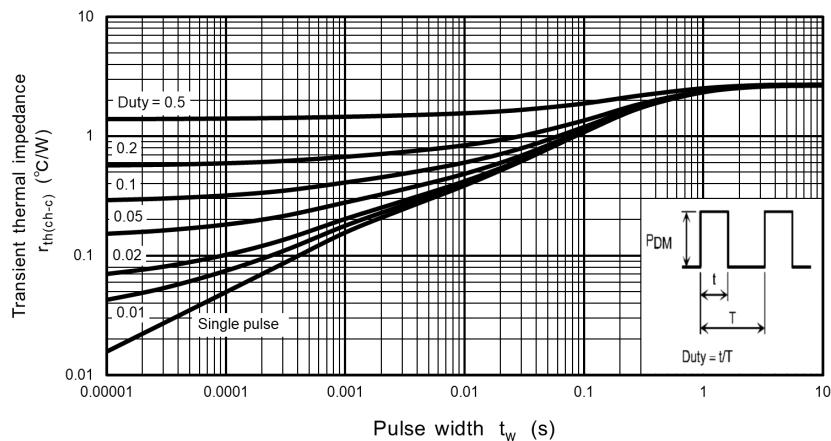


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

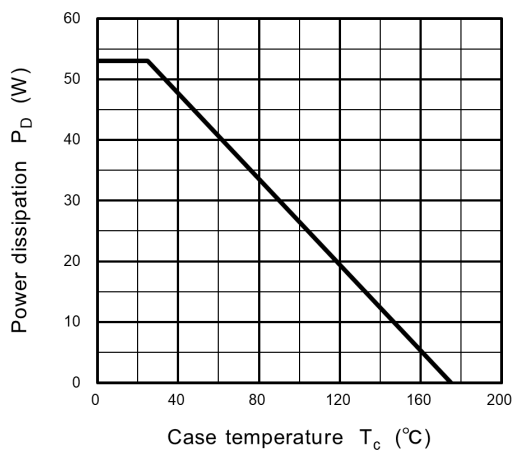


Fig. 8.14 $P_D - T_c$
(Guaranteed Maximum)

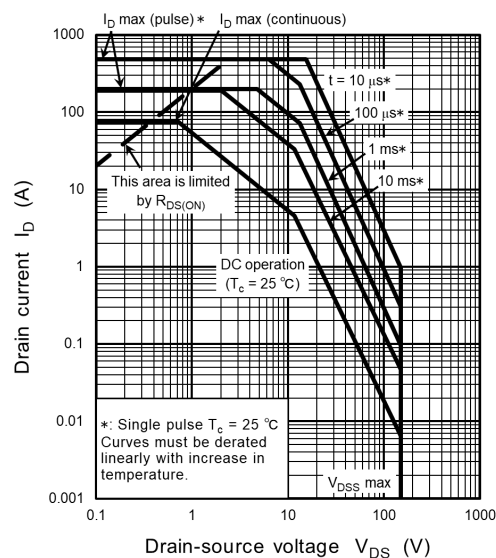


Fig. 8.15 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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