TPS7A16 具有使能和电源正常指示功能的 60V、5μA I_Q、100mA、低压降稳压器

1 特性

- 宽输入电压范围：3V 至 60V
- 超低静态电流：5μA
- 关断时的静态电流：1μA
- 输出电流：100mA
- 低压降电压：电流为 20mA 时为 60mV
- 精度：2%
- 可提供：
  - 固定输出电压：3.3V，5V
  - 可调节输出电压：1.2V 至 18.5V
- 具有可编程延迟的电源正常指示功能
- 限流和热关断保护
- 与陶瓷输出电容搭配使用时可保持稳定：≥ 2.2μF
- 封装：高耐热性能微型小外形尺寸 (MSOP)-8 和小外形尺寸无引线 (SON)-8 封装 PowerPAD™
- 工作温度范围：–40°C 至 125°C

2 应用

- 笔记本个人电脑 (PC)、数字电视和私有局域网 (LAN) 系统电源
- 用于电动工具和其它由电池供电的微处理器和微控制器系统的高节数电池组
- 车载音频、导航、信息娱乐、和其它汽车系统
- 烟雾和 CO_2 探测器以及电池供电类警报和安全系统

3 说明

TPS7A16 系列超低功耗、低降压 (LDO) 稳压器提供超低静态电流、高输入电压和小型化、高散热性能封装所具备的优势。

TPS7A16 系列器件针对连续或断续（备用电源）电池供电 应用 而设计，超低静态电流在此类应用中对于延长系统电池寿命至关重要。

TPS7A16 系列产品提供一个与标准互补金属氧化物半导体 (CMOS) 逻辑电路兼容的使能引脚 (EN) 和一个具有用户可编程延迟的集成开漏高电平有效的电源正常输出 (PG)。这些引脚专用于需要进行电源轨排序、 基于微控制器的电池供电类应用。

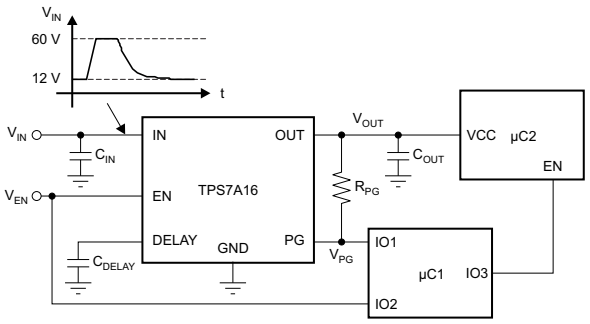
此外，TPS7A16 器件非常适用于从多节电池解决方案生成低压电源（从多节电动工具组到汽车 应用）；该器件不但能够提供一个稳压良好的电压轨，而且还能够承受瞬态电压并在电压瞬态期间保持稳压状态。这些功能 意味着电涌保护电路更加简单且更为经济高效。

器件信息(1)

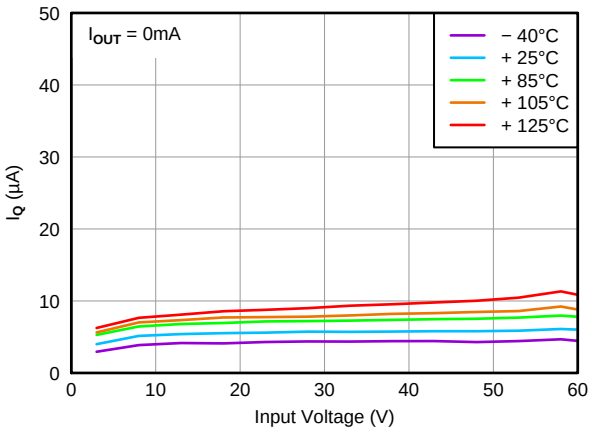
器件型号	封装	封装尺寸（标称值）
TPS7A16	HVSSOP (8)	3.00mm × 3.00mm
	VSON (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

典型应用电路原理图



静态电流与输入电压间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (August 2015) to Revision F — **Page**

- Changed ψ_{JB} value in *Thermal Information* table from 141.2 to 11.2 (typo) ... 6

Changes from Revision D (January 2014) to Revision E — **Page**

- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Changed MIN value of Regulated output from 1.2 to 1.169 ... 5
- Changed MAX value of Regulated output from 18 to 18.5 ... 5
- Changed MAX value of Operating junction temperature from 150 to 125 ... 5
- Changed value in Power-Good section from 5.5-V to 5-V ... 11

Changes from Revision C (November 2013) to Revision D — **Page**

- Changed Feedback Current min, typ, and max values from –1.0, 0.0, and 1.0 to –0.1, –0.01, and 0.1, respectively ... 6
- Changed Enable Current typ value from 0.01 to –0.01 ... 6

Changes from Revision B (April 2013) to Revision C — **Page**

- 已将 DRB 封装从产品预览改为生产数据 ... 1
- Added DRB package to thermal information ... 6
- Changed Figure 4 Y-axis unit from V to mV (typo) ... 7

Changes from Revision A (December 2011) to Revision B — **Page**

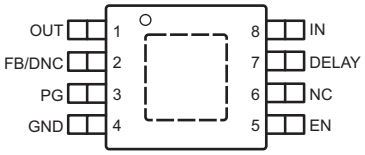
- 已添加 DRB 封装的产品预览至数据表。 ... 1

Changes from Original (December 2011) to Revision A **Page**

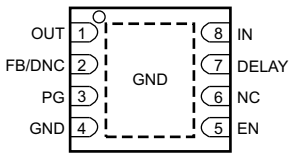
- 已将数据表由“产品预览”改为“量产数据” 1

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



DRB Package
8-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	I	For the adjustable version (TPS7A1601), the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed voltage versions: **Do not connect** to this pin. Do not route this pin to any electrical net, not even GND or IN.
GND	4	GND	Ground pin.
IN	8	IN	Regulator input supply pin. A capacitor ≥ 0.1 µF must be tied from this pin to ground to assure stability. TI recommends connecting a 10-µF ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	6	—	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor ≥ 2.2 µF must be tied from this pin to ground to assure stability. TI recommends connecting a 10-µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize AC performance.
PG	3	O	Power-good pin. Open collector output; leave open or connect to GND if the power-good function is not needed.
PowerPAD	—	—	Solder to printed-circuit-board (PCB) to enhance thermal performance. Although it can be left floating, TI highly recommends connecting the PowerPAD to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range –40°C ≤ T_J ≤ 125°C (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	62	V
	OUT pin to GND pin	–0.3	20	
	OUT pin to IN pin	–62	0.3	
	FB pin to GND pin	–0.3	3	
	FB pin to IN pin	–62	0.3	
	EN pin to IN pin	–62	0.3	
	EN pin to GND pin	–0.3	62	
	PG pin to GND pin	–0.3	5.5	
	DELAY pin to GND pin	–0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Unregulated input	3		60	V
V_{OUT}	Regulated output	1.169		18.5	V
EN		0		40	V
DELAY		0		5	V
PG		0		5	V
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A1601		UNIT
		DGN (HVSSOP)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.2	44.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	45.9	49.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	14.9	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		60	V
V_{REF}	Internal reference	T_J = 25°C, V_{FB} = V_{REF}, V_{IN} = 3 V, I_{OUT} = 10 µA	1.169	1.193	1.217	V
V_{UVLO}	Undervoltage lockout threshold			2.7		V
V_{OUT}	Output voltage range	$V_{IN} \geq V_{OUT(NOM)}$ + 0.5 V	V_{REF}		18.5	V
	Nominal accuracy	T_J = 25°C, V_{IN} = 3 V, I_{OUT} = 10 µA	–2%		2%	V_{OUT}
	Overall accuracy	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 60 V(1) 10 µA ≤ I_{OUT} ≤ 100 mA	–2%		2%	V_{OUT}
$\Delta V_{O(\Delta VI)}$	Line regulation	3 V ≤ V_{IN} ≤ 60 V		±1%		V_{OUT}
$\Delta V_{O(\Delta IO)}$	Load regulation	10 µA ≤ I_{OUT} ≤ 100 mA		±1%		V_{OUT}
V_{DO}	Dropout voltage	V_{IN} = 4.5 V, $V_{OUT(NOM)}$ = 5 V, I_{OUT} = 20 mA		60		mV
		V_{IN} = 4.5 V, $V_{OUT(NOM)}$ = 5 V, I_{OUT} = 100 mA		265	500	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 3 V	101	225	400	mA
I_{GND}	Ground current	3 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 10 µA		5	15	µA
		I_{OUT} = 100 mA		5		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		0.59	5	µA
I_{FB}	Feedback current(2)		–0.1	–0.01	0.1	µA
I_{EN}	Enable current	3 V ≤ V_{IN} ≤ 12 V, V_{IN} = V_{EN}	–1	–0.01	1	µA
V_{EN_HI}	Enable high-level voltage		1.2			V
V_{EN_LO}	Enable low- level voltage				0.3	V
V_{IT}	PG trip threshold	OUT pin floating, V_{FB} increasing, $V_{IN} \geq V_{IN\_MIN}$	85%		95%	V_{OUT}
		OUT pin floating, V_{FB} decreasing, $V_{IN} \geq V_{IN\_MIN}$	83%		93%	V_{OUT}
V_{HYS}	PG trip hysteresis			2.3%	4%	V_{OUT}
$V_{PG,\ LO}$	PG output low voltage	OUT pin floating, V_{FB} = 80% V_{REF}, I_{PG}= 1mA			0.4	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG}= $V_{OUT(NOM)}$	–1		1	µA
I_{DELAY}	DELAY pin current			1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, f = 100 Hz		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature range		–40		125	°C

(1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load (P ≈ (V_{IN} – V_{OUT}) × I_{OUT} = (24 V – V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(2) I_{FB} > 0 flows out of the device.

6.6 Typical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

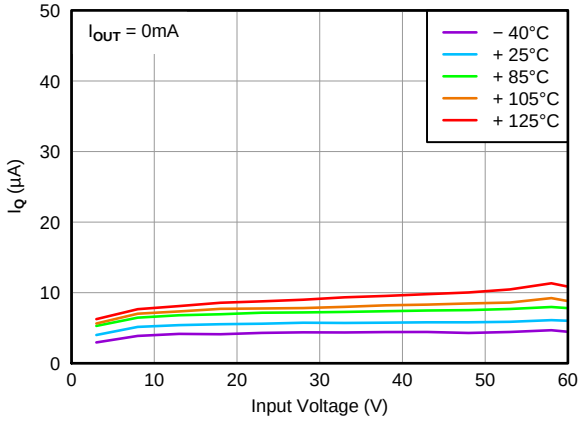


Figure 1. Quiescent Current vs Input Voltage

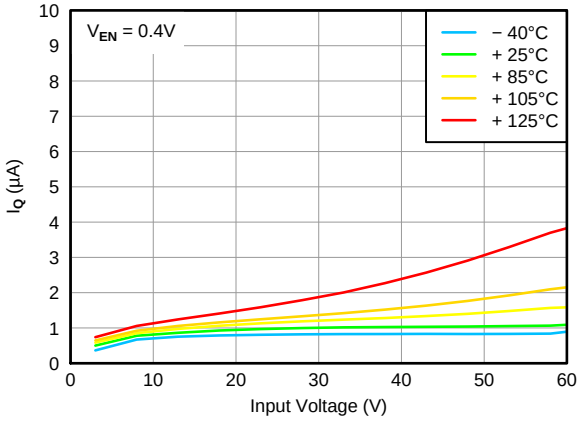


Figure 2. Shutdown Current vs Input Voltage

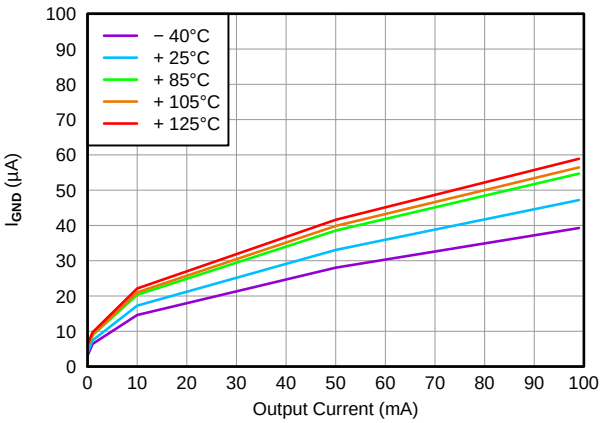


Figure 3. Ground Current vs Output Current

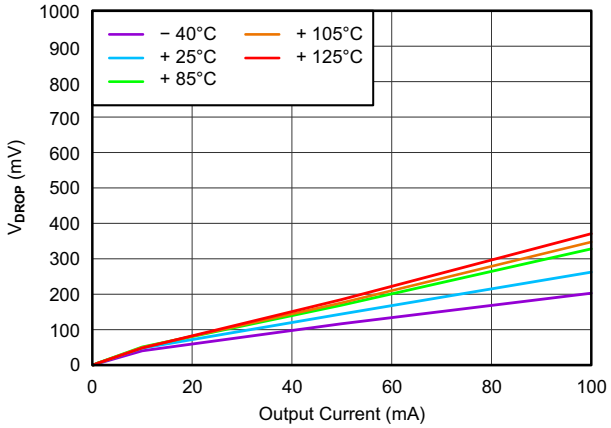


Figure 4. Dropout Voltage vs Output Current

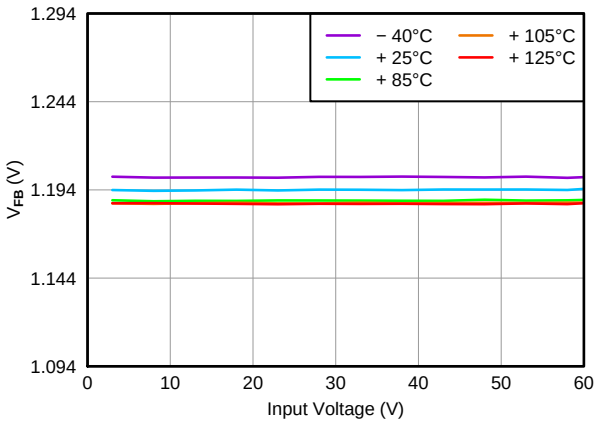


Figure 5. Feedback Voltage vs Input Voltage

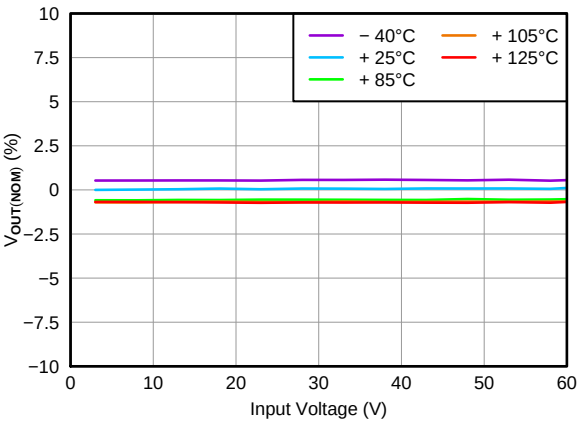


Figure 6. Line Regulation

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

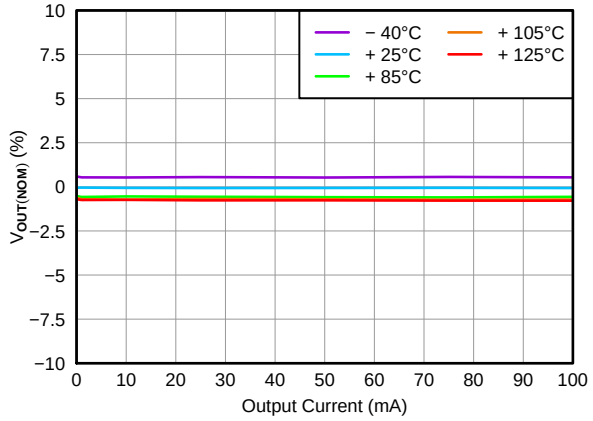


Figure 7. Load Regulation

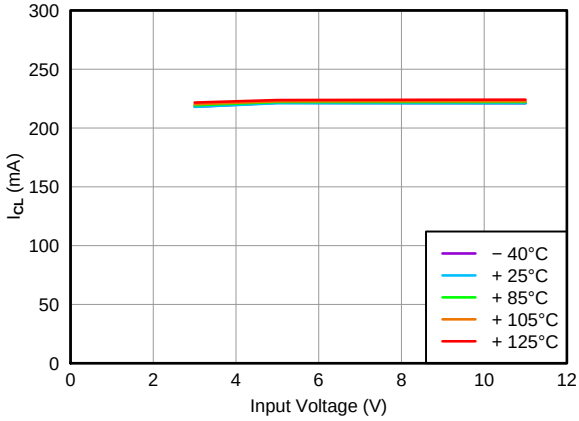


Figure 8. Current Limit vs Input Voltage

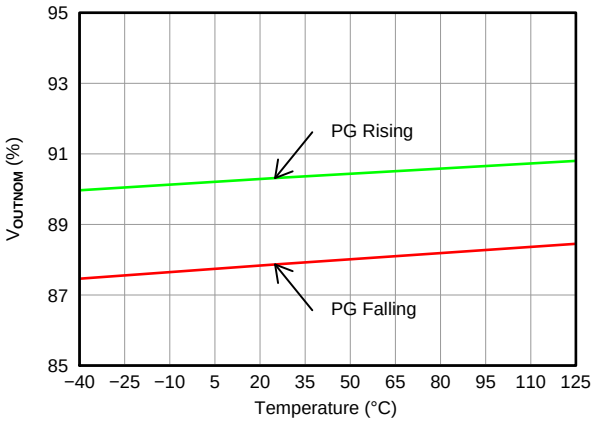


Figure 9. Power-Good Threshold Voltage vs Temperature

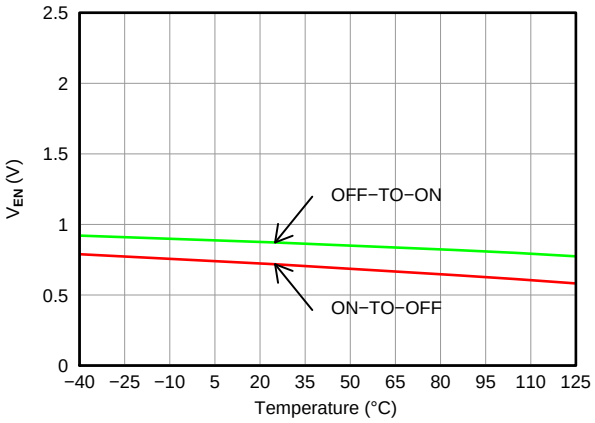


Figure 10. Enable Threshold Voltage vs Temperature

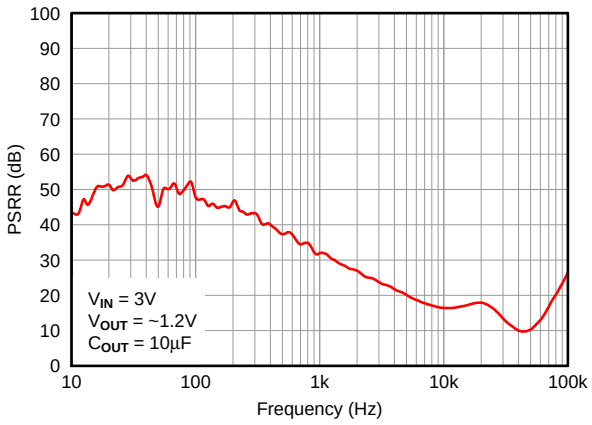


Figure 11. Power-Supply Rejection Ratio

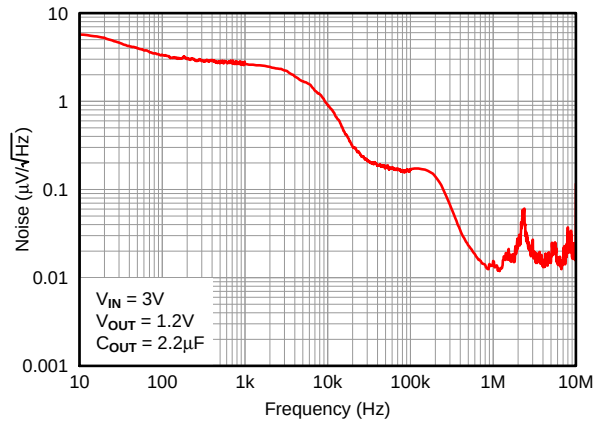


Figure 12. Output Spectral Noise Density

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT, unless otherwise noted.

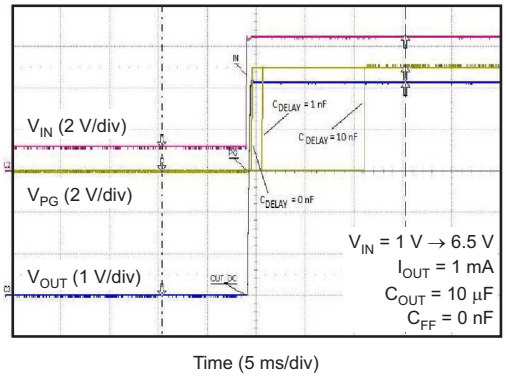


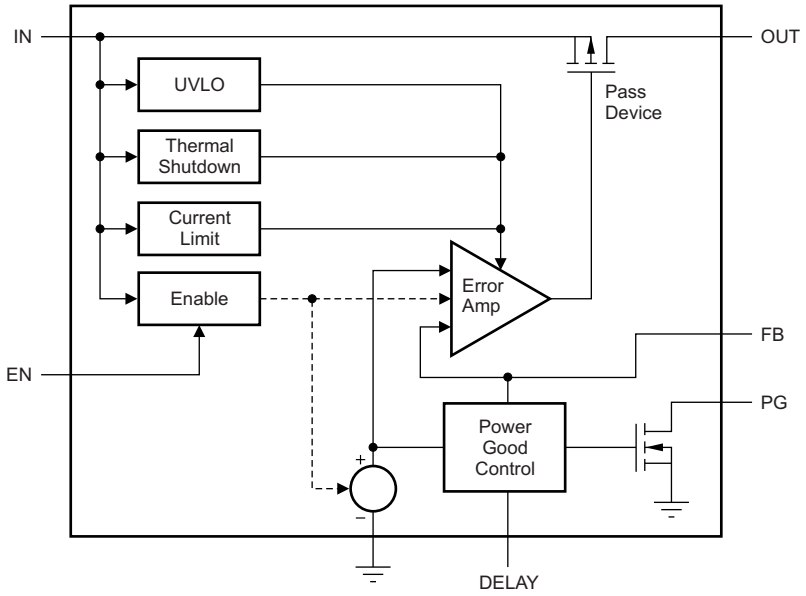
Figure 13. Power-Good Delay

7 Detailed Description

7.1 Overview

The TPS7A16 family of devices are ultralow power, low-dropout (LDO) voltage regulators that offer the benefits of ultralow quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16 family also offers an enable pin (EN) and integrated open-drain active-high power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable terminal is a high-voltage-tolerant terminal. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the V_{IN} terminal.

7.3.2 Regulated Output (V_{OUT})

The V_{OUT} terminal is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5-V or lower rail through an external pull-up resistor. When no C_{DELAY} is used, the PG output is high-impedance when V_{OUT} is greater than the PG trip threshold (V_{IT}). If V_{OUT} drops below V_{IT}, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

The power-good feature functionality is only guaranteed when $V_{IN} \geq 3$ V ($V_{IN\_(MIN)}$)

7.3.4 PG Delay Timer (DELAY)

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I_{DELAY}) once V_{OUT} exceeds the PG trip threshold (V_{IT}).

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}.

The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when C_{DELAY} = 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.193 V) / 1 µA = 11.93 ms.

7.3.5 Internal Current Limit

The fixed internal current limit of the TPS7A16 family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (225 mA, typical), and is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(MIN)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(NOM)} + V_{DO}$ and $V_{IN} > V_{IN(MIN)}$	$V_{EN} > V_{EN\_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{EN\_HI}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device	—	$V_{EN} < V_{EN\_HI}$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A16 family of ultralow power voltage regulators offers the benefit of ultralow quiescent current, high input voltage, and miniaturized, high thermal-performance packaging.

The TPS7A16 family is designed for continuous or sporadic (power backup) battery-operated applications where ultralow quiescent current is critical to extending system battery life.

8.2 Typical Applications

8.2.1 TPS7A1601 Circuit as an Adjustable Regulator

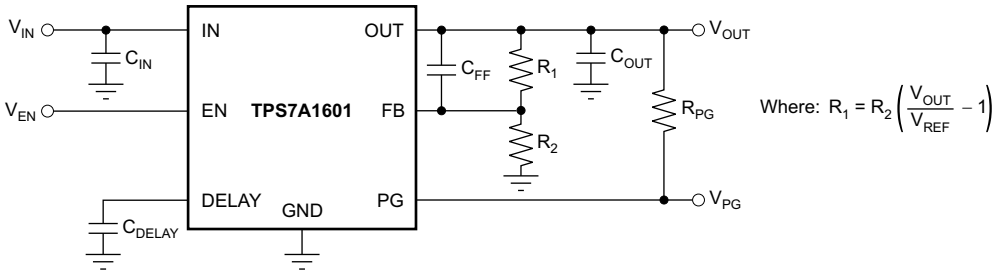


Figure 14. TPS7A1601 Circuit as an Adjustable Regulator Schematic

8.2.1.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A1601 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in Figure 15:

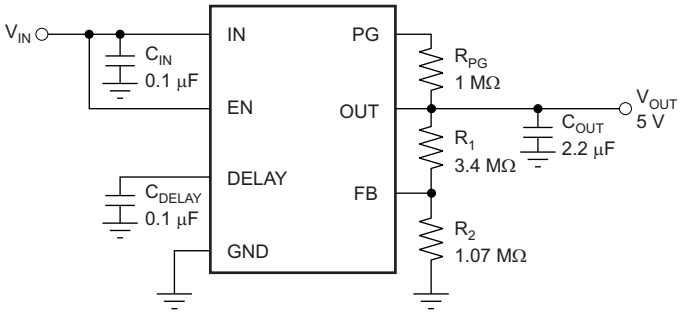


Figure 15. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

8.2.1.2.1.1 Resistor Selection

TI recommends using resistors in the order of MΩ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the device's quiescent current).

If greater voltage accuracy is required, consider the voltage offset contributions as a result of feedback current and use of 0.1% tolerance resistors.

Table 3 shows the resistor combination to achieve a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while abiding to the formula shown in Equation 1.

Table 3. Selected Resistor Combinations

V_{OUT}	R_1	R_2	$V_{OUT}/(R_1 + R_2) \ll I_Q$	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 µA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2..5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants may significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16 or using resistors in the order of hundreds or tens of kΩ.

8.2.1.2.1.2 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

High ESR capacitors may degrade PSRR.

8.2.1.2.1.3 Input and Output Capacitor Requirements

The TPS7A16 family of ultralow power, high-voltage linear regulators achieves stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, TI recommends using 10-µF ceramic capacitors to maximize AC performance.

8.2.1.2.1.4 Feed-Forward Capacitor

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, TI recommends using a 0.01-µF feed-forward capacitor to maximize AC performance.

8.2.1.2.1.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves

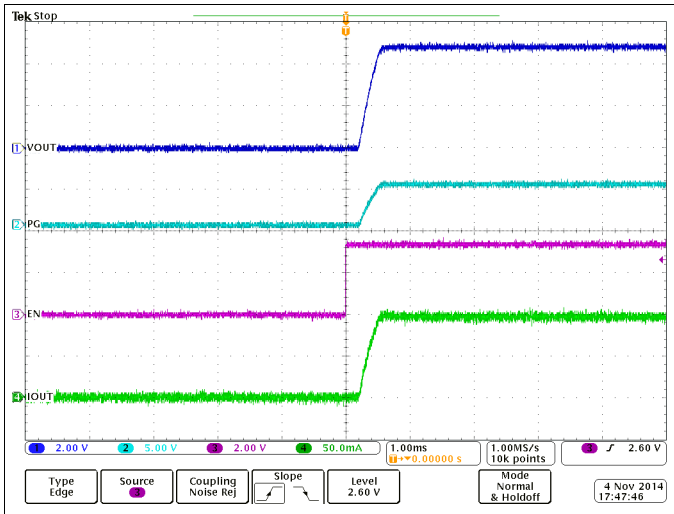


Figure 16. CH1 is VOUT, CH2 is PG, CH3 is EN, CH4 is IOUT, VIN is 12 V and Ready Before EN

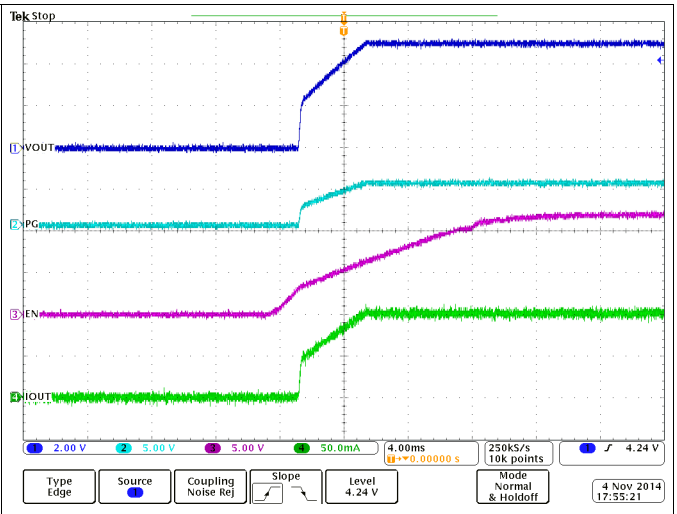


Figure 17. CH1 is VOUT, CH2 is PG, CH3 is EN, CH4 is IOUT, VIN is 12 V Connected to EN

8.2.2 Automotive Applications

The TPS7A16 family maximum input voltage of 60 V makes it ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) may cause voltage spikes from 25 V to 60 V. To prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16 family can be used to simplify and lower costs in such cases. The TPS7A16 very high voltage range allows this regulator to not only withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

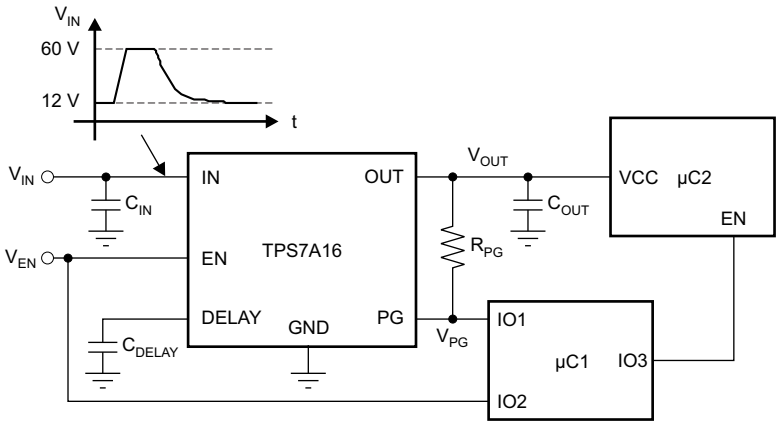


Figure 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

8.2.2.1 Design Requirements

Table 4 lists the design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.2.2 Detailed Design Procedure

See *Capacitor Recommendations* and *Input and Output Capacitor Requirements*.

8.2.2.2.1 Device Recommendations

The output is 5 V, so choose either the fixed output version TPS7A1650 or the adjustable output version TPS7A1601, and set the resistor divider appropriately. See *Resistor Selection* for more details.

8.2.2.3 Application Curves

See Figure 16 and Figure 17.

8.2.3 Multicell Battery Packs

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, may have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that may degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI's MSP430.

The microcontroller continuously monitors the battery itself, whether the battery is in use or not. Although this microcontroller could be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack itself, degrading its life or adding cost to implement more complex cell balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

TPS7A16 is the ideal regulator for this application because it can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

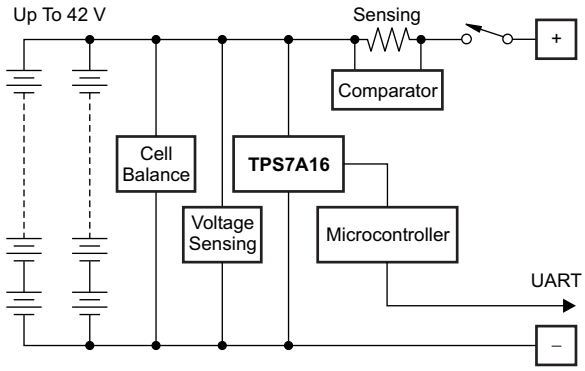


Figure 19. Protection Based on Low-Power Microcontroller Power from Multicell Battery Packs

8.2.3.1 Design Requirements

Table 5 lists the design parameters.

Table 5. Device Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 55 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.3.2 Detailed Design Procedure

See *Device Recommendations*, *Capacitor Recommendations*, and *Input and Output Capacitor Requirements*.

8.2.3.3 Application Curves

See Figure 16 and Figure 17.

8.2.4 Battery-Operated Power Tools

High voltage multicell battery packs support high-power applications, such as power tools, with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients due to the motor inductance.

The TPS7A16 can be used to power the motor-controlled microcontroller or microprocessor; its low quiescent current maximizes battery shelf life and its very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

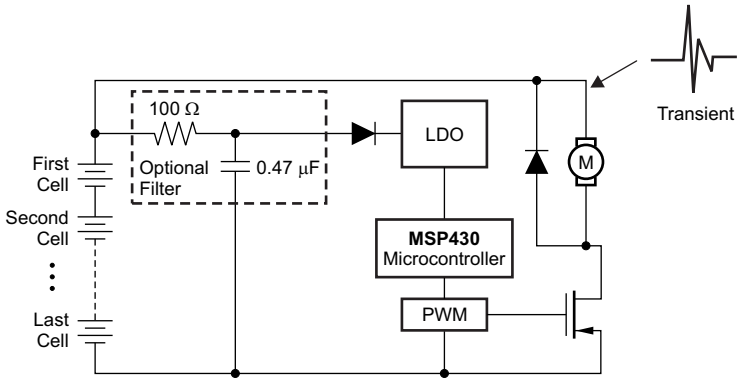


Figure 20. Low Power Microcontroller Power From Multicell Battery Packs In Power Tools

8.2.4.1 Design Requirements

Table 6 lists the design parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.4.2 Detailed Design Procedure

See *Device Recommendations*, *Capacitor Recommendations*, and *Input and Output Capacitor Requirements*.

8.2.4.3 Application Curves

See Figure 16 and Figure 17.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. The TPS7A16 family of ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, TI recommends using 10-µF ceramic capacitors to maximize ac performance.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A16 evaluation board, available at www.ti.com.

10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from near-by components (specially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends using a fixed-voltage version of the TPS7A16, or isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

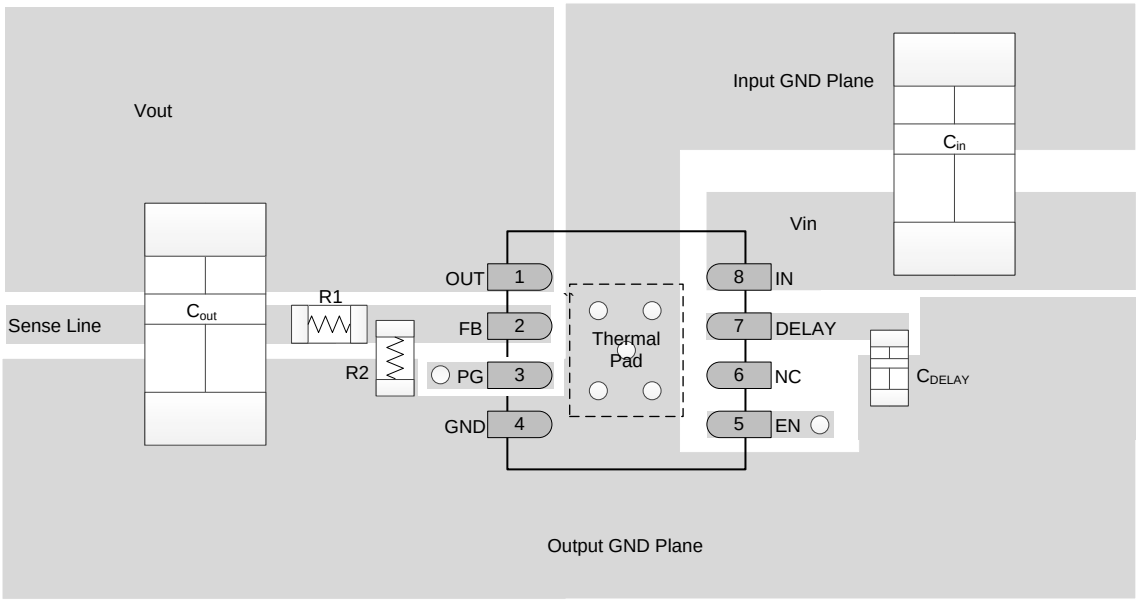
10.2 Layout Example

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 21 shows the schematic for the suggested layout. Figure 22 and Figure 23 show the top and bottom printed-circuit-board (PCB) layers for the suggested layout.

Layout Example (continued)



Notes: Cin and C_{out} are 1208 packages
C_{NR}, R_1, and R_2 are 0402 packages
○ Denotes a via to a connection made on another layer

Figure 21. Schematic for Suggested Layout

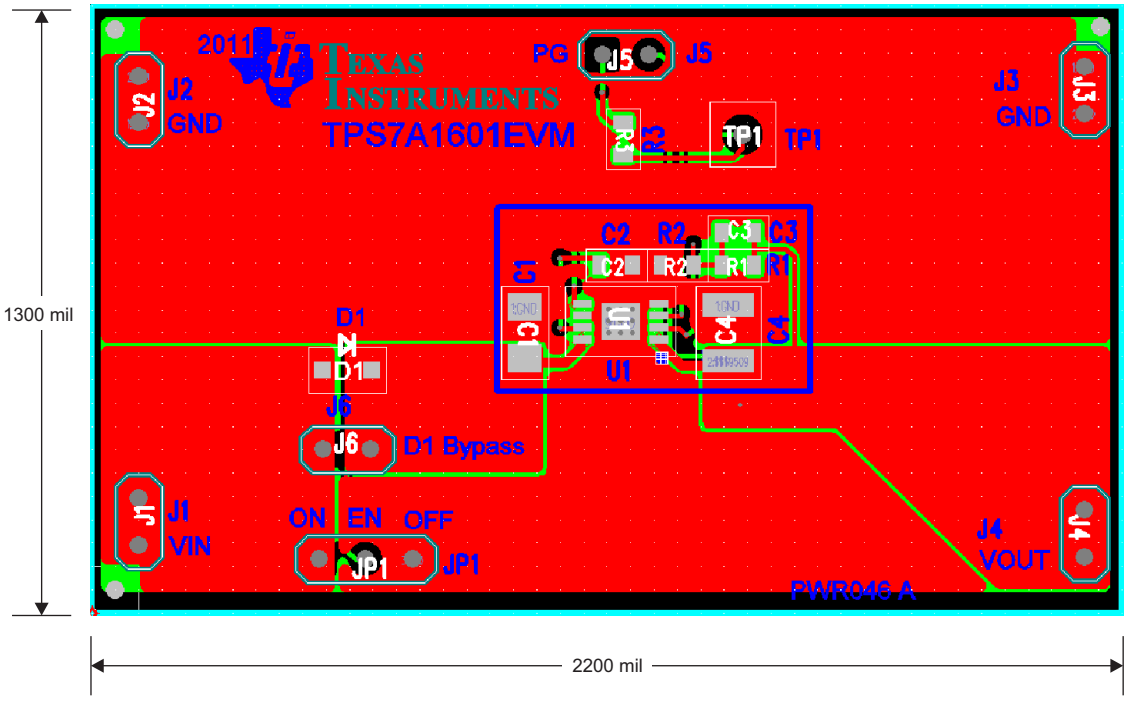


Figure 22. Suggested Layout: Top Layer

Layout Example (continued)

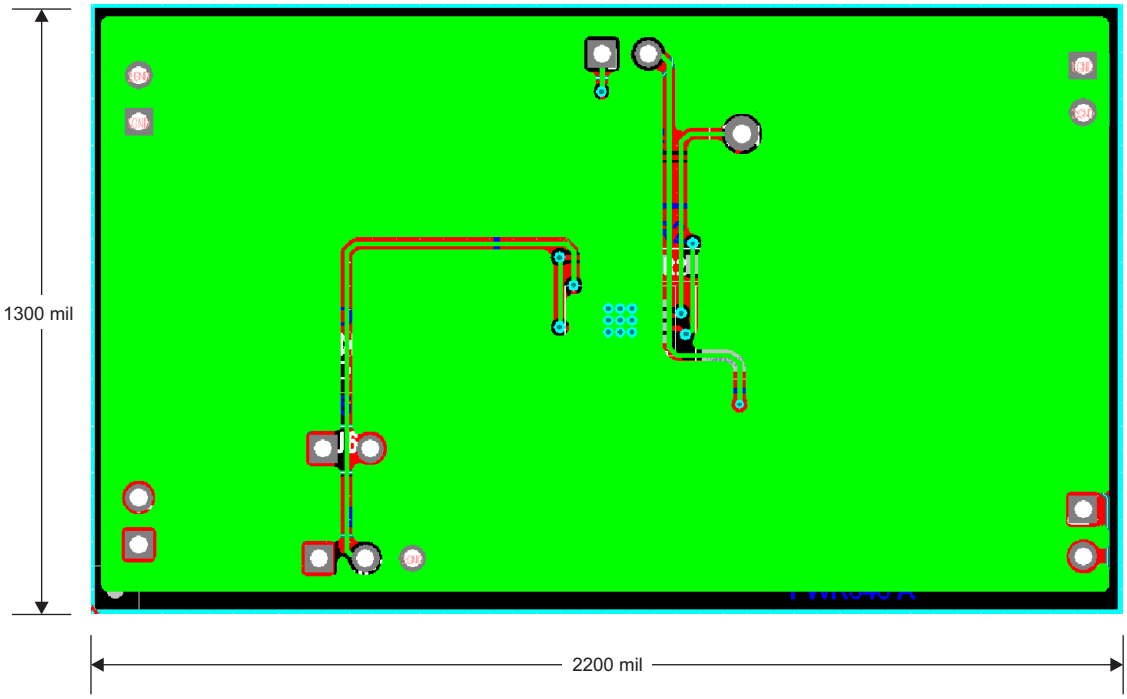


Figure 23. Suggested Layout: Bottom Layer

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

10.4 Thermal Considerations

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat spreading area. For reliable operation, junction temperature should be limited to a maximum of +125°C at the worst case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A16 into thermal shutdown degrades device reliability.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- *《使用前馈电容和低压降稳压器的优缺点》*，SBVA042
- *《使用新的热指标》*，SBVA025

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1601DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTYQ	Samples
TPS7A1601DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTYQ	Samples
TPS7A1601DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA5M	Samples
TPS7A1601DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA5M	Samples
TPS7A1633DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPNQ	Samples
TPS7A1633DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPNQ	Samples
TPS7A1633DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPNQ	Samples
TPS7A1633DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPNQ	Samples
TPS7A1650DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPOQ	Samples
TPS7A1650DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPOQ	Samples
TPS7A1650DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPOQ	Samples
TPS7A1650DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPOQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

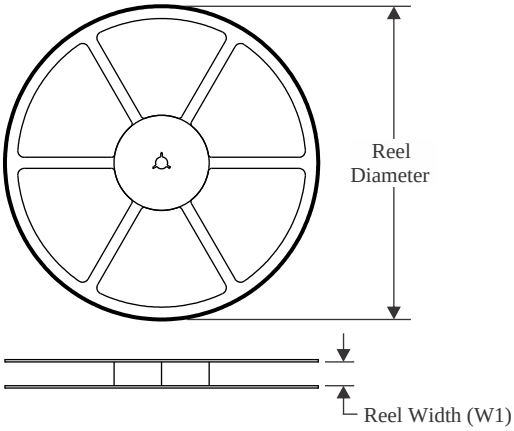
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

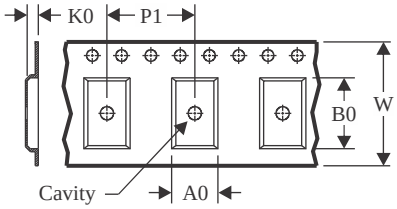
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

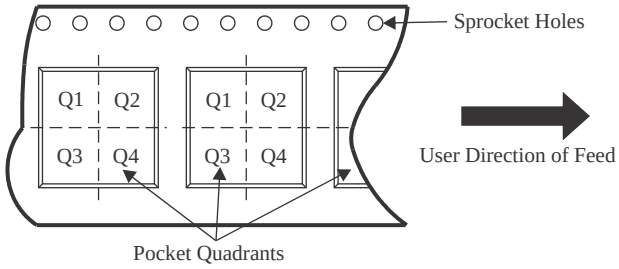


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

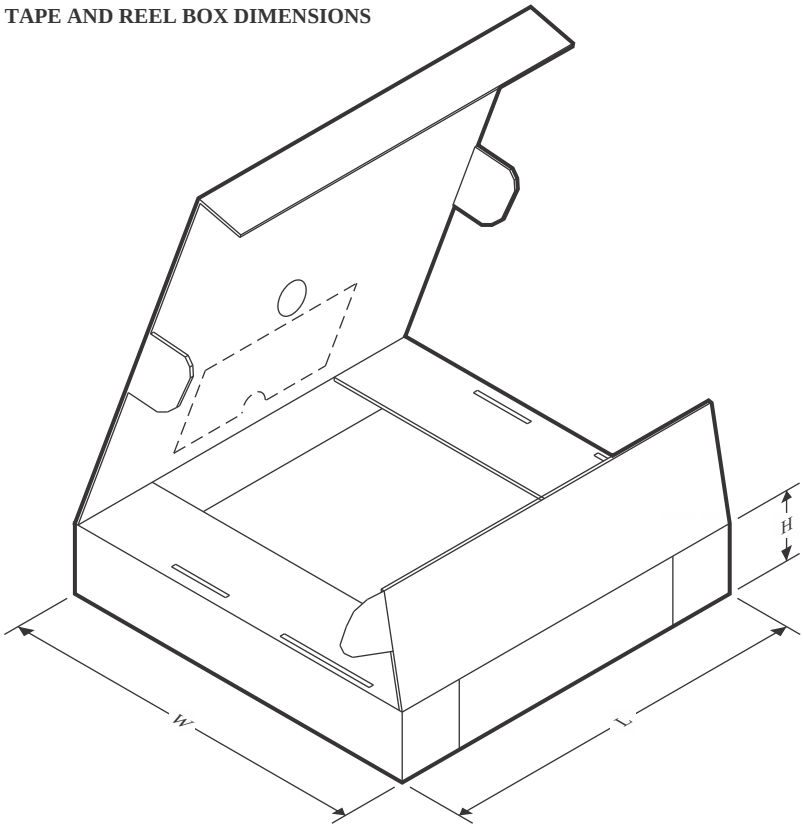
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1601DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS7A1601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS7A1633DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS7A1633DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS7A1650DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS7A1650DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601DGNR	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1601DGNT	HVSSOP	DGN	8	250	213.0	191.0	35.0
TPS7A1601DRBR	SON	DRB	8	3000	367.0	367.0	38.0
TPS7A1601DRBT	SON	DRB	8	250	213.0	191.0	35.0
TPS7A1633DGNR	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1633DGNT	HVSSOP	DGN	8	250	213.0	191.0	35.0
TPS7A1633DRBR	SON	DRB	8	3000	367.0	367.0	38.0
TPS7A1633DRBT	SON	DRB	8	250	213.0	191.0	35.0
TPS7A1650DGNR	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1650DGNT	HVSSOP	DGN	8	250	213.0	191.0	35.0
TPS7A1650DRBR	SON	DRB	8	3000	367.0	367.0	38.0
TPS7A1650DRBT	SON	DRB	8	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

DRB 8

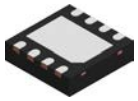
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

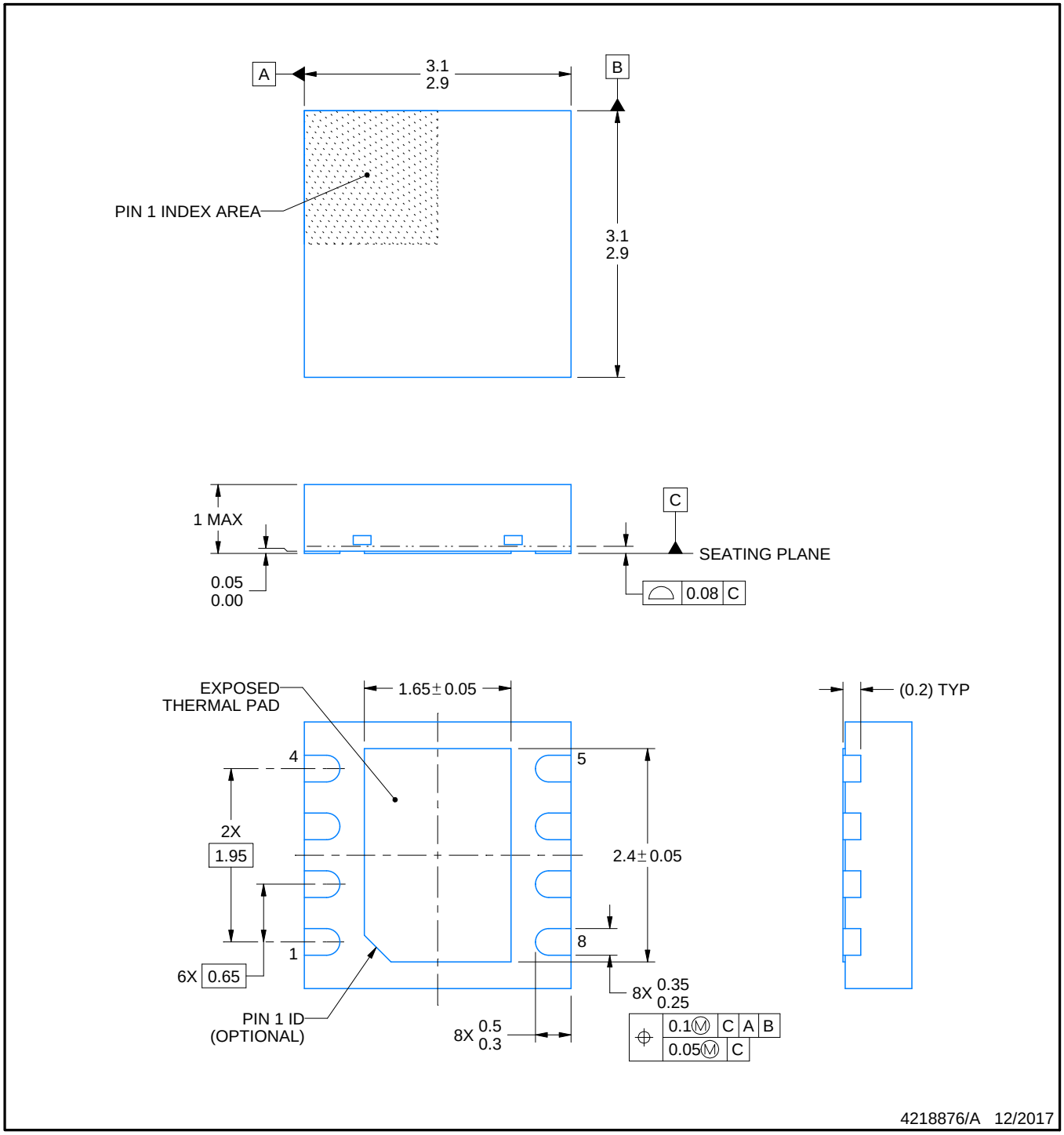
DRB0008B



PACKAGE OUTLINE

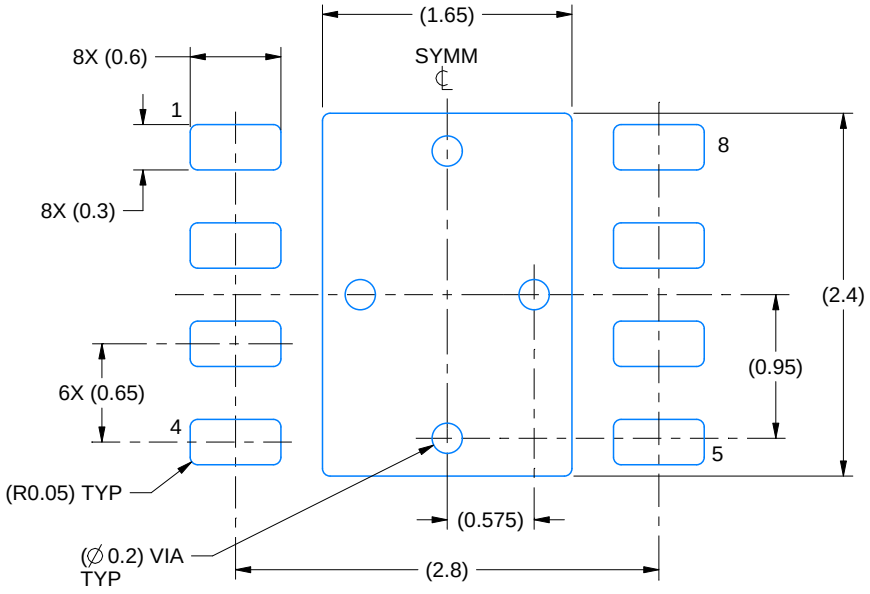
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

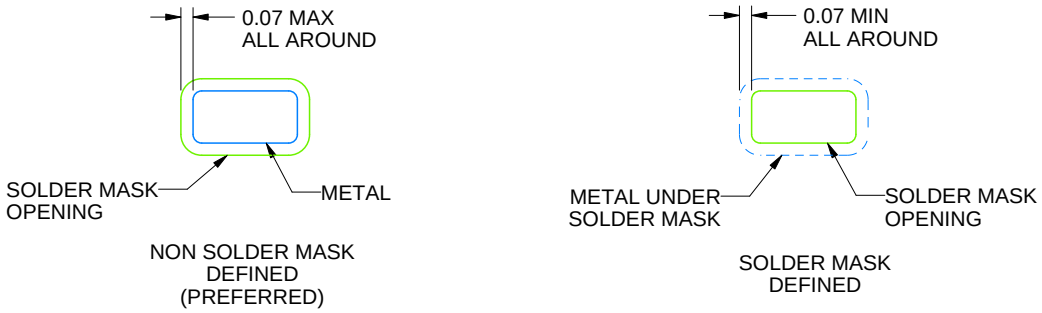


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

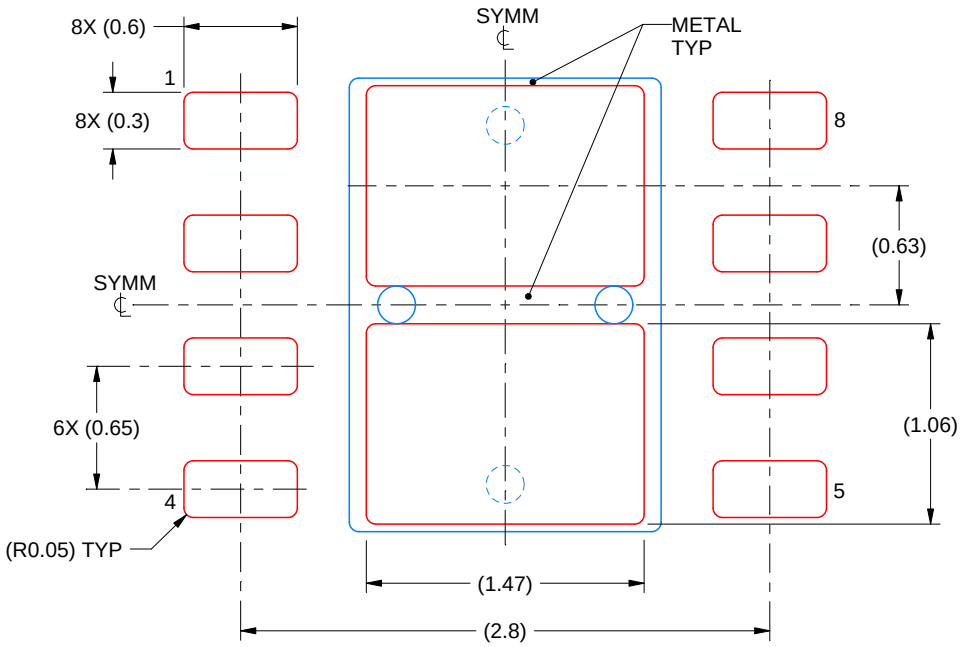


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

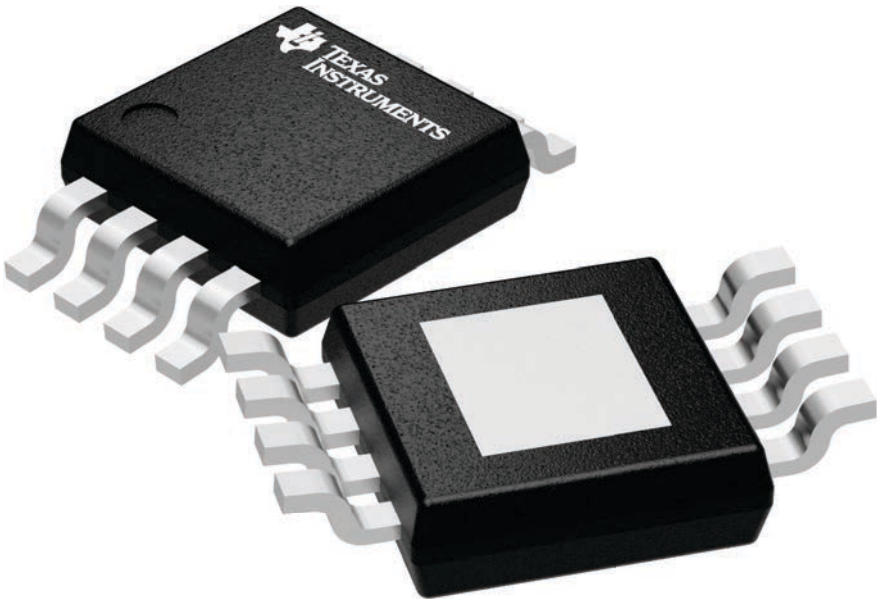
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

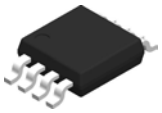
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

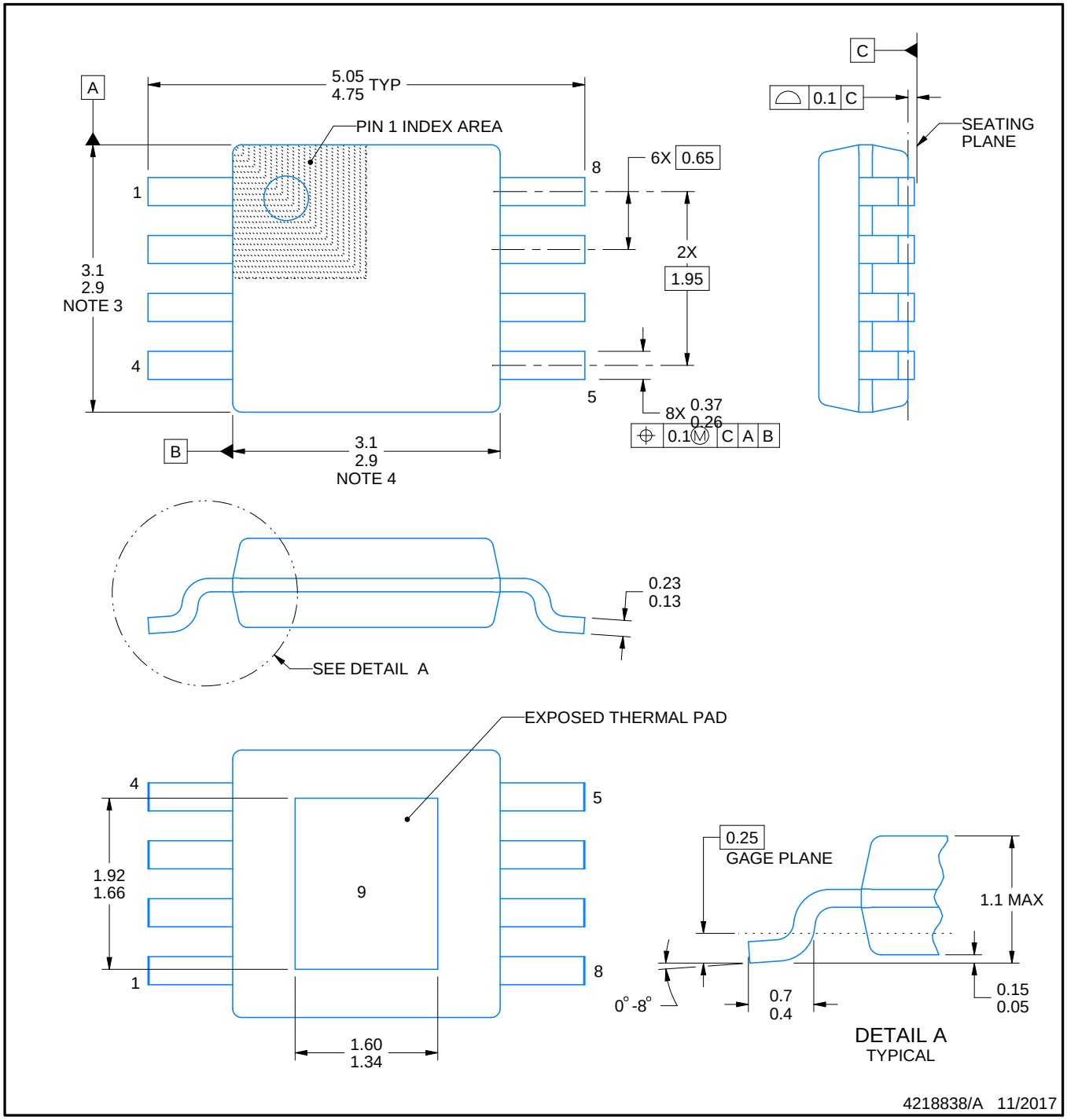
PACKAGE OUTLINE

DGN0008C



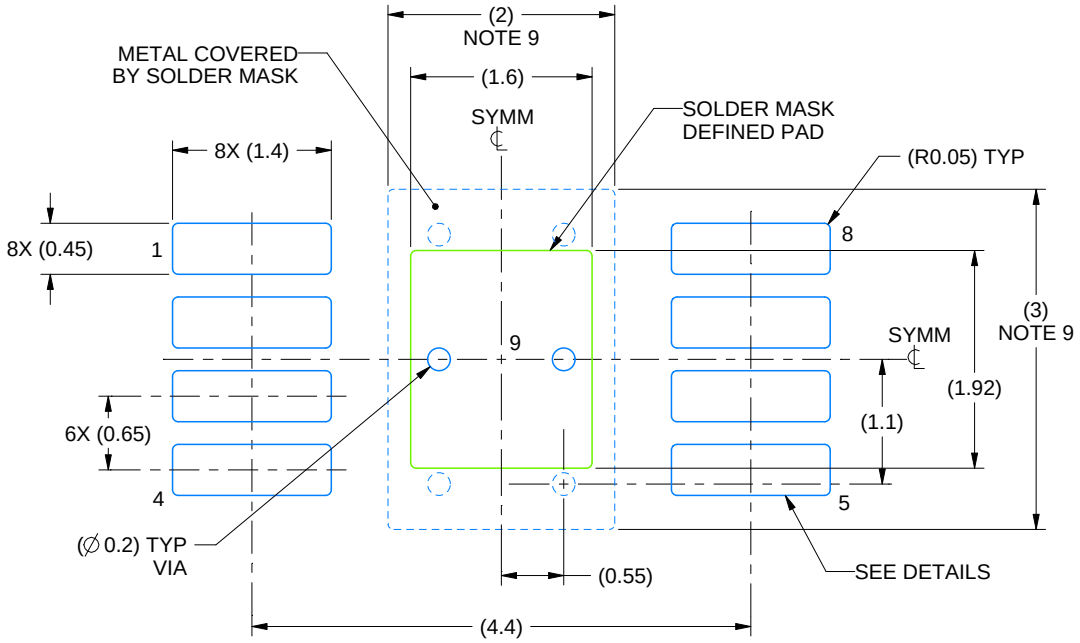
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

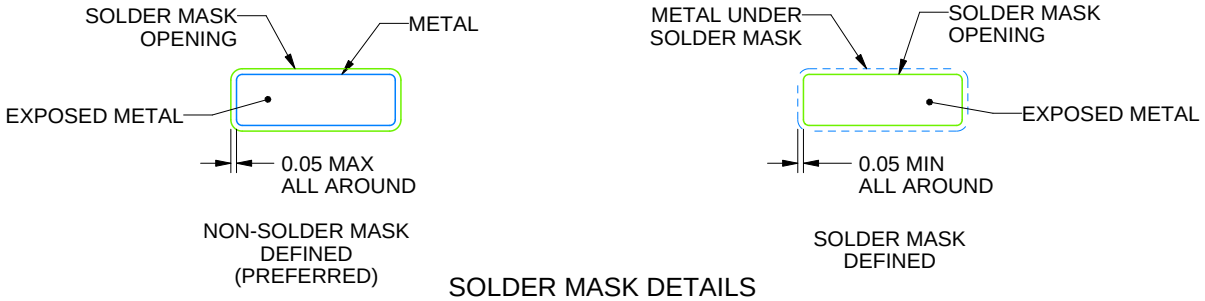


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

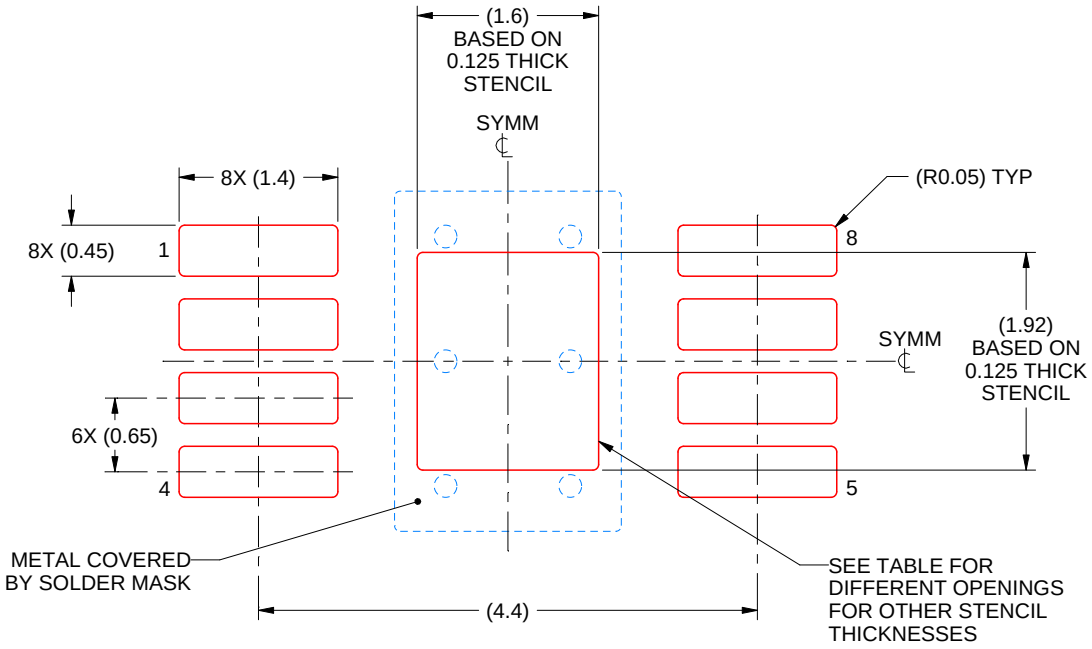


SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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