用于生物电势测量的 ADS129x 低功耗、双通道、24 位模拟前端

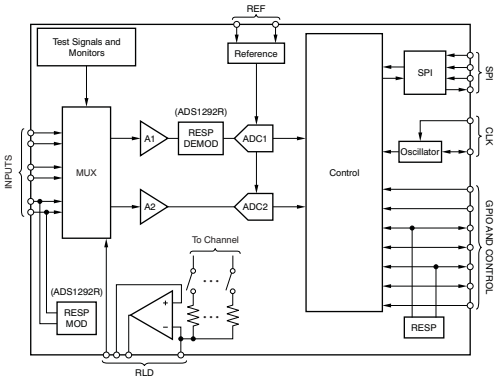
1 特性

- 两个低噪声 PGA 和两个高分辨率 ADC（ADS1292 和 ADS1292R）
- 低功耗：335µW/通道
- 输入参考噪声：8μV_{PP}（150Hz 带宽，G = 6）
- 输入偏置电流：200pA
- 数据速率：125SPS 至 8kSPS
- CMRR：120dB
- 可编程增益：1、2、3、4、6、8 或 12
- 电源：单极或者双极
  - 模拟：2.7V 至 5.25V
  - 数字：1.7V 至 3.6V
- 内置右腿驱动放大器、持续断线检测、测试信号
- 集成型呼吸阻抗测量 (ADS1292R)
- 内置振荡器和基准
- 灵活的断电、待机模式
- SPI™兼容串行接口
- 工作温度范围：–40°C 至 +85°C

2 应用

- 医疗仪器 (ECG) 包括：
  - 患者监护：动态心电图 (Holter)、事件、压力和生命体征，包括心电图、AED 和远程医疗
  - 个人护理和健身监视器（心率、呼吸和 ECG）
- 高精度、同步、多通道数据采集

简化框图



3 说明

ADS1291、ADS1292 和 ADS1292R 是多通道同步采样 24 位 Δ-Σ 模数转换器 (ADC)，它们具有内置的可编程增益放大器 (PGA)、内部基准和板载振荡器。

ADS1291、ADS1292 和 ADS1292R 包含 便携式 低功耗医疗心电图 (ECG)、体育和健身 应用通常所需的所有功能。

凭借高集成度和出色的性能，ADS1291、ADS1292 和 ADS1292R 可在显著减少尺寸、功耗和总体成本的前提下创建可扩展的医疗仪器系统。

ADS1291、ADS1292 和 ADS1292R 每通道具有灵活的输入多路复用器，此多路复用器可独立连接至内部生成的信号，实现测试、温度和持续断线检测。此外，可选择输入通道的任一配置生成右腿驱动 (RLD) 输出信号。ADS1291、ADS1292 和 ADS1292R 工作时的数据速率高达 8kSPS。通过器件内部激励灌电流或拉电流，可在器件内部执行持续断线检测。ADS1292R 版本包括一个完全集成的呼吸阻抗测量功能。

这些器件采用 5mm × 5mm、32 引脚薄型四方扁平封装 (TQFP) 和 4mm x 4mm、32 引脚无引线四方扁平封装 (VQFN)。额定工作温度范围 –40°C 至 +85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS129x	TQFP (32)	5.00mm × 5.00mm
	VQFN (32)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (September 2012) to Revision C **Page**

- 已添加 添加了*器件信息* 表、*ESD 额定值* 表、首页图的标题、*建议运行条件* 表、*特性 说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已更改 将 CMRR 值从 *105dB* 更改为 *120dB*（位于*特性* 部分） ... 1
- 已更改 更改了*应用* 部分 ... 1
- 已更改 通篇将 *QFN* 更改为 *VQFN* ... 1
- Added thermal pad data to RDM pin out package drawing ... 4
- Changed *Pin Functions* title from *Pin Assignments*, changed *Terminal* column header to *Pin*, and corrected format to show both package options ... 4
- Changed function and description of RESP_MODN/IN3N and RESP_MODP/IN3P pins, changed function of RLDOUT pin from *Analog input* to *Analog output*, and added Thermal Pad row to *Pin Assignments* table ... 4
- Deleted *Family and Ordering Information* table ... 6
- Changed CMRR parameter values from *–105 dB* to *105 dB* (minimum) and from *–120 dB* to *120 dB* (typical) in *Electrical Characteristics* table ... 7
- Changed *Noise Measurements* section: deleted SNR equation, changed *DYN RANGE* and *EFF RESOL* column headers in section tables ... 15
- Added last sentence to *Internal Respiration Circuitry with External Clock (ADS1292R)* section ... 39
- Changed denominator of equation 10 ... 41
- Changed first paragraph of *Data Output (DOUT)* section ... 42
- Changed *RDATAC Usage* figure ... 48
- Changed *RDATA Usage* figure ... 49
- Changed *ADS1292R Application* section to fulfill *Typical Application* section ... 62

Changes from Revision A (March 2012) to Revision B **Page**

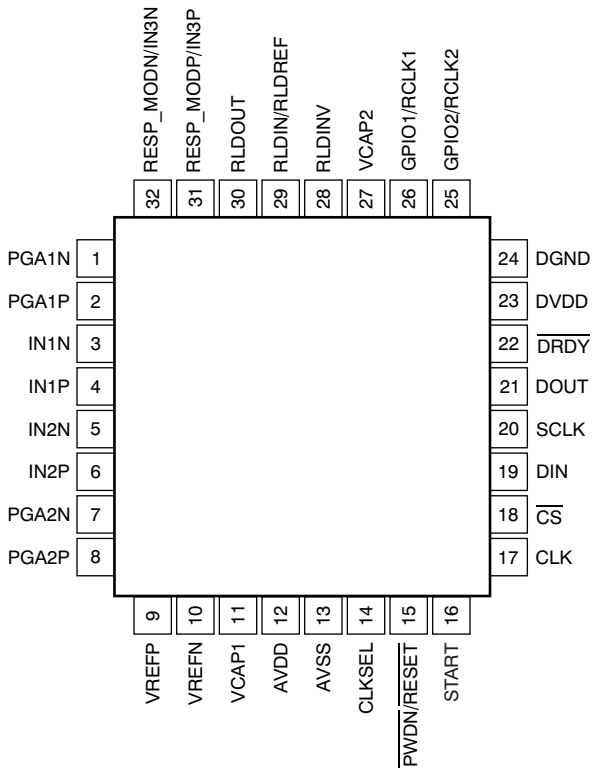
- 已添加 向器件图形添加了 QFN 封装 1
- Added QFN pin out drawing 4
- Changed AVSS to DGND row in Absolute Maximum Ratings table 6
- Changed parameters of Supply Current (RLD Amplifier Turned Off) section in Electrical Characteristics table 10
- Changed description of bit 6 in LOFF_STATUS: Lead-Off Status register 59

Changes from Original (December 2011) to Revision A **Page**

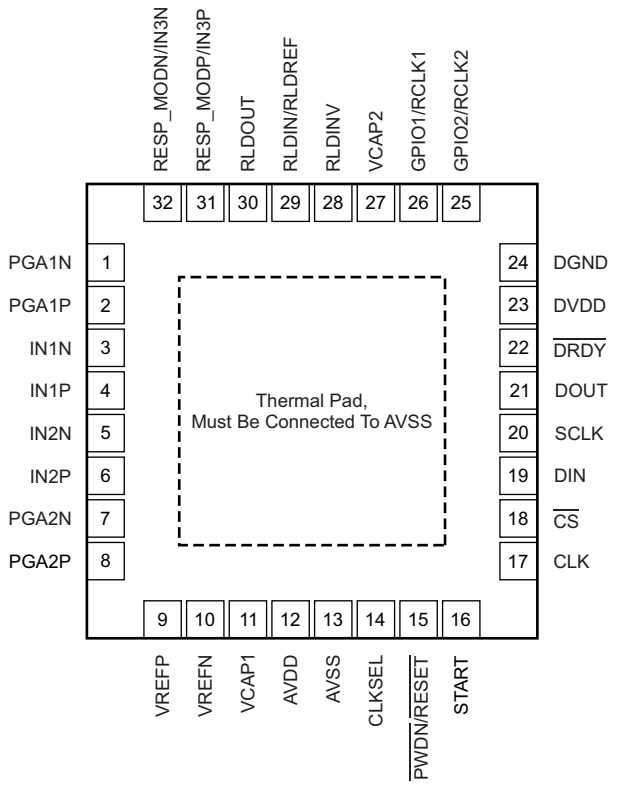
- 已更改 更改了器件图形 1
- 已更改 将器件状态从“混合状态”更改为“生产数据” 1
- 已更改 更改了第二个 “特性” 项目符号 1
- Updated Family and Ordering Information table 6
- Moved ADS1292R to production status 6
- Deleted footnote 2 from Family and Ordering Information table 6
- Changed values of AVDD to AVSS and DVDD to DGND rows in Absolute Maximum Ratings table 6
- Changed *Operating temperature range* parameter in Absolute Maximum Ratings table 6
- Changed DC Channel Performance, *INL* parameter test conditions in Electrical Characteristics table 7
- Changed AC Channel Performance, *SNR* and *THD* parameters test conditions in Electrical Characteristics table 7
- Added third Channel Performance, *THD* parameter row to Electrical Characteristics table 7
- Added Digital Filter section to Electrical Characteristics table 8
- Deleted Right Leg Drive Amplifier, *Quiescent power consumption* parameter test condition from Electrical Characteristics table 8
- Changed Respiration, *Impedance measurement noise* parameter test conditions in Electrical Characteristics table 8
- Changed Respiration, *Maximum modulator current* parameter in Electrical Characteristics table 8
- Changed Power-Supply Requirements, *Digital supply* parameter in Electrical Characteristics table 9
- Changed first I_{DVDD} Supply Current, *Normal mode* parameter test conditions in Electrical Characteristics table 10
- Changed 3-V Power Dissipation, *Quiescent power dissipation, per channel* parameter typical specifications in Electrical Characteristics table 10
- Added C_{FILTER} to Typical Characteristics conditions 12
- Updated Figure 5 12
- Updated Figure 9 and Figure 12 12
- Changed description of CHnSET setting in *Supply Measurements (MVDDP, MVDDN)* section 21
- Changed second paragraph of *PGA Settings and Input Range* section 23
- Changed description of $\overline{\text{PD\_REFBUF}}$ bit in the *Reference* section 27
- Updated second column title in Table 9 28
- Updated Figure 33 30
- Updated Figure 42 38
- Added description of Figure 43, Figure 43, and Table 12 to *Internal Respiration Circuitry with External Clock (ADS1292R)* section 39
- Updated description of DOUT and $\overline{\text{DRDY}}$ in *RDATAC: Read Data Continuous* section 48
- Updated RLD_STAT in address 08h of Table 16 51
- Changed description of bit 1 in CONFIG2: Configuration Register 2 53
- Changed descriptions of bits[3:0] in CH2SET: Channel 2 Settings 56
- Updated Figure 70 and Figure 71 64
- Updated Figure 73 and added footnote 1 67
- Updated Figure 74 and added footnote 1 68

5 Pin Configuration and Functions

PBS Package
32-Pin TQFP
Top View



RSM Package
32-Pin VQFN
Top View



Pin Functions

PIN			FUNCTION	DESCRIPTION
NO.	PBS (TQFP)	RSM (VQFN)		
1	PGA1N	PGA1N	Analog output	PGA1 inverting output
2	PGA1P	PGA1P	Analog output	PGA1 noninverting output
3	IN1N(1)	IN1N(1)	Analog input	Differential analog negative input 1
4	IN1P(1)	IN1P(1)	Analog input	Differential analog positive input 1
5	IN2N(1)	IN2N(1)	Analog input	Differential analog negative input 2
6	IN2P(1)	IN2P(1)	Analog input	Differential analog positive input 2
7	PGA2N	PGA2N	Analog output	PGA2 inverting output
8	PGA2P	PGA2P	Analog output	PGA2 noninverting output
9	VREFP	VREFP	Analog input/output	Positive reference voltage
10	VREFN	VREFN	Analog input	Negative reference voltage; must be connected to AVSS
11	VCAP1	VCAP1	—	Analog bypass capacitor
12	AVDD	AVDD	Supply	Analog supply
13	AVSS	AVSS	Supply	Analog ground
14	CLKSEL	CLKSEL	Digital input	Master clock select
15	$\overline{\text{PWDN/RESET}}$	$\overline{\text{PWDN/RESET}}$	Digital input	Power-down or system reset; active low
16	START	START	Digital input	Start conversion
17	CLK	CLK	Digital input	Master clock input
18	$\overline{\text{CS}}$	$\overline{\text{CS}}$	Digital input	Chip select
19	DIN	DIN	Digital input	SPI data in

(1) Connect unused analog inputs to AVDD.

Pin Functions (continued)

PIN			FUNCTION	DESCRIPTION
NO.	PBS (TQFP)	RSM (VQFN)		
20	SCLK	SCLK	Digital input	SPI clock
21	DOUT	DOUT	Digital output	SPI data out
22	$\overline{\text{DRDY}}$	$\overline{\text{DRDY}}$	Digital output	Data ready; active low
23	DVDD	DVDD	Supply	Digital power supply
24	DGND	DGND	Supply	Digital ground
25	GPIO2/RCLK2	GPIO2/RCLK2	Digital input/output	General-purpose I/O 2 or resp clock 2 (ADS1292R)
26	GPIO1/RCLK1	GPIO1/RCLK1	Digital input/output	General-purpose I/O 1 or resp clock 1 (ADS1292R)
27	VCAP2	VCAP2	—	Analog bypass capacitor
28	RLDINV	RLDINV	Analog input	Right leg drive inverting input; connect to AVDD if not used
29	RLDIN/ RLDREF	RLDIN/ RLDREF	Analog input	Right leg drive input to MUX or RLD amplifier noninverting input; connect to AVDD if not used
30	RLDOUT	RLDOUT	Analog output	Right leg drive output
31	RESP_MODP/ IN3P(1)	RESP_MODP/ IN3P(1)	Analog output/input	P-side respiration excitation signal for respiration (analog output) or auxiliary input 3P (analog input)
32	RESP_MODN/ IN3N(1)	RESP_MODN/ IN3N(1)	Analog output/input	N-side respiration excitation signal for respiration (analog output) or auxiliary input 3N (analog input)
Power Pad	—	Pad	—	Thermal pad; must be connected to AVSS

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AVDD to AVSS		–0.3	5.5	V
DVDD to DGND		–0.3	3.9	V
AVSS to DGND		–3	0.2	V
Analog input to AVSS		AVSS – 0.3	AVDD + 0.3	V
Digital input to DVDD		DVSS – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins			±10	mA
Input current	Momentary		±100	mA
	Continuous		±10	
Operating temperature range		–40	+85	°C
Maximum junction temperature (T_J)			150	°C
Storage temperature, T_{stg}		–60	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply, AVDD to AVSS	2.7	5	5.25	V
DVDD	Digital power supply, DVDD to DGND	1.7	3	3.6	V
	Analog input voltage	AVSS		AVDD	V
	Digital input voltage	DVSS		DVDD	V
T_A	Operating ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS1291, ADS1292, ADS1292R		UNIT
		PBS (TQFP)	RSM (VQFN)	
		32 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.4	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.5	25.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.3	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from –40°C to +85°C; typical specifications are at +25°C; all specifications are at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Full-scale differential input voltage (AINP – AINN)			$\pm V_{REF}$ / gain		V
	Input common-mode range			See the *Input Common-Mode Range* subsection of the *PGA Settings and Input Range* section		
	Input capacitance			20		pF
	Input bias current (PGA chop = 8 kHz)	T_A = +25°C, input = 1.5 V			±200	pA
		T_A = –40°C to +85°C, input = 1.5 V		±1		nA
		Chop rates other than 8 kHz		See *Pace Detect* section		
	DC input impedance	No pull-up or pull-down current source	1000			MΩ
		Current source lead-off detection (nA), AVSS + 0.3 V < AIN < AVDD – 0.3 V		500		MΩ
		Current source lead-off detection (µA), AVSS + 0.6 V < AIN < AVDD – 0.6 V		100		MΩ
PGA PERFORMANCE						
	Gain settings			1, 2, 3, 4, 6, 8, 12		
	Bandwidth	With a 4.7-nF capacitor on PGA output (see *PGA Settings and Input Range* section for details)		8.5		kHz
ADC PERFORMANCE						
	Resolution		24			Bits
	Data rate	f_{CLK} = 512 kHz	125		8000	SPS
CHANNEL PERFORMANCE (DC Performance)						
	Input-referred noise	Gain = 6(3), 10 seconds of data		8		μV_{PP}
		Gain = 6, 256 points, 0.5 seconds of data		8	11	μV_{PP}
		Gain settings other than 6, data rates other than 500 SPS		See *Noise Measurements* section		
	Integral nonlinearity	Full-scale with gain = 6, best fit		2		ppm
	Offset error			±100		µV
	Offset error drift			2		µV/°C
	Offset error with calibration			15		µV
	Gain error	Excluding voltage reference error		±0.1	±0.2	% of FS
	Gain drift	Excluding voltage reference drift		2		ppm/°C
	Gain match between channels			0.2		% of FS
CHANNEL PERFORMANCE (AC performance)						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz(4)	105	120		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz and 60 Hz		90		dB
	Crosstalk	f_{IN} = 50 Hz and 60 Hz		–120		dB
SNR	Signal-to-noise ratio	f_{IN} = 10 Hz input, gain = 6		107		dB
THD	Total harmonic distortion	10 Hz, –0.5 dBFs, C_{FILTER} = 4.7nF		–104		dB
		100 Hz, –0.5 dBFs, C_{FILTER} = 4.7nF		–95		dB
		ADS1292R channel 1, 10 Hz, –0.5 dBFS, C_{FILTER} = 47 nF		–82		dB

(1) Performance is applicable for 5-V operation as well. Production testing for limits is performed at 3 V.
(2) C_{FILTER} is the capacitor accross the PGA outputs; see the *PGA Settings and Input Range* section for details.
(3) Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.
(4) CMRR is measured with a common-mode signal of AVSS + 0.3 V to AVDD – 0.3 V. The values indicated are the minimum of the two channels.

Electrical Characteristics (continued)

minimum and maximum specifications apply from –40°C to +85°C; typical specifications are at +25°C; all specifications are at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER						
	–3-dB bandwidth			0.262 f_{DR}		Hz
	Digital filter settling	Full setting		4		Conversions
RIGHT LEG DRIVE (RLD) AMPLIFIER						
	RLD integrated noise	BW = 150 Hz		1.4		μV_{RMS}
GBP	Gain bandwidth product	50 kΩ || 10 pF load, gain = 1		100		kHz
SR	Slew rate	50 kΩ || 10 pF load, gain = 1		0.07		V/µs
THD	Total harmonic distortion	f_{IN} = 100 Hz, gain = 1		–85		dB
CMIR	Common-mode input range		AVSS + 0.3		AVDD – 0.3	V
	Common-mode resistor matching	Internal 200-kΩ resistor matching		0.1		%
I_{SC}	Short-circuit current			1.1		mA
	Quiescent power consumption			5		µA
LEAD-OFF DETECT						
	Frequency	See *Register Map* section for settings		0, f_{DR} / 4		kHz
	Current	ILEAD_OFF [1:0] = 00		6		nA
		ILEAD_OFF [1:0] = 01		22		nA
		ILEAD_OFF [1:0] = 10		6		µA
		ILEAD_OFF [1:0] = 11		22		µA
	Current accuracy			±10		%
	Comparator threshold accuracy			±10		mV
RESPIRATION (ADS1292R)						
	Frequency	Internal source		32, 64		kHz
		External source	32		64	kHz
	Phase shift	See *Register Map* section for settings	0	112.5	168.75	Degrees
	Impedance range	I_{RESP} = 30 µA		2000	10,000	Ω
	Impedance measurement noise	0.05-Hz to 2-Hz brick wall filter, 32-kHz modulation clock, phase = 112.5, using I_{RESP} = 30 µA with 2-kΩ baseline load, gain = 4		40		$m\Omega_{PP}$
	Maximum modulator current	Using Internal reference		100		µA
EXTERNAL REFERENCE						
	Reference input voltage	3-V supply V_{REF} = (VREFP – VREFN)	2	2.5	VDD – 0.3	V
		5-V supply V_{REF} = (VREFP – VREFN)	2	4	VDD – 0.3	V
VREFN	Negative input			AVSS		V
VREFP	Positive input			AVSS + 2.5		V
	Input impedance			120		kΩ

Electrical Characteristics (continued)

minimum and maximum specifications apply from –40°C to +85°C; typical specifications are at +25°C; all specifications are at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE							
	Output voltage		Register bit CONFIG2.VREF_4V = 0		2.42		V
			Register bit CONFIG2.VREF_4V = 1		4.033		V
	Output current drive		Available for external use		100		µA
	V_{REF} accuracy				±0.5		%
	Internal reference drift		–40°C ≤ T_A ≤ +85°C		45		ppm/°C
	Start-up time		Settled to 0.2% with 10-µF capacitor on VREFP pin		100		ms
	Quiescent current consumption				20		µA
SYSTEM MONITORS							
	Analog supply reading error				1		%
	Digital supply reading error				1		%
	Device wake up		From power-supply ramp after power-on reset (POR) to $\overline{DRDY}$ low		32		ms
			From power-down mode to $\overline{DRDY}$ low		10		ms
			From STANDBY mode to $\overline{DRDY}$ low		10		ms
	VCAP1 settling time		1% accuracy		0.5		s
	Temperature sensor reading	Voltage	T_A = +25°C		145		mV
		Coefficient			490		µV/°C
TEST SIGNAL							
	Signal frequency		See *Register Map* section for settings		At dc and 1 Hz		Hz
	Signal voltage		See *Register Map* section for settings		±1		mV
	Accuracy				±2		%
CLOCK							
	Internal oscillator clock frequency		Nominal frequency		512		kHz
	Internal clock accuracy		T_A = +25°C			±0.5	%
			–40°C ≤ T_A ≤ +85°C			±1.5	%
	Internal oscillator start-up time				32		µs
	Internal oscillator power consumption				30		µW
	External clock input frequency		CLKSEL pin = 0, CLK_DIV = 0	485	512	562.5	kHz
			CLKSEL pin = 0, CLK_DIV = 1	1.94	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT							
V_{IH}	Logic level	DVDD = 1.8 V to 3.6 V		0.8 DVDD		DVDD + 0.1	V
V_{IL}		DVDD = 1.8 V to 3.6 V		–0.1		0.2 DVDD	V
V_{IH}		DVDD = 1.7 V to 1.8 V		DVDD – 0.2			V
V_{IL}		DVDD = 1.7 V to 1.8 V				0.2	V
V_{OH}		DVDD = 1.7 V to 3.6 V	I_{OH} = –500 µA	0.9 DVDD			V
V_{OL}		DVDD = 1.7 V to 3.6 V	I_{OL} = +500 µA			0.1 DVDD	V
I_{IN}		Input current	0 V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER-SUPPLY REQUIREMENTS							
AVDD	Analog supply	AVDD – AVSS		2.7	3	5.25	V
DVDD	Digital supply	DVDD – DGND		1.7	1.8	3.6	V
	AVDD – DVDD			–2.1		3.6	V

Electrical Characteristics (continued)

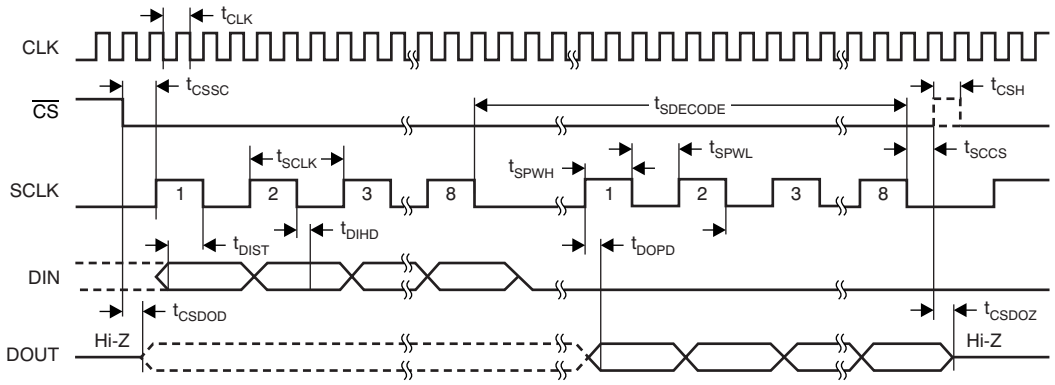
minimum and maximum specifications apply from –40°C to +85°C; typical specifications are at +25°C; all specifications are at DVDD = 1.8 V, AVDD – AVSS = 3 V(1), V_{REF} = 2.42 V, external f_{CLK} = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF(2), and gain = 6 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (RLD Amplifier Turned Off)							
	I_{AVDD}	ADS1292 and ADS1292R	AVDD – AVSS = 3 V		205		µA
			AVDD – AVSS = 5 V		250		µA
	I_{DVDD}	ADS1292 and ADS1292R	DVDD = 3.3 V		75		µA
			DVDD = 1.8 V		32		µA
POWER DISSIPATION (Analog Supply = 3 V, RLD Amplifier Turned Off)							
	Quiescent power dissipation	ADS1292 and ADS1292R	Normal mode		670	740	µW
			Standby mode		160		µW
		ADS1291	Normal mode		450	495	µW
			Standby mode		160		µW
	Quiescent power dissipation, per channel	ADS1292R	Normal mode		335		µW
		ADS1292	Normal mode		335		µW
		ADS1291	Normal mode		450		µW
POWER DISSIPATION (Analog Supply = 5 V, RLD Amplifier Turned Off)							
	Quiescent power dissipation	ADS1292 and ADS1292R	Normal mode		1300		µW
			Standby mode		340		µW
		ADS1291	Normal mode		950		µW
			Standby mode		340		µW
	Quiescent power dissipation, per channel	ADS1292R	Normal mode		670		µW
		ADS1292	Normal mode		670		µW
		ADS1291	Normal mode		860		µW
POWER DISSIPATION IN POWER-DOWN MODE							
	Analog supply = 3 V	DVDD = 1.8 V			1		µW
		DVDD = 3.3 V			4		µW
	Analog supply = 5 V	DVDD = 1.8 V			5		µW
		DVDD = 3.3 V			10		µW
TEMPERATURE							
	Specified temperature range			–40		+85	°C
	Operating temperature range			–40		+85	°C
	Storage temperature range			–60		+150	°C

6.6 Timing Requirements

specifications apply from –40°C to +85°C; load on D_{OUT} = 20 pF || 100 kΩ

		2.7 V ≤ DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_{CLK}	Master clock period (CLK_DIV bit of LOFF_STAT register = 0)	1775		2170	1775		2170	ns
	Master clock period (CLK_DIV bit of LOFF_STAT register = 1)	444		542	444		542	ns
t_{CSSC}	$\overline{CS}$ low to first SCLK, setup time	6			17			ns
t_{SCLK}	SCLK period	50			66.6			ns
$t_{SPWH, L}$	SCLK pulse width, high and low	15			25			ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10			10			ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10			11			ns
t_{DOPD}	SCLK rising edge to DOUT valid			12			22	ns
t_{CSH}	$\overline{CS}$ high pulse	2			2			t_{CLKs}
t_{CSDOD}	$\overline{CS}$ low to DOUT driven	10			20			ns
t_{SCCS}	Eighth SCLK falling edge to $\overline{CS}$ high	3			3			t_{CLKs}
$t_{SDECODE}$	Command decode time	4			4			t_{CLKs}
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z			10			20	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

6.7 Typical Characteristics

at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.42 V, VREFN = AVSS, external clock = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF, and gain = 6 (unless otherwise noted)

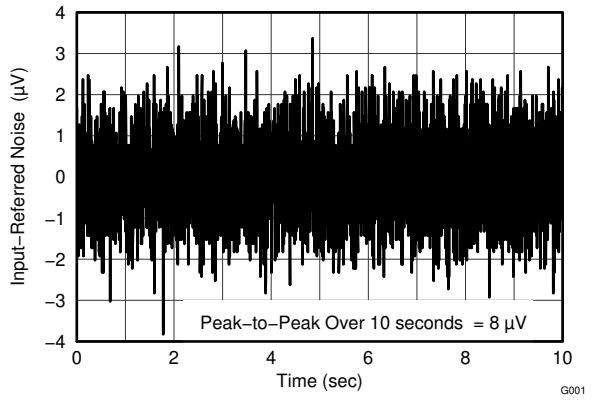


Figure 2. Input-Referred Noise

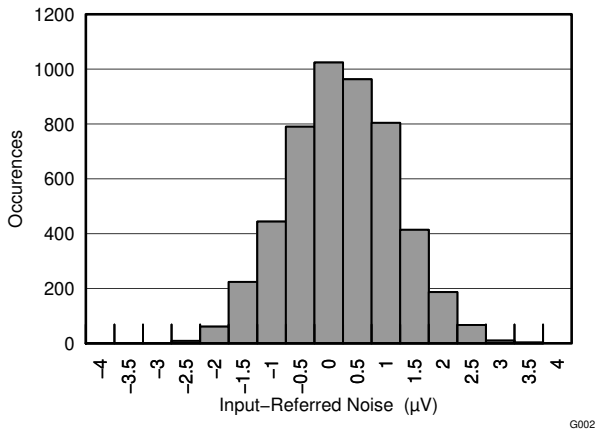


Figure 3. Noise Histogram

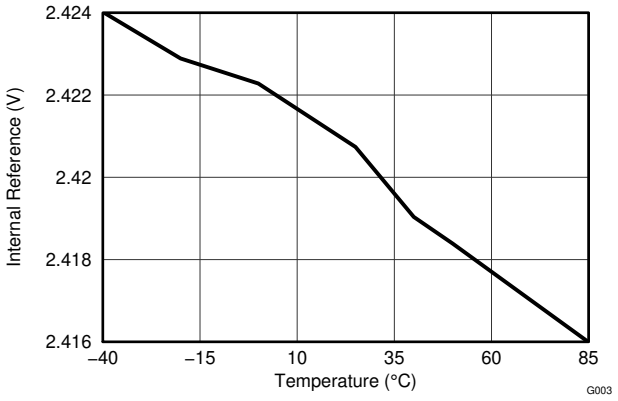


Figure 4. Internal Reference vs Temperature

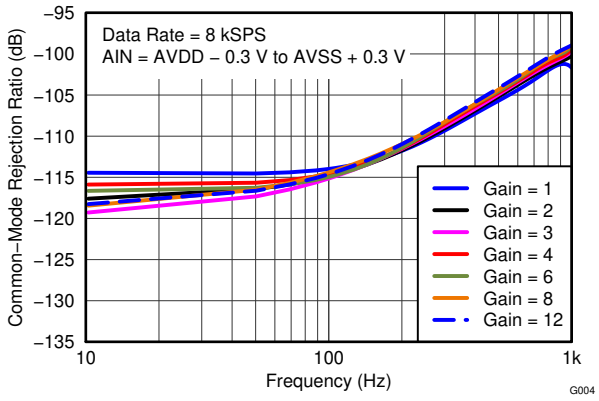


Figure 5. CMRR vs Frequency

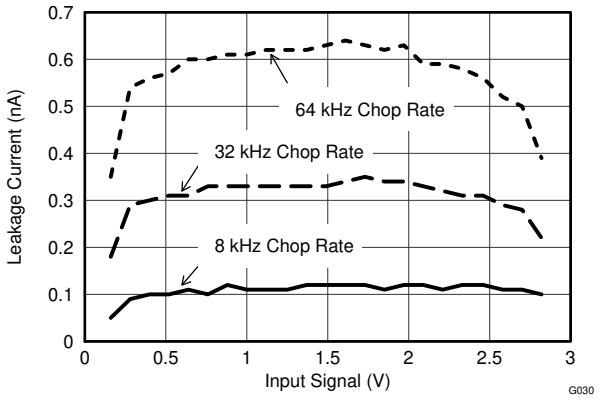


Figure 6. Leakage Current vs Input Voltage

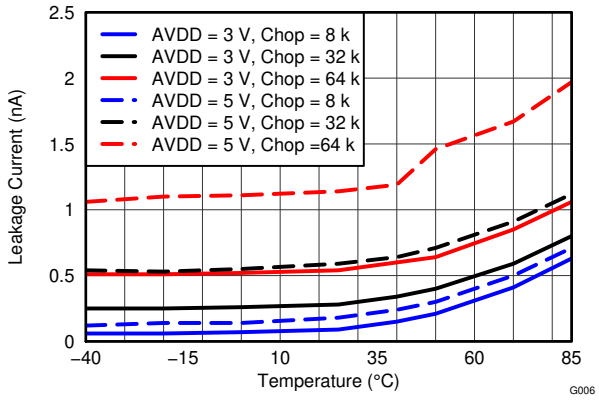


Figure 7. Leakage Current vs Temperature

Typical Characteristics (continued)

at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.42 V, VREFN = AVSS, external clock = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF, and gain = 6 (unless otherwise noted)

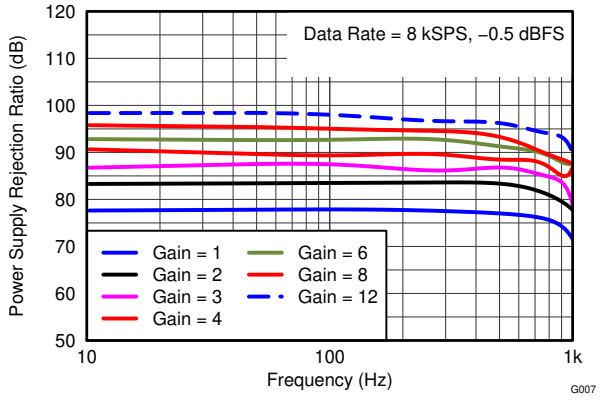


Figure 8. PSRR vs Frequency

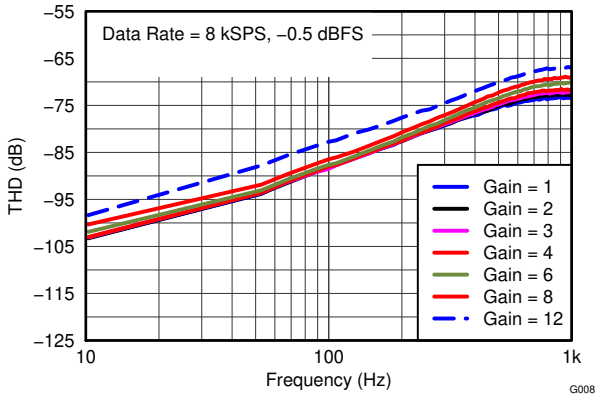


Figure 9. THD vs Frequency

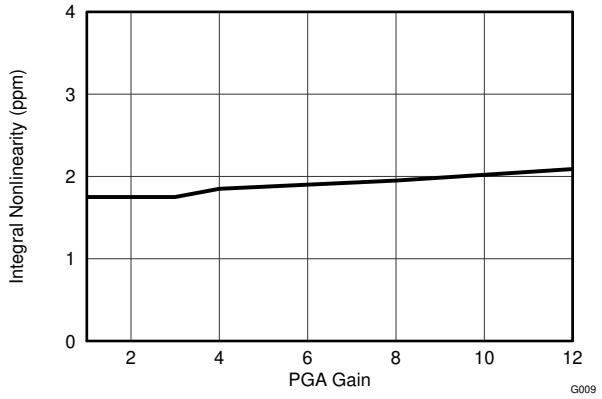


Figure 10. INL vs PGA Gain

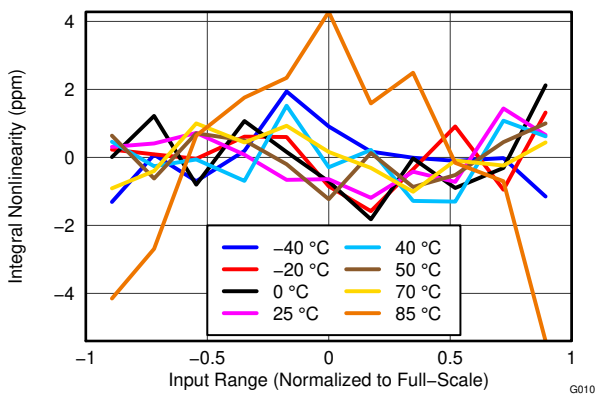


Figure 11. INL vs Temperature

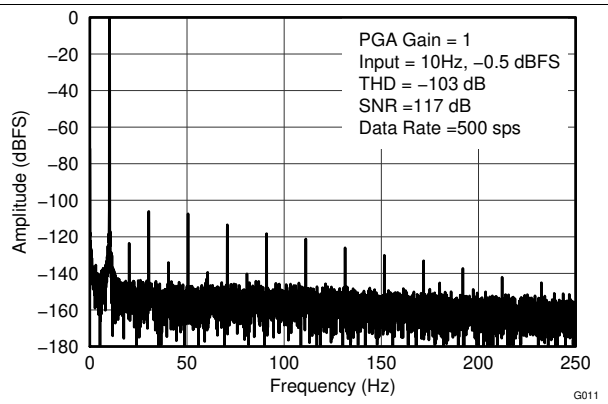


Figure 12. THD FFT Plot (60-Hz Signal)

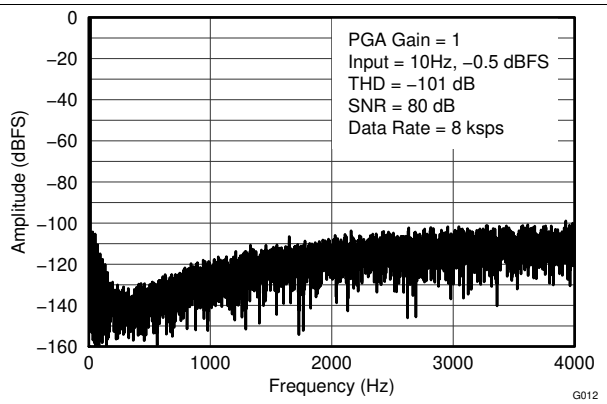


Figure 13. FFT Plot (60-Hz Signal)

Typical Characteristics (continued)

at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.42 V, VREFN = AVSS, external clock = 512 kHz, data rate = 500 SPS, C_{FILTER} = 4.7 nF, and gain = 6 (unless otherwise noted)

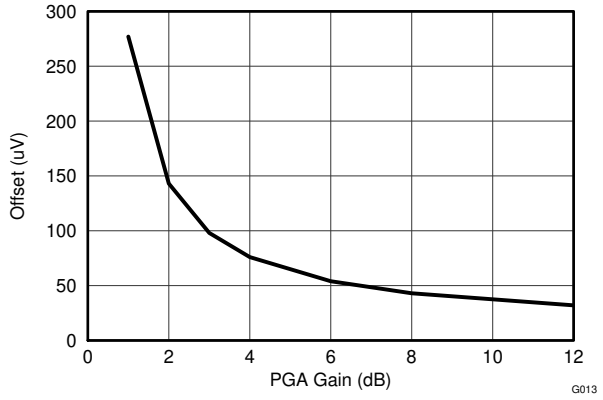


Figure 14. Offset vs PGA Gain (Absolute Value)

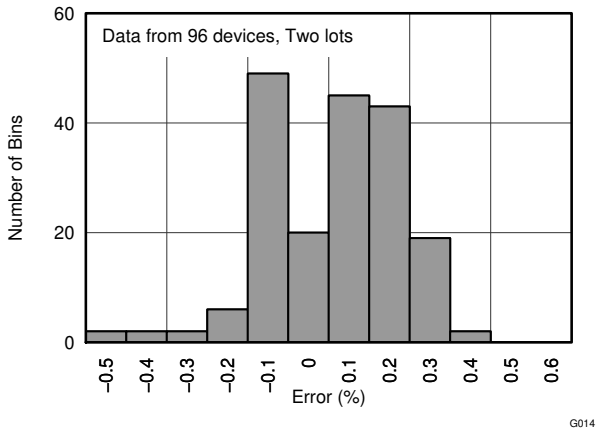


Figure 15. Test Signal Amplitude Accuracy

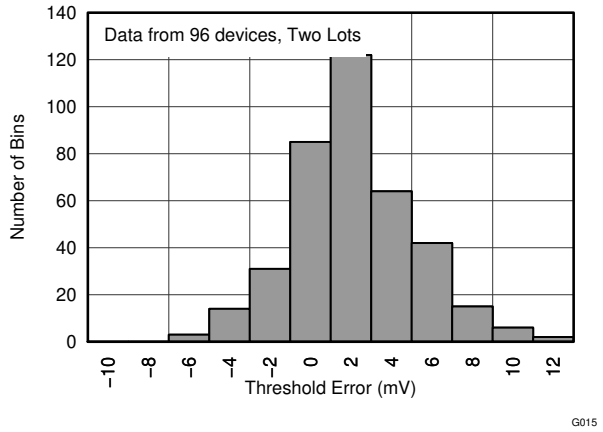


Figure 16. Lead-Off Comparator Threshold Accuracy

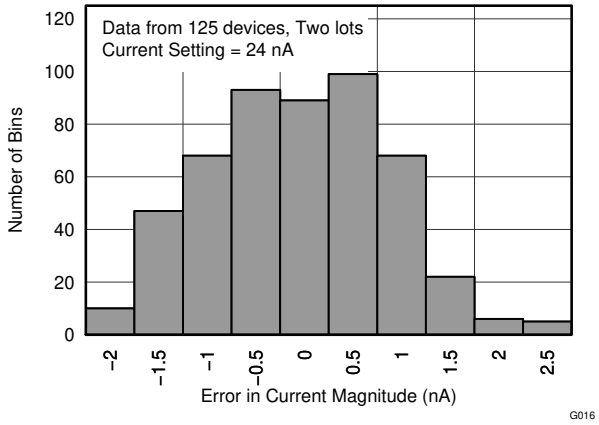


Figure 17. Lead-Off Current Source Accuracy Distribution

7 Parameter Measurement Information

7.1 Noise Measurements

The ADS1291, ADS1292, and ADS1292R noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the programmable gain amplifier (PGA) value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 1 through Table 8 summarize the ADS1291, ADS1292, and ADS1292R noise performance. The data are representative of typical noise performance at T_A = +25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. For the shown data rates, the ratio is approximately 6.6.

Table 1 through Table 8 show measurements taken with an internal reference. The data are also representative of the ADS1291, ADS1292, and ADS1292R noise performance when using a low-noise external reference such as the REF5025.

In Table 1 through Table 8, μV_{RMS} and μV_{PP} are measured values. Effective resolution (EFF RESOL) and dynamic range (DYN RANGE) are calculated with Equation 1 and Equation 2.

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \quad (1)$$

$$\text{Dynamic Range} = 20 \times \log_{10}\left|\frac{\text{VREF}}{\sqrt{2} \times V_{RMS\_Noise} \times \text{Gain}}\right| \quad (2)$$

Table 1. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3-V Analog Supply and 2.42-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 1					PGA GAIN = 2				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	1.5	10.3	121.0	18.83	20.10	0.8	5.6	120.0	18.71	19.94
001	250	65.5	2.2	14.4	117.8	18.34	19.58	1.2	7.5	117.1	18.29	19.46
010	500	131	3.0	18.9	115.1	17.95	19.11	1.7	10.9	113.9	17.75	18.91
011	1000	262	4.6	30.8	111.3	17.25	18.49	2.5	15.6	110.6	17.23	18.37
100	2000	524	10.1	99	104.5	15.57	17.36	5.3	48	104.0	15.60	17.28
101	4000	1048	55.2	563	89.7	13.06	14.91	26.0	265	90.3	13.14	15.00
110	8000	2096	287.3	2930	75.4	10.68	12.53	144.1	1470	75.4	10.67	12.52
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 2. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3-V Analog Supply and 2.42-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 3					PGA GAIN = 4				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.6	4.1	119.2	18.58	19.80	0.5	3.4	117.9	18.42	19.58
001	250	65.5	0.9	5.5	115.9	18.15	19.26	0.8	5.0	114.8	17.88	19.07
010	500	131	1.3	7.7	113.0	17.67	18.77	1.1	6.6	111.9	17.47	18.59
011	1000	262	1.9	12.0	109.5	17.02	18.19	1.6	10.3	108.7	16.83	18.06
100	2000	524	3.7	31	103.7	15.65	17.23	2.9	23	103.2	15.69	17.14
101	4000	1048	17.0	173	90.5	13.18	15.03	12.2	124	90.8	13.24	15.09
110	8000	2096	91.9	937	75.8	10.74	12.59	66.8	681	76.1	10.78	12.63
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 3. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3-V Analog Supply and 2.42-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 6					PGA GAIN = 8				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.5	3.0	115.9	18.04	19.26	0.4	2.6	114.0	17.82	18.94
001	250	65.5	0.7	4.1	112.8	17.58	18.73	0.6	3.9	111.0	17.22	18.44
010	500	131	0.9	5.6	109.9	17.14	18.25	0.8	5.5	108.0	16.75	17.93
011	1000	262	1.3	8.7	106.8	16.49	17.73	1.2	7.6	104.9	16.26	17.42
100	2000	524	2.2	16	102.1	15.64	16.96	2.0	14	100.7	15.36	16.72
101	4000	1048	7.5	77	91.5	13.34	15.19	5.5	56	91.7	13.39	15.24
110	8000	2096	42.7	436	76.4	10.84	12.69	31.3	319	76.6	10.88	12.73
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 4. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3-V Analog Supply and 2.42-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 12				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.4	2.5	111.3	17.31	18.48
001	250	65.5	0.5	3.5	108.4	16.81	18.01
010	500	131	0.8	5.0	105.0	16.29	17.44
011	1000	262	1.1	6.9	102.1	15.82	16.97
100	2000	524	1.7	11	98.6	15.21	16.38
101	4000	1048	3.5	36	92.0	13.44	15.29
110	8000	2096	20.1	205	76.9	10.93	12.78
111	NA	NA	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 5. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5-V Analog Supply and 4.033-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 1					PGA GAIN = 2				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	1.6	10.2	124.9	19.58	20.75	0.9	5.4	124.3	19.50	20.65
001	250	65.5	2.2	13.3	122.3	19.20	20.31	1.2	8.1	121.3	18.91	20.15
010	500	131	3.1	18.9	119.3	18.69	19.82	1.7	10.6	118.2	18.52	19.63
011	1000	262	4.9	31.9	115.2	17.94	19.14	2.7	17.9	114.4	17.77	19.00
100	2000	524	15.5	167	105.2	15.55	17.48	7.5	80	105.5	15.62	17.53
101	4000	1048	89.6	959	90.0	13.03	14.95	45.0	481	89.9	13.02	14.94
110	8000	2096	460.1	4923	75.8	10.67	12.59	229.0	2450	75.8	10.67	12.59
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 6. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5-V Analog Supply and 4.033-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 3					PGA GAIN = 4				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.6	4.2	123.4	19.28	20.50	0.5	3.6	122.3	19.08	20.32
001	250	65.5	0.9	5.7	120.7	18.82	20.04	0.7	4.8	119.5	18.66	19.86
010	500	131	1.3	8.4	117.3	18.27	19.49	1.1	7.4	116.2	18.04	19.31
011	1000	262	2.0	13.3	113.5	17.62	18.85	1.6	11.0	112.7	17.48	18.72
100	2000	524	5.1	53	105.3	15.61	17.49	3.9	38	105.2	15.67	17.47
101	4000	1048	28.7	307	90.3	13.08	15.00	20.7	222	90.6	13.14	15.06
110	8000	2096	149.3	1598	76.0	10.70	12.62	111.8	1196	76.0	10.71	12.63
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 7. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5-V Analog Supply and 4.033-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 6					PGA GAIN = 8				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB	μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.5	3.0	120.4	18.78	19.99	0.4	2.7	118.5	18.48	19.68
001	250	65.5	0.6	4.0	117.5	18.36	19.52	0.6	3.8	115.7	18.01	19.21
010	500	131	0.9	6.0	114.3	17.75	18.99	0.8	5.3	112.8	17.53	18.74
011	1000	262	1.4	8.8	110.8	17.20	18.41	1.2	8.1	109.5	16.92	18.19
100	2000	524	2.8	24	104.6	15.74	17.38	2.3	18	103.6	15.73	17.22
101	4000	1048	13.3	142	91.0	13.20	15.12	9.3	100	91.5	13.29	15.21
110	8000	2096	71.5	765	76.4	10.77	12.69	52.3	560	76.6	10.80	12.72
111	NA	NA	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 8. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5-V Analog Supply and 4.033-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 12				
			μV_{RMS}	μV_{PP}	DYN RANGE	EFF RESOL	ENOB
000	125	32.75	0.4	2.6	115.7	17.96	19.21
001	250	65.5	0.5	3.4	112.9	17.59	18.75
010	500	131	0.8	5.2	109.8	16.96	18.24
011	1000	262	1.1	6.9	106.6	16.56	17.70
100	2000	524	1.9	14	101.9	15.57	16.83
101	4000	1048	5.9	63	92.0	13.37	15.29
110	8000	2096	33.8	362	76.9	10.85	12.77
111	NA	NA	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

8 Detailed Description

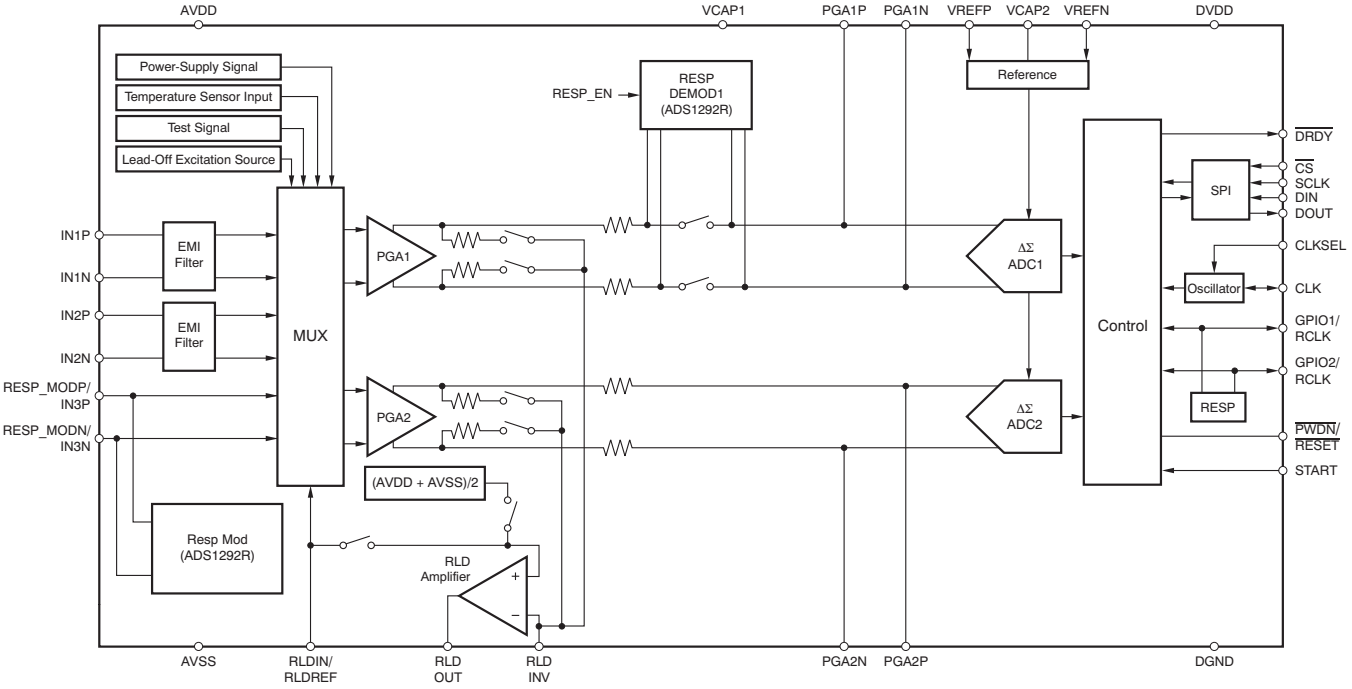
8.1 Overview

The ADS1291, ADS1292, and ADS1292R are low-power, multichannel, simultaneously-sampling, 24-bit delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGAs). These devices integrate various electrocardiogram (ECG)-specific functions that make them well-suited for scalable ECG, sports, and fitness applications. The devices can also be used in high-performance, multichannel data acquisition systems by powering down the ECG-specific circuitry.

The ADS1291, ADS1292, and ADS1292R have a highly programmable multiplexer that allows for temperature, supply, input short, and RLD measurements. Additionally, the multiplexer allows any of the input electrodes to be programmed as the patient reference drive. The PGA gain can be chosen from one of seven settings (1, 2, 3, 4, 6, 8, and 12). The ADCs in the device offer data rates from 125 SPS to 8 kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides two general-purpose I/O (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.42 V or 4.033 V. The internal oscillator generates a 512-kHz clock. The versatile right leg drive (RLD) block allows the user to choose the average of any combination of electrodes to generate the patient drive signal. Lead-off detection can be accomplished either by using an external pull-up or pull-down resistor or the device internal current source or sink. An internal ac lead-off detection feature is also available. Apart from the above features, the ADS1292R provides options for internal respiration circuitry. *Functional Block Diagram* shows a block diagram for the ADS1291, ADS1292, and ADS1292R.

8.2 Functional Block Diagram



8.3 Feature Description

This section contains details of the ADS1291, ADS1292, and ADS1292R internal functional elements. The analog blocks are discussed first followed by the digital interface. Blocks implementing ECG-specific functions are covered in the end.

Throughout this document, f_{CLK} denotes the signal frequency at the CLK pin, t_{CLK} denotes the signal period of the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the output data time period, and f_{MOD} denotes the frequency at which the modulator samples the input.

8.3.1 EMI Filter

An RC filter at the input acts as an electromagnetic interference (EMI) filter on channels 1 and 2. The –3-dB filter bandwidth is approximately 3 MHz.

8.3.2 Input Multiplexer

The ADS1291, ADS1292, and ADS1292R input multiplexers are very flexible and provide many configurable signal-switching options. Figure 18 shows the multiplexer for the ADS1291, ADS1292, and ADS1292R. Note that TESTP, TESTM, and RLDIN/RLDREF are common to both channels. INP and INN are separate for each of the three pins. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CH1SET or CH2SET register (see the *CH1SET* and *CH2SET* Registers in the *Register Maps* section for details). More details of the ECG-specific features of the multiplexer are discussed in the *Input Multiplexer* subsection of the *ECG-Specifc Functions*.

8.3.2.1 Device Noise Measurements

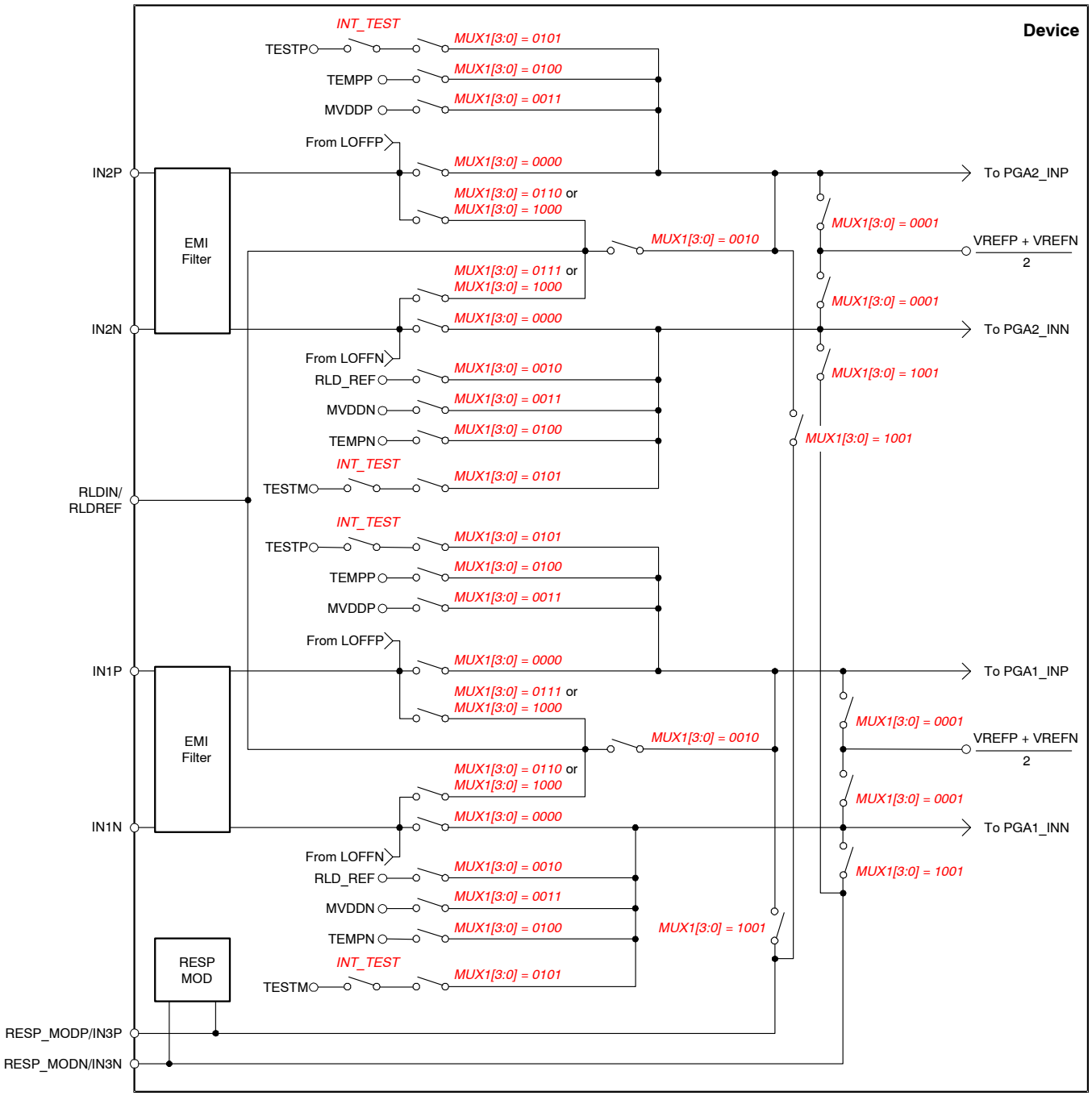
Setting CHnSET[3:0] = 0001 sets the common-mode voltage of (VREFP + VREFN) / 2 to both inputs of the channel. This setting can be used to test the inherent noise of the device in the user system.

8.3.2.2 Test Signals (TestP and TestN)

Setting CHnSET[3:0] = 0101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the entire signal chain to be tested out. Although the test signals are similar to the CAL signals described in the IEC60601-2-51 specification, this feature is not intended for use in compliance testing.

Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Maps* section for details). INT_TEST enables the test signal and TEST_FREQ controls switching at the required frequency.

Feature Description (continued)



NOTE: MVDD monitor voltage supply depends on channel number; see the *Supply Measurements (MVDDP, MVDDN)* section.

Figure 18. Input Multiplexer Block for Both Channels

Feature Description (continued)

8.3.2.3 Auxiliary Differential Input (RESP_MODN/IN3N, RESP_MODN/IN3P)

In applications where the respiration modulator output is not used, the RESP_MODN/IN3N and RESP_MODN/IN3P signals can be used as a third multiplexed differential input channel. These inputs can be multiplexed to either of the ADC channels.

8.3.2.4 Temperature Sensor (TEMPP, TEMPN)

The ADS1291, ADS1292, and ADS1292R contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 19. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

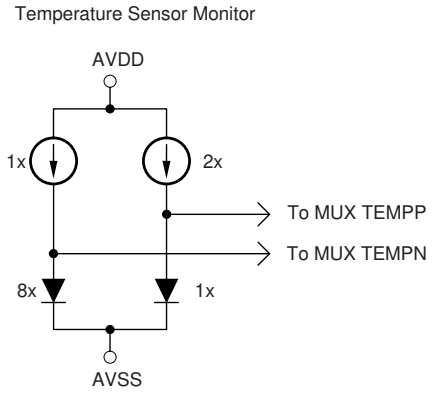


Figure 19. Temperature Sensor Measurement in the Input

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADS1291, ADS1292, and ADS1292R causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 3 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to μV.

$$\text{Temperature (°C)} = \left(\frac{\text{Temperature Reading (μV)} - 145{,}300\ \mu\text{V}}{490\ \mu\text{V/°C}} \right) + 25°\text{C} \quad (3)$$

8.3.2.5 Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[3:0] = 0011 sets the channel inputs to different supply voltages of the device. For channel 1 (MVDDP – MVDDN) is [0.5(AVDD + AVSS)]; for channel 2 (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

8.3.2.6 Lead-Off Excitation Signals (LoffP, LoffN)

The lead-off excitation signals are fed into the multiplexer before the switches. The comparators that detect the lead-off condition are also connected to the multiplexer block before the switches. For a detailed description of the lead-off block, refer to the *Lead-Off Detection* subsection in the *ECG-Specific Functions* section.

8.3.2.7 Auxiliary Single-Ended Input

The RLDIN/RLDREF pin is primarily used for routing the right leg drive signal to any of the electrodes in case the right leg drive electrode falls off. However, the RLDIN/RLDREF pin can be used as a multiple single-ended input channel. The signal at the RLDIN/RLDREF pin can be measured with respect to the midsupply [(AVDD + AVSS) / 2]. This measurement is done by setting the channel multiplexer setting MUXn[3:0] to '0010' in the CH1SET and CH2SET registers.

Feature Description (continued)

8.3.3 Analog Input

The ADS1291, ADS1292, and ADS1292R analog input is fully differential. Assuming PGA = 1, the differential input (INP – INN) can span between $–V_{REF}$ to $+V_{REF}$. Note that the absolute range for INP and INN must be between AVSS – 0.3 V and AVDD + 0.3 V. Refer to Table 10 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the ADS1291, ADS1292, and ADS1292R analog input: single-ended or differential, as shown in Figure 20 and Figure 21. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2 V_{REF}) and (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by (INP + INN) / 2. Both INP and INN inputs swing from (common-mode + 1/2 V_{REF} to common-mode – 1/2 V_{REF}). For optimal performance, it is recommended that the ADS1291, ADS1292, and ADS1292R be used in a differential configuration.

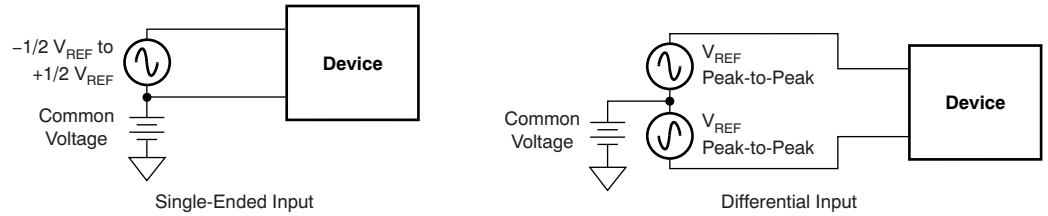


Figure 20. Methods of Driving the ADS1291, ADS1292, and ADS1292R: Single-Ended or Differential

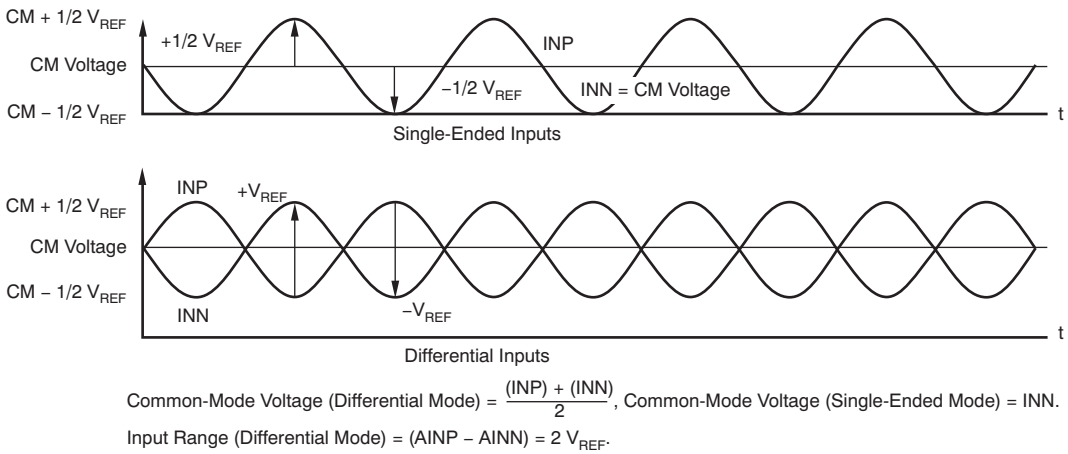


Figure 21. Using the ADS1291, ADS1292, and ADS1292R in Single-Ended and Differential Input Modes

8.3.4 PGA Settings and Input Range

The PGA is a differential input or differential output amplifier, as shown in Figure 22. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that can be set by writing to the CHnSET register (see the *CH1SET* and *CH2SET* Registers in the *Register Map* section for details). The ADS1291, ADS1292, and ADS1292R have CMOS inputs and hence have negligible current noise.

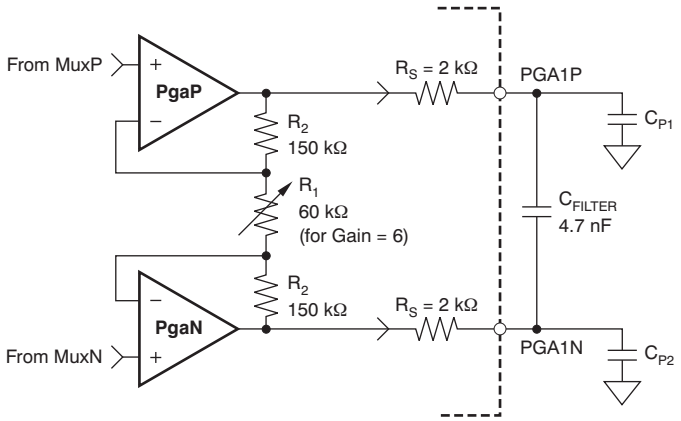


Figure 22. PGA Implementation

The PGA resistor string that implements the gain has 360 kΩ of resistance for a gain of 6. This resistance provides a current path across the outputs of the PGA in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input. The PGA output is filtered by an RC filter before it goes to the ADC. The filter is formed by an internal resistor R_S = 2 kΩ and an external capacitor C_{FILTER} (4.7 nF, typical). This filter acts as an anti-aliasing filter with the –3-dB bandwidth of 8.4 kHz. The internal R_S resistor is accurate to 15% so actual bandwidth will vary. This RC filter also suppresses the glitch at the PGA output caused by ADC sampling. The minimum value of C_{EXT} that can be used is 4 nF. A larger value C_{FILTER} capacitor can be used for increased attenuation at higher frequencies for anti-aliasing purposes. If channel 1 of the ADS1292R is used for respiration measurement, then a 4.7-nF external capacitor is recommended. The tradeoff is that a larger capacitor value gives degraded THD performance. See Figure 23 for a diagram explaining the THD versus C_{FILTER} value for a 10-Hz input signal.

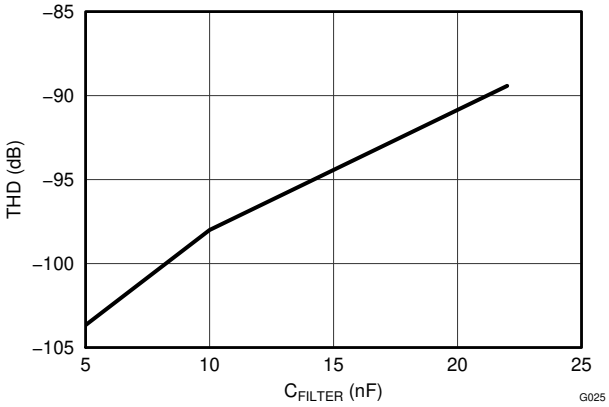


Figure 23. THD versus C_{FILTER} Value

Special care must be taken in PCB layout to minimize the parasitic capacitance C_{P1} / C_{P2}. The absolute value of these capacitances must be less than 20 pF. Ideally, C_{FILTER} should be placed right at the pins to minimize these capacitors. Mismatch between these capacitors will lead to CMRR degradation. Assuming everything else is perfectly matched, the 60-Hz CMRR as a function of this mismatch is given by Equation 4.

$$\text{CMRR} = 20\log \frac{\text{Gain}}{2\pi \times 2e3 \times \Delta C_P \times 60} \tag{4}$$

where $\Delta C_P = C_{P1} - C_{P2}$

For example, a mismatch of 20 pF with a gain of 6 limits the CMRR to 112 dB. If ΔC_P is small, then the CMRR is limited by the PGA itself and is as specified in the Electrical Characteristics table. The PGA are chopped internally at either 8, 32, or 64 kSPS, as determined by the CHOP bits (see the *RLD_SENS: Right Leg Drive Sense Selection* register, bits[7:6]). The digital decimation filter filters out the chopping ripple in the normal path so the chopping ripple is not a concern. If PGA output is used for hardware PACE detection, the chopping ripple must be filtered. First-order filtering is provided by the RC filter at the PGA output. Additional filtering may be needed to suppress the chopping ripple. If the PGA output is routed to other circuitry, a 20-kΩ series resistance must be added in the path near the C_{FILTER} capacitor. The routing should be matched to maintain the CMRR performance.

8.3.4.1 Input Common-Mode Range

The usable input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. Equation 5 describes this range.

$$\text{AVDD} - 0.2\ \text{V} - \left(\frac{\text{Gain} \times V_{MAX\_DIFF}}{2}\right) > \text{CM} > \text{AVSS} + 0.2\ \text{V} + \left(\frac{\text{Gain} \times V_{MAX\_DIFF}}{2}\right)$$

where:

V_{MAX_DIFF} = maximum differential signal at the input of the PGA

CM = common-mode range (5)

For example:

If V_{DD} = 3 V, gain = 6, and V_{MAX_DIFF} = 350 mV
Then 1.25 V < CM < 1.75 V

8.3.4.2 Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. Equation 6 shows this range.

$$\text{Max (INP – INN)} < \frac{V_{REF}}{\text{Gain}}\ ; \qquad \text{Full-Scale Range} = \frac{\pm V_{REF}}{\text{Gain}} = \frac{2\ V_{REF}}{\text{Gain}} \tag{6}$$

The 3-V supply, with a reference of 2.42 V and a gain of 6 for ECGs, is optimized for power with a differential input signal of approximately 300 mV. For higher dynamic range, a 5-V supply with a reference of 4.033 V (set by the VREF_4V bit of the CONFIG2 register) can be used to increase the differential dynamic range.

8.3.4.3 ADC ΔΣ Modulator

Each channel of the ADS1291, ADS1292, and ADS1292R has a 24-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of f_{MOD} = f_{CLK} / 4 or f_{CLK} / 16, as determined by the CLK_DIV bit. In both cases, the sampling clock has a typical value of 128 kHz. As in the case of any ΔΣ modulator, the ADS1291, ADS1292, and ADS1292R noise is shaped until f_{MOD} / 2, as shown in Figure 24. The on-chip digital decimation filters explained in the *Digital Decimation Filter* section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This feature of the ΔΣ converters drastically reduces the complexity of analog antialiasing filters that are typically needed with nyquist ADCs.

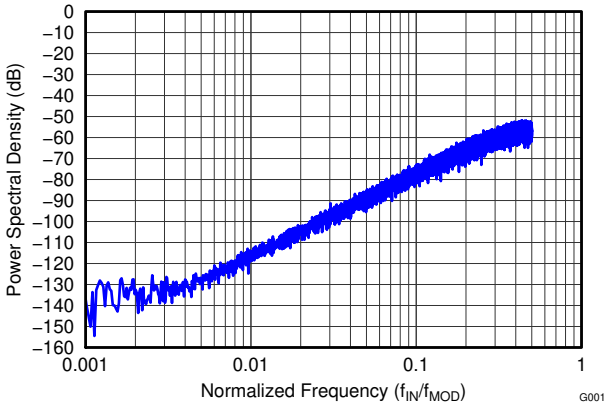


Figure 24. Power Spectral Density (PSD) of a ΔΣ Modulator (4-Bit Quantizer)

8.3.5 Digital Decimation Filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in ECG applications for implement software pace detection and ac lead-off detection.

The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters can be adjusted by the DR bits in the CONFIG1 register (see the *Register Map* section for details). This setting is a global setting that affects all channels and, therefore, in a device all channels operate at the same data rate.

8.3.5.1 Sinc Filter Stage (sinx / x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 7 shows the scaled Z-domain transfer function of the sinc filter.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^3 \tag{7}$$

The frequency domain transfer function of the sinc filter is shown in Equation 8.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3$$

where:

N = decimation ratio (8)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 25 shows the sinc filter frequency response and Figure 26 shows the sinc filter roll-off. With a step change at input, the filter takes 3 t_{DR} to settle. After a START signal rising edge, the filter takes t_{SETTLE} time to give the first data output. The filter settling times at various data rates are discussed in the *START* subsection of the *SPI Interface* section. Figure 27 and Figure 28 show the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 29 shows the transfer function extended until 4 f_{MOD}. It can be seen that the ADS1291, ADS1292, and ADS1292R passband repeats itself at every f_{MOD}. The input R-C anti-aliasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

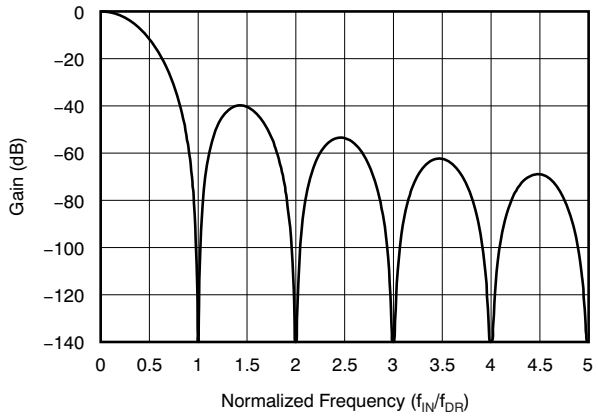


Figure 25. Sinc Filter Frequency Response

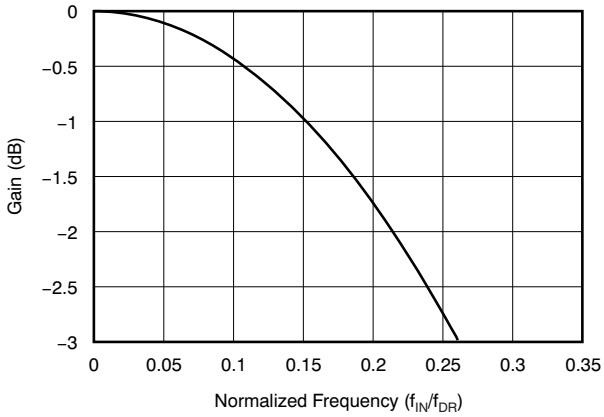


Figure 26. Sinc Filter Roll-Off

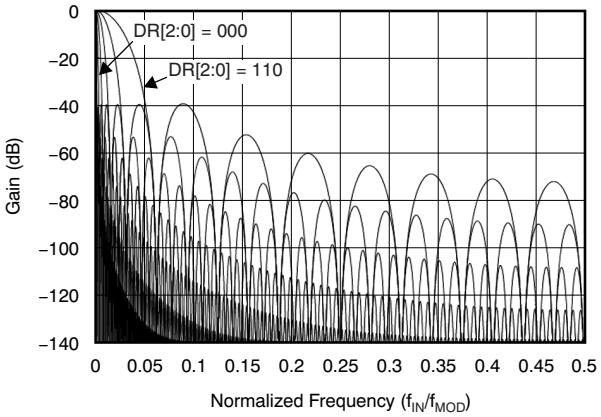


Figure 27. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 2

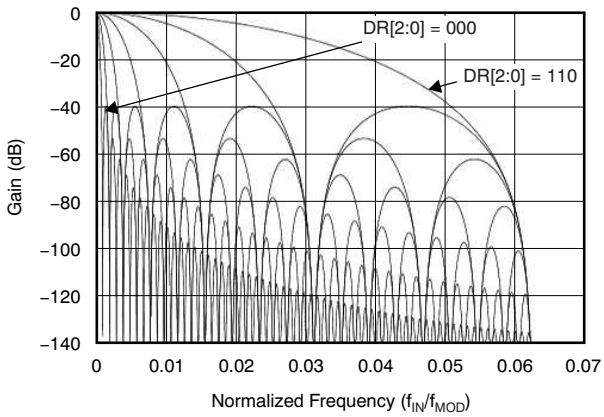


Figure 28. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 16

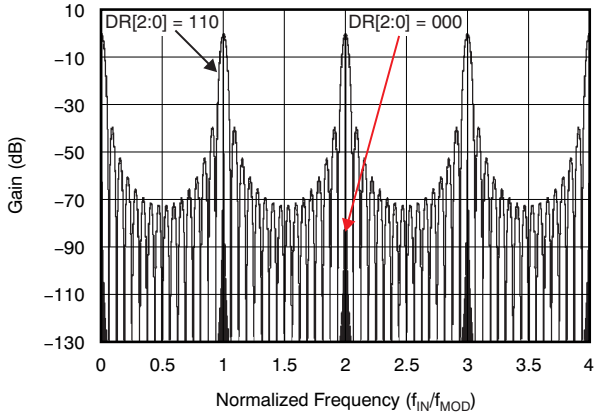
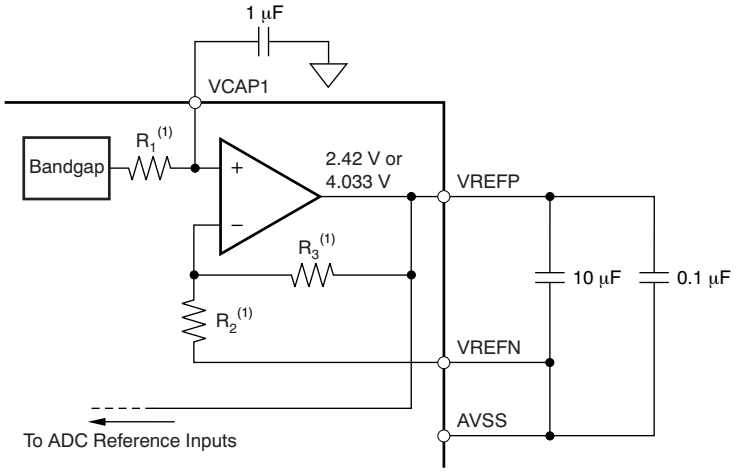


Figure 29. Transfer Function of On-Chip Decimation Filters Until 4f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

8.3.6 Reference

Figure 30 shows a simplified block diagram of the ADS1291, ADS1292, and ADS1292R internal reference. The reference voltage is generated with respect to AVSS. The VREFN pin must always be connected to AVSS.



(1) For V_{REF} = 2.42 V: R_1 = 100 kΩ, R_2 = 200 kΩ, and R_3 = 200 kΩ. For V_{REF} = 4.033 V: R_1 = 84 kΩ, R_2 = 120 kΩ, and R_3 = 280 kΩ.

Figure 30. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end ECG systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz so that the reference noise does not dominate the system noise. When using a 3-V analog supply, the internal reference must be set to 2.42 V. In case of a 5-V analog supply, the internal reference can be set to 4.033 V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 31 shows a typical external reference drive circuitry. Power-down is controlled by the PD_REFBUF bit in the CONFIG2 register. This power-down is also used to share internal references when two devices are cascaded. By default the device wakes up in external reference mode.

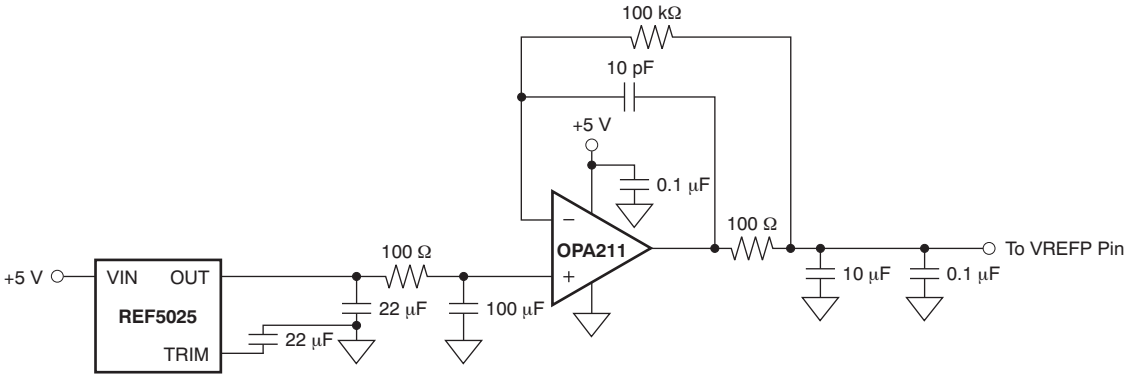


Figure 31. External Reference Driver

8.3.7 Clock

The ADS1291, ADS1292, and ADS1292R provide two different methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Over the specified temperature range the accuracy varies; see the Electrical Characteristics. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG2 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 9. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock be shut down to save power.

Table 9. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG2.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

The ADS1291, ADS1292, and ADS1292R have the option to choose between two different external clock frequencies (512 kHz or 2.048 MHz). This frequency is selected by setting the CLK_DIV bit (bit 6) in the LOFF_STAT register. The modulator must be clocked at 128 kHz, regardless of the external clock frequency. Figure 32 shows the relationship between the external clock (f_{CLK}) and the modulator clock (f_{MOD}). The default mode of operation is f_{CLK} = 512 kHz. The higher frequency option has been provided to allow the SPI to run at a higher speed. SCLK can be only twice the speed of f_{CLK} during a register read or write, see section on sending multi-byte commands. Having the 2.048 MHz option allows for register read and writes to be performed at SCLK speeds up to 4.096 MHz.

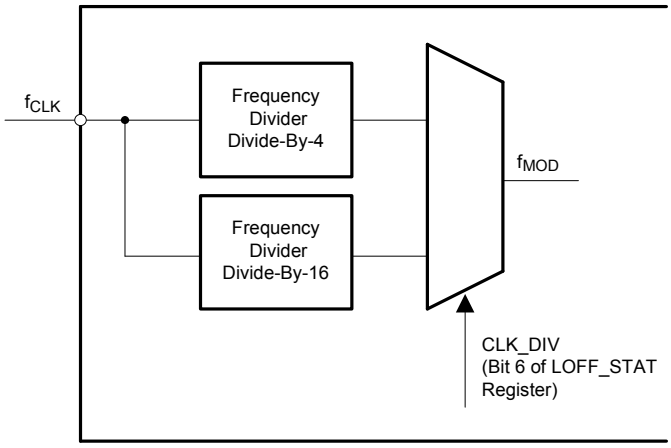


Figure 32. Relationship Between External Clock (f_{CLK}) and Modulator Clock (f_{MOD})

8.3.8 Data Format

The ADS1291, ADS1292, and ADS1292R outputs 24 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of V_{REF} / (2^{23} – 1). A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 10 summarizes ideal output codes for different input signals. All 24 bits toggle when the analog input is at positive or negative full-scale.

Table 10. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V_{REF}	7FFFFFh
+V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / 2^{23} – 1)	800000h

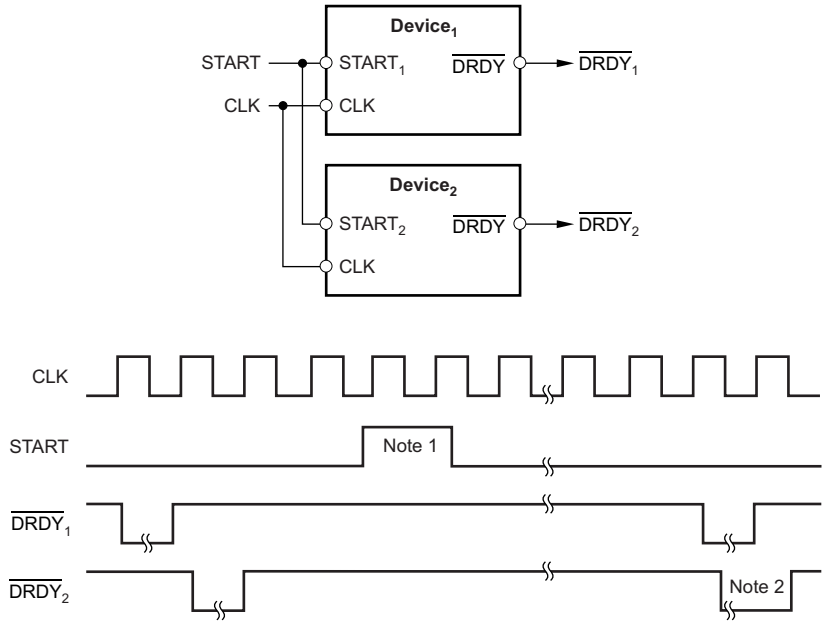
(1) Excludes effects of noise, linearity, offset, and gain error.

8.3.9 Multiple Device Configuration

The ADS1291, ADS1292, and ADS1292R are designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface *n* devices is 3 + *n*.

The right leg drive amplifiers can be daisy-chained as explained in the *RLD Configuration with Multiple Devices* subsection of the *ECG-Specific Functions* section. To use the internal oscillator in a daisy-chain configuration, one of the devices must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to '1'. This master device clock is used as the external clock source for the other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{DRDY}$ signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on the settling times). Figure 33 shows the behavior of two devices when synchronized with the START signal.



(1) Start pulse must be at least one t_{MOD} cycle wide.

(2) Settling time number uncertainty is one t_{MOD} cycle.

Figure 33. Synchronizing Multiple Converters

8.3.9.1 Standard Mode

Figure 34 shows a configuration with two devices cascaded together. One of the devices is an ADS1292R (two-channel with RESP) and the other is an ADS1292 (two-channel). Together, they create a system with four channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus.

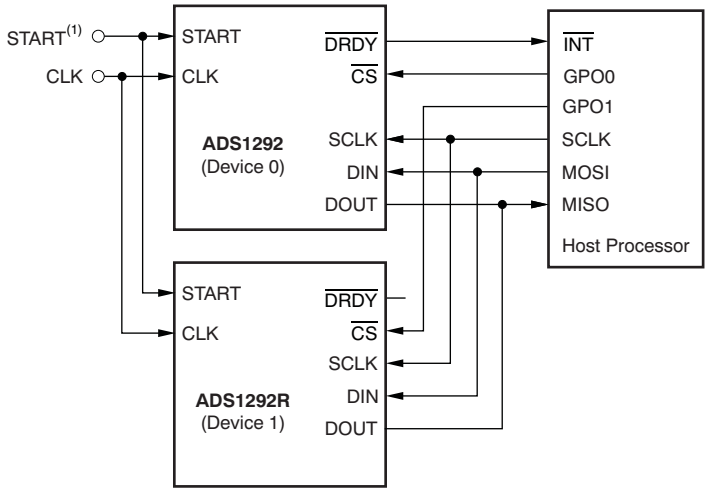
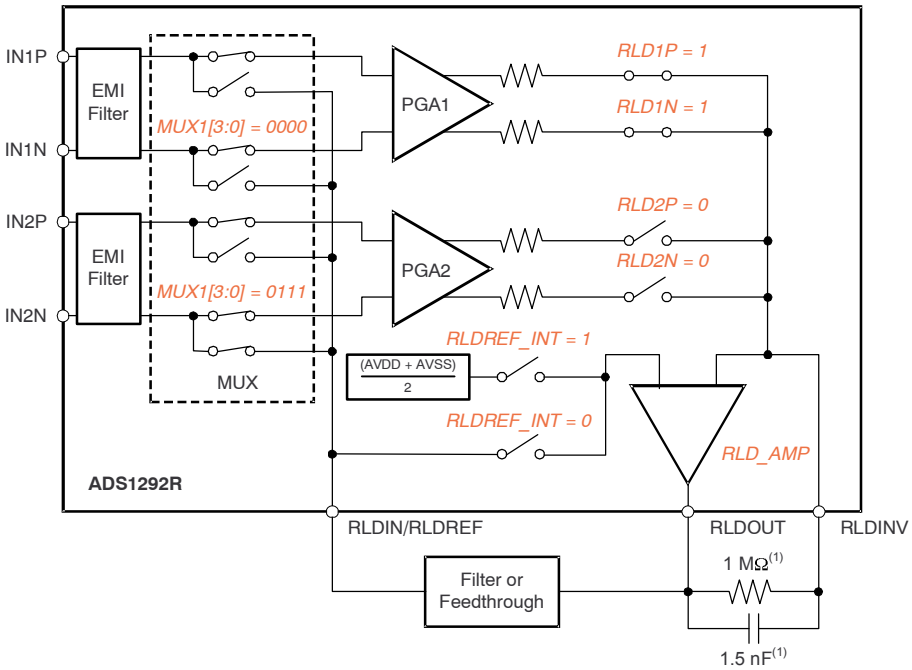


Figure 34. Multiple Device Configurations

8.3.10 ECG-Specific Functions

8.3.10.1 Input Multiplexer (Rerouting the Right Leg Drive Signal)

The input multiplexer has ECG-specific functions for the right leg drive signal. The RLD signal is available at the RLDOUT pin once the appropriate channels are selected for RLD derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can be fed after filtering or fed directly into the RLDIN pin, as shown in Figure 35. This RLDIN signal can be multiplexed into any one of the input electrodes by setting the MUX bits of the appropriate channel set registers to '0110' for P-side or '0111' for N-side. Figure 35 shows the RLD signal generated from channel 1 and routed to the N-side of channel 2. This feature can be used to dynamically change the electrode that is used as the reference signal to drive the patient body. Note that the corresponding channel cannot be used and can be powered down.

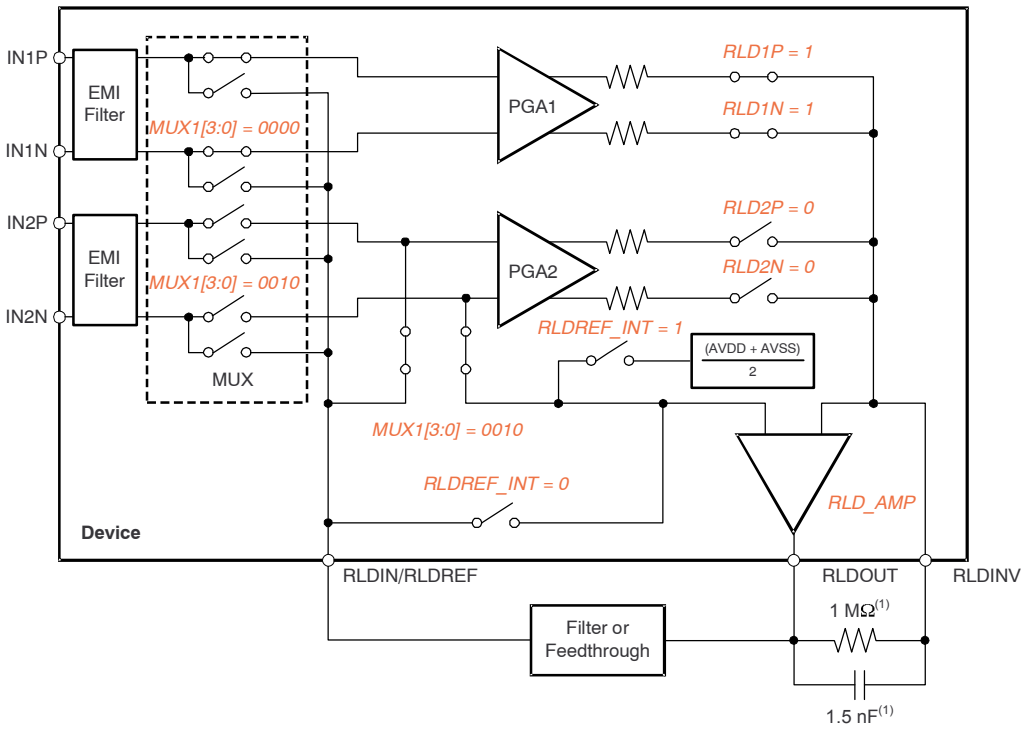


(1) Typical values for example only.

Figure 35. Example RLDOUT Signal Configured to be Routed to IN2N

8.3.10.1.1 Input Multiplexer (Measuring the Right Leg Drive Signal)

The RLDOUT signal can also be routed to a channel (that is not used for the calculation of RLD) for measurement. Figure 36 shows the register settings to route the RLDIN signal to channel 2. The measurement is done with respect to the voltage (AVDD + AVSS) / 2. This feature is useful for debugging purposes during product development.



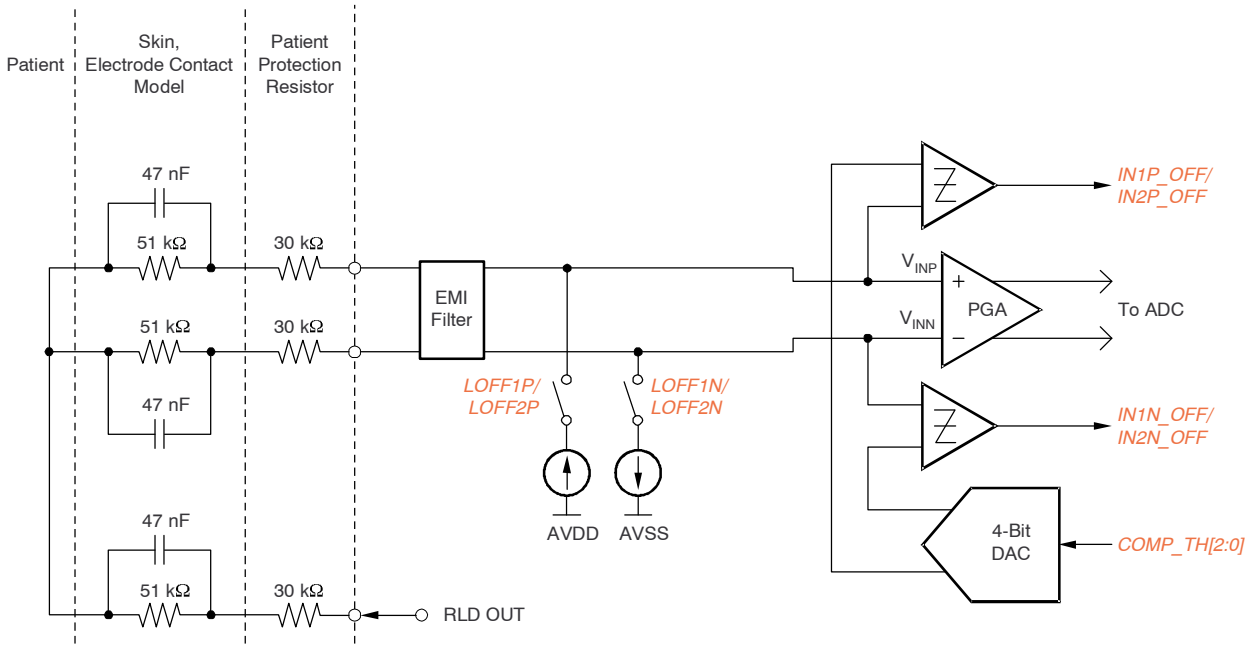
(1) Typical values for example only.

Figure 36. RLDOUT Signal Configured to be Read Back by Channel 2

8.3.10.2 Lead-Off Detection

Patient electrode impedances are known to decay over time. It is necessary to continuously monitor these electrode connections to verify a suitable connection is present. The ADS1291, ADS1292, and ADS1292R lead-off detection functional block provides significant flexibility to the user to choose from various lead-off detection strategies. Though called lead-off detection, this is in fact an *electrode-off* detection.

The basic principle is to inject an excitation signal and measure the response to find out if the electrode is off. As shown in the lead-off detection functional block diagram in Figure 37, this circuit provides two different methods of determining the state of the patient electrode. The methods differ in the frequency content of the excitation signal. Lead-off can be selectively done on a per channel basis using the LOFF_SENS register. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification the latest revision of IEC 60601).

Figure 37. Lead-Off Detection

8.3.10.2.1 DC Lead-Off

In this method, the lead-off excitation is with a dc signal. The dc excitation signal can be chosen from either an external pull-up or pull-down resistor or a current source or sink, as shown in Figure 38. One side of the channel is pulled to supply and the other side is pulled to ground. The internal current source and current sink can be swapped by setting the FLIP1 and FLIP2 bits in the LOFF_SENS register. In case of current source or sink, the magnitude of the current can be set by using the ILEAD_OFF[1:0] bits in the LOFF register. The current source or sink gives larger input impedance compared to the 10-MΩ pull-up or pull-down resistor.

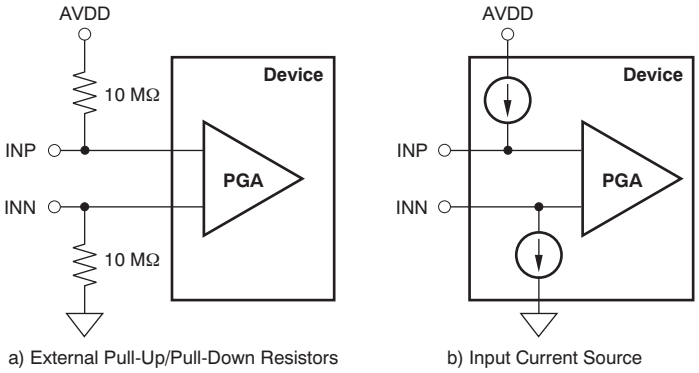


Figure 38. DC Lead-Off Excitation Options

Sensing of the response can be done either by looking at the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either of the electrodes is off, the pull-up resistors and the pull-down resistors saturate the channel. By looking at the output code it can be determined that either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 4-bit digital-to-analog converter (DAC) whose levels are set by the COMP_TH[2:0] bits in the LOFF register. The output of the comparators are stored in the LOFF_STAT register. These two registers are available as a part of the output data stream. (See the *Data Output Protocol (DOUT)* subsection of the *SPI Interface* section.) If dc lead-off is not used, the lead-off comparators can be powered down by setting the PD_LOFF_COMP bit in the CONFIG2 register.

An example procedure to turn on dc lead-off is given in the *Lead-Off* section.

8.3.10.2.2 AC Lead-Off

In this method, an out-of-band ac signal is used for excitation. The ac signal is generated by alternatively providing an internal current source and current sink at the input with a fixed frequency. The excitation frequency is a function of the output data rate and is f_{DR} / 4. This out-of-band excitation signal is passed through the channel and measured at the output.

Sensing of the ac signal is done by passing the signal through the channel to digitize it and measure at the output. The ac excitation signals are introduced at a frequency that is above the band of interest, generating an out-of-band differential signal that can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the lead-off status can be calculated. Therefore, the ac lead-off detection can be accomplished simultaneously with the ECG signal acquisition.

8.3.10.2.3 RLD Lead-Off

The ADS1291, ADS1292, and ADS1292R provide two modes for determining whether the RLD is correctly connected:

- RLD lead-off detection during normal operation
- RLD lead-off detection during power-up

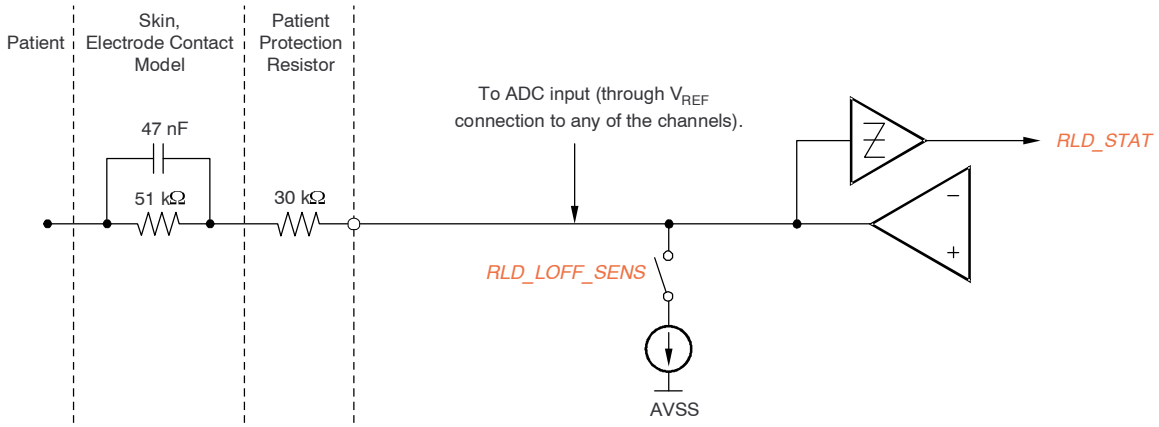
The following sections provide details of the two modes of operation.

RLD Lead-Off Detection During Normal Operation

During normal operation, the ADS1291, ADS1292, and ADS1292R RLD lead-off at power-up function cannot be used because it is necessary to power off the RLD amplifier.

RLD Lead-Off Detection At Power-Up

This feature is included in the ADS1291, ADS1292, and ADS1292R for use in determining whether the right leg electrode is suitably connected. At power-up, the ADS1291, ADS1292, and ADS1292R provides a procedure to determine the RLD electrode connection status using a current sink, as shown in Figure 39. The reference level of the comparator is set to determine the acceptable RLD impedance threshold.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification the latest revision of IEC 60601).

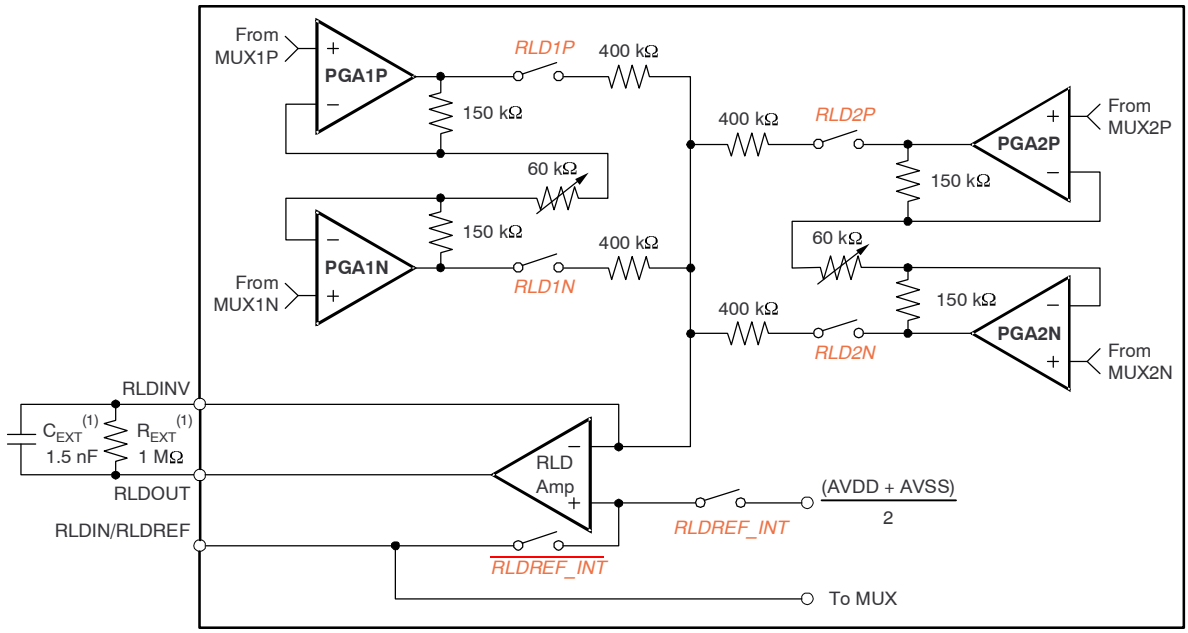
Figure 39. RLD Lead-Off Detection at Power-Up

When the RLD amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the RLD amplifier. The comparator thresholds are set by the same LOFF[7:5] bits used to set the thresholds for other negative inputs.

8.3.10.2.4 Right Leg Drive (RLD DC Bias Circuit)

The right leg drive (RLD) circuitry is used as a means to counter the common-mode interference in a ECG system as a result of power lines and other sources, including fluorescent lights. The RLD circuit senses the common-mode of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADS1291, ADS1292, and ADS1292R integrates the muxes to select the channel and an operational amplifier. All the amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit shown in Figure 40 shows the overall functional connectivity for the RLD bias circuit.

The reference voltage for the right leg drive can be chosen to be internally generated (AVDD + AVSS) / 2 or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the RLD loop is defined by writing the appropriate value to the RLDREF_INT bit in the RESP2 register.



(1) Typical values.

Figure 40. RLD Channel Selection

If the RLD function is not used, the amplifier can be powered down using the PDB_RLD bit. This bit is also used in daisy-chain mode to power-down all but one of the RLD amplifiers.

The functionality of the RLDIN pin is explained in the *Input Multiplexer* section.

8.3.10.2.4.1 RLD Configuration With Multiple Devices

Figure 41 shows multiple devices connected to an RLD.

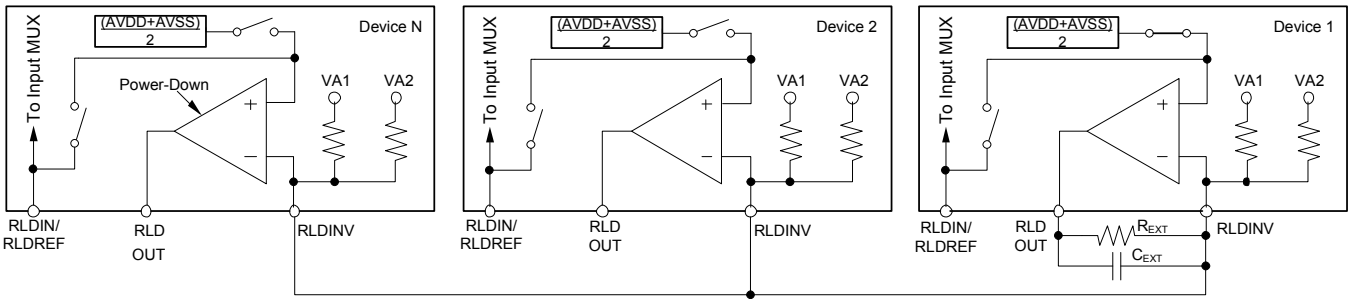


Figure 41. RLD Connection for Multiple Devices

8.3.10.3 PACE Detect

The ADS1291 and ADS1292 provide flexibility for PACE detection by using an external hardware. The external hardware approach is made possible by bringing out the output of the PGA at pins: PGA1P, PGA1N and PGA2P, PGA2N.

External hardware circuitry can be used to detect the presence of the pulse. The output of the PACE detection logic can then be fed into the device through one of the GPIO pins. The GPIO data are transmitted through the SPI port and loaded 2 t_{CLK}s before $\overline{DRDY}$ goes low.

When in pace detection mode, the chopping ripple can interfere with pace detect in hardware. It is therefore preffered to chop thee PGA at a higher frequency (32 kHz or 64 kHz). The RC filter at the PGA output, suppresses this ripple to a reasonable level. Additionally, suppression can be obtained with an additional RC stage. The trade-off with chopping the PGA at a higher frequency is an increase in the input bias current. Figure 6 shows bias current versus input voltage for three different chop frequencies.

8.3.10.4 Respiration

The ADS1292R provides two options for respiration: internal respiration with external clock and internal respiration with internal clock, as shown in Table 11.

Table 11. Respiration Control

RESP_CTRL	DESCRIPTION
0	Internal respiration with internal clock
1	Internal respiration with external clock

8.3.10.4.1 Internal Respiration Circuitry With Internal Clock (ADS1292R)

This mode is set by RESP_CTRL = 0. Figure 42 shows a block diagram of the internal respiration circuitry. The internal modulation and demodulator circuitry can be selectively used. The modulation block is controlled by the RESP_MOD_EN bit and the demodulation block is controlled by the RESP_DEMOD_EN bit. The modulation signal is a square wave of the magnitude VREFP – AVSS. When the internal modulation circuitry is used, the output of the modulation circuitry is available at the RESP_MODP and RESP_MODM pins of the device. This availability allows custom filtering to be added to the square wave modulation signal. In this mode, GPIO1 and GPIO2 can be used for other purposes. The modulation frequency of the respiration circuit is set by the RESP_FREQ bits.

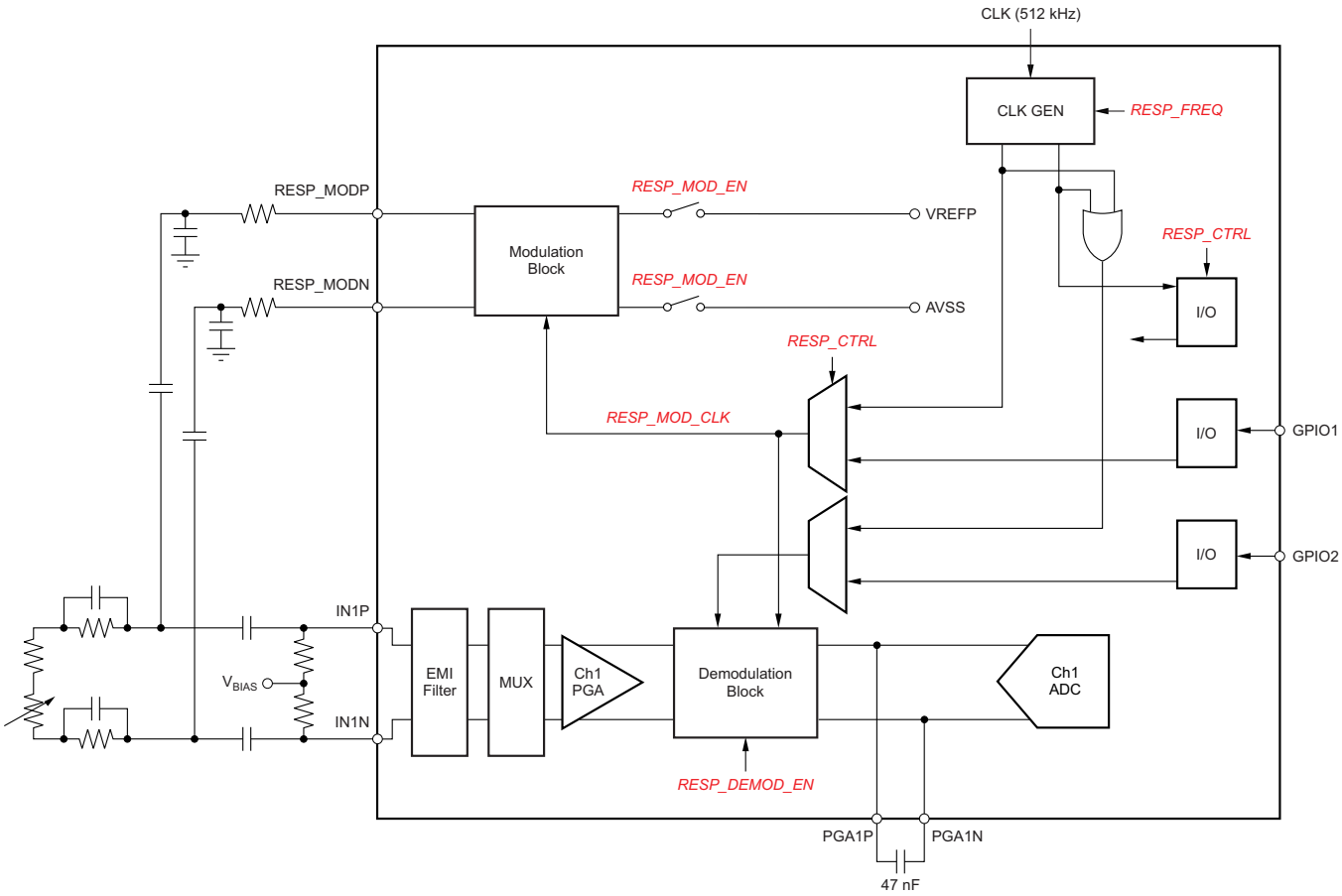


Figure 42. Internal Respiration Timing Diagram

8.3.10.4.2 Internal Respiration Circuitry With External Clock (ADS1292R)

This mode is set by RESP_CTRL = 1. In this mode GPIO1 and GPIO2 are automatically configured as inputs. GPIO1 and GPIO2 cannot be used for other purposes. The signals must be provided as described in Figure 43. An external, synchronous master clock (CLK) is required for this mode in order to operate.

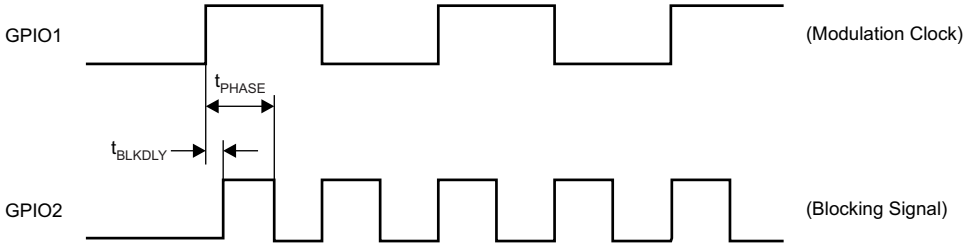


Figure 43. Internal Respiration (RESP_CTRL = 1) Timing Diagram

Table 12. Timing Characteristics for Figure 43(1)

PARAMETER		1.65 V ≤ DVDD ≤ 3.6 V			UNIT
		MIN	TYP	MAX	
t_{PHASE}	Respiration phase delay	0		168.75	Degrees
t_{BLKDLY}	Modulation clock rising edge to XOR signal		0	5	ns

(1) Specifications apply from –40°C to +85°C.

8.3.11 Setting the Device for Basic Data Capture

This section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user's system. It is recommended that this procedure be followed initially to get familiar with the device settings. Once this procedure has been verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. Also, some sample programming codes are added for the ECG-specific functions. Figure 44 details a flow chart of the configuration procedure.

8.3.11.1 Lead-Off

Sample code to set dc lead-off with current source or sink resistors on all channels

WREG LOFF 10h // Comparator threshold at 95% and 5%, current source or sink resistor // DC lead-off

WREG CONFIG2 E0h // Turn-on dc lead-off comparators

WREG LOFF_SENS 0Fh // Turn on both P- and N-side of all channels for lead-off sensing

Observe the status bits of the output data stream to monitor lead-off status.

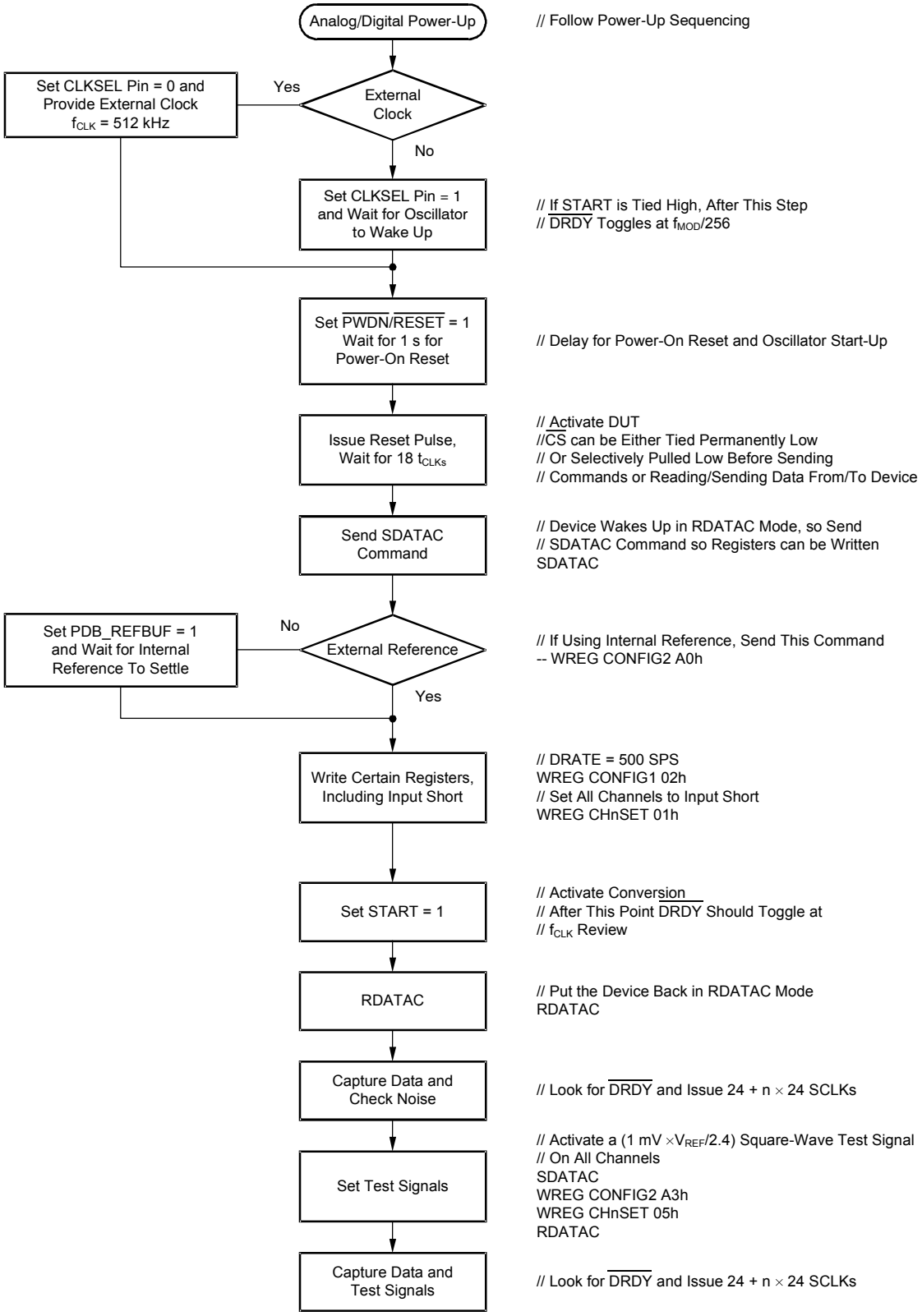


Figure 44. Initial Flow at Power-Up

8.4 Device Functional Modes

The ADS1291, ADS1292, and ADS1292R can be used in different functional modes, as a single device in a system, or as multiple devices in a system. The ADS1291, ADS1292, and ADS1292R are designed to provide configuration flexibility when multiple devices are used in a system, as explained in the *Multiple Device Configuration* section.

In terms of data conversion, the device can operate in continuous mode as explained in the *Continuous mode* section, or in single-shot mode as explained in the *Single-shot mode* section.

8.5 Programming

8.5.1 SPI Interface

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls ADS1291, ADS1292, and ADS1292R operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

8.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ selects the ADS1291, ADS1292, and ADS1292R for SPI communication. $\overline{CS}$ must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

8.5.1.2 Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. SCLK is used to shift commands in and shift data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS1291, ADS1292, and ADS1292R. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum SCLK limit is specified in the *Serial Interface Timing* table. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed needed for the SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Cascade Mode* subsection of the *Multiple Device Configuration* section.) The minimum speed can be calculated with Equation 9.

$$t_{SCLK} < \frac{t_{DR} - 4\,t_{CLK}}{72\ (2 \times 24\ \text{bits} + \text{STATUS})} \tag{9}$$

For example, if the ADS1292R is used in a 500-SPS mode (2 channels, 24-bit resolution), the minimum SCLK speed is approximately 36 kHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing a RDATA command for data on demand. The above SCLK rate limitation applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. Equation 9 assumes that there are no other commands issued in between data captures. SCLK can only be twice the speed of f_{CLK} during register reads and writes. For faster SPI interface, use f_{CLK} = 2.048 MHz and set the CLK_DIV register bit (in the LOFF_STAT register) to '1'.

Programming (continued)

8.5.1.3 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS1291, ADS1292, and ADS1292R (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

8.5.1.4 Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS1291, ADS1292, and ADS1292R. The START pin must transition from low to high before the data output pin can generate any data. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high.

Figure 45 shows the data output protocol for the ADS1292 and ADS1292R.

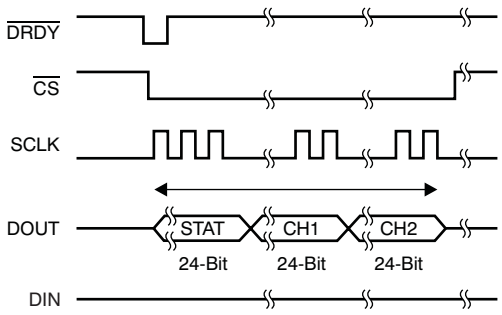


Figure 45. SPI Bus Data Output for the ADS1292 and ADS1292R (Two Channels)

8.5.1.5 Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Read Data Continuous* section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the *RDATA: Read Data* section) can be used to read just one data output from the device (see the *SPI Command Definitions* section for more details). The conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{DRDY}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS1292R, the number of data outputs is (24 status bits + 24 bits × 2 channels) = 72 bits. The format of the 24 status bits is: (1100 + LOFF_STAT[4:0] + GPIO[1:0] + 13 '0's). The data format for each channel data is twos complement, MSB first. When channels are powered down using user register settings, the corresponding channel output is set to '0'. However, the sequence of channel outputs remains the same.

The ADS1291, ADS1292, and ADS1292R also provide a multiple readback feature. Data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte.

8.5.1.6 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When it transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. The behavior of $\overline{DRDY}$ is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the *RDATAC: Read Data Continuous* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

Programming (continued)

Figure 46 shows the relationship between $\overline{\text{DRDY}}$, DOUT, and SCLK during data retrieval (in case of an ADS1291, ADS1292, and ADS1292R with a selected data rate that gives 24-bit resolution). DOUT is latched out at the SCLK rising edge. $\overline{\text{DRDY}}$ is pulled high at the SCLK falling edge. Note that $\overline{\text{DRDY}}$ goes high on the first SCLK falling edge regardless of the status of $\overline{\text{CS}}$ and regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

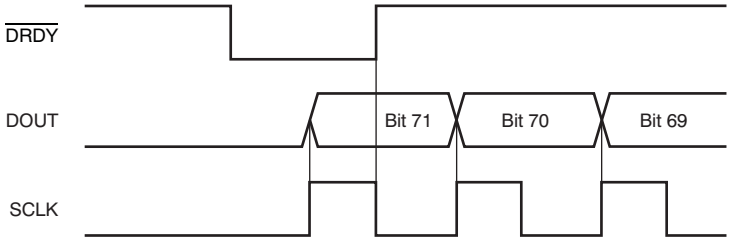


Figure 46. $\overline{\text{DRDY}}$ with Data Retrieval ($\overline{\text{CS}}$ = 0)

8.5.1.7 GPIO

The ADS1291, ADS1292, and ADS1292R have a total of two general-purpose digital input/output (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 47 shows the GPIO port structure. The pins should be shorted to DGND with a series resistor if not used.

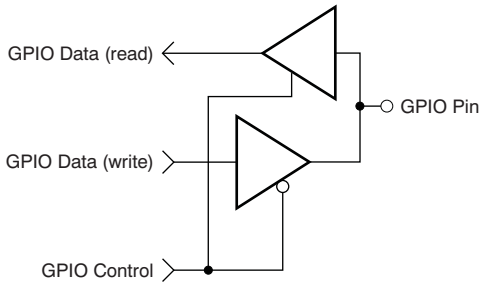


Figure 47. GPIO Port Pin

8.5.1.8 Power-Down and Reset ($\overline{\text{PWDN}}$/$\overline{\text{RESET}}$)

The $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pins are shared. If $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ is held low for longer than 2^9 f_{MOD} clock cycles, the device is powered down. The implementation is such that the device is always reset when $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ makes a transition from high to low. If the device is powered down it is reset first and then if 2^{10} clock elapses it is powered down. Hence, all registers must be rewritten after power up.

There are two methods to reset the ADS1291, ADS1292, and ADS1292R: pull the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin low, or send the RESET opcode command. When using the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{PWDN}}$/$\overline{\text{RESET}}$ pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1, RESP1, and RESP2 registers are set to a new value with a WREG command.

Programming (continued)

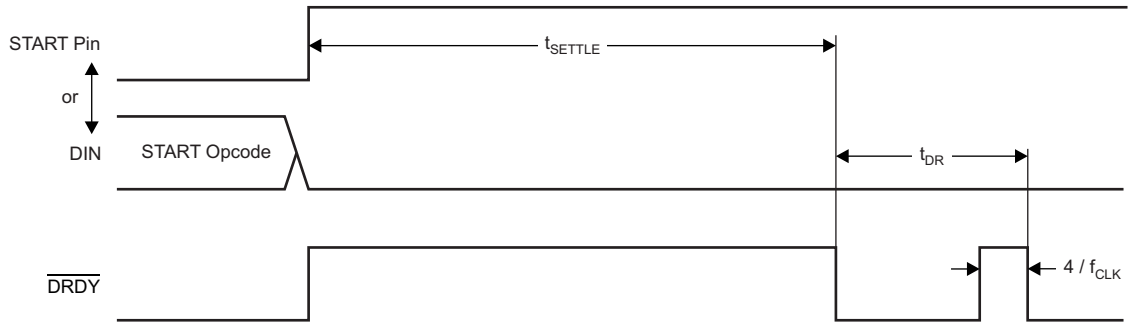
8.5.1.9 START

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a DRDY signal (conversions are halted).

When using the START opcode to control conversion, hold the START pin low. The ADS1291, ADS1292, and ADS1292R feature two modes to control conversion: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 7 of the CONFIG1 register). In multiple device configurations the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection of the *SPI Interface* section for more details).

8.5.1.10 Settling Time

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully settled data when the START signal is pulled high. Once START is pulled high, DRDY is also pulled high. The next DRDY falling edge indicates that data are ready. Figure 48 shows the timing diagram and Table 13 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Refer to Table 10 for the settling time as a function of t_{MOD}. Note that when START is held high and there is a step change in the input signal, it takes 3 t_{DR} for the filter to settle to the new value. Settled data are available on the fourth DRDY pulse. Settling time number uncertainty is one t_{MOD} cycle. Therefore, it is recommended to add one t_{MOD} cycle delay before issuing SCLK to retrieve data.



(1) Settling time uncertainty is one t_{MOD} cycle.

Figure 48. Settling Time

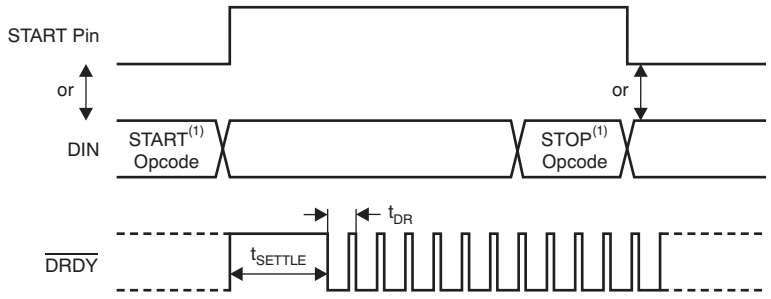
Table 13. Settling Time for Different Data Rates

DR[2:0]	SETTLING TIME(1)	UNIT(2)
000	4100	t_{MOD}
001	2052	t_{MOD}
010	1028	t_{MOD}
011	516	t_{MOD}
100	260	t_{MOD}
101	132	t_{MOD}
110	68	t_{MOD}
111	—	—

(1) Settling time uncertainty is one t_{MOD} cycle.
(2) t_{MOD} = 4 t_{CLK} for CLK_DIV = 0 and t_{MOD} = 16 t_{CLK} for CLK_DIV = 1.

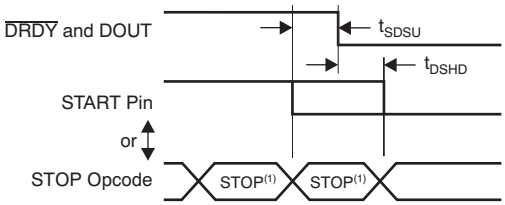
8.5.1.11 Continuous Mode

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 49, the $\overline{\text{DRDY}}$ output goes high when conversions are started and goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 50 and Table 14 show the required $\overline{\text{DRDY}}$ timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued, followed by a START command. This conversion mode is ideal for applications that require a fixed continuous stream of conversions results.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 49. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 50. START to $\overline{\text{DRDY}}$ Timing

Table 14. Timing Characteristics for Figure 50(1)

PARAMETER		MIN	UNIT
t_{SDSU}	START pin low or STOP opcode to $\overline{\text{DRDY}}$ setup time to halt further conversions	8	t_{MOD}
t_{DSHD}	START pin low or STOP opcode to complete current conversion	8	t_{MOD}

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

8.5.1.12 Single-Shot Mode

The single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG1 register to '1'. In single-shot mode, the ADS1291, ADS1292, and ADS1292R perform a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 50, when a conversion is complete, $\overline{\text{DRDY}}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{\text{DRDY}}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. When switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

This conversion mode is provided for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively dropping the data rate by a factor of four. Note that this mode leaves the system more susceptible to aliasing effects, requiring more complex analog anti-aliasing filters at the inputs. Loading on the host processor increases because it must toggle the START pin or send a START command to initiate a new conversion cycle.

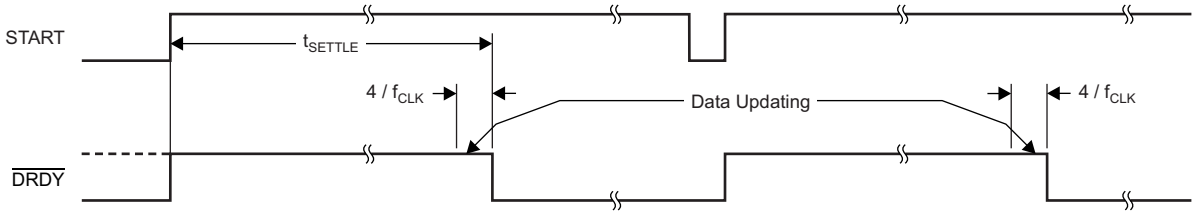


Figure 51. $\overline{\text{DRDY}}$ with No Data Retrieval in Single-Shot Mode

8.5.2 SPI Command Definitions

The ADS1291, ADS1292, and ADS1292R provide flexible configuration control. The opcode commands summarized in Table 15 control and configure the ADS1291, ADS1292, and ADS1292R operation. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADS1291, ADS1292, and ADS1292R on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 15. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start or restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read and write opcodes.

8.5.2.1 WAKEUP: Exit STANDBY Mode

This opcode exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Time is required when exiting standby mode (see the Electrical Characteristics for details). **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Any following command must be sent after 4 t_{CLK} cycles.

8.5.2.2 STANDBY: Enter STANDBY Mode

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Do not send any other command other than the wakeup command after the device enters the standby mode.

8.5.2.3 RESET: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to the default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** It takes 9 f_{MOD} cycles to execute the RESET command. Avoid sending any commands during this time.

8.5.2.4 START: Start Conversions

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) **There are no restrictions on the SCLK rate for this command and it can be issued any time.**

8.5.2.5 STOP: Stop Conversions

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no restrictions on the SCLK rate for this command and it can be issued any time.

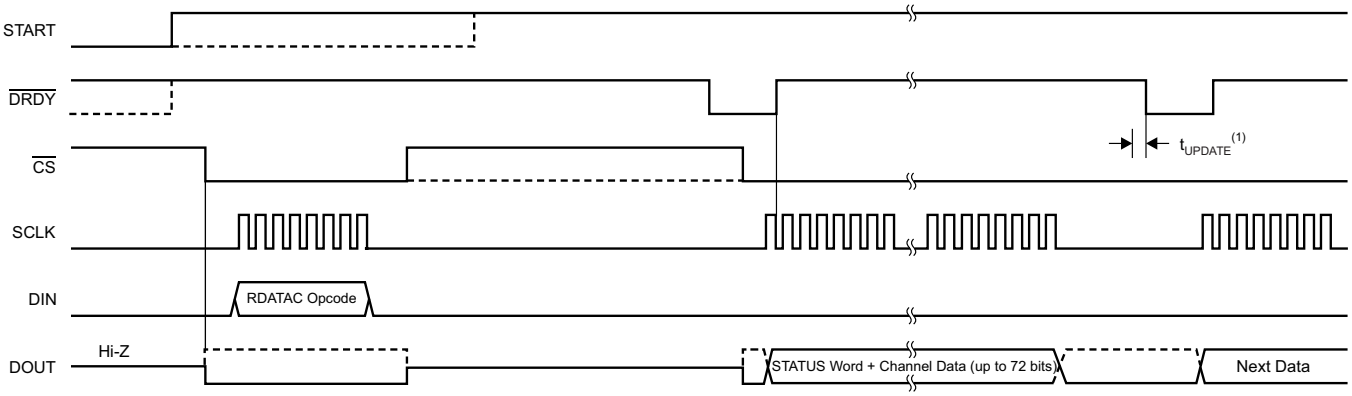
8.5.2.6 OFFSETCAL: Channel Offset Calibration

This command is used to cancel the channel offset. The CALIB_ON bit in the RESP2 register must be set to '1' before issuing this command. OFFSETCAL must be executed every time there is a change in the PGA gain settings.

8.5.2.7 RDATAC: Read Data Continuous

This opcode enables the output of conversion data on each $\overline{DRDY}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the device default mode; the device defaults to this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands can be sent to the device. There is no restriction on the SCLK rate for this command. However, the subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. RDATAC timing is shown in Figure 52. As Figure 52 shows, there is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{DRDY}$ pulse where this command cannot be issued in. To retrieve data from the device after RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 52 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders where registers are set once and do not need to be re-configured.



(1) $t_{UPDATE} = 4 \times t_{CLK}$. Do not read data during this time.

Figure 52. RDATAC Usage

8.5.2.8 SDATAC: Stop Read Data Continuous

This opcode cancels the Read Data Continuous mode. There is no restriction on the SCLK rate for this command, but the following command must wait for 4 t_{CLK} cycles.

8.5.2.9 RDATA: Read Data

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There is no restriction on the SCLK rate for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. Figure 53 shows the recommended way to use the RDATA command. RDATA is best suited for ECG- and EEG-type systems where register setting must be read or changed often between conversion cycles.

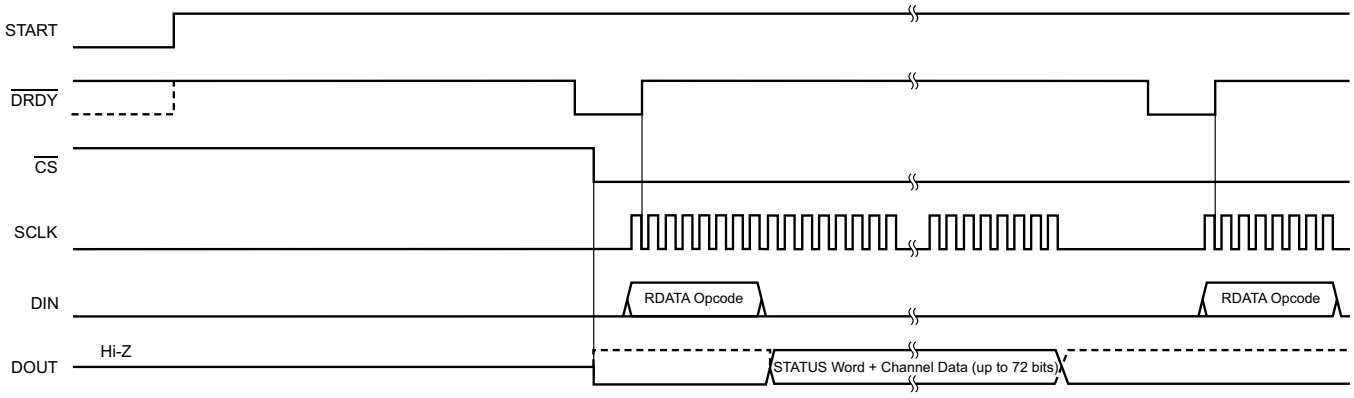


Figure 53. RDATA Usage

8.5.2.10 Sending Multi-Byte Commands

The ADS1291, ADS1292, and ADS1292R serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assume CLK is 512 kHz, then $t_{SDECODE}$ (4 t_{CLK}) is 7.8125 µs. When SCLK is 16 MHz, one byte can be transferred in 500 ns. This byte-transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so the end of the second byte arrives 7.3125 µs later. If SCLK is 1 MHz, one byte is transferred in 8 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfer per cycle to multiple bytes.

8.5.2.11 RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 54. When the device is in read data continuous mode it is necessary to issue a SDATAC command before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

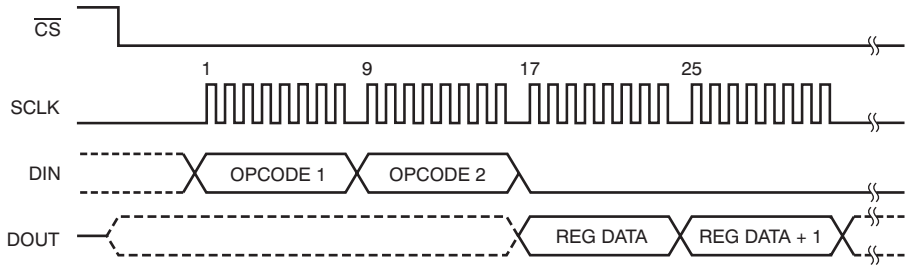


Figure 54. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

8.5.2.12 WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address.

The second byte of the opcode specifies the number of registers to write – 1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 55. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

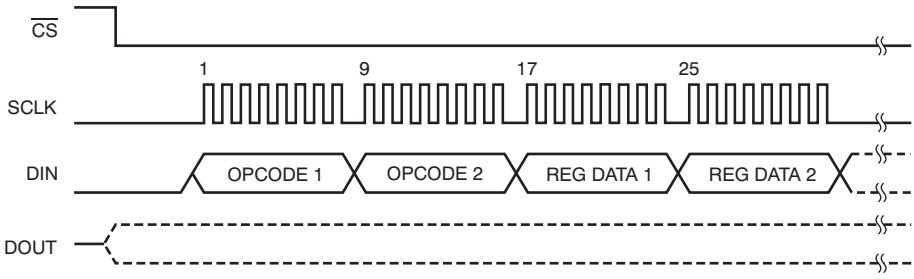


Figure 55. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

8.6 Register Maps

Table 16 describes the various ADS1291, ADS1292, and ADS1292R registers.

Table 16. Register Assignments

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settings (Read-Only Registers)										
00h	ID	XX	REV_ID7	REV_ID6	REV_ID5	1	0	0	REV_ID1	REV_ID0
Global Settings Across Channels										
01h	CONFIG1	02	SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0
02h	CONFIG2	80	1	PDB_LOFF_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ
03h	LOFF	10	COMP_TH2	COMP_TH1	COMP_TH0	1	ILEAD_OFF1	ILEAD_OFF0	0	FLEAD_OFF
Channel-Specific Settings										
04h	CH1SET	00	PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0
05h	CH2SET	00	PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0
06h	RLD_SENS	00	CHOP1	CHOP0	PDB_RLD	RLD_LOFF_SENS	RLD2N	RLD2P	RLD1N	RLD1P
07h	LOFF_SENS	00	0	0	FLIP2	FLIP1	LOFF2N	LOFF2P	LOFF1N	LOFF1P
08h	LOFF_STAT	00	0	CLK_DIV	0	RLD_STAT	IN2N_OFF	IN2P_OFF	IN1N_OFF	IN1P_OFF
GPIO and Other Registers										
09h	RESP1	00	RESP_DEMOD_EN1	RESP_MOD_EN	RESP_PH3	RESP_PH2	RESP_PH1	RESP_PH0	1	RESP_CTRL
0Ah	RESP2	02	CALIB_ON	0	0	0	0	RESP_FREQ	RLDREF_INT	1
0Bh	GPIO	0C	0	0	0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1

8.6.1 User Register Description

8.6.1.1 ID: ID Control Register (Factory-Programmed, Read-Only) (address = 00h)

This register is programmed during device manufacture to indicate device characteristics.

Figure 56. ID: ID Control Register (Factory-Programmed, Read-Only)

7	6	5	4	3	2	1	0
REV_ID7	REV_ID6	REV_ID5	1	0	0	REV_ID1	REV_ID0

Table 17. ID: ID Control Register (Factory-Programmed, Read-Only) Field Descriptions

Bits[7:5]	**REV_ID[7:5]: Revision identification**
	000 = Reserved 001 = Reserved 010 = ADS1x9x device 011 = ADS1292R device 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
Bit 4	**Reads high**
Bits[3:2]	**Reads low**
Bits[1:0]	**REV_ID[1:0]: Revision identification**
	00 = ADS1191 01 = ADS1192 10 = ADS1291 11 = ADS1292 and ADS1292R

8.6.1.2 CONFIG1: Configuration Register 1 (address = 01h)

This register configures each ADC channel sample rate.

Figure 57. CONFIG1: Configuration Register 1

7	6	5	4	3	2	1	0
SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0

Table 18. CONFIG1: Configuration Register 1 Field Descriptions

Bit 7	**SINGLE_SHOT: Single-shot conversion**		
	This bit sets the conversion mode 0 = Continuous conversion mode (default) 1 = Single-shot mode		
Bits[6:3]	**Must be set to '0'**		
Bits[2:0]	**DR[2:0]: Channel oversampling ratio**		
	These bits determine the oversampling ratio of both channel 1 and channel 2.		
	BIT	**OVERSAMPLING RATIO**	**DATA RATE(1)**
	000	f_{MOD} / 1024	125 SPS
	001	f_{MOD} / 512	250 SPS
	010	f_{MOD} / 256	500 SPS (default)
	011	f_{MOD} / 128	1 kSPS
	100	f_{MOD} / 64	2 kSPS
	101	f_{MOD} / 32	4 kSPS
	110	f_{MOD} / 16	8 kSPS
	111	Do not use	Do not use

(1) f_{CLK} = 512 kHz and CLK_DIV = 0 or f_{CLK} = 2.048 MHz and CLK_DIV = 1.

8.6.1.3 CONFIG2: Configuration Register 2 (address = 02h)

This register configures the test signal, clock, reference, and LOFF buffer.

Figure 58. CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
1	PDB_LOFF_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ

Table 19. CONFIG2: Configuration Register 2 Field Descriptions

Bit 7	**Must be set to '1'**
Bit 6	**PDB_LOFF_COMP: Lead-off comparator power-down**
	This bit powers down the lead-off comparators. 0 = Lead-off comparators disabled (default) 1 = Lead-off comparators enabled
Bit 5	**PDB_REFBUF: Reference buffer power-down**
	This bit powers down the internal reference buffer so that the external reference can be used. 0 = Reference buffer is powered down (default) 1 = Reference buffer is enabled
Bit 4	**VREF_4V: Enables 4-V reference**
	This bit chooses between 2.42-V and 4.033-V reference. 0 = 2.42-V reference (default) 1 = 4.033-V reference
Bit 3	**CLK_EN: CLK connection**
	This bit determines if the internal oscillator signal is connected to the CLK pin when an internal oscillator is used. 0 = Oscillator clock output disabled (default) 1 = Oscillator clock output enabled
Bit 2	**Must be set to '0'**
Bit 1	**INT_TEST: Test signal selection**
	This bit determines whether the test signal is turned on or off. 0 = Off (default) 1 = On; amplitude = ±(VREFP – VREFN) / 2400
Bit 0	**TEST_FREQ: Test signal frequency**
	This bit determines the test signal frequency. 0 = At dc (default) 1 = Square wave at 1 Hz

8.6.1.4 LOFF: Lead-Off Control Register (address = 03h)

This register configures the lead-off detection operation.

Figure 59. LOFF: Lead-Off Control Register

7	6	5	4	3	2	1	0
COMP_TH2	COMP_TH1	COMP_TH0	1	ILEAD_OFF1	ILEAD_OFF0	0	FLEAD_OFF

Table 20. LOFF: Lead-Off Control Register Field Descriptions

Bits[7:5]	**COMP_TH[2:0]: Lead-off comparator threshold**
	These bits determine the lead-off comparator threshold. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for a detailed description.
	Comparator positive side
	000 = 95% (default) 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70%
	Comparator negative side
	000 = 5% (default) 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
Bit 4	**Must be set to '1'**
Bits[3:2]	**ILEAD_OFF[1:0]: Lead-off current magnitude**
	These bits determine the magnitude of current for the current lead-off mode. 00 = 6 nA (default) 01 = 22 nA 10 = 6 µA 11 = 22 µA
Bit 1	**Must be set to '0'**
Bit 0	**FLEAD_OFF: Lead-off frequency**
	This bit selects ac or dc lead-off. 0 = At dc lead-off detect (default) 1 = At ac lead-off detect at f_{DR} / 4 (500 Hz for an 2-kHz output rate)

8.6.1.5 CH1SET: Channel 1 Settings (address = 04h)

This register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details.

Figure 60. CH1SET: Channel 1 Settings

7	6	5	4	3	2	1	0
PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0

Table 21. CH1SET: Channel 1 Settings Field Descriptions

Bit 7	**PD1: Channel 1 power-down**
	0 = Normal operation (default) 1 = Channel 1 power-down(1)
Bits[6:4]	**GAIN1[2:0]: Channel 1 PGA gain setting**
	These bits determine the PGA gain setting for channel 1.
	000 = 6 (default) 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
Bits[3:0]	**MUX1[3:0]: Channel 1 input selection**
	These bits determine the channel 1 input selection.
	0000 = Normal electrode input (default) 0001 = Input shorted (for offset measurements) 0010 = RLD_MEASURE 0011 = MVDD(2) for supply measurement 0100 = Temperature sensor 0101 = Test signal 0110 = RLD_DRP (positive input is connected to RLDIN) 0111 = RLD_DRM (negative input is connected to RLDIN) 1000 = RLD_DRPM (both positive and negative inputs are connected to RLDIN) 1001 = Route IN3P and IN3N to channel 1 inputs 1010 = Reserved

(1) When powering down channel 1, make sure the input multiplexer is set to input short configuration. Bits[3:0] = 001.
(2) For channel 1, (MVDDP – MVDDN) is [0.5(AVDD + AVSS)]; for channel 2, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

8.6.1.6 CH2SET: Channel 2 Settings (address = 05h)

This register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details.

Figure 61. CH2SET: Channel 2 Settings

7	6	5	4	3	2	1	0
PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0

Table 22. CH2SET: Channel 2 Settings Field Descriptions

Bit 7	**PD2: Channel 2 power-down**
	0 = Normal operation (default) 1 = Channel 2 power-down(1)
Bits[6:4]	**GAIN2[2:0]: Channel 2 PGA gain setting**
	These bits determine the PGA gain setting for channel 2.
	000 = 6 (default) 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
Bits[3:0]	**MUX2[3:0]: Channel 2 input selection**
	These bits determine the channel 2 input selection.
	0000 = Normal electrode input (default) 0001 = Input shorted (for offset measurements) 0010 = RLD_MEASURE 0011 = VDD / 2 for supply measurement 0100 = Temperature sensor 0101 = Test signal 0110 = RLD_DRP (positive input is connected to RLDIN) 0111 = RLD_DRM (negative input is connected to RLDIN) 1000 = RLD_DRPM (both positive and negative inputs are connected to RLDIN) 1001 = Route IN3P and IN3N to channel 2 inputs 1010 = Reserved

(1) When powering down channel 2 and for ADS1291, make sure the input multiplexer is set to input short configuration. Bits[3:0] = 001.

8.6.1.7 RLD_SENS: Right Leg Drive Sense Selection (address = 06h)

This register controls the selection of the positive and negative signals from each channel for right leg drive derivation. See the *Right Leg Drive (RLD DC Bias Circuit)* subsection of the *ECG-Specific Functions* section for details.

Figure 62. RLD_SENS: Right Leg Drive Sense Selection

7	6	5	4	3	2	1	0
CHOP1	CHOP0	PDB_RLD	RLD_LOFF_SENS	RLD2N	RLD2P	RLD1N	RLD1P

Table 23. RLD_SENS: Right Leg Drive Sense Selection Field Descriptions

Bits[7:6]	**CHOP[1:0]: Chop frequency**
	These bits determine PGA chop frequency 00 = f_{MOD} / 16 01 = Reserved 10 = f_{MOD} / 2 11 = f_{MOD} / 4
Bit 5	**PDB_RLD: RLD buffer power**
	This bit determines the RLD buffer power state. 0 = RLD buffer is powered down (default) 1 = RLD buffer is enabled
Bit 4	**RLD_LOFF_SENSE: RLD lead-off sense function**
	This bit enables the RLD lead-off sense function. 0 = RLD lead-off sense is disabled (default) 1 = RLD lead-off sense is enabled
Bit 3	**RLD2N: Channel 2 RLD negative inputs**
	This bit controls the selection of negative inputs from channel 2 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN2N
Bit 2	**RLD2P: Channel 2 RLD positive inputs**
	This bit controls the selection of positive inputs from channel 2 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN2P
Bit 1	**RLD1N: Channel 1 RLD negative inputs**
	This bit controls the selection of negative inputs from channel 1 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN1N
Bit 0	**RLD1P: Channel 1 RLD positive inputs**
	This bit controls the selection of positive inputs from channel 1 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN1P

8.6.1.8 LOFF_SENS: Lead-Off Sense Selection (address = 07h)

This register selects the positive and negative side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Note that the LOFF_STAT register bits should be ignored if the corresponding LOFF_SENS bits are set to '1'.

Figure 63. LOFF_SENS: Lead-Off Sense Selection

7	6	5	4	3	2	1	0
0	0	FLIP2	FLIP1	LOFF2N	LOFF2P	LOFF1N	LOFF1P

Table 24. LOFF_SENS: Lead-Off Sense Selection Field Descriptions

Bits[7:6]	**Must be set to '0'**
Bit 5	**FLIP2: Current direction selection**
	This bit controls the direction of the current used for lead-off derivation for channel 2. 0 = Disabled (default) 1 = Enabled
Bit 4	**FLIP1: Current direction selection**
	This bit controls the direction of the current used for lead-off derivation for channel 1. 0 = Disabled (default) 1 = Enabled
Bit 3	**LOFF2N: Channel 2 lead-off detection negative inputs**
	This bit controls the selection of negative input from channel 2 for lead-off detection. 0 = Disabled (default) 1 = Enabled
Bit 2	**LOFF2P: Channel 2 lead-off detection positive inputs**
	This bit controls the selection of positive input from channel 2 for lead-off detection. 0 = Disabled (default) 1 = Enabled
Bit 1	**LOFF1N: Channel 1 lead-off detection negative inputs**
	This bit controls the selection of negative input from channel 1 for lead-off detection. 0 = Disabled (default) 1 = Enabled
Bit 0	**LOFF1P: Channel 1 lead-off detection positive inputs**
	This bit controls the selection of positive input from channel 1 for lead-off detection. 0 = Disabled (default) 1 = Enabled

8.6.1.9 LOFF_STAT: Lead-Off Status (address = 08h)

This register stores the status of whether the positive or negative electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Ignore the LOFF_STAT values if the corresponding LOFF_SENS bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off. When the LOFF_SENS bits[3:0] are '0', the LOFF_STAT bits should be ignored.

Figure 64. LOFF_STAT: Lead-Off Status

7	6	5	4	3	2	1	0
0	CLK_DIV	0	RLD_STAT (read only)	IN2N_OFF (read only)	IN2P_OFF (read only)	IN1N_OFF (read only)	IN1P_OFF (read only)

Table 25. LOFF_STAT: Lead-Off Status Field Descriptions

Bit 7	**Must be set to '0'**
Bit 6	**CLK_DIV : Clock divider selection**
	This bit sets the modultar divider ratio between f_{CLK} and f_{MOD}. Two external clock values are supported: 512 kHz and 2.048 MHz. 0 = f_{MOD} = f_{CLK} / 4 (default, use when f_{CLK} = 512 kHz) 1 = f_{MOD} = f_{CLK} / 16 (use when f_{CLK} = 2.048 MHz)
Bit 5	**Must be set to '0'**
Bit 4	**RLD_STAT: RLD lead-off status**
	This bit determines the status of RLD. 0 = RLD is connected (default) 1 = RLD is not connected
Bit 3	**IN2N_OFF: Channel 2 negative electrode status**
	This bit determines if the channel 2 negative electrode is connected or not. 0 = Connected (default) 1 = Not connected
Bit 2	**IN2P_OFF: Channel 2 positive electrode status**
	This bit determines if the channel 2 positive electrode is connected or not. 0 = Connected (default) 1 = Not connected
Bit 1	**IN1N_OFF: Channel 1 negative electrode status**
	This bit determines if the channel 1 negative electrode is connected or not. 0 = Connected (default) 1 = Not connected
Bit 0	**IN1P_OFF: Channel 1 positive electrode status**
	This bit determines if the channel 1 positive electrode is connected or not. 0 = Connected (default) 1 = Not connected

8.6.1.10 RESP1: Respiration Control Register 1 (address = 09h)

This register controls the respiration functionality. This register applies to the ADS1292R version only. For the ADS1291 and ADS1292 devices, 02h must be written to the RESP1 register.

Figure 65. RESP1: Respiration Control Register 1

7	6	5	4	3	2	1	0
RESP_DEMOD_EN1	RESP_MOD_EN	RESP_PH3	RESP_PH2	RESP_PH1	RESP_PH0	1	RESP_CTRL

Table 26. RESP1: Respiration Control Register 1 Field Descriptions

Bit 7	**RESP_DEMOD_EN1: Enables respiration demodulation circuitry**		
	This bit enables and disables the demodulation circuitry on channel 1. 0 = RESP demodulation circuitry turned off (default) 1 = RESP demodulation circuitry turned on		
Bit 6	**RESP_MOD_EN: Enables respiration modulation circuitry**		
	This bit enables and disables the modulation circuitry on channel 1. 0 = RESP modulation circuitry turned off (default) 1 = RESP modulation circuitry turned on		
Bits[5:2]	**RESP_PH[3:0]: Respiration phase(1)**		
	These bits control the phase of the respiration demodulation control signal.		
	RESP_PH[3:0]	**RESP_CLK = 32kHz**	**RESP_CLK = 64 kHz**
	0000	0° (default)	0° (default)
	0001	11.25°	22.5°
	0010	22.5°	45°
	0011	33.75°	67.5°
	0100	45°	90°
	0101	56.25°	112.5°
	0110	67.5°	135°
	0111	78.75°	157.5°
	1000	90°	Not available
	1001	101.25°	Not available
	1010	112.5°	Not available
	1011	123.75°	Not available
	1100	135°	Not available
	1101	146.25°	Not available
	1110	157.5°	Not available
	1111	168.75°	Not available
Bit 1	**Must be set to '1'**		
Bit 0	**RESP_CTRL: Respiration control**		
	This bit sets the mode of the respiration circuitry. 0 = Internal respiration with internal clock 1 = Internal respiration with external clock		

(1) The RESP_PH3 bit is ignored when RESP_CLK = 64 kHz.

8.6.1.11 RESP2: Respiration Control Register 2 (address = 0Ah)

This register controls the respiration and calibration functionality.

Figure 66. RESP2: Respiration Control Register 2

7	6	5	4	3	2	1	0
CALIB_ON	0	0	0	0	RESP_FREQ	RLDREF_INT	1

Table 27. RESP2: Respiration Control Register 2 Field Descriptions

Bit 7	**CALIB_ON: Calibration on**
	This bit is used to enable offset calibration. 0 = Off (default) 1 = On
Bits[6:3]	**Must be '0'**
Bit 2	**RESP_FREQ: Respiration control frequency (ADS1292R only)**
	This bit controls the respiration control frequency when RESP_CTRL = 0. This bit must be written with '1' for the ADS1291 and ADS1292. 0 = 32 kHz (default) 1 = 64 kHz
Bit 1	**RLDREF_INT: RLDREF signal**
	This bit determines the RLDREF signal source. 0 = RLDREF signal fed externally 1 = RLDREF signal (AVDD – AVSS) / 2 generated internally (default)
Bit 0	**Must be set to '1'**

8.6.1.12 GPIO: General-Purpose I/O Register (address = 0Bh)

This register controls the GPIO pins.

Figure 67. GPIO: General-Purpose I/O Register

7	6	5	4	3	2	1	0
0	0	0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1

Table 28. GPIO: General-Purpose I/O Register Field Descriptions

Bits[7:4]	**Must be '0'**
Bits[3:2]	**GPIOC[2:1]: GPIO 1 and 2 control**
	These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input (default)
Bits[1:0]	**GPIOD[2:1]: GPIO 1 and 2 data**
	These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

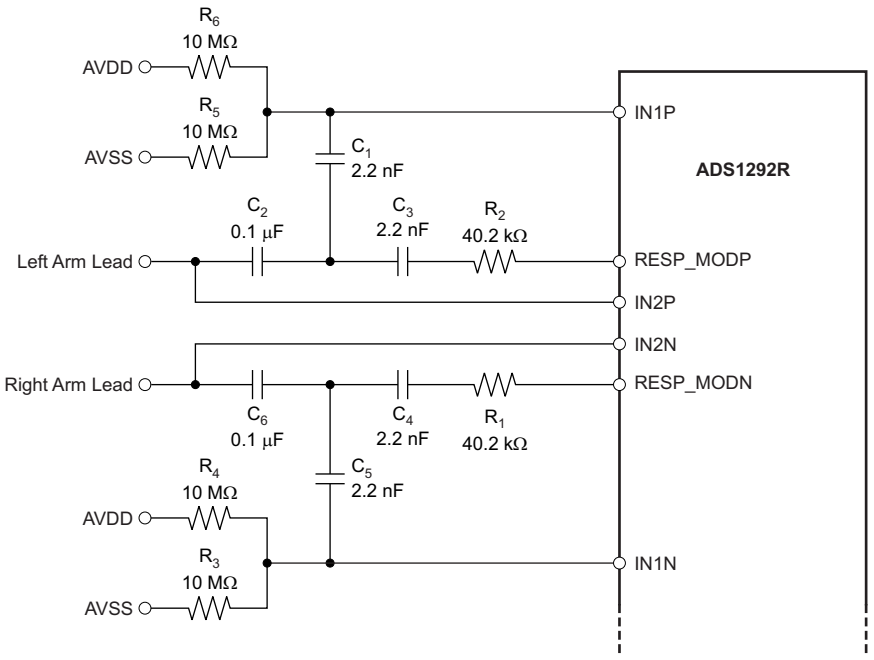
The ADS1291, ADS1292, and ADS1292R incorporate all features commonly required in a low-power medical electrocardiogram (ECG) application.

The ADS1291, ADS1292, and ADS1292R have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the right leg drive (RLD) output signal. Lead-off detection can be implemented internal to the device, using the device internal excitation current sink or source. The ADS1292R version includes a fully integrated respiration impedance measurement function.

9.2 Typical Application

A typical application for the ADS1292R is the acquisition of ECG signals in combination with a respiration impedance measurement.

The ADS1292R channel 1 with respiration enabled mode cannot be used to acquire ECG signals. If the right arm (RA) and left arm (LA) leads are intended to measure respiration and ECG signals, the two leads can be wired into channel 1 for respiration and channel 2 for ECG signals, as shown in Figure 68.



NOTE: Patient and input protection circuitry not shown.

Figure 68. Typical Respiration Circuitry

Typical Application (continued)

9.2.1 Design Requirements

This design requires the measurement of respiration and ECG signals on the right arm (RA) and left arm (LA) with very low noise. Standard requirements are respiration impedance values ranging from 2 kΩ to 15 kΩ, modulation clock frequencies of 32 kHz or 64 kHz, and noise levels of less than 10 µV.

9.2.2 Detailed Design Procedure

Figure 69 shows a respiration test circuit. Figure 70 and Figure 71 plot noise on channel 1 for the ADS1292R as baseline impedance, gain, and phase are swept. The x-axis is the baseline impedance, normalized to a 30-µA modulation current (as shown in Equation 10).

$$R_{NORMALIZED} = \frac{R_{ACTUAL} \times I_{ACTUAL}}{30\ \mu A} \quad (10)$$

where:

R_{ACTUAL} is the baseline body impedance

I_{ACTUAL} is the modulation current, as calculated by (VREFP – AVSS) divided by the impedance of the modulation circuit

For example, if modulation frequency = 32 kHz, R_{ACTUAL} = 3 kΩ, I_{ACTUAL} = 50 µA, and $R_{NORMALIZED}$ = (3 kΩ × 50 µA) / 29 µA = 5.1 kΩ.

Referring to Figure 70 and Figure 71, it can be noted that gain = 4 and phase = 112.5° yield the best performance at 4.6 μV_{PP}. Low-pass filtering this signal with a high-order 2-Hz cutoff can reduce the noise to less than 1200 nV_{PP}. The impedance resolution is 1200 nV_{PP} / 30 µA = 40 mΩ.

When the modulation frequency is 32 kHz, gains of 3 and 4 and phase of 112.5° and 135° are recommended.

When the modulation frequency is 64 kHz, gains of 2 and 3 and phase of 135° and 157° are recommended for best performance.

Typical Application (continued)

9.2.3 Application Curves

Figure 70 and Figure 71 show the results for the respiration test circuit of Figure 69 by plotting noise on channel 1 for the ADS1292R as baseline impedance, gain, and phase are swept. The x-axis is the baseline impedance, normalized to a 30-µA modulation current (as shown in Equation 10).

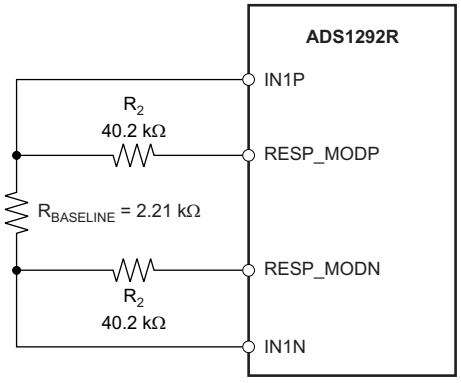


Figure 69. Respiration Noise Test Circuit

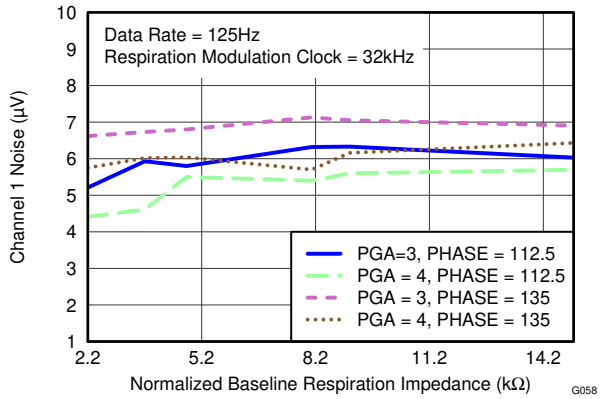


Figure 70. Channel 1 Noise versus Impedance for 32-kHz Modulation Clock and Phase (BW = 32 Hz, Respiration Modulation Clock = 32 kHz)

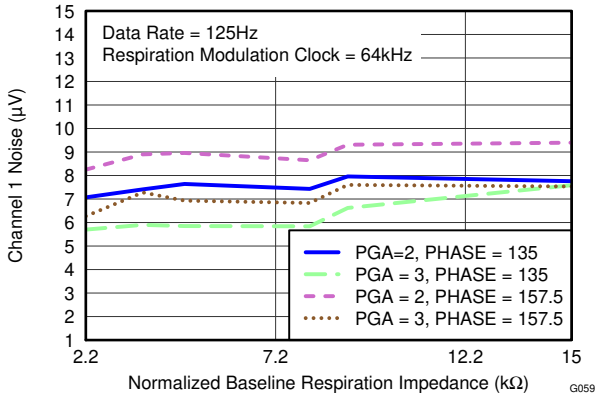


Figure 71. Channel 1 Noise versus Impedance for 64-kHz Modulation Clock and Phase (BW = 32 Hz, Respiration Modulation Clock = 64 kHz)

10 Power Supply Recommendations

The nominal performance of the device is specified with an analog supply voltage AVDD of 3 V and an internal reference voltage VREFP of 2.42 V. The device also operates using power supplies at the AVDD pin from 2.7 V to 5.5 V with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are listed in the *Typical Characteristics* section.

10.1 Power-Up Sequencing

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 72. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed, see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details. The power-up sequence timing is shown in Table 29.

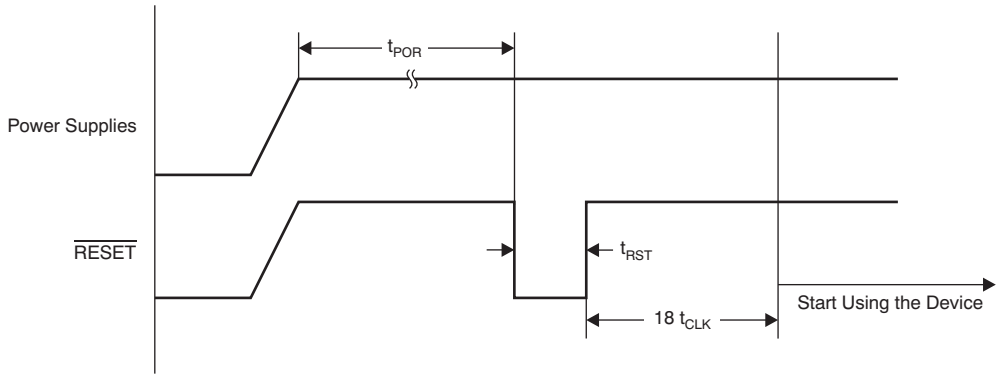


Figure 72. Power-Up Timing Diagram

Table 29. Power-Up Sequence Timing

PARAMETER		MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	2^{12}			t_{MOD}
t_{RST}	Reset low width	1			t_{MOD}

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices.

Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.

Place the external components as close to the device as possible.

Keep the traces as short as possible.

11.1.1 PCB Layout

11.1.1.1 Power Supplies and Grounding

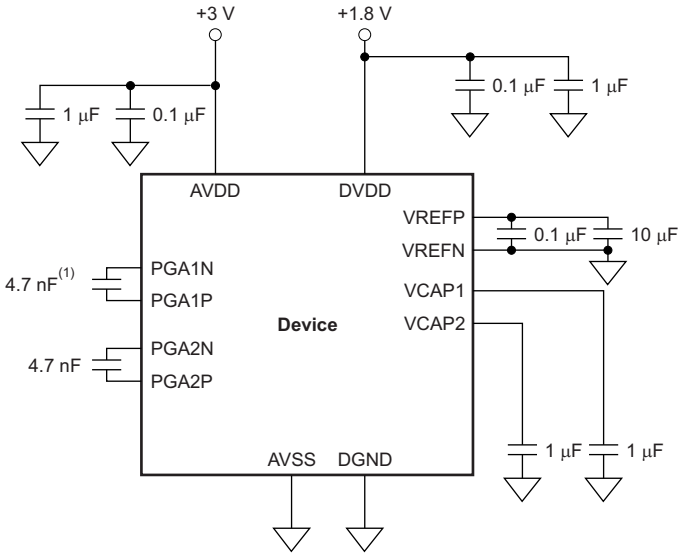
The ADS1291, ADS1292, and ADS1292R have two supplies: AVDD and DVDD. AVDD should be as quiet as possible. AVDD provides the supply to the charge pump block and has transients at f_{CLK}. It is important to eliminate noise from AVDD that is non-synchronous with the ADS1291, ADS1292, and ADS1292R operation. Each ADS1291, ADS1292, and ADS1292R supply should be bypassed with 10-µF and a 0.1-µF solid ceramic capacitors. It is recommended that placement of the digital circuits (such as the DSP, microcontrollers, and FPGAs) in the system is done such that the return currents on those devices do not cross the ADS1291, ADS1292, and ADS1292R analog return path. The ADS1291, ADS1292, and ADS1292R can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be of the surface-mount, low-cost, low-profile multi-layer ceramic type. In most cases the VCAP1 capacitor can also be a multi-layer ceramic, but in systems where the board is subjected to high or low frequency vibration, it is recommend that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (for example, C0G or NPO) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, X8R, and such) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using internal reference, noise on the VCAP1 node results in performance degradation.

Layout Guidelines (continued)

11.1.1.1.1 Connecting the Device to Unipolar (+3 V or +1.8 V) Supplies

Figure 73 shows the ADS1291, ADS1292, and ADS1292R connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supply (DVDD) is referenced to digital ground (DGND).



NOTE: Place the capacitors for supply, reference, VCAP1, and VCAP2 as close to the package as possible.

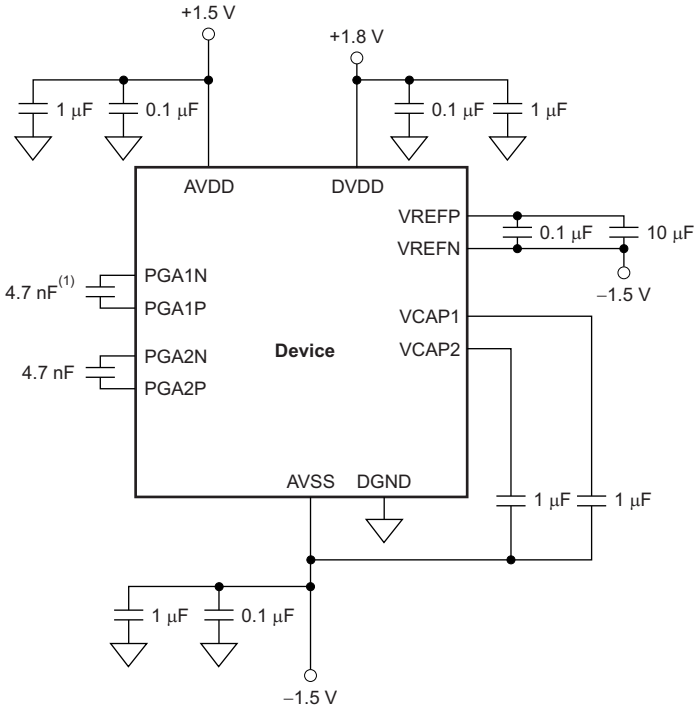
(1) When using the ADS1292R and the channel 1 respiration function, this capacitor must be 47 nF.

Figure 73. Single-Supply Operation

Layout Guidelines (continued)

11.1.1.1.2 Connecting the Device to Bipolar (±1.5 V or 1.8 V) Supplies

Figure 74 illustrates the ADS1291, ADS1292, and ADS1292R connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, VCAP1, and VCAP2 as close to the package as possible.

(1) When using the ADS1292R and the channel 1 respiration function, this capacitor must be 47 nF.

Figure 74. Bipolar Supply Operation

11.1.1.2 Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADS1291, ADS1292, and ADS1292R input bias current if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

11.2 Layout Example

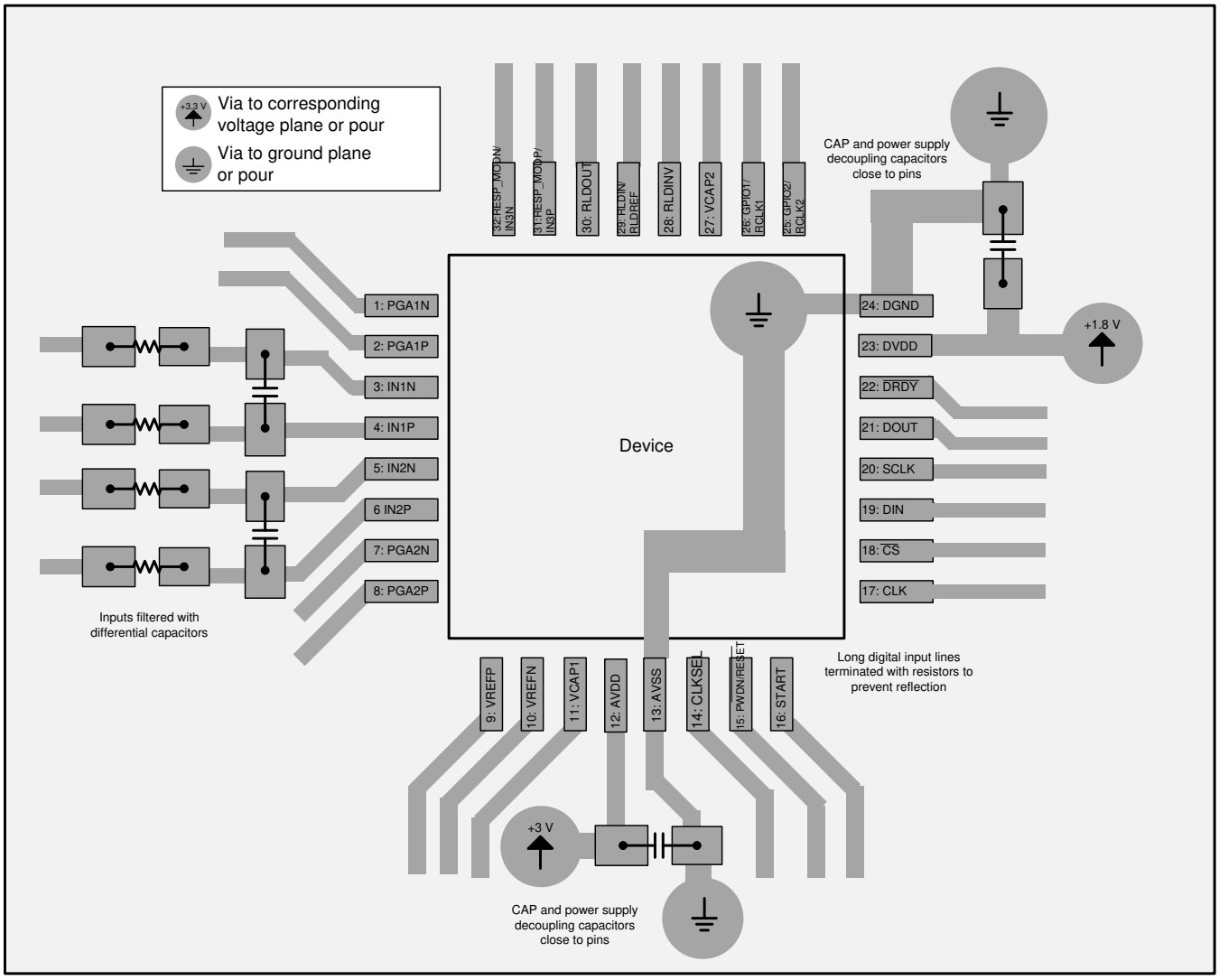


Figure 75. Example PCB Layout for Single-Supply Operation

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **30.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
ADS1291	单击此处	单击此处	单击此处	单击此处	单击此处
ADS1292	单击此处	单击此处	单击此处	单击此处	单击此处
ADS1292R	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商标

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1291IPBS	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1291	Samples
ADS1291IPBSR	ACTIVE	TQFP	PBS	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1291	Samples
ADS1291IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1291	Samples
ADS1291IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1291	Samples
ADS1292IPBS	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1292	Samples
ADS1292IPBSR	ACTIVE	TQFP	PBS	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1292	Samples
ADS1292IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1292	Samples
ADS1292IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1292	Samples
ADS1292RIPBS	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1292R	Samples
ADS1292RIPBSR	ACTIVE	TQFP	PBS	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1292R	Samples
ADS1292RIRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1292R	Samples
ADS1292RIRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1292R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

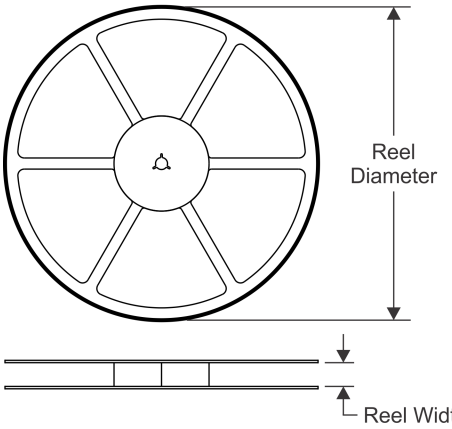
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

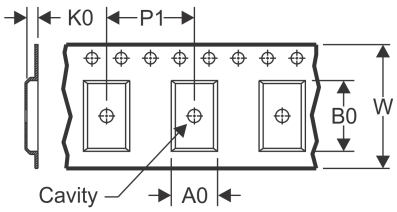
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

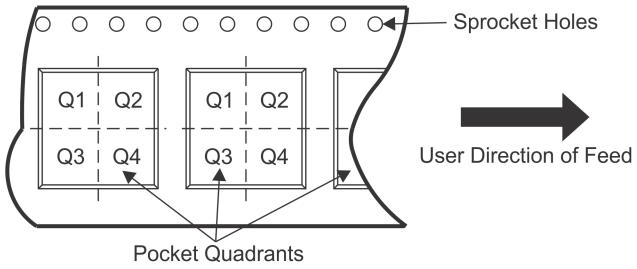


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

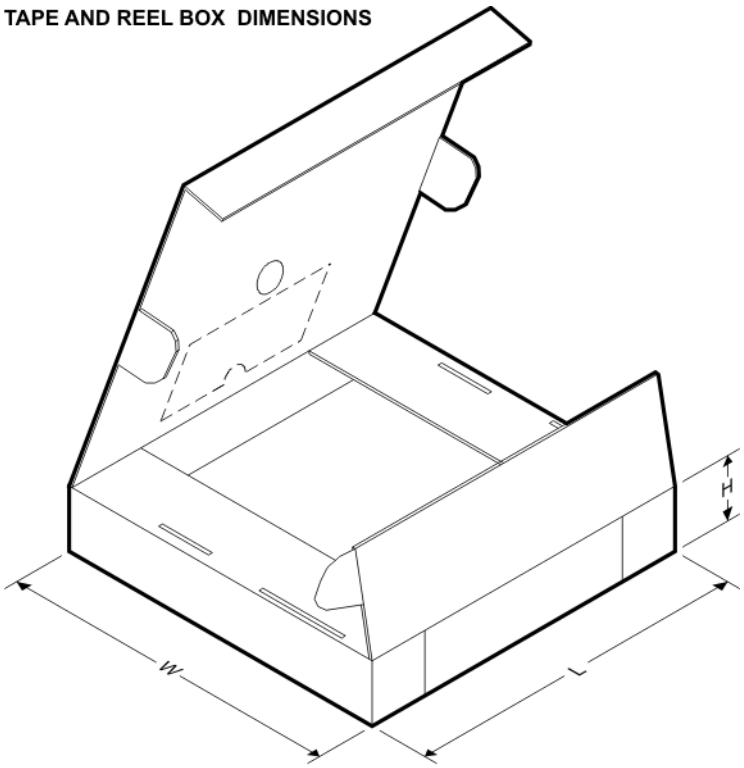
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1291IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1291IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1292IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1292IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1292RIRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS1292RIRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

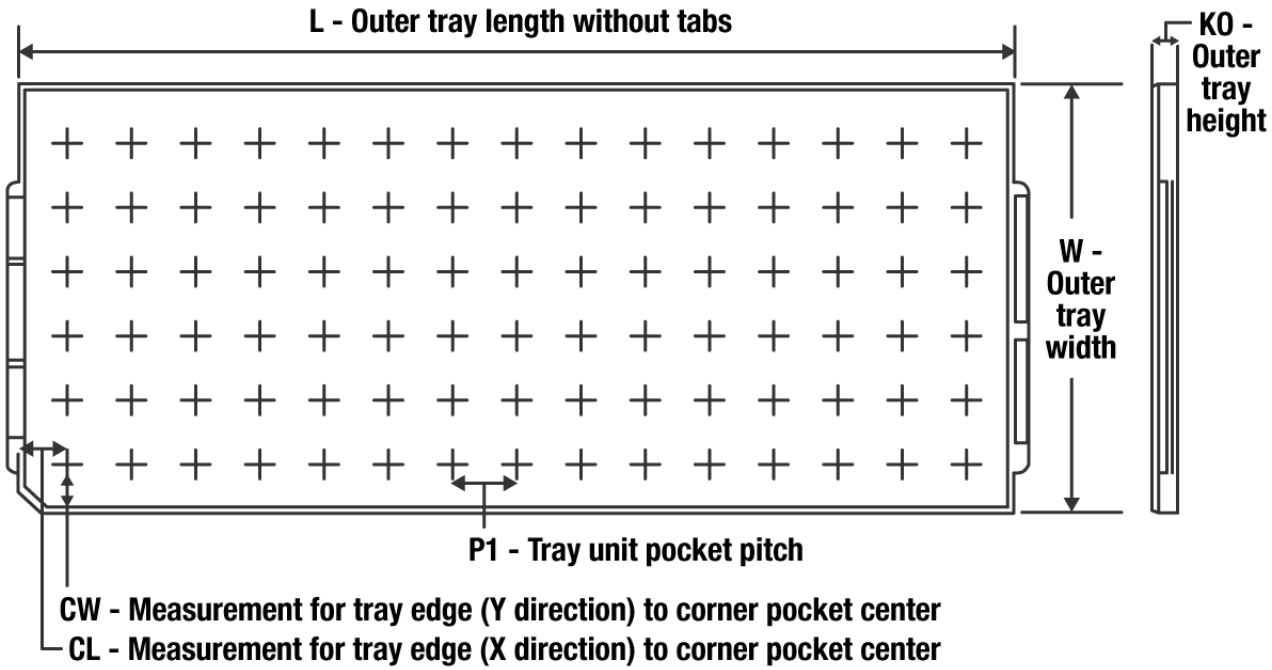
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1291IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADS1291IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADS1292IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADS1292IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADS1292RIRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADS1292RIRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

TRAY

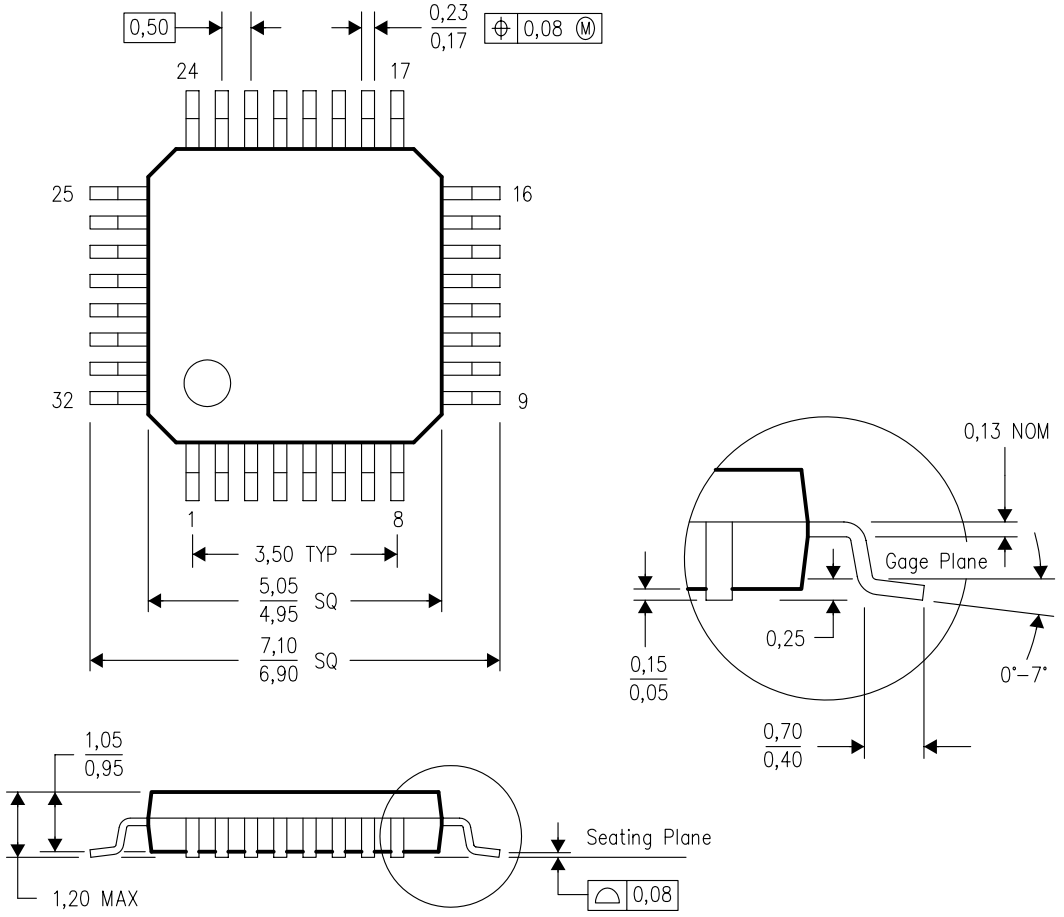


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS1291IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS1292IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS1292RIPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



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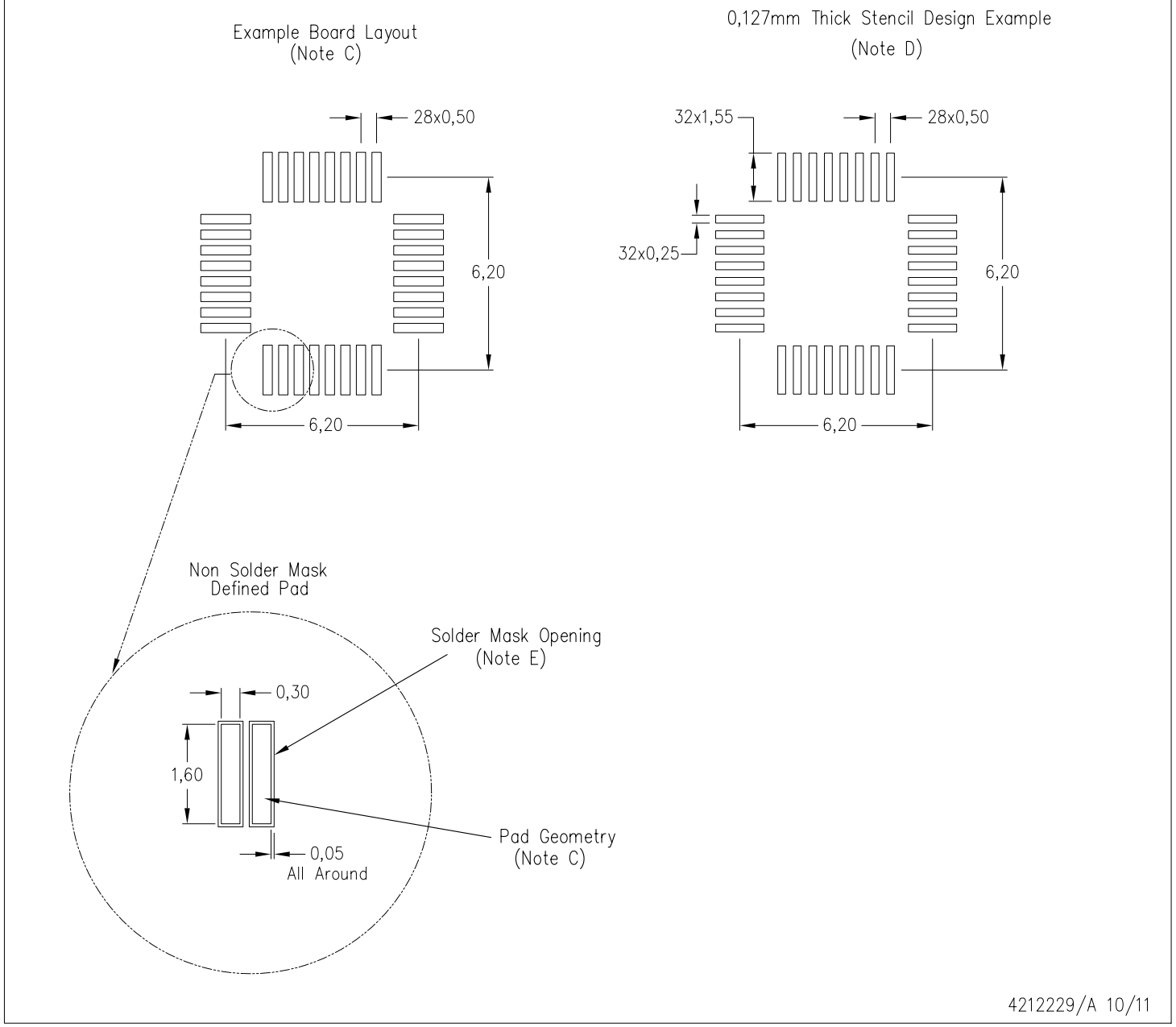
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

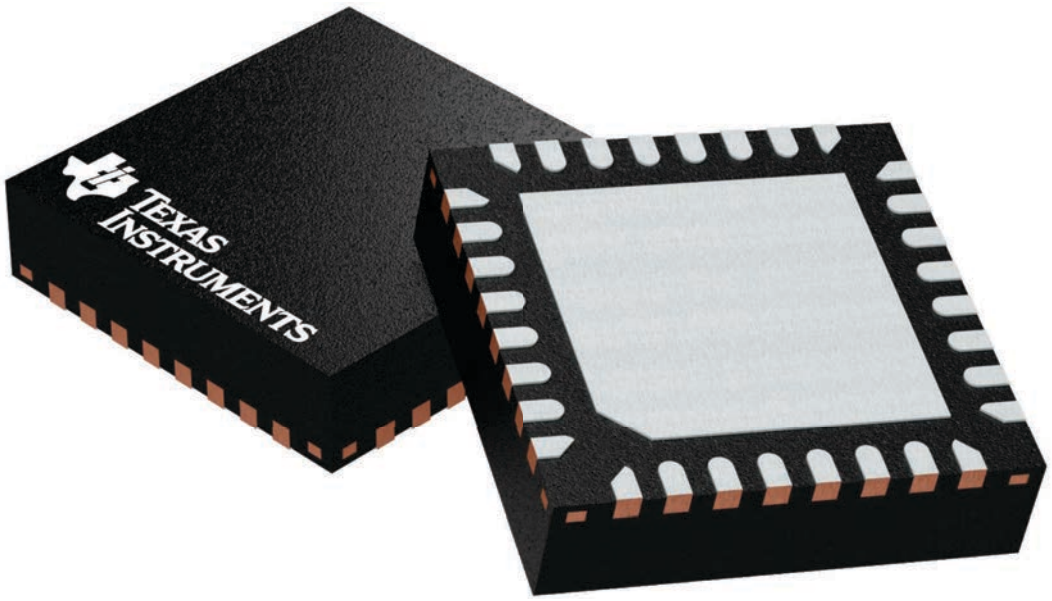
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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