具有 PGA 和电压基准的 ADS125H02 ±20V 输入、双通道、40kSPS、24 位 Δ-Σ ADC

1 特性

- ±20V 输入、24 位 Δ-Σ ADC
- 可编程数据速率：2.5SPS 至 40000SPS
- 高压高阻抗 PGA：
  - 差分输入范围：高达 ±20V
  - 可编程增益：0.125 至 128
  - 共模输入电压：高达 ±15.5V
  - 输入阻抗：1GΩ（最小值）
- 高性能 ADC：
  - 输入噪声：45nV$_{RMS}$ (20SPS)
  - CMRR：105dB
  - 在 50Hz、60Hz 下的常规模式抑制：95dB
  - 温漂：5nV/°C
  - 增益漂移：1ppm/°C
  - 积分非线性 (INL)：2ppm
- 集成 特性 和诊断功能：
  - 2.5V 基准：3ppm/°C 漂移
  - 时钟振荡器：2.5% 误差（最大值）
  - 激励电流源
  - GPIO 可驱动外部多路复用器
  - 信号和基准电压监控器
  - 循环冗余校验 (CRC)
- 电源：
  - AVDD：4.75V 至 5.25V
  - DVDD：2.7V 至 5.25V
  - HVDD：±5V 至 ±18V
- 工作温度：–40°C 至 +125°C
- 5mm × 5mm VQFN 封装

2 应用

- PLC 模拟输入模块：
  - 电压（例如 ±10V 或 0V 至 5V）
  - 电流（例如 4mA 至 20mA，具有分流器）
  - 温度（例如 RTD、热电偶）
- 测试和测量：
  - 高共模电压输入
  - 电池测试
  - 高侧电流测量

3 说明

ADS125H02 是一款 ±20V 输入、24 位、Δ-Σ 模数转换器 (ADC)。该 ADC 配备 低噪声可编程增益放大器 (PGA)、内部基准电压、时钟振荡器和信号或基准电压超范围监控器。

与分立的解决方案相比，该产品将一个宽输入电压范围、±18V PGA 和 ADC 集成到单个封装中，可将电路板面积减小最多 50%。

具有 0.125 至 128 的可编程增益（相当于 ±20V 至 ±20mV 的等效输入范围），因而无需外部衰减器或外部增益级。1GΩ 的最低输入阻抗可减小由传感器负载导致的误差。而且，由于具备低噪声和低漂移性能，因而能直接连接桥、电阻式温度检测器 (RTD) 和热电偶传感器。

数字滤波器可减弱数据速率 ≤ 50SPS 或 60SPS 时的 50Hz 和 60Hz 线路周期噪声，以减小测量误差。滤波器还可提供无延迟转换数据，从而在通道定序期间实现高数据吞吐量。

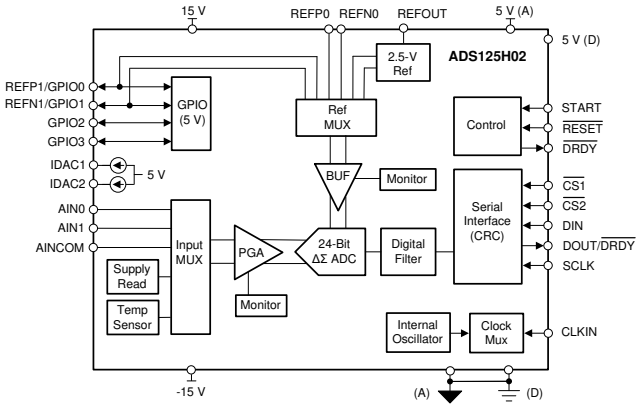
ADS125H02 采用 5mm × 5mm VQFN 封装，额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS125H02	VQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

功能方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2019) to Revision C **Page**

- 已删除 从文档中删除了 ADS125H01 ... 1
- Changed *Device Comparison Table* ... 3
- Added *Effective resolution* parameter to *Electrical Characteristics* table ... 7
- 已添加 *Offset Voltage Long-Term Drift* curves to *Typical Characteristics* ... 15
- 已添加 *Gain Long-Term Drift* curves to *Typical Characteristics* ... 16
- 已添加 *Internal Reference Voltage Long-Term Drift* curve to *Typical Characteristics* ... 17
- 已添加 *Oscillator Frequency Long-Term Drift* curve to *Typical Characteristics* ... 19
- 已更改 *Noise Performance* section ... 20
- 已添加 effective resolution and noise-free resolution data in *Noise Performance* ... 23
- 已更改 sinc1, sinc3, sinc4, and sinc5 values and footnote in *Conversion Latency Time* table ... 40
- 已更改 start-conversion delay value from 0 µs to 50 µs in the *Start-Conversion Delay* section ... 40
- 已更改 sinc mode values in *Calibration Time* table ... 44
- 已更改 address 00h default value from xxh to 6xh in *Register Map Summary* table ... 53
- 已更改 reset value from xxh to 6xh in *Device Identification (ID) Register* ... 54

Changes from Revision A (January 2019) to Revision B **Page**

- 已更改 将 ADS125H02 的状态从“预告信息”更改成了“生产数据” ... 1

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5 Device Comparison Table

PART NUMBER	SINGLE-ENDED, DIFFERENTIAL CHANNELS	INTERNAL REFERENCE	GPIOs	SENSOR CURRENT SOURCES	TEMPERATURE SENSOR
ADS125H01	1, 1	No	0	0	No
ADS125H02	2, 1	Yes	4	2	Yes

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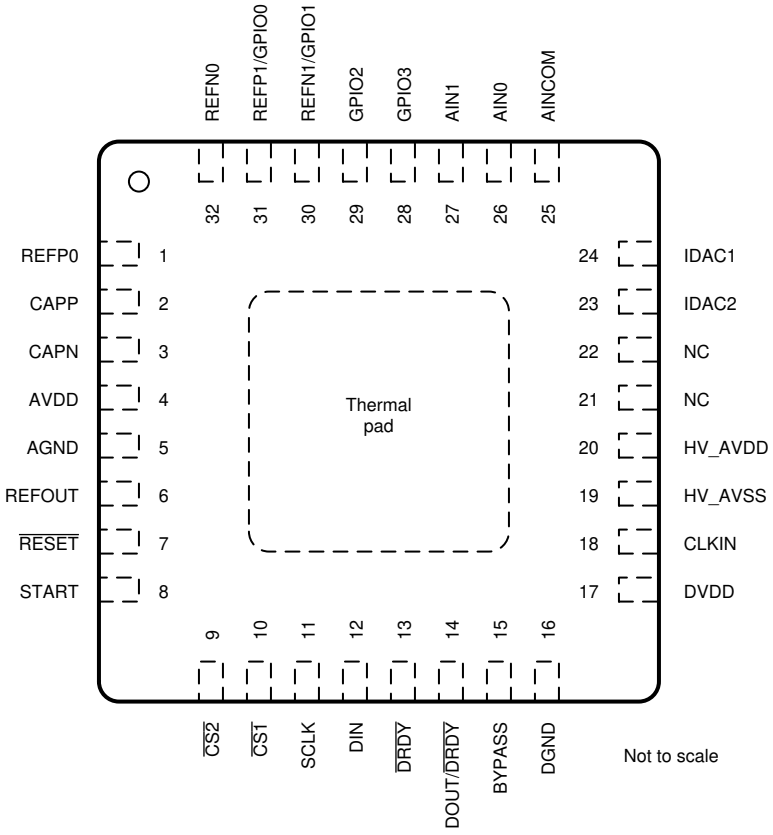
6 Pin Configuration and Functions

RHB Package: ADS125H02
32-Pin VQFN
Top View



Pin Functions

NO.	NAME	I/O	DESCRIPTION
1	REFP0	Analog input	Reference input 0 positive
2	CAPP	Analog output	PGA output P; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
3	CAPN	Analog output	PGA output N; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
4	AVDD	Analog	Low-voltage analog power supply (5 V)
5	AGND	Analog	Analog ground; connect to the ADC ground plane
6	REFOUT	Analog output	2.5-V reference output; connect a 10-µF capacitor to AGND
7	$\overline{\text{RESET}}$	Digital input	Reset; active low
8	START	Digital input	Conversion start, active high
9	$\overline{\text{CS2}}$	Digital input	Serial interface chip select 2 to select the PGA for communication
10	$\overline{\text{CS1}}$	Digital input	Serial interface chip select 1 to select the ADC for communication
11	SCLK	Digital input	Serial interface shift clock
12	DIN	Digital input	Serial interface data input
13	$\overline{\text{DRDY}}$	Digital output	Data-ready indicator; active low
14	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial interface data output and data-ready indicator (active low)
15	BYPASS	Analog output	2-V subregulator output; connect a 1-µF capacitor to DGND
16	DGND	Digital	Digital ground; connect to the ADC ground plane
17	DVDD	Digital	Digital power supply (3 V to 5 V)
18	CLKIN	Digital input	External clock input. Connect to DGND for internal oscillator operation.

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Pin Functions (continued)

NO.	NAME	I/O	DESCRIPTION
19	HV_AVSS	Analog	High-voltage negative analog power supply
20	HV_AVDD	Analog	High-voltage positive analog power supply
21, 22	NC	—	No connection; electrically float or tie to AGND
23	IDAC2	Analog output	Current source 2 output
24	IDAC1	Analog output	Current source 1 output
25	AINCOM	Analog input	Analog input common (single-ended common input)
26	AIN0	Analog input	Analog input 0
27	AIN1	Analog input	Analog input 1
28	GPIO3	Digital input/output	General-purpose input/output 3
29	GPIO2	Digital input/output	General-purpose input/output 2
30	REFN1/GPIO1	Analog, digital input/output	Reference input 1 negative and general-purpose input/output 1
31	REFP1/GPIO0	Analog, digital input/output	Reference input 1 positive and general-purpose input/output 0
32	REFN0	Analog input	Reference input 0 negative
Thermal pad		—	Exposed thermal pad; connect to DGND; see the recommended PCB land pattern at the end of the document.

7 Specifications

7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	HV_AVDD to HV_AVSS	–0.3	38	V
	HV_AVSS to AGND	–19	0.3	
	AVDD to AGND	–0.3	6	
	DVDD to DGND	–0.3	6	
	AGND to DGND	–0.1	0.1	
Analog input voltage	AIN0, AIN1, AINCOM	HV_AVSS – 0.3	HV_AVDD + 0.3	V
	GPIO[3:0], REFP[1:0], REFN[1:0], IDAC[2:1]	AGND – 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, START, $\overline{RESET}$, CLKIN, $\overline{DRDY}$, DOUT/$\overline{DRDY}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous (2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10 mA in the event the analog input voltage exceeds HV_AVDD + 0.3 V or HV_AVSS – 0.3 V, or if the reference input, GPIO, or IDAC voltage exceeds AVDD + 0.3 V or AGND – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or DGND – 0.3 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-voltage analog power supplies	HV_AVDD to HV_AVSS	10		36	V
		HV_AVSS to AGND	–18		0	
		HV_AVDD to AGND(1)	5		36	
	Low-voltage analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	2.7		5.25	V
SIGNAL INPUTS						
$V_{(AINX)}$	Absolute input voltage		See the *PGA Operating Range* section			V
V_{IN}	Differential input voltage range(2)	$V_{IN} = V_{AINP} – V_{AINN}$	–20	±V_{REF} / Gain	20	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Reference voltage input	$V_{REF} = V_{(REFPx)} – V_{(REFNx)}$	0.9		AVDD	V
$V_{(REFNx)}$	Negative reference voltage		AGND – 0.05		$V_{(REFPx)}$ – 0.9	V
$V_{(REFPx)}$	Positive reference voltage		$V_{(REFNx)}$ + 0.9		AVDD + 0.05	V
GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)						
	Input voltage		AGND		AVDD	V
DIGITAL INPUTS (Other Than GPIOs)						
	Input voltage		DGND		DVDD	V
EXTERNAL CLOCK						
$f_{(CLK)}$	Frequency	Data rate < 40000 SPS	1	7.3728	8	MHz
		Data rate = 40000 SPS	1	10.24	10.75	
	Duty cycle		40%		60%	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

(1) HV_AVDD can be connected to AVDD if AVDD ≥ 5 V.
(2) The full differential input voltage range is limited under certain conditions. See the *PGA Operating Range* section for details.

7.4 Thermal Information

THERMAL METRIC(1)		ADS125H02 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	$V_{(AINx)}$ = 0 V, T_A ≤ 105°C	–15	±0.5	15	nA
	Absolute input current drift			20		pA/°C
	Differential input current	V_{IN} = 2.5 V		±0.1		nA
		V_{IN} = 2.5 V, auto-zero mode(1)		±2		nA/V
	Differential input current drift	V_{IN} = 2.5 V		10		pA/°C
	Differential input impedance		1	20		GΩ
	Crosstalk			0.1		µV/V
PGA						
	Gain		0.125, 0.1875, 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64,128			V/V
	Antialias filter frequency			230		kHz
PERFORMANCE						
	Resolution	No missing codes	24			Bits
	Data rate		2.5		40000	SPS
e_n	Noise performance		See 表 1 and 表 2			
	Effective resolution		See 图 52 and 图 53			
INL	Integral nonlinearity	Gain = 0.125 to 32		2	10	ppm_{FSR}
		Gain = 64, 128		4	12	
V_{OS}	Offset voltage(2)	T_A = 25°C	–30 – 300 / Gain	±10 + 100 / Gain	30 + 300 / Gain	µV
		T_A = 25°C, auto-zero mode	–0.5 – 0.5 / Gain	±0.5 / Gain	0.5 + 0.5 / Gain	
	Offset voltage drift	Gain = 0.125 to 8		150 / Gain	700 / Gain	nV/°C
		Gain = 16 to 128		10	50	
		Auto-zero mode		5 / Gain		
GE	Gain error(2)	T_A = 25°C, all gains	–0.7%	±0.1%	0.7%	
	Gain drift	All gains		1	4	ppm/°C
NMRR	Normal-mode rejection ratio(3)		See 表 7			
CMRR	Common-mode rejection ratio(4)	Data rate = 20 SPS		130		dB
		Data rate = 400 SPS	90	105		
PSRR	Power-supply rejection ratio(5)	HV_AVDD, HV_AVSS		2	20	µV/V
		AVDD		20	60	
		DVDD		5	30	
VOLTAGE REFERENCE INPUTS						
	Absolute input current			±250		nA
	Input current vs reference voltage			15		nA/V
	Input current drift			0.2		nA/°C
	Input impedance	Differential		30		MΩ

(1) Auto-zero mode input current is proportional to the data rate.
(2) Offset and gain errors are reduced to the level of noise by calibration.
(3) Normal-mode rejection ratio performance is dependent on the digital filter configuration.
(4) Common-mode rejection ratio is specified at 60 Hz.
(5) Power-supply rejection ratio is specified at dc.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCE(6)						
	Voltage			2.5		V
	Initial error	T_A = 25°C	–0.2%	±0.1%	0.2%	
	Temperature drift	T_A = 0°C to 85°C		3	10	ppm/°C
		T_A = –40°C to 125°C		7	20	
	Thermal hysteresis	First 0°C to 105°C cycle		70		ppm
		Second 0°C to 105°C cycle		25		
	Output current		–10		10	mA
	Load regulation			20		µV/mA
	Start-up time	Settling to ±0.001% final value		100		ms
TEMPERATURE SENSOR						
	Voltage	T_A = 25°C		120		mV
	Temperature coefficient			390		µV/°C
EXCITATION CURRENT SOURCES (IDACS)						
	Currents		50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000			µA
	Compliance range	All currents	AGND		AVDD – 1.1	V
	Absolute error	All currents	–6%	±0.7%	6%	
	Relative error	Equal values	–1.5%	±0.1%	1.5%	
		Unequal values		±1%		
	Temperature drift	Absolute		100		ppm/°C
		Equal values, I ≤ 750 µA		5	25	
PGA MONITORS(7)						
	Input and output low threshold			HV_AVSS + 2		V
	Input and output high threshold			HV_AVDD – 2		V
REFERENCE MONITOR						
	Low voltage threshold			0.4	0.6	V
INTERNAL OSCILLATOR						
	Accuracy	Data rate < 40000 SPS	–2.5%	±0.5%	2.5%	
		Data rate = 40000 SPS	–3.5%	±0.5%	3.5%	
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD		AVDD	V
V_{IL}	Low-level input voltage				0.3 × AVDD	V
	Input hysteresis			0.5		V

(6) Voltage reference specifications apply after the device is soldered on the PCB using the recommended PCB layout pattern and using the reflow profile per JEDEC standard J-STD-020D1.
(7) See the *PGA Monitor* section for details.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS (OTHER THAN GPIOs)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
		I_{OH} = 8 mA		0.75 × DVDD		
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × DVDD	V
		I_{OL} = –8 mA		0.2 × DVDD		
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD	V
V_{IL}	Low-level input voltage				0.3 × DVDD	V
	Input hysteresis			0.1		V
	Input leakage		–10		10	µA
POWER SUPPLY						
I_{HV_AVDD} I_{HV_AVSS}	HV_AVDD, HV_AVSS supply current			1.1	1.8	mA
I_{AVDD}	AVDD supply current			2.8	4.6	mA
	Additional AVDD supply current	Voltage reference enabled		0.2		mA
		When data rate = 40000 SPS		0.8		
		Current sources enabled		As programmed		µA
I_{DVDD}	DVDD supply current	Internal oscillator active		0.5	0.7	mA
		Data rate = 40000 SPS		0.7	1	
P_D	Power dissipation			49	79	mW

7.6 Timing Requirements

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V (unless otherwise noted)

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS1}$ or $\overline{CS2}$ falling edge	50		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	25		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
$t_{c(SC)}$	SCLK period	97		ns
$t_{w(SCH)}$, $t_{w(SCL)}$	Pulse duration, SCLK high or low	40		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge before $\overline{CS1}$ or $\overline{CS2}$ rising edge	50		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS1}$ or $\overline{CS2}$ high to reset interface	25		ns
RESET				
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	4		1 / f_{CLK}
CONVERSION CONTROL				
$t_{w(STH)}$	Pulse duration, START high	4		1 / f_{CLK}
$t_{w(STL)}$	Pulse duration, START low	4		1 / f_{CLK}
$t_{su(STDR)}$	Setup time, START low or STOP command before $\overline{DRDY}$ falling edge to stop the next conversion (continuous mode)		100	1 / f_{CLK}
$t_{h(DRSP)}$	Hold time, START low or STOP command after $\overline{DRDY}$ falling edge to continue the next conversion (continuous mode)	150		1 / f_{CLK}

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7.7 Switching Characteristics

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V, and DOUT/$\overline{\text{DRDY}}$ load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$t_{w(DRH)}$	Pulse duration, $\overline{\text{DRDY}}$ high		16			1 / f_{CLK}
$t_{p(CSDO)}$	Propagation delay time, $\overline{\text{CS1}}$ or $\overline{\text{CS2}}$ falling edge to DOUT/$\overline{\text{DRDY}}$ driven		0		50	ns
$t_{p(SCDO1)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{\text{DRDY}}$				40	ns
$t_{h(SCDO1)}$	Hold time, SCLK rising edge to invalid DOUT/$\overline{\text{DRDY}}$		0			ns
$t_{h(SCDO2)}$	Hold time, last SCLK falling edge to invalid DOUT/$\overline{\text{DRDY}}$ data output function		15			ns
$t_{p(SCDO2)}$	Propagation delay time, last SCLK falling edge to DOUT/$\overline{\text{DRDY}}$ data-ready function				110	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{\text{CS1}}$ or $\overline{\text{CS2}}$ rising edge to DOUT/$\overline{\text{DRDY}}$ high impedance				50	ns
RESET						
$t_{p(RSCN)}$	Propagation delay time, $\overline{\text{RESET}}$ rising edge or RESET command to conversion start		512			1 / f_{CLK}
$t_{p(PRCM)}$	Propagation delay time, power-on threshold voltage to ADC communication			2^{16}		1 / f_{CLK}
$t_{p(CMCN)}$	Propagation delay time, ADC communication to conversion start		512			1 / f_{CLK}
CONVERSION CONTROL						
$t_{p(STDR)}$	Propagation delay time, START pin high or START command to $\overline{\text{DRDY}}$ high				2	1 / f_{CLK}

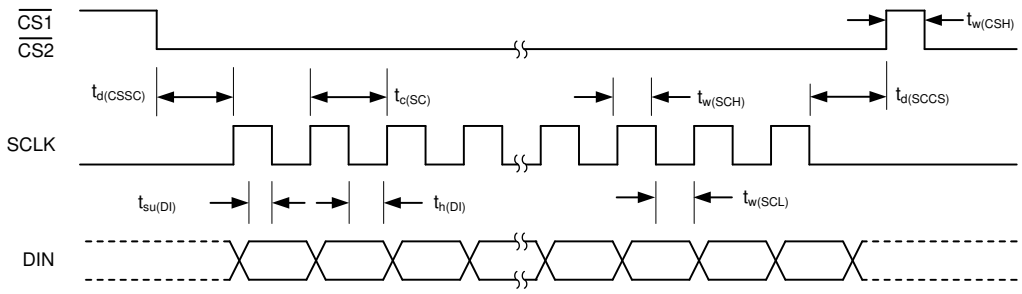
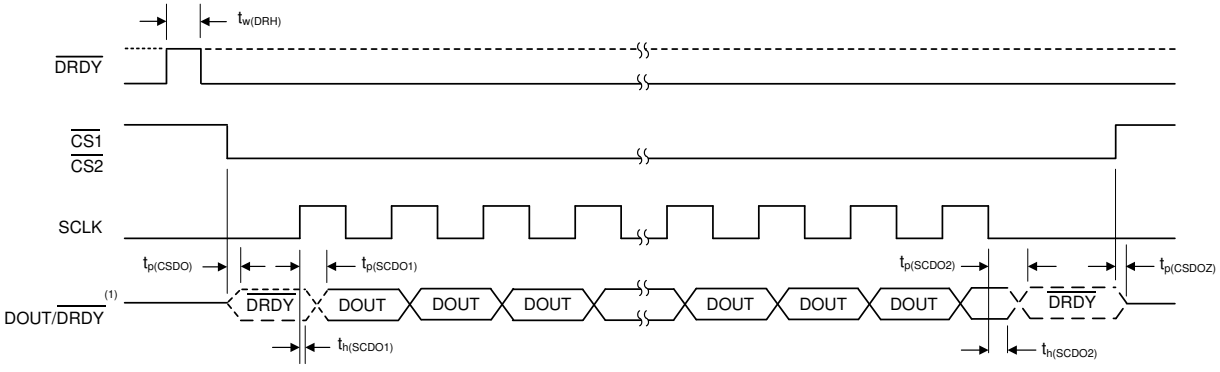


图 1. Serial Interface Timing Requirements



(1) $\overline{\text{DRDY}}$ is the data-ready function in the interval between $\overline{\text{CS1}}$ low and the first SCLK rising edge, and in the interval between the last SCLK falling edge of the command to $\overline{\text{CS1}}$ high. DOUT is the data output function during the data read operation.

图 2. Serial Interface Switching Characteristics

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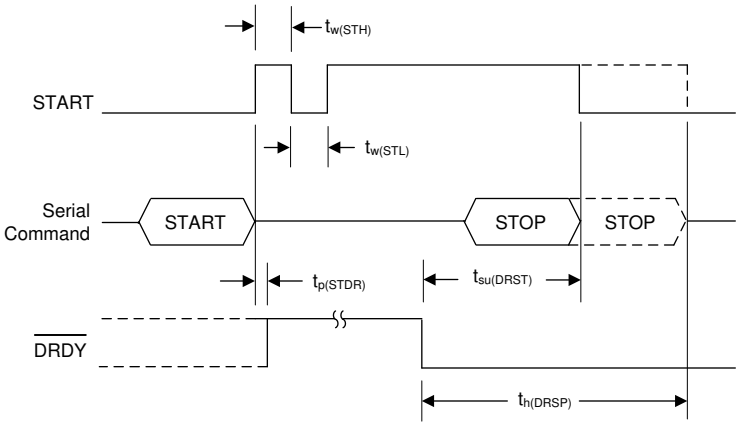


图 3. Conversion Control Timing Requirements

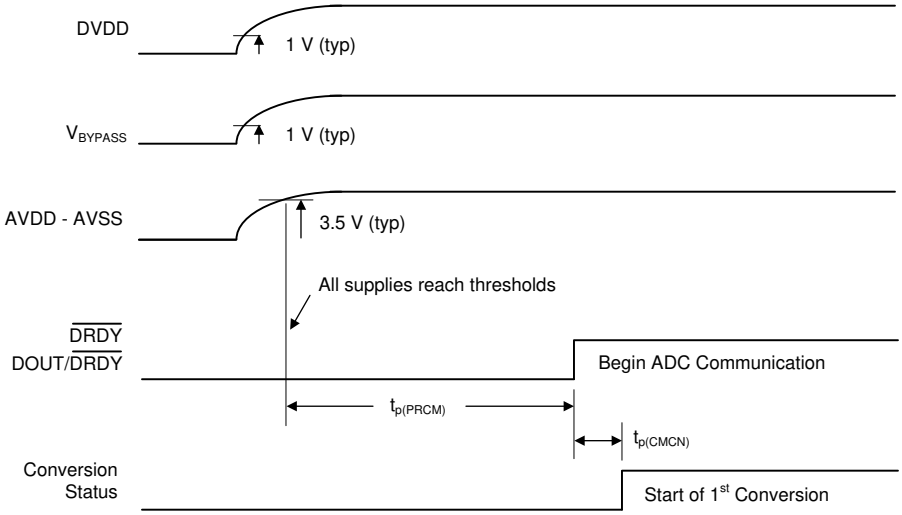


图 4. Power-Up Characteristics

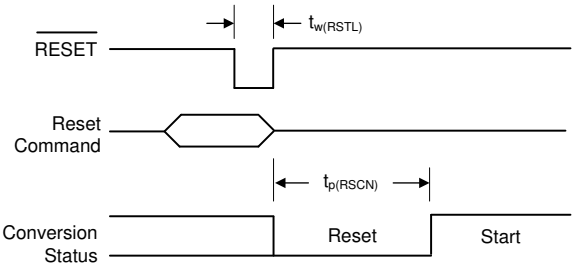
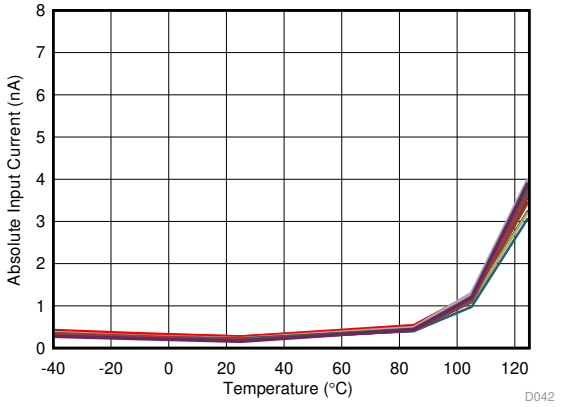


图 5. RESET Pin and Reset Command Timing Requirements

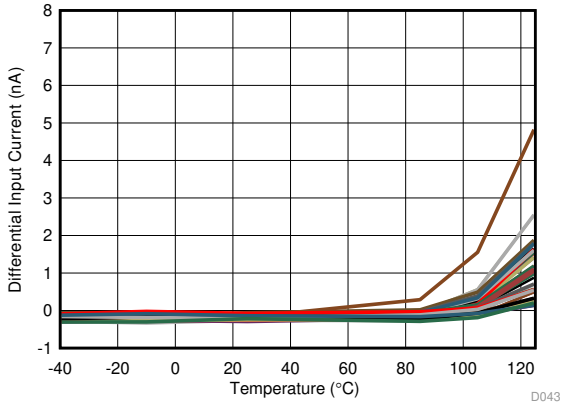
7.8 Typical Characteristics

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



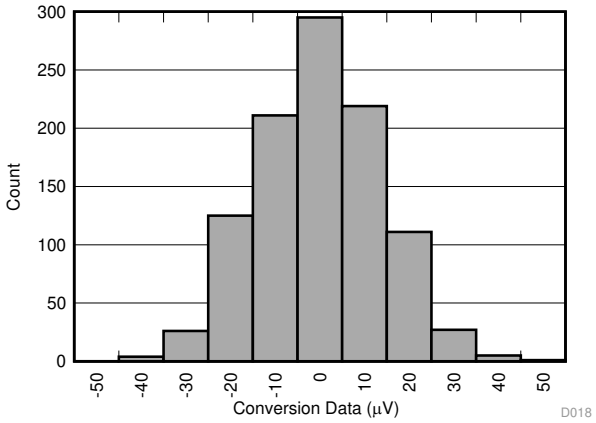
$V_{(AINx)}$ = 0 V

图 6. Absolute Analog Input Current vs Temperature



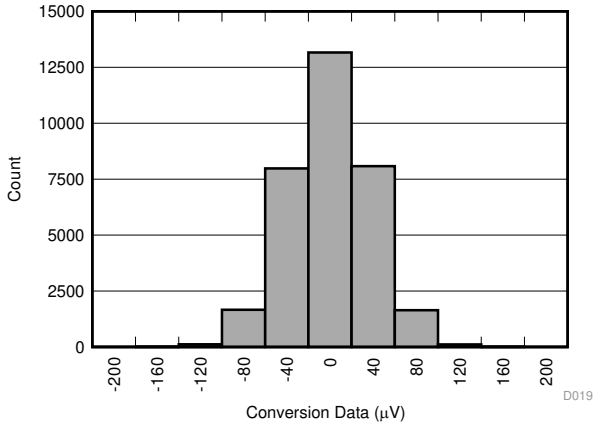
V_{IN} = 2.5 V

图 7. Differential Analog Input Current vs Temperature



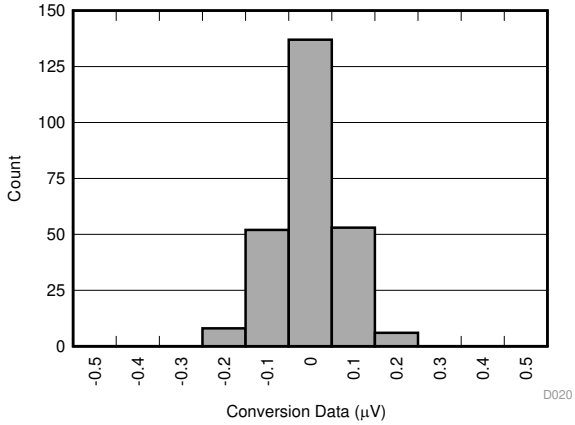
Gain = 0.1875, data rate = 1200 SPS, sinc1 filter, calibrated offset, e_n = 13.6 μV_{RMS}

图 8. Noise Histogram



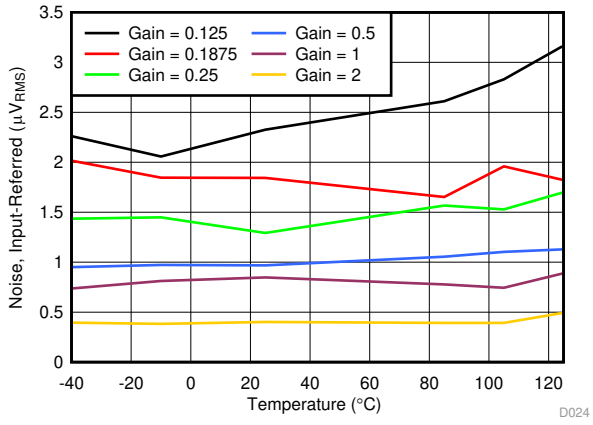
Gain = 1, data rate = 40000 SPS, calibrated offset, e_n = 37 μV_{RMS}

图 9. Noise Histogram



Gain = 32, data rate = 20 SPS, FIR filter, calibrated offset, e_n = 0.076 μV_{RMS}

图 10. Noise Histogram



Gain = 0.125 to 2, data rate = 20 SPS

图 11. Noise vs Temperature

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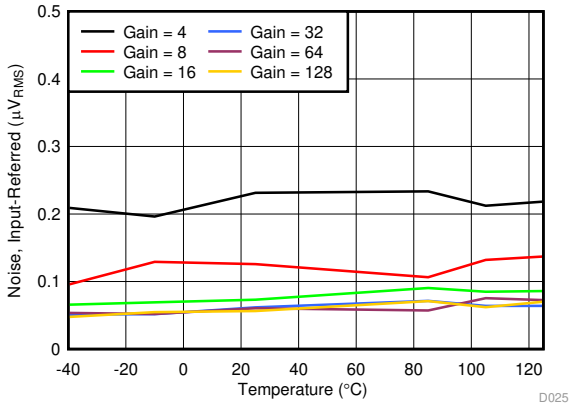
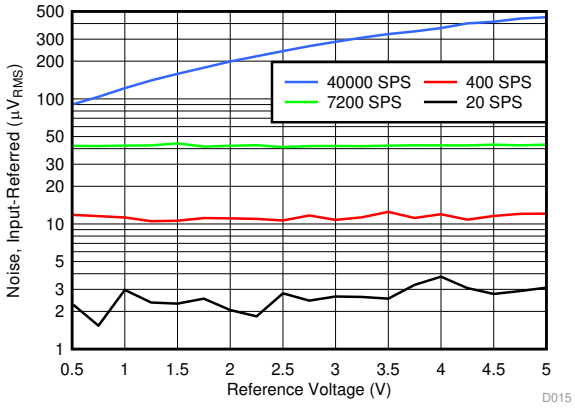
Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



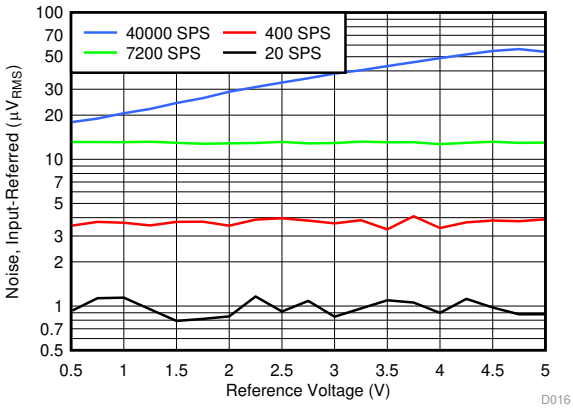
Gain = 4 to 128, data rate = 20 SPS

图 12. Noise vs Temperature



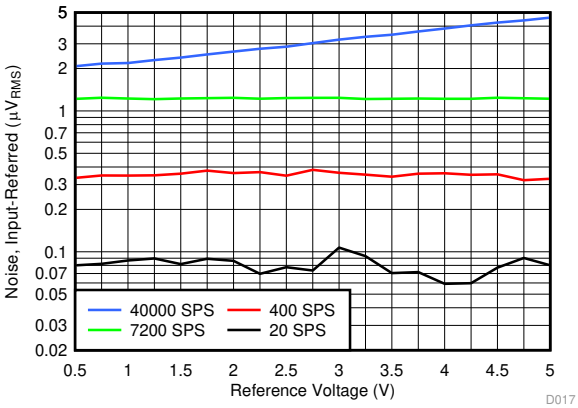
Gain = 0.125

图 13. Noise vs Reference Voltage



Gain = 1

图 14. Noise vs Reference Voltage



Gain = 16

图 15. Noise vs Reference Voltage

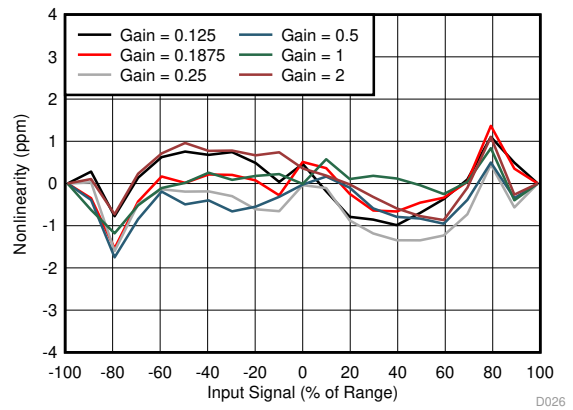


图 16. Nonlinearity vs Input Signal

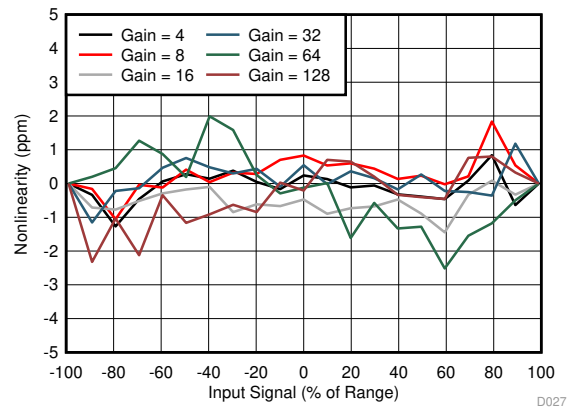


图 17. Nonlinearity vs Input Signal

Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

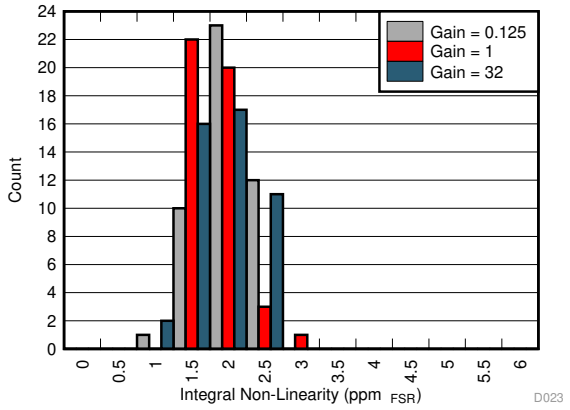


图 18. Integral Nonlinearity Distribution

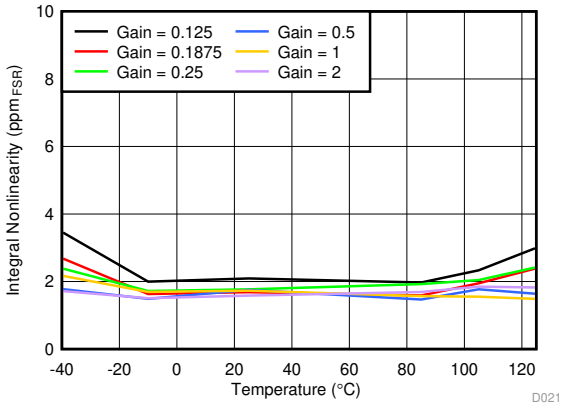


图 19. Integral Nonlinearity vs Temperature

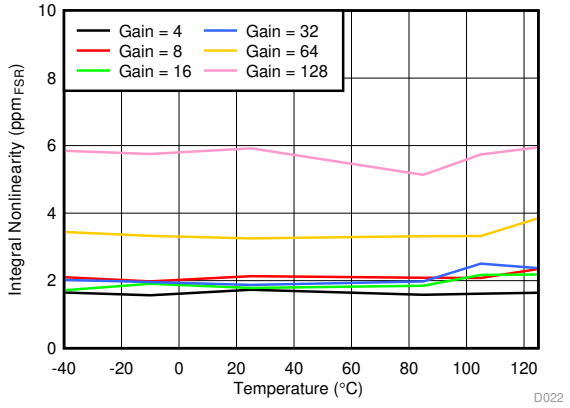
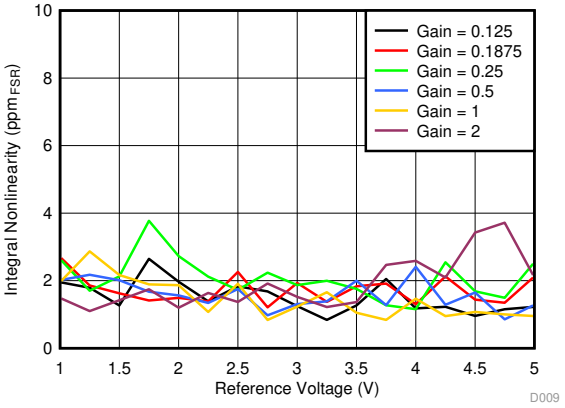
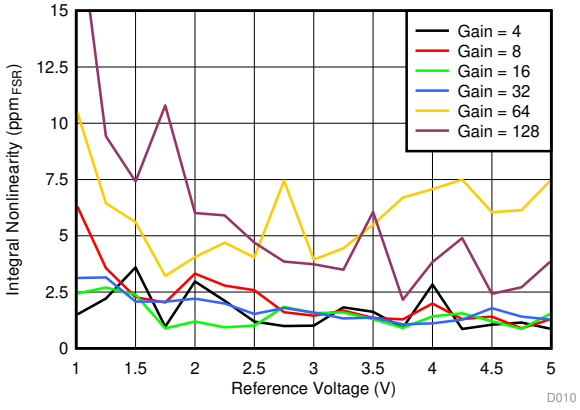


图 20. Integral Nonlinearity vs Temperature



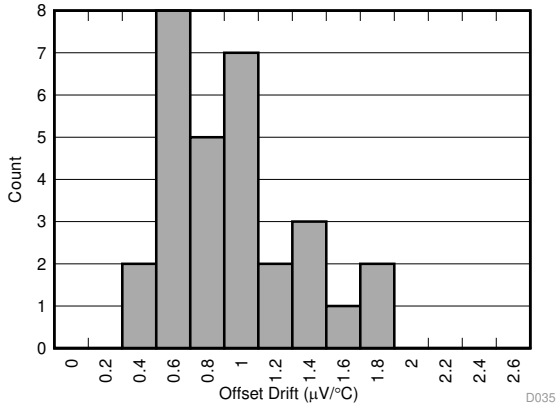
Input range limited to: ±4 V / Gain when V_{REF} > 4 V

图 21. Integral Nonlinearity vs Reference Voltage



Input range limited to: ±4 V / Gain when V_{REF} > 4 V

图 22. Integral Nonlinearity vs Reference Voltage



Gain = 0.125

图 23. Offset Voltage Drift Distribution

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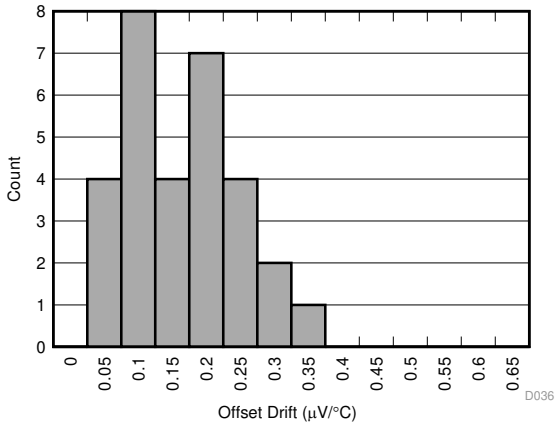
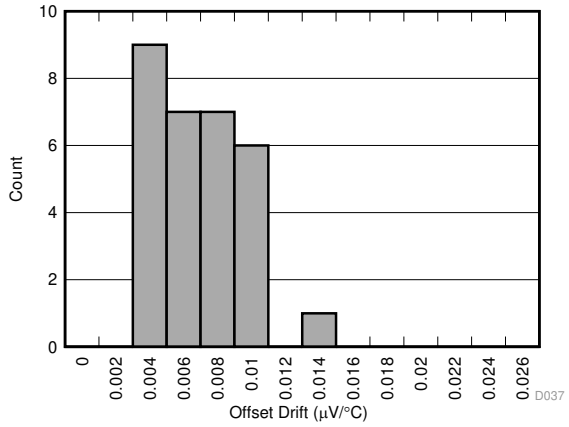
Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



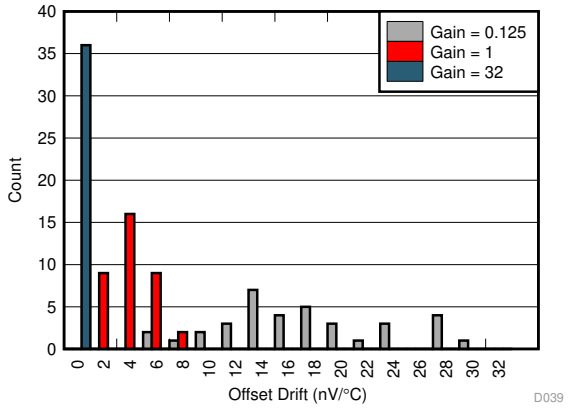
Gain = 1

图 24. Offset Voltage Drift Distribution



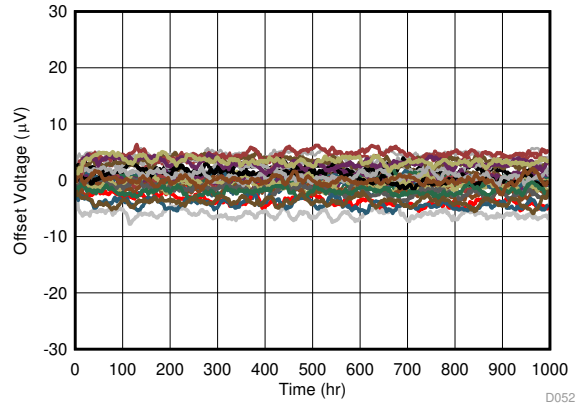
Gain = 32

图 25. Offset Voltage Drift Distribution



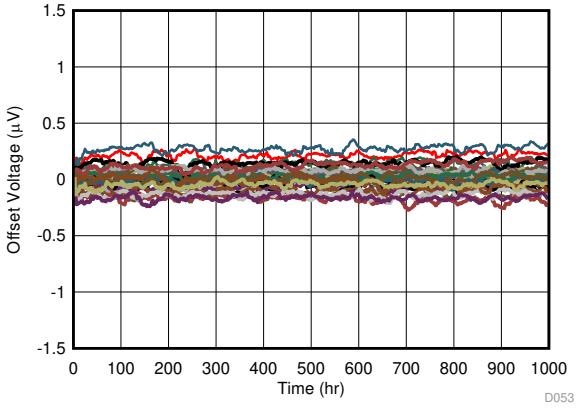
Auto-zero mode

图 26. Offset Voltage Drift Distribution



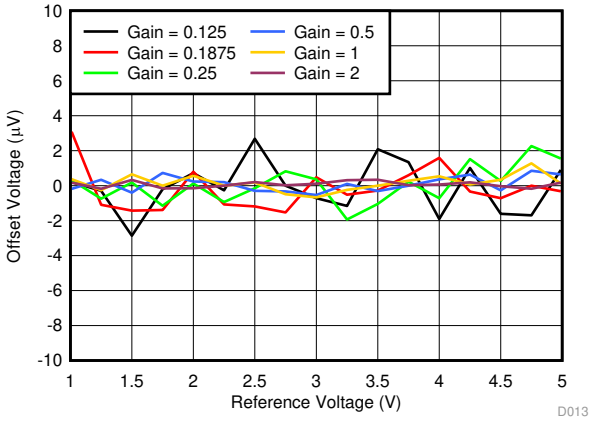
32 units, gain = 0.1875, after calibration

图 27. Offset Voltage Long-Term Drift



32 units, gain = 32, after calibration

图 28. Offset Voltage Long-Term Drift

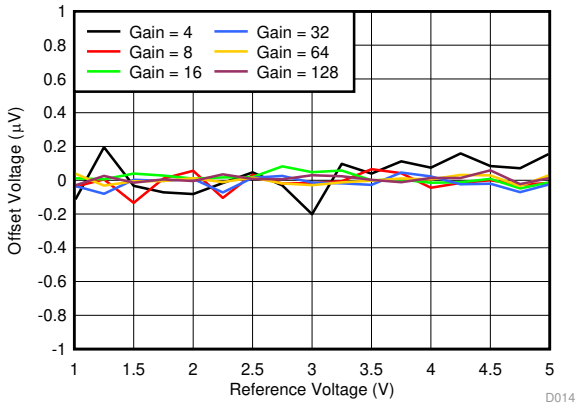


Gain = 0.125 to 2, after calibration

图 29. Offset Voltage vs Reference Voltage

Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



Gain = 4 to 128, after calibration

图 30. Offset Voltage vs Reference Voltage

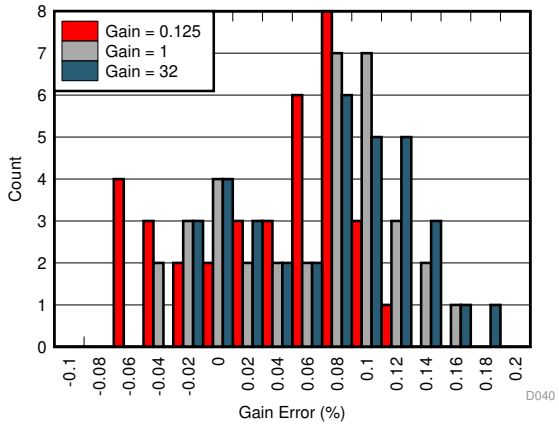


图 31. Gain Error Distribution

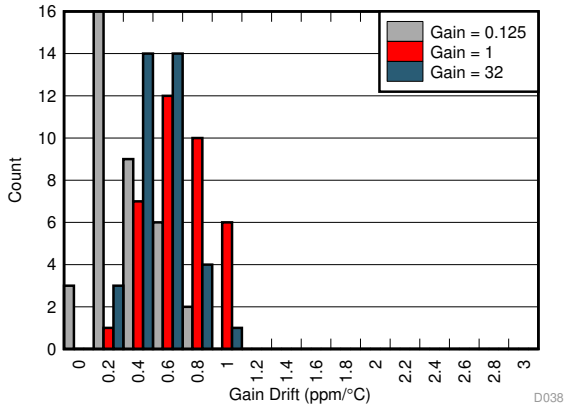
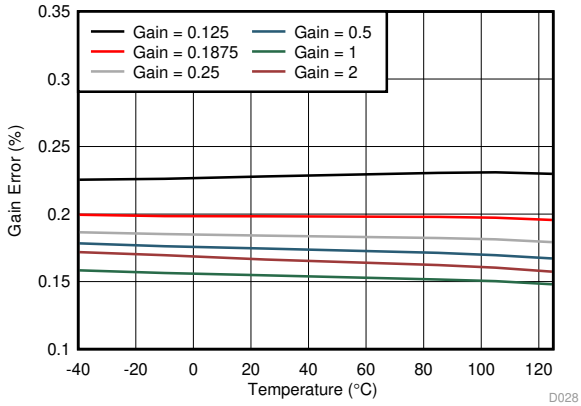
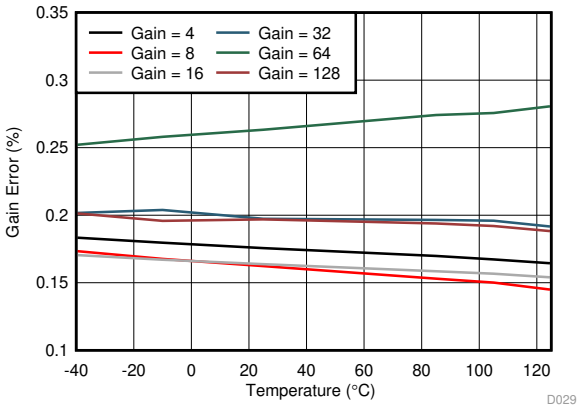


图 32. Gain Drift Distribution



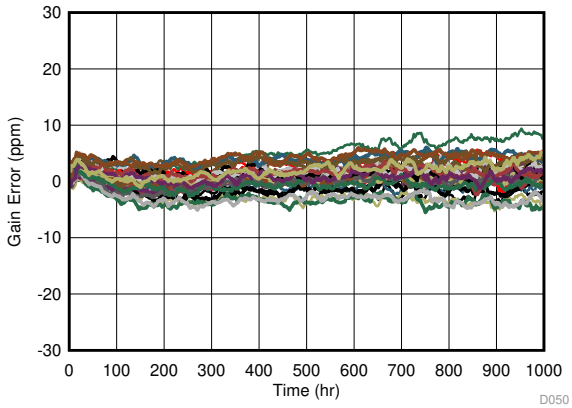
Gain = 0.125 to 2

图 33. Gain Error vs Temperature



Gain = 4 to 128

图 34. Gain Error vs Temperature



32 units, gain = 0.1875, after calibration

图 35. Gain Long-Term Drift

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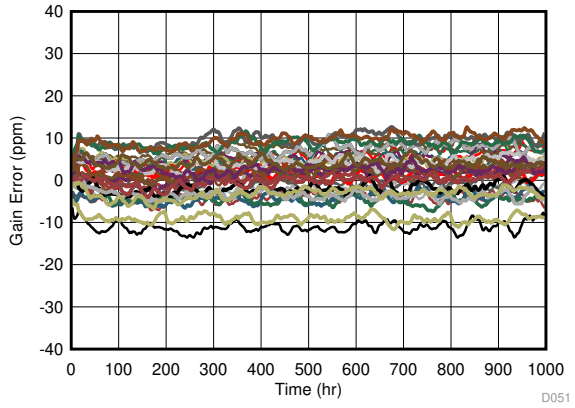
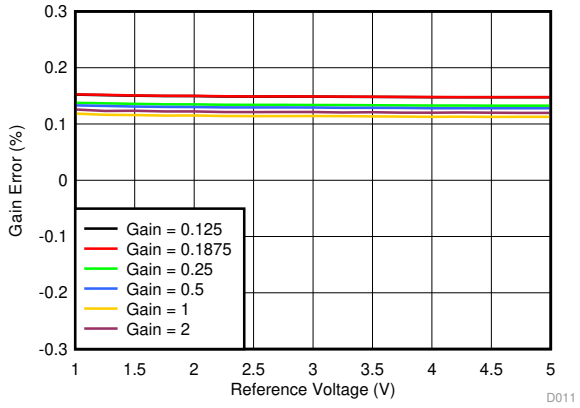
Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



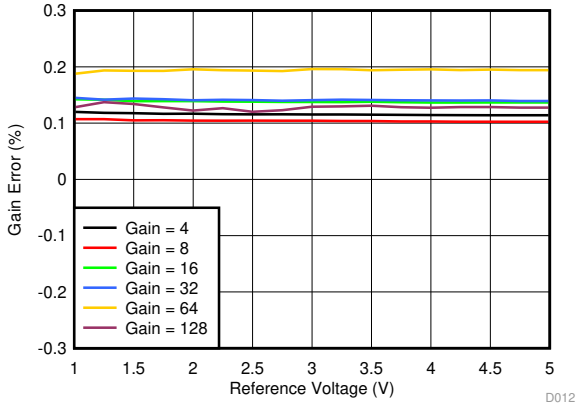
32 units, gain = 32, after calibration

图 36. Gain Long-Term Drift



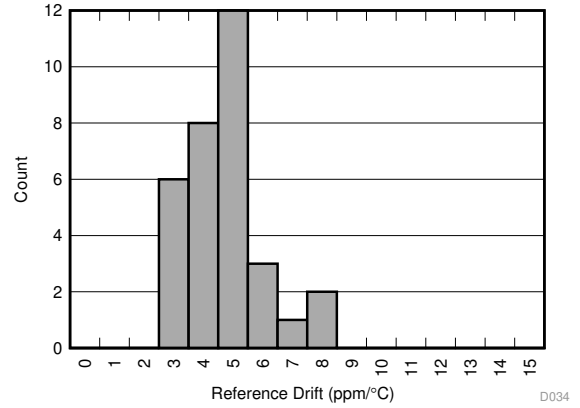
Measurement input range limited to: ±4 V / Gain when V_{REF} > 4 V

图 37. Gain Error vs Reference Voltage



Measurement input range limited to: ±4 V / Gain when V_{REF} > 4 V

图 38. Gain Error vs Reference Voltage



T_A = –40°C to +125°C

图 39. Internal Reference Voltage Drift Distribution

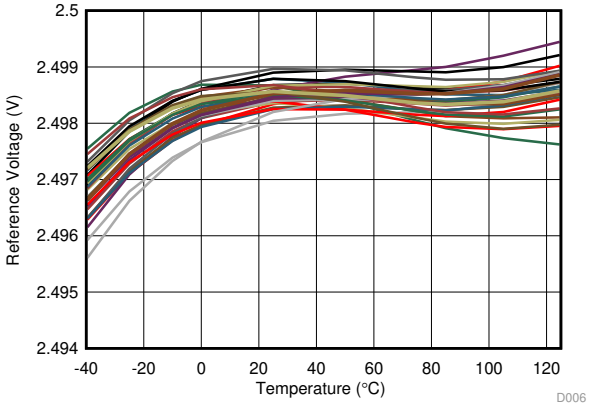
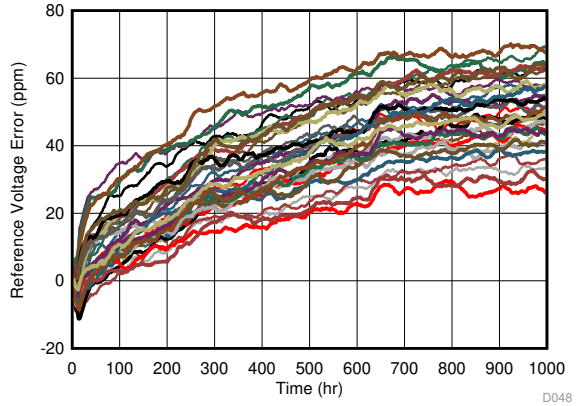


图 40. Internal Reference Voltage vs Temperature



32 units, normalized data

图 41. Internal Reference Voltage Long-Term Drift

Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

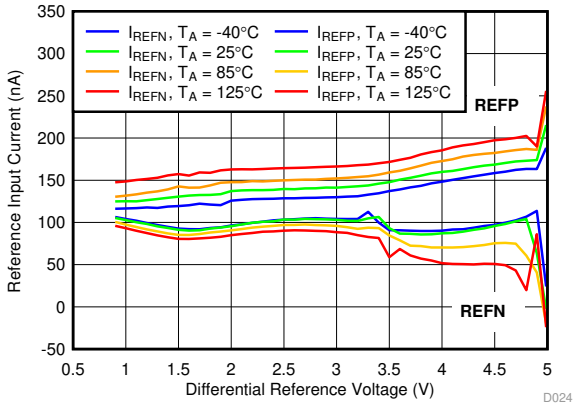


图 42. Reference Input Current vs Reference Voltage

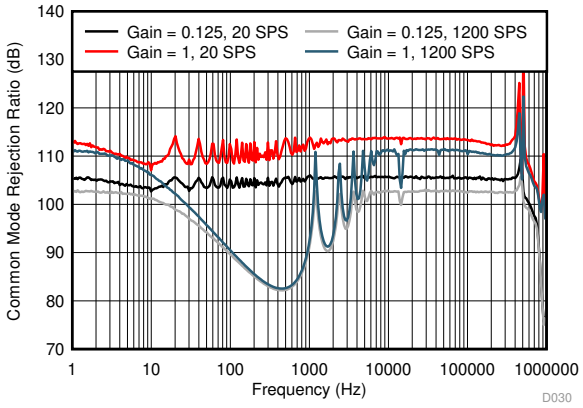
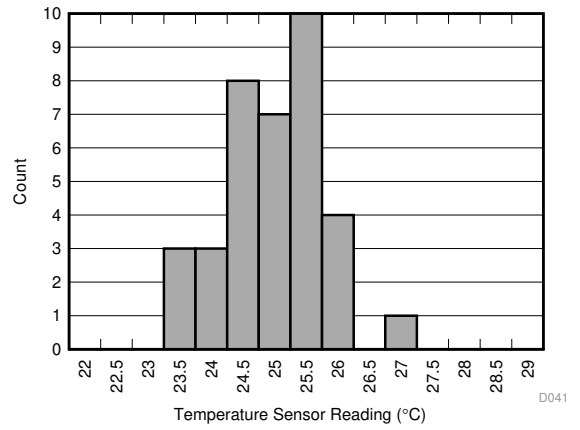
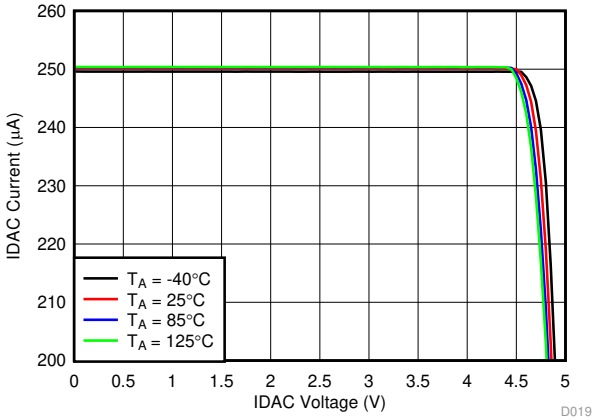


图 43. Common-Mode Rejection Ratio vs Frequency



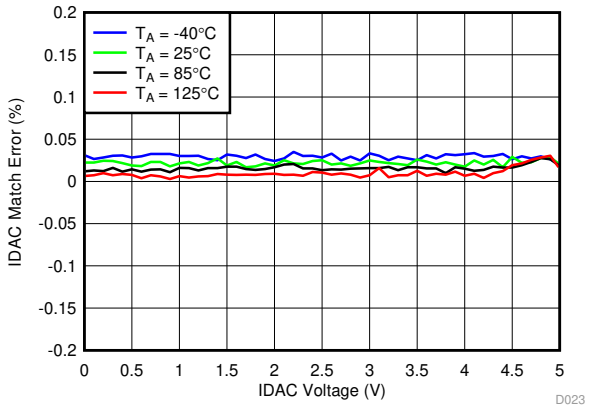
T_A = 25°C

图 44. Temperature Sensor Reading Distribution



IDAC = 250 µA

图 45. IDAC Current vs IDAC Voltage



IDAC = 250 µA

图 46. IDAC Match Error vs IDAC Voltage

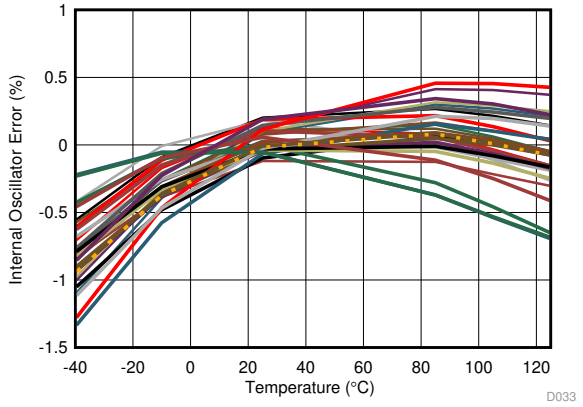


图 47. Oscillator Frequency Error vs Temperature

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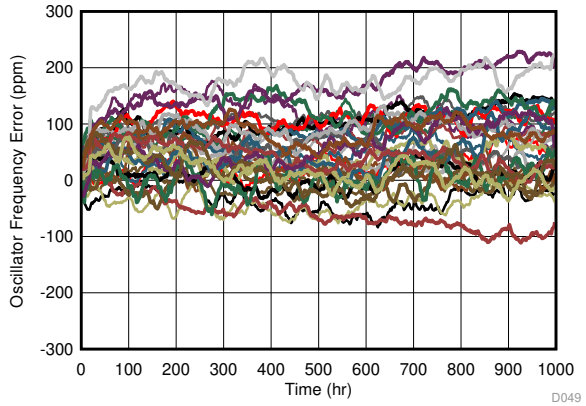
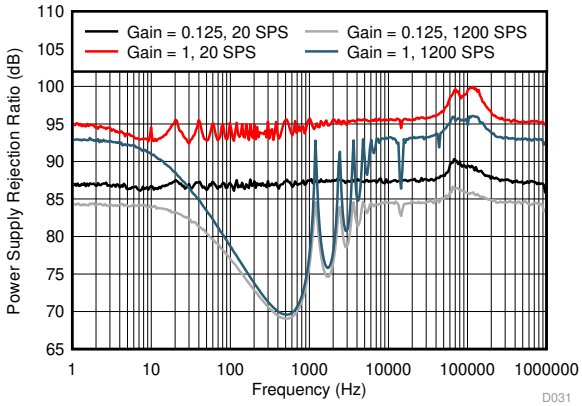
Typical Characteristics (接下页)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



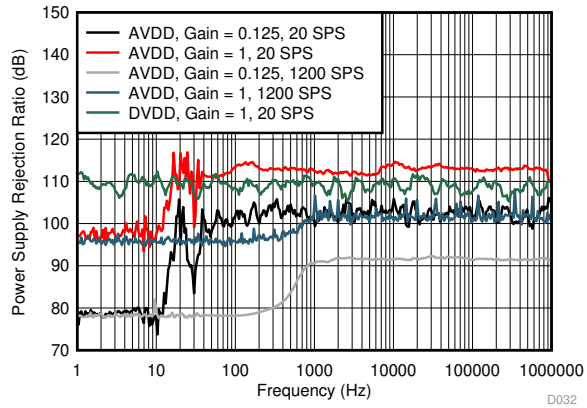
32 units, normalized data

图 48. Oscillator Frequency Long-Term Drift



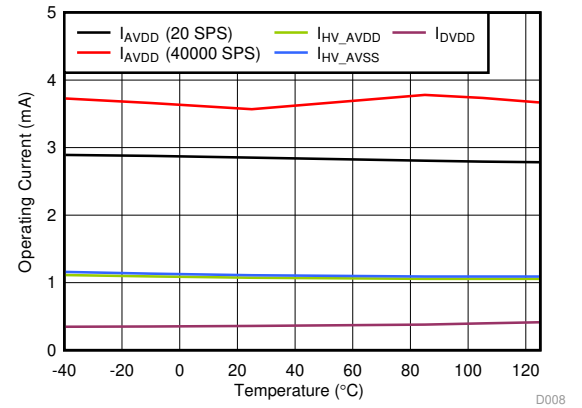
HV_AVDD and HV_AVSS

图 49. PSRR vs Frequency



AVDD and DVDD

图 50. PSRR vs Frequency



All gains

图 51. Operating Current vs Temperature

8 Parameter Measurement Information

8.1 Noise Performance

Noise performance depends on the device configuration: data rate, input gain, digital filter mode, and auto-zero mode. Two significant factors affecting noise performance are data rate and input gain. Decreasing the data rate lowers the noise because the bandwidth is reduced over the fixed noise profile of the ADC. Increasing the gain reduces noise (when noise is treated as an input-referred quantity) because the noise of the PGA is lower than that of the ADC. Noise performance also depends on the digital filter and auto-zero mode. As the digital filter order increases, the bandwidth decreases, which results in lower noise. As a result of two-point data averaging in auto-zero mode, noise performance improves by $\sqrt{2}$ compared to the normal operating mode.

表 1 lists the noise data of gain equal to 0.125 to 2 (corresponding input ranges of ±20 V to ±1.25 V) as input-referred values. 表 2 lists the noise data of gain equal to 4 to 128 (corresponding input ranges of ±625 mV to ±19.5 mV). The noise data are in units of μV_{RMS} (RMS = root mean square) under the conditions listed. Values in parenthesis are peak-to-peak (μV_{pp}).

The noise data represent typical ADC performance at T_A = 25°C, 2.5-V reference voltage, and auto-zero mode disabled. The noise data are the standard deviation and peak-to-peak computations of the ADC data. The data are acquired with inputs shorted, based on consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first. Because of the statistical nature of noise, repeated measurements may yield higher or lower noise results. Similarly, longer periods of data acquisition may result in higher peak-to-peak noise results.

表 1. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}), Gain = 0.125 to 2, V_{REF} = 2.5 V

DATA RATE (SPS)	FILTER MODE	GAIN (Full-Scale Range)					
		0.125 (±20 V)	0.1875 (±13.3 V)	0.25 (±10 V)	0.5 (±5 V)	1 (±2.5 V)	2 (±1.25 V)
2.5	FIR	1.3 (4.8)	0.89 (3.6)	0.69 (2.1)	0.49 (1.9)	0.37 (1.5)	0.17 (0.67)
2.5	Sinc1	1.1 (4.2)	0.6 (2.4)	0.57 (2.4)	0.39 (1.5)	0.29 (1)	0.15 (0.63)
2.5	Sinc2	1 (3.6)	0.68 (2)	0.44 (1.8)	0.32 (1)	0.26 (0.97)	0.12 (0.52)
2.5	Sinc3	1.1 (3)	0.67 (2)	0.49 (1.5)	0.32 (1)	0.24 (0.89)	0.11 (0.41)
2.5	Sinc4	0.98 (3.6)	0.64 (2)	0.48 (1.2)	0.3 (1)	0.26 (0.97)	0.11 (0.41)
5	FIR	1.7 (6.6)	1.2 (4.8)	0.93 (4.2)	0.57 (2.5)	0.45 (2)	0.24 (1.2)
5	Sinc1	1.5 (6.6)	0.98 (3.6)	0.77 (3.6)	0.53 (2.2)	0.4 (1.9)	0.2 (0.93)
5	Sinc2	1.3 (4.8)	0.91 (4)	0.68 (2.4)	0.44 (1.8)	0.35 (1.6)	0.18 (0.82)
5	Sinc3	1.2 (4.8)	0.83 (3.2)	0.62 (2.4)	0.39 (1.6)	0.3 (1.3)	0.16 (0.75)
5	Sinc4	1.2 (3.6)	0.75 (3.2)	0.54 (2.1)	0.38 (1.5)	0.27 (1.2)	0.14 (0.56)
10	FIR	2.4 (11)	1.6 (7.9)	1.2 (5.7)	0.82 (4.3)	0.69 (3.3)	0.34 (1.7)
10	Sinc1	1.9 (9.5)	1.4 (6.8)	1.1 (5.4)	0.7 (3.4)	0.55 (2.7)	0.3 (1.5)
10	Sinc2	1.7 (8.9)	1.2 (5.6)	0.9 (4.5)	0.56 (2.7)	0.47 (2.3)	0.24 (1.2)
10	Sinc3	1.5 (6.6)	1.1 (5.2)	0.89 (4.2)	0.54 (2.7)	0.46 (2.5)	0.24 (1.1)
10	Sinc4	1.5 (6.6)	0.99 (4.4)	0.79 (3.6)	0.49 (2.4)	0.39 (1.9)	0.2 (1)
16.6	Sinc1	2.6 (11)	1.7 (8.7)	1.4 (6.6)	0.87 (4.5)	0.72 (3.5)	0.37 (2)
16.6	Sinc2	2.1 (10)	1.5 (7.5)	1.1 (5.7)	0.78 (3.7)	0.62 (3.2)	0.32 (1.6)
16.6	Sinc3	1.9 (9.5)	1.4 (7.2)	1.1 (5.1)	0.72 (3.6)	0.54 (2.5)	0.27 (1.3)
16.6	Sinc4	1.8 (7.7)	1.3 (6.4)	0.97 (4.8)	0.65 (3.1)	0.48 (2.5)	0.24 (1.2)
20	FIR	3 (15)	2.1 (11)	1.8 (8.6)	1.1 (5.2)	0.89 (4.8)	0.46 (2.6)
20	Sinc1	2.7 (13)	1.9 (9.5)	1.5 (7.5)	0.97 (5.5)	0.76 (4.2)	0.43 (2.3)
20	Sinc2	2.2 (11)	1.5 (7.2)	1.3 (6)	0.83 (4.2)	0.69 (3.7)	0.35 (1.8)
20	Sinc3	2.1 (10)	1.6 (8.3)	1.2 (5.4)	0.77 (4)	0.64 (3.1)	0.31 (1.6)
20	Sinc4	2 (9.5)	1.3 (6.8)	1.1 (4.8)	0.65 (3.1)	0.56 (2.7)	0.28 (1.4)
50	Sinc1	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (7.7)	1.2 (7.5)	0.64 (3.7)
50	Sinc2	3.2 (18)	2.3 (12)	1.9 (11)	1.3 (7)	1.1 (5.8)	0.54 (3.1)
50	Sinc3	3.3 (18)	2.2 (13)	1.8 (9.2)	1.2 (6.7)	0.93 (5.3)	0.49 (3)
50	Sinc4	3.1 (17)	2 (11)	1.6 (8.3)	1 (5.8)	0.87 (4.7)	0.43 (2.4)
60	Sinc1	4.5 (27)	3.1 (17)	2.4 (13)	1.6 (9.2)	1.4 (8.3)	0.69 (3.8)

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Noise Performance (接下页)

表 1. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}), Gain = 0.125 to 2, V_{REF} = 2.5 V (接下页)

DATA RATE (SPS)	FILTER MODE	GAIN (Full-Scale Range)					
		0.125 (±20 V)	0.1875 (±13.3 V)	0.25 (±10 V)	0.5 (±5 V)	1 (±2.5 V)	2 (±1.25 V)
60	Sinc2	3.8 (23)	2.6 (14)	2.1 (11)	1.4 (7.3)	1.2 (5.9)	0.57 (3.1)
60	Sinc3	3.4 (19)	2.3 (13)	1.8 (9.2)	1.3 (6.9)	1 (5.4)	0.54 (3.1)
60	Sinc4	3.3 (18)	2.1 (12)	1.9 (9.8)	1.2 (6.6)	0.95 (5.2)	0.52 (2.8)
100	Sinc1	5.6 (34)	4.1 (23)	3.3 (20)	2.1 (12)	1.8 (9.7)	0.91 (5.7)
100	Sinc2	4.9 (30)	3.4 (21)	2.7 (16)	1.8 (11)	1.5 (8.7)	0.75 (4.4)
100	Sinc3	4.4 (26)	3.1 (18)	2.5 (14)	1.7 (10)	1.3 (8.2)	0.69 (4.2)
100	Sinc4	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (8.5)	1.3 (7.7)	0.63 (4)
400	Sinc1	12 (74)	8.1 (55)	6.4 (43)	4.3 (27)	3.6 (25)	1.8 (11)
400	Sinc2	9.3 (60)	6.7 (44)	5.3 (32)	3.5 (23)	2.9 (19)	1.5 (10)
400	Sinc3	8.6 (54)	6.2 (39)	4.9 (32)	3.2 (20)	2.7 (17)	1.4 (9.1)
400	Sinc4	8 (52)	5.6 (37)	4.5 (30)	3 (20)	2.5 (16)	1.3 (8.3)
1200	Sinc1	20 (140)	14 (98)	11 (75)	7.3 (48)	6 (40)	3.1 (20)
1200	Sinc2	17 (110)	12 (78)	9.2 (62)	6.1 (41)	5 (33)	2.6 (18)
1200	Sinc3	15 (100)	11 (72)	8.4 (56)	5.6 (37)	4.6 (31)	2.4 (16)
1200	Sinc4	14 (95)	9.9 (68)	7.8 (51)	5.2 (37)	4.3 (29)	2.2 (15)
2400	Sinc1	27 (200)	19 (140)	15 (110)	10 (72)	8.3 (60)	4.2 (30)
2400	Sinc2	23 (180)	16 (120)	13 (97)	8.7 (62)	7 (53)	3.6 (26)
2400	Sinc3	21 (160)	15 (110)	12 (94)	7.9 (59)	6.5 (50)	3.3 (23)
2400	Sinc4	20 (140)	14 (100)	11 (78)	7.3 (53)	6 (43)	3.1 (22)
4800	Sinc1	37 (270)	26 (200)	21 (160)	14 (110)	11 (83)	5.6 (42)
4800	Sinc2	33 (250)	23 (170)	18 (140)	12 (88)	9.8 (73)	5 (40)
4800	Sinc3	31 (230)	21 (150)	17 (130)	11 (83)	9 (65)	4.7 (36)
4800	Sinc4	29 (220)	20 (150)	16 (120)	11 (81)	8.5 (63)	4.4 (33)
7200	Sinc1	44 (330)	31 (230)	24 (180)	16 (120)	13 (98)	6.5 (48)
7200	Sinc2	39 (300)	28 (210)	22 (170)	14 (100)	12 (90)	5.9 (46)
7200	Sinc3	37 (280)	26 (200)	21 (160)	13 (100)	11 (82)	5.5 (41)
7200	Sinc4	35 (260)	25 (180)	20 (150)	13 (95)	10 (81)	5.3 (41)
14400	Sinc5	53 (430)	36 (290)	29 (220)	18 (140)	14 (120)	7.4 (58)
19200	Sinc5	72 (560)	50 (390)	39 (320)	23 (180)	17 (130)	8.8 (71)
25600	Sinc5	150 (1300)	100 (870)	79 (640)	42 (350)	26 (220)	13 (110)
40000	Sinc5	250 (2000)	160 (1300)	120 (1000)	65 (530)	37 (310)	19 (150)

表 2. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}), Gain = 4 to 128, V_{REF} = 2.5 V

DATA RATE (SPS)	FILTER MODE	GAIN (Full-Scale Range)					
		4 (±625 mV)	8 (±312 mV)	16 (±156 mV)	32 (±78.1 mV)	64 (±39.1 mV)	128 (±19.5 mV)
2.5	FIR	0.082 (0.35)	0.051 (0.2)	0.032 (0.14)	0.027 (0.11)	0.027 (0.1)	0.029 (0.12)
2.5	Sinc1	0.088 (0.35)	0.05 (0.19)	0.024 (0.089)	0.024 (0.089)	0.023 (0.098)	0.024 (0.1)
2.5	Sinc2	0.059 (0.24)	0.037 (0.14)	0.021 (0.084)	0.018 (0.072)	0.017 (0.076)	0.019 (0.076)
2.5	Sinc3	0.06 (0.24)	0.034 (0.13)	0.019 (0.075)	0.017 (0.07)	0.016 (0.073)	0.018 (0.075)
2.5	Sinc4	0.054 (0.19)	0.034 (0.13)	0.019 (0.075)	0.016 (0.065)	0.015 (0.062)	0.016 (0.069)
5	FIR	0.12 (0.52)	0.071 (0.33)	0.046 (0.21)	0.038 (0.19)	0.039 (0.17)	0.037 (0.18)
5	Sinc1	0.11 (0.48)	0.061 (0.28)	0.038 (0.18)	0.029 (0.14)	0.029 (0.15)	0.029 (0.13)
5	Sinc2	0.093 (0.43)	0.048 (0.21)	0.029 (0.14)	0.024 (0.11)	0.026 (0.12)	0.023 (0.1)
5	Sinc3	0.081 (0.41)	0.044 (0.2)	0.03 (0.13)	0.023 (0.1)	0.022 (0.1)	0.022 (0.11)
5	Sinc4	0.066 (0.3)	0.043 (0.2)	0.027 (0.13)	0.022 (0.093)	0.022 (0.11)	0.021 (0.096)
10	FIR	0.19 (1)	0.099 (0.51)	0.064 (0.36)	0.053 (0.29)	0.051 (0.3)	0.054 (0.3)
10	Sinc1	0.16 (0.82)	0.086 (0.46)	0.054 (0.3)	0.045 (0.22)	0.043 (0.21)	0.044 (0.23)
10	Sinc2	0.12 (0.56)	0.068 (0.36)	0.044 (0.23)	0.037 (0.2)	0.034 (0.18)	0.033 (0.18)

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表 2. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}), Gain = 4 to 128, V_{REF} = 2.5 V (接下页)

DATA RATE (SPS)	FILTER MODE	GAIN (Full-Scale Range)					
		4 (±625 mV)	8 (±312 mV)	16 (±156 mV)	32 (±78.1 mV)	64 (±39.1 mV)	128 (±19.5 mV)
10	Sinc3	0.11 (0.52)	0.066 (0.31)	0.042 (0.21)	0.032 (0.17)	0.032 (0.16)	0.032 (0.16)
10	Sinc4	0.096 (0.45)	0.059 (0.31)	0.039 (0.2)	0.032 (0.17)	0.031 (0.16)	0.03 (0.15)
16.6	Sinc1	0.19 (1)	0.11 (0.56)	0.075 (0.38)	0.054 (0.3)	0.055 (0.29)	0.056 (0.31)
16.6	Sinc2	0.16 (0.89)	0.086 (0.4)	0.054 (0.27)	0.044 (0.22)	0.049 (0.24)	0.046 (0.24)
16.6	Sinc3	0.15 (0.73)	0.084 (0.41)	0.053 (0.27)	0.041 (0.22)	0.04 (0.22)	0.041 (0.2)
16.6	Sinc4	0.13 (0.67)	0.076 (0.39)	0.053 (0.29)	0.042 (0.24)	0.04 (0.21)	0.036 (0.17)
20	FIR	0.24 (1.2)	0.14 (0.72)	0.088 (0.45)	0.072 (0.38)	0.071 (0.37)	0.074 (0.37)
20	Sinc1	0.22 (1.1)	0.12 (0.58)	0.079 (0.41)	0.064 (0.32)	0.061 (0.32)	0.06 (0.34)
20	Sinc2	0.18 (1)	0.1 (0.57)	0.062 (0.34)	0.049 (0.25)	0.049 (0.26)	0.047 (0.29)
20	Sinc3	0.16 (0.89)	0.089 (0.48)	0.063 (0.32)	0.046 (0.22)	0.045 (0.21)	0.045 (0.23)
20	Sinc4	0.15 (0.82)	0.083 (0.41)	0.056 (0.29)	0.045 (0.23)	0.042 (0.22)	0.046 (0.24)
50	Sinc1	0.35 (2.1)	0.19 (1.1)	0.12 (0.69)	0.097 (0.52)	0.096 (0.57)	0.098 (0.58)
50	Sinc2	0.28 (1.6)	0.15 (0.84)	0.099 (0.56)	0.075 (0.43)	0.077 (0.43)	0.076 (0.46)
50	Sinc3	0.25 (1.5)	0.14 (0.75)	0.093 (0.51)	0.074 (0.41)	0.07 (0.38)	0.071 (0.37)
50	Sinc4	0.23 (1.4)	0.13 (0.76)	0.087 (0.47)	0.066 (0.37)	0.065 (0.35)	0.065 (0.37)
60	Sinc1	0.38 (2.2)	0.21 (1.2)	0.14 (0.79)	0.11 (0.57)	0.1 (0.59)	0.1 (0.6)
60	Sinc2	0.3 (1.7)	0.17 (0.93)	0.11 (0.66)	0.085 (0.47)	0.084 (0.49)	0.083 (0.49)
60	Sinc3	0.27 (1.6)	0.15 (0.79)	0.097 (0.53)	0.078 (0.43)	0.078 (0.43)	0.076 (0.42)
60	Sinc4	0.27 (1.6)	0.14 (0.89)	0.092 (0.5)	0.075 (0.46)	0.076 (0.4)	0.073 (0.4)
100	Sinc1	0.49 (2.8)	0.27 (1.5)	0.17 (1)	0.14 (0.81)	0.14 (0.88)	0.13 (0.81)
100	Sinc2	0.39 (2.3)	0.22 (1.4)	0.14 (0.87)	0.11 (0.63)	0.11 (0.69)	0.11 (0.66)
100	Sinc3	0.35 (2.1)	0.2 (1.2)	0.13 (0.75)	0.1 (0.63)	0.1 (0.61)	0.1 (0.69)
100	Sinc4	0.32 (2)	0.18 (1.2)	0.13 (0.73)	0.094 (0.57)	0.092 (0.56)	0.093 (0.57)
400	Sinc1	0.94 (6)	0.53 (3.5)	0.34 (2.1)	0.27 (1.8)	0.27 (1.7)	0.27 (1.8)
400	Sinc2	0.78 (5.2)	0.44 (3.1)	0.29 (1.8)	0.22 (1.4)	0.22 (1.4)	0.22 (1.4)
400	Sinc3	0.72 (4.6)	0.4 (2.6)	0.26 (1.6)	0.2 (1.3)	0.2 (1.3)	0.2 (1.3)
400	Sinc4	0.67 (4.2)	0.37 (2.4)	0.24 (1.6)	0.19 (1.2)	0.19 (1.2)	0.19 (1.1)
1200	Sinc1	1.6 (12)	0.91 (6.3)	0.59 (4.1)	0.46 (3.1)	0.45 (3.1)	0.45 (3.1)
1200	Sinc2	1.3 (9.3)	0.76 (5.2)	0.49 (3.2)	0.39 (2.6)	0.38 (2.6)	0.38 (2.6)
1200	Sinc3	1.2 (8.2)	0.69 (4.7)	0.45 (3.1)	0.35 (2.4)	0.35 (2.4)	0.35 (2.2)
1200	Sinc4	1.2 (7.6)	0.64 (4.3)	0.41 (2.7)	0.33 (2.3)	0.32 (2.2)	0.32 (2.3)
2400	Sinc1	2.2 (17)	1.2 (8.9)	0.81 (5.8)	0.64 (4.5)	0.62 (4.5)	0.62 (4.6)
2400	Sinc2	1.9 (14)	1.1 (7.7)	0.68 (5)	0.54 (3.9)	0.54 (3.9)	0.54 (4)
2400	Sinc3	1.7 (14)	0.97 (7.1)	0.62 (4.4)	0.49 (3.5)	0.48 (3.4)	0.49 (3.5)
2400	Sinc4	1.6 (12)	0.91 (6.7)	0.59 (4.1)	0.46 (3.5)	0.46 (3.4)	0.46 (3.4)
4800	Sinc1	3 (23)	1.6 (13)	1.1 (7.8)	0.83 (6.2)	0.83 (6.2)	0.82 (6.1)
4800	Sinc2	2.6 (20)	1.5 (12)	0.95 (7.2)	0.75 (5.6)	0.74 (5.4)	0.73 (5.5)
4800	Sinc3	2.4 (19)	1.4 (10)	0.89 (6.4)	0.69 (5)	0.68 (5.2)	0.69 (5.5)
4800	Sinc4	2.3 (17)	1.3 (9.8)	0.82 (6.2)	0.64 (5)	0.65 (4.9)	0.64 (4.9)
7200	Sinc1	3.3 (25)	1.9 (15)	1.2 (9)	0.95 (7)	0.94 (6.9)	0.94 (7.1)
7200	Sinc2	3.1 (24)	1.7 (13)	1.1 (8.7)	0.87 (6.6)	0.86 (6.5)	0.86 (6.4)
7200	Sinc3	2.9 (22)	1.6 (12)	1.1 (7.9)	0.83 (6.1)	0.82 (6.2)	0.82 (6.4)
7200	Sinc4	2.8 (21)	1.6 (12)	1 (7.7)	0.79 (5.8)	0.78 (6)	0.78 (5.8)
14400	Sinc5	3.8 (29)	2.1 (17)	1.4 (11)	1.1 (8.4)	1.1 (8.1)	1 (8.4)
19200	Sinc5	4.6 (36)	2.5 (20)	1.6 (13)	1.2 (9.6)	1.2 (9.3)	1.2 (9.5)
25600	Sinc5	6.7 (56)	3.6 (29)	2.1 (17)	1.5 (13)	1.4 (12)	1.4 (12)
40000	Sinc5	9.6 (80)	5 (43)	2.9 (23)	2 (16)	1.8 (15)	1.8 (15)

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ADC noise performance can also be expressed as *effective resolution* and *noise-free resolution (bits)*. The resolution in bits are computed from the measured noise data. Effective resolution is computed from the RMS value of the measured noise data. Noise-free resolution is computed from the peak-to-peak value of the measured noise data, and is therefore the resolution with no code flicker. 公式 1 is used to compute effective resolution (bits) and noise-free resolution (bits) based on the noise values listed in 表 1 and 表 2.

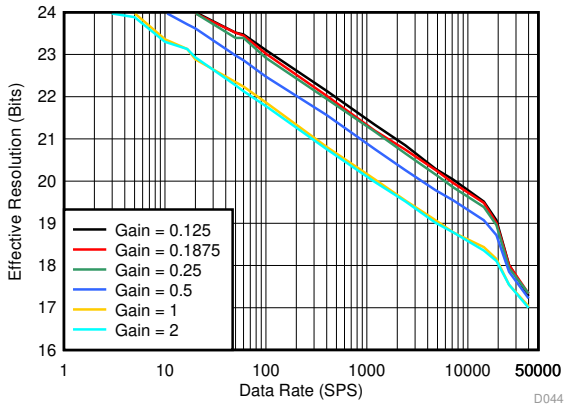
Effective Resolution or Noise-Free Resolution (Bits) = 3.32 log (FSR / e_n)

where:

- FSR = Full-scale range = 2 V_{REF} / Gain
- e_n = Input-referred noise (RMS value for *effective resolution*, peak-to-peak value for *noise-free resolution*) (1)

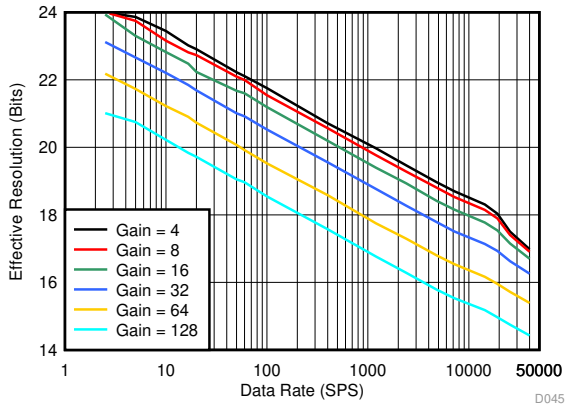
For example, with a full-scale range = ±13.3 V, data rate = 20 SPS, and filter mode = FIR, the RMS noise value (from 表 1) is 2.1 µV. The effective resolution is: 3.32 log (26.6 V / 2.1 µV) = 23.6 bits.

图 52 and 图 53 show effective resolution (bits) using 公式 1. 图 54 and 图 55 show the noise-free resolution (bits) using 公式 1. The data are based on 2.5-V reference operation and the sinc3 filter mode. Effective resolution and noise-free resolution (bits) are improved by increasing the reference voltage (up to 5 V).



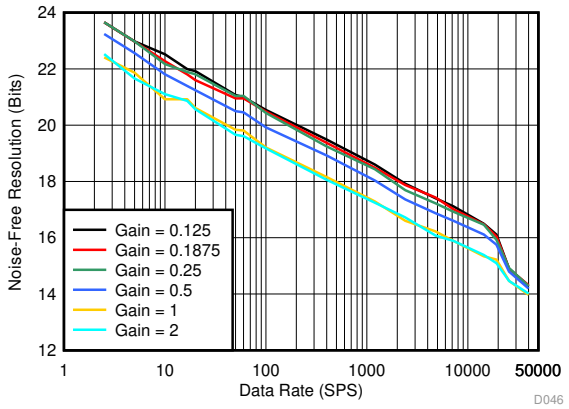
V_{REF} = 2.5 V, sinc3 filter mode

图 52. Effective Resolution, Gain = 0.125 to 2



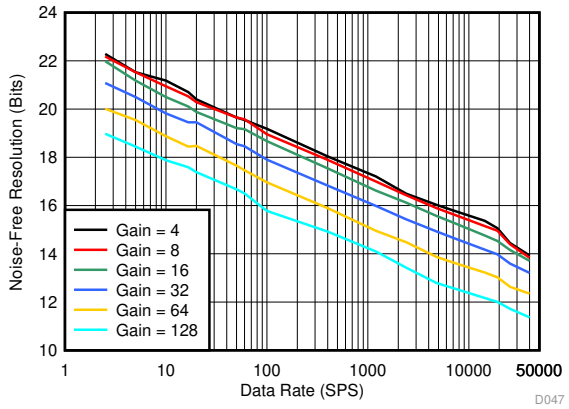
V_{REF} = 2.5 V, sinc3 filter mode

图 53. Effective Resolution, Gain = 4 to 128



V_{REF} = 2.5 V, sinc3 filter mode

图 54. Noise-Free Resolution, Gain = 0.125 to 2



V_{REF} = 2.5 V, sinc3 filter mode

图 55. Noise-Free Resolution, Gain = 4 to 128

9 Detailed Description

9.1 Overview

The ADS125H02 is a ±20-V signal input, 24-bit, 40-kSPS, delta-sigma (ΔΣ) analog-to-digital converter. The device features gain from 0.125 to 128 that program the input voltage range from ±20 V to ±20 mV (V_{REF} = 2.5 V). The inputs are configurable as one differential input or two single-ended inputs. The device includes a low-noise, low-drift PGA with high input impedance, signal monitors to detect overload conditions, and a voltage reference. A temperature sensor is provided to monitor the surrounding temperature.

The ADC provides a compact one-chip measurement solution for a wide range of input voltages, including typical current and voltage inputs to industrial programmable logic controllers (PLCs), such as ±10-V and 4-mA to 20-mA transmitters (using an external shunt resistor). The ADC provides the resolution necessary to interface directly to low-level sensors such as strain-gauge sensors, thermocouples, and resistance temperature detectors (RTDs). Four general-purpose, input/output (GPIO) pins expand the number of measurement channels with the use of an external multiplexer. Two current sources (IDAC1 and IDAC2) are provided for RTD biasing.

In summary, the ADC features:

- 12 selectable gains for input ranges from ±20 mV to ±20 V (differential)
- 1-GΩ input impedance PGA
- 2.5-V voltage reference
- Internal or external reference operation
- Internal or external clock operation
- PGA, voltage reference, and power-supply monitors
- Temperature sensor
- SPI-compatible serial interface with CRC error check
- Two IDACs
- Four GPIOs

Analog inputs (AIN0, AIN1, AINCOM) connect to the input multiplexer (MUX) to select the ADC input channel. The ADC supports one differential or two single-ended input measurement configurations.

The programmable gain amplifier (PGA) follows the input multiplexer. The PGA is a high input impedance, complementary metal oxide semiconductor (CMOS), differential-input and differential-output amplifier. The PGA has gain and attenuation modes to match the signal amplitude requirements. In attenuation mode, the PGA reduces the input voltage to the range of the ADC. In gain mode, the input voltage is amplified to the range of the ADC. The PGA output connects to the CAPP and CAPN pins. The ADC antialias filter is provided by the combination of the internal PGA output resistors and the external capacitor connected to these pins.

The input channel multiplexer and the PGA are powered by the high-voltage power-supply pins (HV_AVDD and HV_AVSS).

The operating state of the PGA are monitored for signal out-of-range conditions. Status bits in the status register indicate the possible PGA out-of-range conditions.

The ΔΣ modulator measures the input voltage relative to the reference voltage to produce a 24-bit conversion result. The input range of the ADC is $\pm V_{REF}$ / Gain, where gain is programable in binary steps from 0.125 to 128.

The ADC reference voltage is either internal (2.5 V) or external. The REFOUT pin is the internal reference voltage output (with respect to the AGND pin). The reference is monitored for out-of-range conditions and the status is reflected in the conversion data STATUS byte. The device provides two pairs of voltage reference input pins (REFP0, REFN0 and REFP1, REFN1).

The digital filter both averages and reduces the data rate of the modulator output to provide the output conversion result. The sinc filter mode of the digital filter provides programmable orders (sinc1 through sinc5) that allow optimization of conversion latency, conversion noise, and line-cycle rejection. The finite impulse response (FIR) filter mode provides no-latency conversion data with simultaneous rejection of 50-Hz and 60-Hz interference for data rates of 20 SPS or less.

User-programmable offset and gain calibration registers correct the conversion data to provide the final conversion result.

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Overview (接下页)

The SPI-compatible serial interface is used to read the conversion data and for ADC configuration and control. Integrity of SPI I/O communication is validated by CRC error checking. The serial interface consists of the following signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/$\overline{DRDY}$ (see the *Chip-Select Pins (CS1 and CS2)* section for details). The dual-function DOUT/$\overline{DRDY}$ pin combines the functions of the serial data output and data-ready indication into one pin. $\overline{DRDY}$ is the data-ready output signal.

The device includes two current sources (IDAC1, IDAC2). The IDACs are powered by the 5-V AVDD power supply. The IDACs provide excitation current to RTDs or other sensors that require constant-current excitation.

The device provides four GPIO pins to control an external signal multiplexer and for general-purpose I/O of 0-V to 5-V logic signals.

The ADC has an internal temperature sensor to monitor the surrounding temperature. The high-voltage power supply is available for readback by the ADC for user diagnostics.

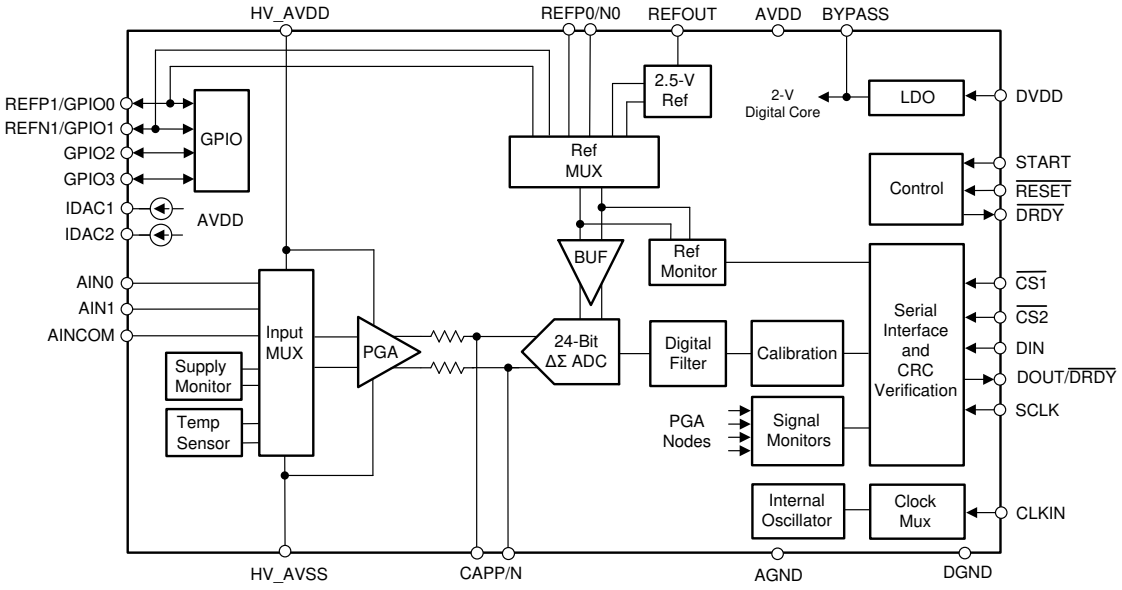
Clock operation is either controlled by the internal oscillator or by an external clock source. The external clock is automatically detected by the ADC. The nominal clock frequency is 7.3728 MHz (10.24 MHz for data rates equal to 40 kSPS).

ADC conversions are controlled by the START pin or by the START command. Conversions are programmable for either continuous mode (gated by START) or one-shot (pulse) conversions.

The ADC auto-resets at power-on, or is manually reset by the $\overline{RESET}$ input or by the RESET command.

The HV_AVDD and HV_AVSS power supplies allow either bipolar or unipolar configuration (bipolar: ±5 V to ±18 V, unipolar: 10 V to 36 V). The digital I/Os are powered by DVDD (3-V to 5-V range). An internal 2-V subregulator powers the ADC digital core for the DVDD supply. An external bypass capacitor is required at the subregulator output (BYPASS pin).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Range

The input range of the ADC (as defined by 公式 2) is determined by the reference voltage and by the PGA gain. 表 3 lists the input range verses gain when operating with a 2.5-V reference voltage. The input range scales with the reference voltage. The maximum input differential signal that can be applied is restricted under certain conditions because of the operating voltage headroom required by the PGA. See the *PGA Operating Range* section for details.

$$\text{Input Range} = \pm V_{REF} / \text{Gain} \quad (2)$$

表 3. ADC Input Range(1)

GAIN[2:0] BITS	GAIN	INPUT RANGE	
		DIFFERENTIAL	SINGLE-ENDED
0000	0.125	±20 V	0 V to ±15.5 V
0001	0.1875	±13.3 V	0 V to ±13.3 V
0010	0.25	±10 V	0 V to ±10 V
0011	0.5	±5 V	0 V to ±5 V
0100	1	±2.5 V	0 V to ±2.5 V
0101	2	±1.25 V	0 V to ±1.25 V
0110	4	±0.625 V	0 V to ±0.625 V
0111	8	±0.312 V	0 V to ±0.312 V
1000	16	±0.156 V	0 V to ±0.156 V
1001	32	±0.0781 V	0 V to ±0.0781 V
1010	64	±0.0391 V	0 V to ±0.0391 V
1011	128	±0.0195 V	0 V to ±0.0195 V

(1) Reference voltage = 2.5 V and HV power supply = ±18 V.

9.3.2 Analog Inputs

As shown in 图 56, the analog inputs of the ADC consist of electrostatic discharge (ESD) protection diodes and an input multiplexer.

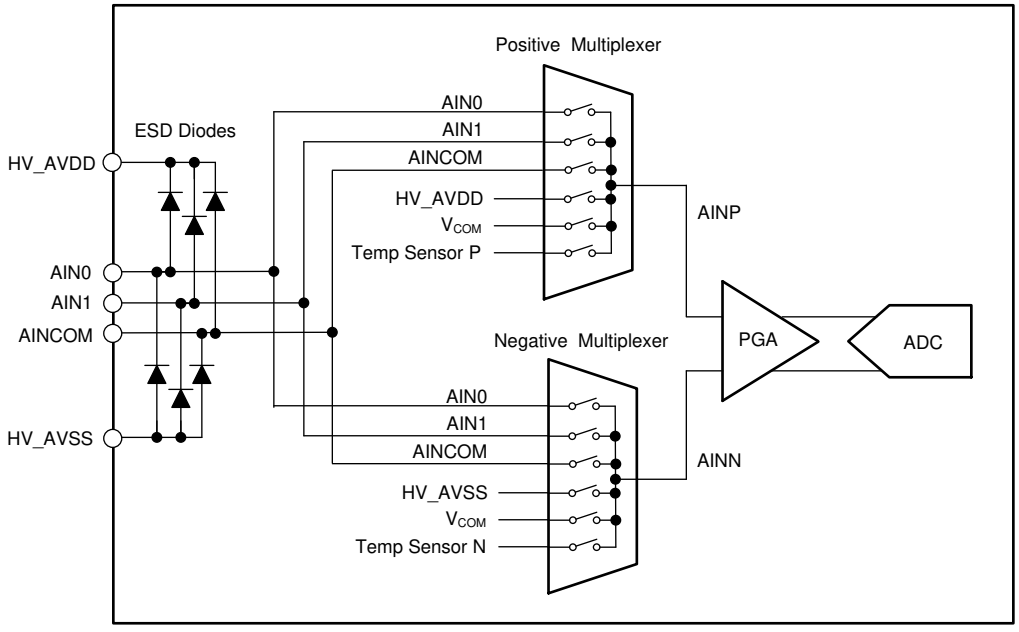


图 56. Analog Input Diagram

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9.3.2.1 ESD Diodes

ESD diodes are incorporated to protect the ADC inputs from possible ESD events occurring during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. For system-level ESD protection, consider the use of external ESD protection devices for pins that are exposed to possible ESD, including the analog inputs.

If an analog input is driven below HV_AVSS – 0.3 V, or above HV_AVDD + 0.3 V, the internal ESD protection diodes can conduct. If this condition is possible, current can flow through the inputs and flow out from the HV_AVDD or HV_AVSS pins. Use external clamp diodes, series resistors, or both to limit the input current to the specified value (see the *PGA Operating Range* section for details).

9.3.2.2 Input Multiplexer

The input multiplexer selects the signal for measurement. The multiplexer is programmed by the MUX[2:0] bits of the MODE4 register (address = 10h). 表 4 lists the input multiplexer settings used to select the signal for measurement.

表 4. Input Multiplexer Settings

MUX[2:0] BITS OF REGISTER MODE4 (10h)	MEASUREMENT (P to N)
000	AIN1 to AIN0
001	AIN0 to AIN1
010	AIN1 to AINCOM
011	AIN0 to AINCOM
100	HV supply: (HV_AVDD – HV_AVSS) / 36
101	V_{COM} voltage: (HV_AVDD + HV_AVSS) / 2 (default)
110	Temperature sensor
111	Reserved

9.3.2.2.1 Analog Inputs (AIN0, AIN1, AINCOM)

The ADC allows one differential input (AIN0 to AIN1, and a reverse polarity connection from AIN1 to AIN0) and two single-ended inputs (AIN0 to AINCOM and AIN1 to AINCOM).

9.3.2.2.2 High-Voltage Power Supply Readback

Read the high-voltage power supply by selecting the voltage with the input multiplexer. The supply voltage is divided by 36 for measurement in order to reduce the voltage to within the PGA input range. 公式 3 shows the supply voltage scaling.

$$\text{High-Voltage Power Supply (V)} = (\text{HV\_AVDD} - \text{HV\_AVSS}) / 36 \quad (3)$$

Measure the high-voltage power supply using the internal or external reference. To measure, set the PGA gain to 1 and disable the auto-zero mode. Write 100b to the MUX[2:0] control bits and then start a new conversion.

9.3.2.2.3 Internal V_{COM} Connection (Default)

In this multiplexer configuration, the external inputs are disconnected and the PGA inputs are shorted to an internal voltage given by: V_{COM} = (HV_AVDD + HV_AVSS) / 2. Use this mode to measure the ADC noise performance and offset voltage, or to short the inputs to perform offset calibration. Be aware that shorting the *external* inputs during calibration yields the best results. Write 101b to the MUX[2:0] control register and start a new conversion to obtain the internal shorted-input reading.

9.3.2.2.4 Temperature Sensor

The ADC has a temperature sensor comprised of two internal diodes with one diode having 80 times the current density of the other. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. To measure the temperature sensor, write 110b to the MUX[2:0] control bits to select the multiplexer for the temperature sensor and then start a new ADC conversion. 公式 4 shows how to convert the temperature sensor reading to degrees Celsius (°C):

$$\text{Temperature (°C)} = [(\text{Temperature Reading (µV)} - 120{,}000) / 390\ \text{µV/°C}] + 25\text{°C} \quad (4)$$

When measuring the temperature sensor, set the gain to 1 and disable auto-zero mode. As a result of the low package-to-PCB thermal resistance, the internal temperature closely tracks the PCB temperature. Be aware that device self-heating increases the internal temperature relative to the surrounding PCB.

9.3.3 Programmable Gain Amplifier (PGA)

The PGA is a low-noise, programmable gain and attenuation, CMOS differential-input, differential-output amplifier. The PGA operates in gain or attenuation mode depending on the gain selected. Typically, the PGA is programmed to provide gain when the expected range of the input signal is less than the reference voltage and is programmed to provide attenuation when the expected range of the input signal is greater than the reference voltage.

图 57 shows the block diagram of the PGA.

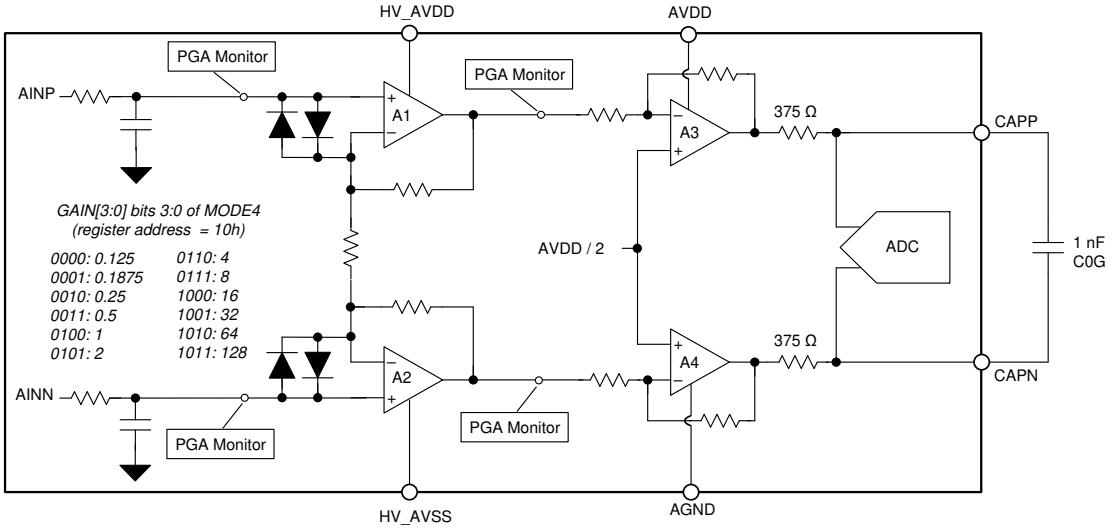

图 57. PGA Block Diagram

The PGA inputs are filtered by an RC network to decrease sensitivity to radio frequency interference (RFI) and electromagnetic interference (EMI) interference. The PGA is comprised of two stages: a gain stage followed by an attenuation stage. The first stage is a high input impedance, noninverting differential amplifier (amplifiers A1 and A2) and provides the PGA gain.

The second stage is an inverting, differential amplifier (amplifiers A3 and A4) and provides the attenuation stage. The second stage provides the PGA attenuation for high-amplitude signals. The common-mode voltage of the differential signal is shifted to AVDD / 2. The second stage drives the modulator input of the ADC and is also connected to the CAPP and CAPN pins. An external 1-nF capacitor filters the modulator input sampling pulses and also provides the antialias filter. Place the capacitor close to the pins using short, direct traces. Avoid running clock traces or other digital traces underneath or in the vicinity of these pins.

Amplifiers A1 and A2 have inverse-parallel-connected protection diodes across the amplifiers inputs to clamp the voltage under signal overrange conditions. When the input is overranged, the diodes may conduct resulting in current flow through the diodes, and subsequently, through the analog input pins. Conditions of high dV/dt input signals, such as those generated by the switching of a signal multiplexer, can lead to transient turn-on of the clamp diodes. Use an RC filter at the PGA inputs to limit the dV/dt of the signal to reduce turn-on of the clamp diodes.

The PGA is monitored for high and low operating voltage headroom at four signal points. The output of the eight total monitor outputs are ORed together into a single error bit contained in the conversion data status byte and the STATUS0 register.

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9.3.3.1 PGA Operating Range

As with many amplifiers, the PGA limits the *absolute input voltage* that must not be exceeded in the linear operating range. The absolute voltage is the combined differential and common-mode voltages. The maximum allowable absolute voltage is determined by the PGA gain, the maximum differential input voltage (V_{IN}), and the minimum value of the high-voltage power supply. Maintain the absolute input voltage (V_{AINX}) within the range as shown in 公式 5, otherwise incorrect conversion data can result:

$$HV\_AVSS + 2.5 + V_{IN} \times (Gain - 1) / 2 < V_{(AINx)} < HV\_AVDD - 2.5 - V_{IN} \times (Gain - 1) / 2$$

where:

- For gain < 1, use value = 1 for gain
- $V_{(AINx)}$ = Absolute input voltage
- $V_{IN} = V_{AINP} - V_{AINN}$ = Maximum expected differential input voltage (5)

The *differential input signal* can also be limited by two other conditions. The first limiting condition is when the reference voltage exceeds AVDD – 1 V (nominally V_{REF} > 4 V). In this case, the differential input signal is limited to: $V_{IN} = \pm(AVDD - 1\ V) / Gain$, instead of the ideal $V_{IN} = \pm V_{REF} / Gain$. The second limiting condition applies to gains of 0.125 and 0.1875. In this case, the differential input signal is limited to: V_{IN} = ±20 V, regardless of the reference voltage.

图 58 and 图 59 show the relationship between the PGA input voltage to the PGA output voltage. In attenuation mode, the first PGA stage is configured as a unity-gain follower. The second PGA stage attenuates the differential input and shifts the signal common-mode voltage to AVDD / 2 to drive the ADC input.

In gain mode, the first PGA stage amplifies the differential signal. The second PGA stage is configured as a unity-gain follower with level-shift. 图 58 and 图 59 show the corresponding output voltage of the PGA stages that must have operating voltage headroom.

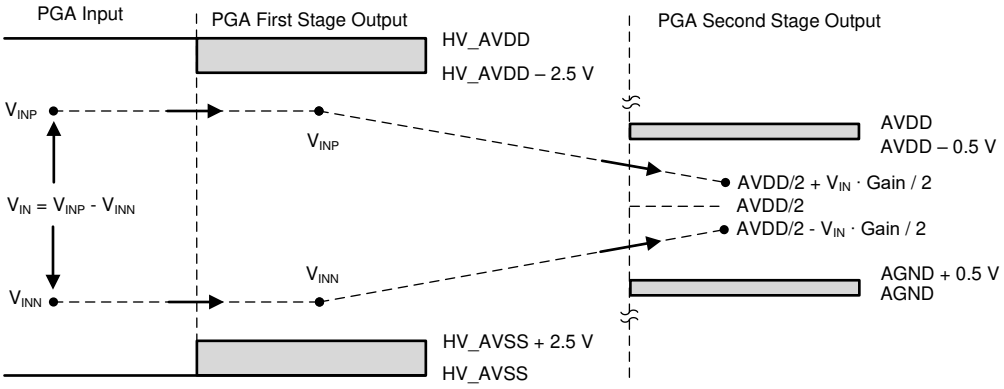

图 58. PGA Attenuation Mode

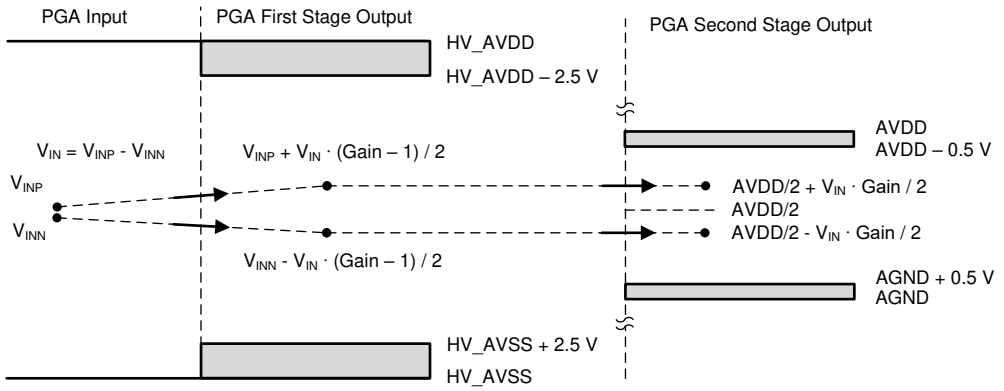

图 59. PGA Gain Mode

9.3.3.2 PGA Monitor

The PGA requires operating voltage headroom at the input and output nodes. The PGA must be within the linear operating range, otherwise the conversion data are not valid. Use the internal PGA monitors to assist in the detection of PGA overload. The PGA has four monitors (two monitors for the input and two monitors for the output) with high and low thresholds for each, for a total of eight possible alarms. The status of each PGA monitor is read in the STATUS1 register. The PGA monitoring points are illustrated in 图 57. 图 60 shows the operation of the low-overload threshold and the high-overload threshold of each PGA monitor point.

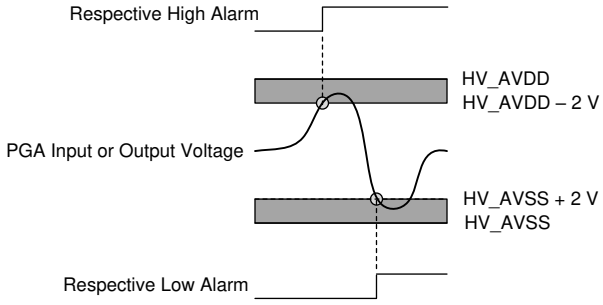

图 60. PGA Monitor Thresholds

Check for PGA overload by polling the STAT12 bit (bit 4 of the STATUS conversion byte or STATUS0 register). The STAT12 bit is the logical OR of all PGA error flags with the CRC-2 error flag. After the STAT12 bit asserts, poll the STATUS1 and STATUS2 registers (address 11h and 12h) to determine the source of the error. The status of the PGA overload is latched in the STATUS1 register and remains latched after the overload condition is removed. Reading the STATUS1 register clears the PGA overload bits (clear-on-read operation). The PGA overload flags *and* the CRC2 flag must be reset in order to clear the STAT12 bit. See the STATUS1 register for a description of the PGA overload bits.

The PGA monitors are analog comparators that can respond to transient overload conditions. Transient conditions can occur, for example, when multiplexing the inputs or when the gain is too high for the voltage of the next channel.

9.3.4 Reference Voltage

The options for the ADC reference voltage are the internal 2.5-V reference, two external reference sources, or the AVDD power supply. The reference voltage is differential and is defined by: $V_{REF} = (V_{REFP} - V_{REFN})$, where V_{REFP} and V_{REFN} are the positive and negative reference voltages. The polarity of V_{REF} must always be positive. 图 61 illustrates the block diagram of the reference input multiplexer used to select the reference.

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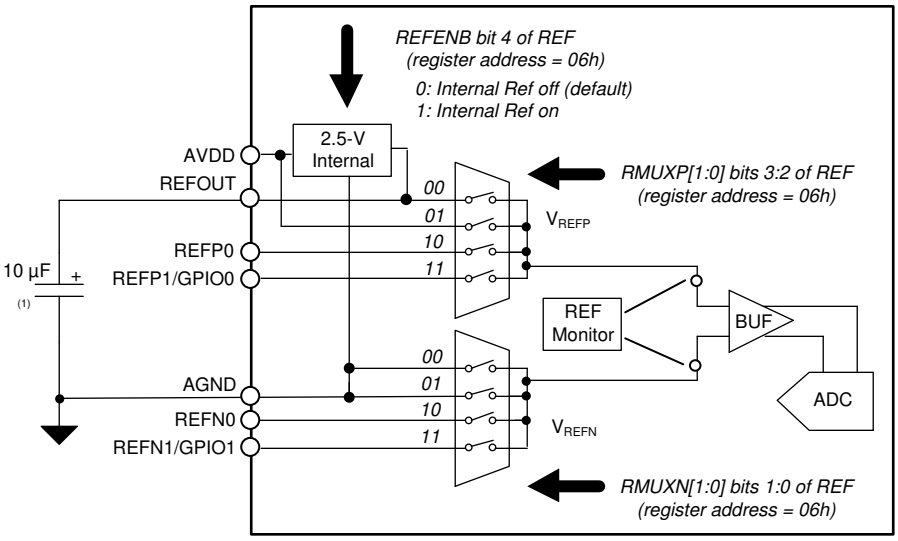

(1) The internal reference requires an external 10-µF capacitor connected from REFOUT to AGND.

图 61. Reference Multiplexer Diagram

Program the RMUXP[1:0] and RMUXN[1:0] bits of the REF register to select the positive and negative reference voltages, respectively. The positive reference options are internal 2.5-V positive, external REFP0, external REFP1, or AVDD. The negative selections are internal 2.5-V negative, external REFN0, external REFN1, or AGND.

The reference voltage is internally monitored for a low-voltage condition; see the *Reference Monitor* section.

9.3.4.1 Internal Reference

The ADC includes a precision 2.5-V reference. The REFENB bit of the REF register enables the reference (default = off). Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to 00b to select the internal reference. A 10-µF capacitor is required between the REFOUT and AGND pins to filter the reference noise. The capacitor is not required if the internal reference is not used. Always enable the internal reference if using the current sources.

REFOUT is the buffered reference output and AGND is the reference return. For good voltage regulation and to minimize ground noise, use a star-layout connection for the reference return and make the return connection close to the AGND pin.

Be aware of AVDD inrush current when the reference is enabled. The inrush current is a result of charging the 10-µF REFOUT capacitor. Also, be aware of the reference voltage stabilization time when starting a conversion or when calibrating the ADC.

9.3.4.2 External Reference

Use an external reference by applying the reference voltage to the reference input pins and then program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0]. Values of 10b select the REFP0 and REFN0 reference input pins and values of 11b select the REFP1 and REFN1 reference input pins. The reference inputs are differential with positive and negative inputs. Follow the specified absolute and differential reference voltage operating conditions; see the *Recommended Operating Conditions* table. Use a 10-nF or larger bypass capacitor across the reference input pins to filter noise. The reference input current can lead to a voltage error if large reference impedances are present. When a reference impedance is present, consider the impact of the reference voltage error to the overall measurement accuracy.

9.3.4.3 AVDD Power-Supply Reference

Use the AVDD power supply as a reference by setting the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to 01 (default mode of operation). For a 6-wire load cell application, connect the excitation sense voltage to the reference inputs to improve measurement accuracy.

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9.3.4.4 Reference Monitor

The ADC incorporates a reference monitor to help detect a low or missing reference voltage. As shown in 图 62, when the reference input voltage (V_{REF} = V_{REFP} – V_{REFN}) falls below 0.4 V, the REFALM bit is set in the STATUS0 register. The alarm is read-only and resets at the next conversion after the fault condition is cleared. To implement detection of a missing reference voltage, use a 100-kΩ resistor across the reference inputs. If either positive or negative reference inputs become disconnected, the reference inputs are biased to 0 V differential, thereby triggering the low reference alarm. Poll bit 3 (REFALM) of the STATUS0 register to determine if the reference alarm has triggered.

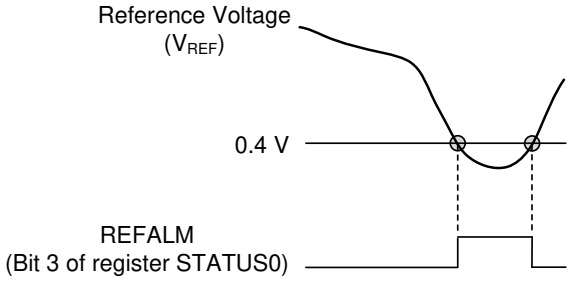

图 62. Reference Monitor Threshold

9.3.5 Current Sources (IDAC1 and IDAC2)

The ADC incorporates current sources designed to provide excitation current to the RTD, thermistor, diode, and other sensor types that require constant-current biasing. The current sources are on the IDAC1 and IDAC2 pins. The current sources are supplied by AVDD; therefore, the operating range is 5 V to AGND. Do not expose the current source to voltages outside of this range. The full-accuracy voltage compliance range is specified in the *Electrical Characteristics* table. The current sources are independently programmable over the 50-µA to 3000-µA range. 图 63 shows the associated registers to configure the current sources (see 表 39). Enable the internal reference to operate the current sources.

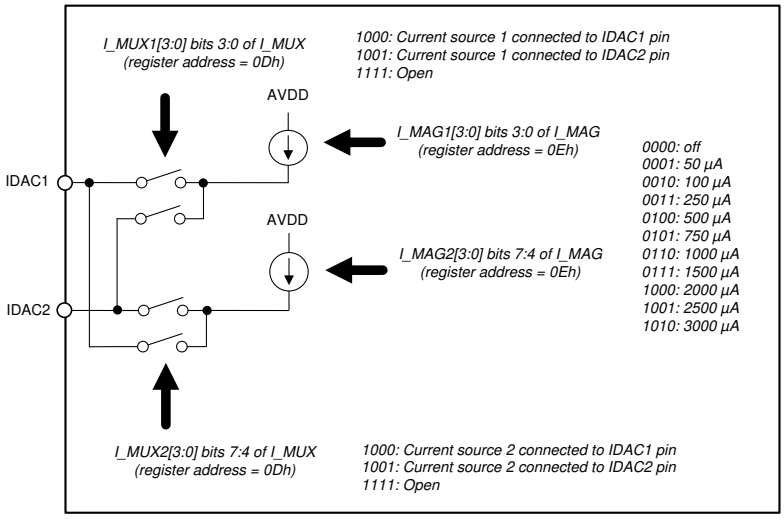

图 63. Current Source Diagram

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9.3.6 General-Purpose Inputs and Outputs (GPIOs)

The ADC provides four GPIO pins (GPIO0 through GPIO4). The GPIO are digital inputs and outputs with logic values that are read and written by the GPIO_DAT bits of the MODE3 register. Two GPIOs are available on dedicated pins and two GPIOs are multiplexed functions with an external reference (REFP1 and REFN1). The GPIO input and output levels are referred to AVDD and AGND. As 图 64 shows, the input threshold value is AVDD / 2 (typical). The GPIO_CON[3:0] bits set the GPIO connection to the designated pin (1 = connected). The GPIO_DIR bits program the direction of the GPIO as an input (1) or output (0). The GPIO_DAT[3:0] bits are the data values for the GPIO. If a GPIO pin is programmed as an output, the value read is the register data previously written.

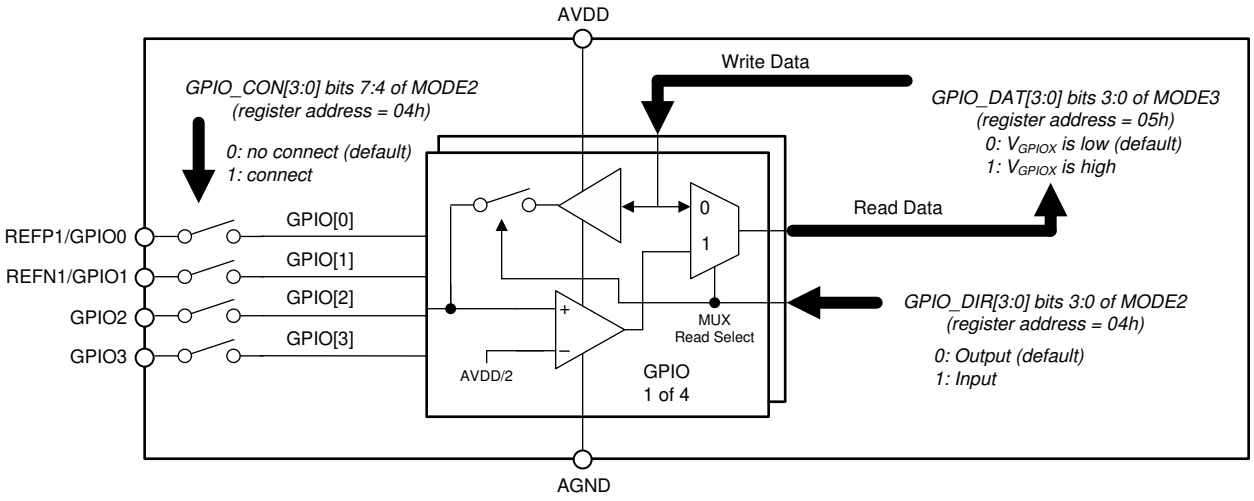

图 64. GPIO Block Diagram

9.3.7 ADC Modulator

The modulator is an inherently stable, fourth-order, 2 + 2 pipelined ΔΣ modulator. The modulator samples the analog input voltage at a high sample rate ($f_{MOD} = f_{CLK} / 8$) and converts the analog input to a ones density bit stream for processing by the digital filter.

9.3.8 Digital Filter

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter low-pass filters and decimates the data (data rate reduction), yielding the final data output. By adjusting the type of filtering, tradeoffs are made between resolution, data rate, and line cycle rejection.

The digital filter has two operating modes, as shown in 图 65: sin(x) / x (sinc) mode and finite impulse response (FIR) mode. The sinc mode provides data rates of 2.5 SPS through 40 kSPS with a selectable filter order of sinc1 through sinc5. The FIR filter provides single-cycle settled conversions and simultaneous rejection of 50-Hz and 60-Hz signal interference frequencies with data rates of 2.5 SPS through 20 SPS.

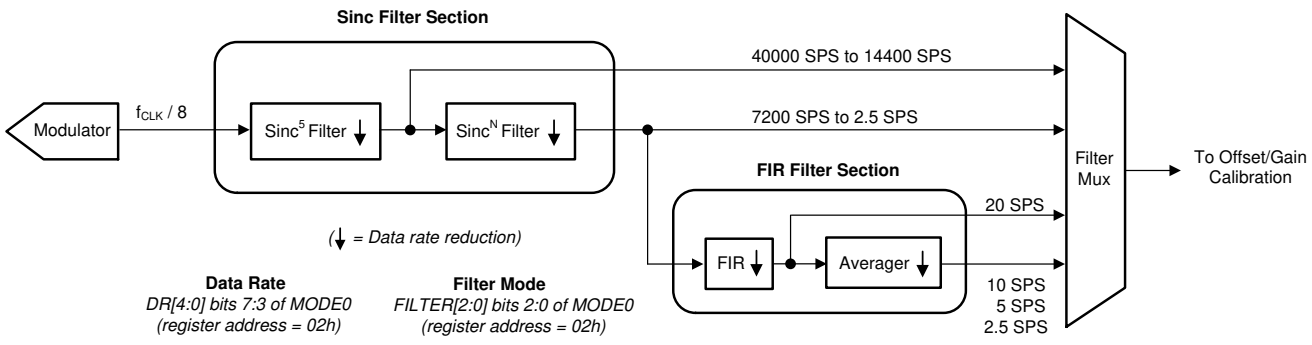

图 65. Digital Filter Block Diagram

9.3.8.1 Sinc Filter Mode

The sinc filter consists of two stages: a variable-decimation sinc5 filter followed by a variable-decimation, variable-order sinc filter. The first stage sinc5 filter averages and down-samples the modulator data (f_{CLK} / 8) to produce 40000 SPS, 25600 SPS, 19200 SPS, and 14400 SPS by using decimation ratios of 32, 36, 48, and 64, respectively. These data outputs bypass the second filter stage and as a result have response characteristics of the first-stage sinc5 filter. The second stage receives the first stage output data at 14400 SPS, and performs additional filtering and decimation to yield data rates of 7200 SPS to 2.5 SPS. The second stage is a programmable order sinc filter.

The data rate is programmed by the DR[4:0] bits of the register MODE0. The filter mode is programmed by the FILTER[2:0] bits of the MODE0 register.

9.3.8.1.1 Sinc Filter Frequency Response

As shown in 图 66 and 图 67, the first-stage sinc5 filter has frequency response nulls occurring at N × f_{DATA} (where N = 1, 2, 3, and so on). At the null frequencies, the filter has zero gain.

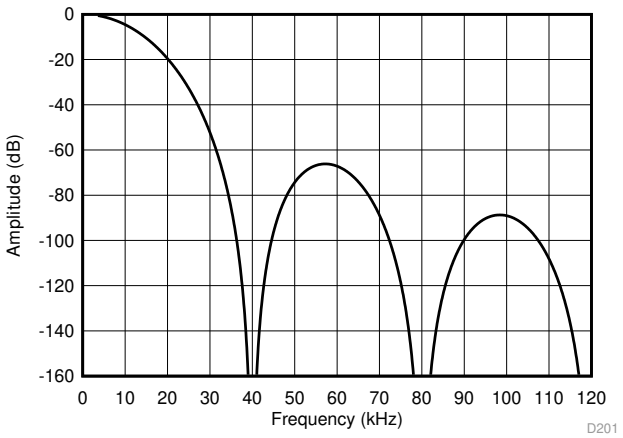

图 66. Sinc Frequency Response (40000 SPS)

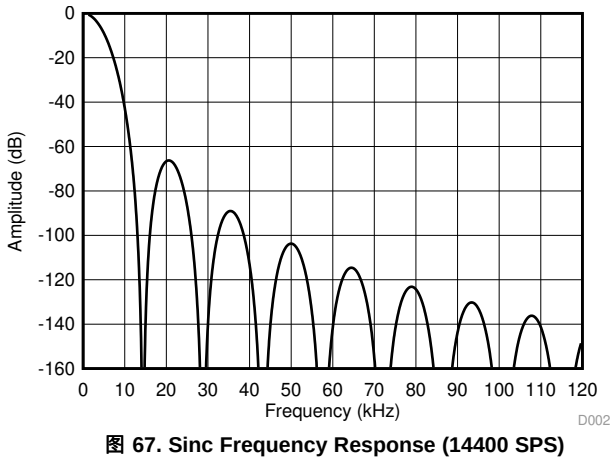

图 67. Sinc Frequency Response (14400 SPS)

The second stage superimposes additional nulls to the nulls produced by the first stage. The first of the superimposed nulls occurs at the output data rate with additional nulls at multiples of the output data rate.

图 68 shows the frequency response of the combined filter stages at 2400 SPS. This data rate has five equally-spaced nulls residing between the larger nulls at 14400-Hz multiples that are produced by the first stage. This frequency response is similar to that of data rates 2.5 SPS to 7200 SPS. 图 69 shows the frequency response nulls at 10 SPS.

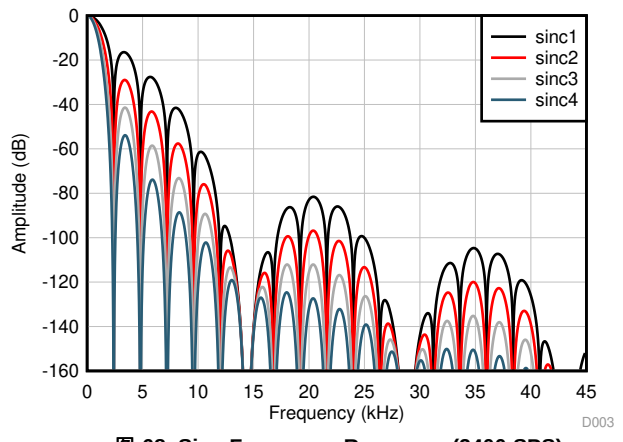

图 68. Sinc Frequency Response (2400 SPS)

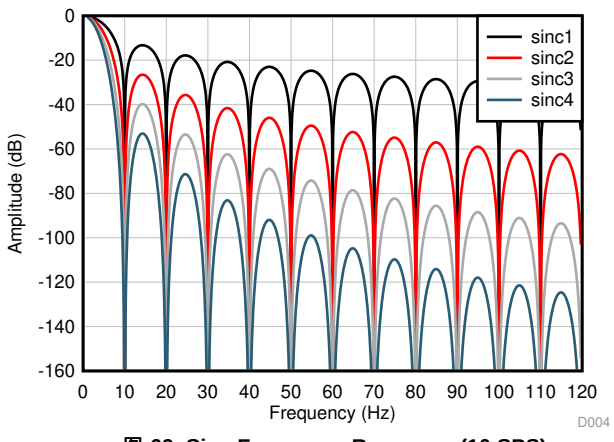

图 69. Sinc Frequency Response (10 SPS)

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图 70 and 图 71 show the frequency response of data rates 50 SPS and 60 SPS, respectively. The frequency response is plotted to the 50-Hz 12th harmonic (10th harmonic for 60 Hz). The 50-Hz or 60-Hz fundamental and harmonic noise of the signal are reduced by increasing the filter order of the second stage.

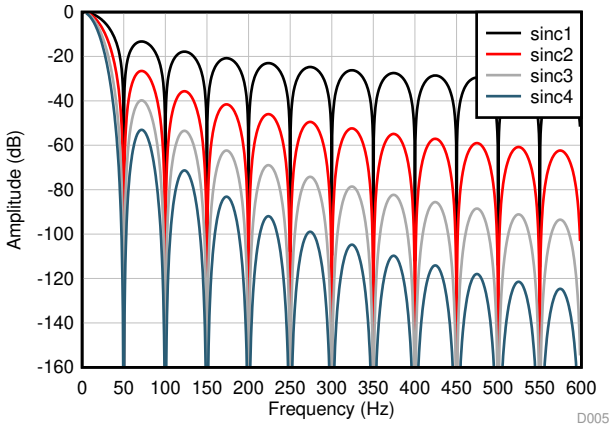

图 70. Sinc Frequency Response (50 SPS)

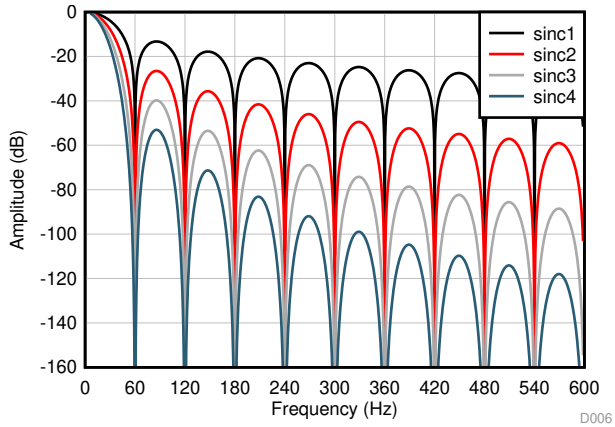

图 71. Sinc Frequency Response (60 SPS)

图 72 and 图 73 plot the detailed frequency response of the 50-SPS and 60-SPS data rates and show various orders of the sinc filter. The high-order sinc filter increases the frequency width of the null, which improves line cycle rejection. Improved 50-Hz or 60-Hz rejection occurs using the sinc3 or sinc4 order filter.

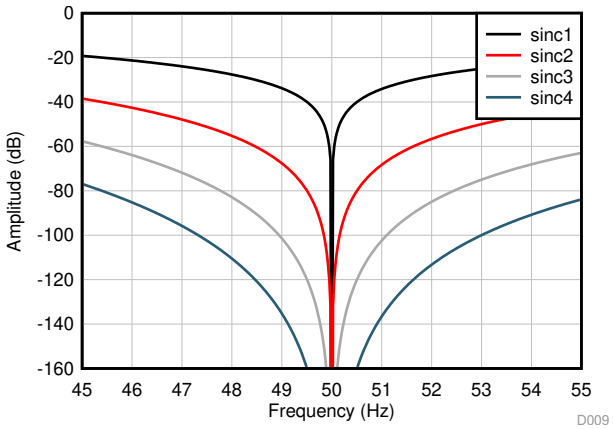

图 72. Sinc Frequency Response, Detailed (50 SPS)

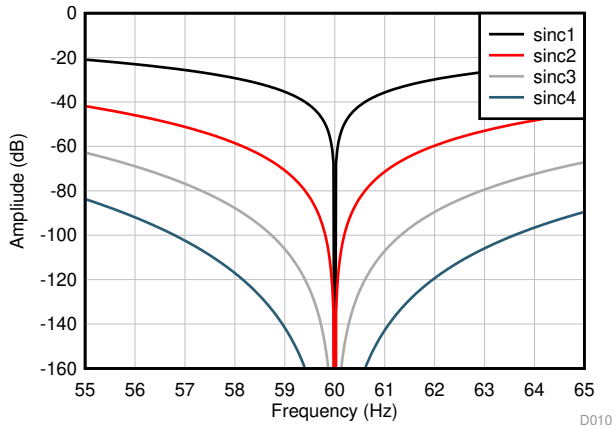

图 73. Sinc Frequency Response, Detailed (60 SPS)

The sinc filter has an overall low-pass response that rolls off high-frequency components of the signal. The filter bandwidth depends on the output data rate and the order of the output data rate. The overall system bandwidth is the combined responses of the digital filter, the PGA antialias filter, and external signal filters. 表 5 lists the –3-dB bandwidth of the sinc filter.

表 5. Sinc Filter Bandwidth

-3-dB BANDWIDTH (Hz)					
DATA RATE (SPS)	SINC1	SINC2	SINC3	SINC4	SINC5
2.5	1.10	0.80	0.65	0.58	—
5	2.23	1.60	1.33	1.15	—
10	4.43	3.20	2.62	2.28	—
16.6	7.38	5.33	4.37	3.80	—
20	8.85	6.38	5.25	4.63	—
50	22.1	16.0	13.1	11.4	—
60	26.6	19.1	15.7	13.7	—
100	44.3	31.9	26.2	22.8	—
400	177	128	105	91.0	—
1200	525	381	314	273	—
2400	1015	751	623	544	—
4800	1798	1421	1214	1077	—
7200	2310	1972	1750	1590	—
14400	—	—	—	—	2940
19200	—	—	—	—	3920
25600	—	—	—	—	5227
40000	—	—	—	—	8167

9.3.8.2 FIR Filter

The finite impulse response (FIR) filter is a coefficient-based filter that provides an overall low-pass filter response. The filter provides simultaneous rejection of 50-Hz and 60-Hz line cycle frequencies and related harmonics at data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS. The conversion latency of the FIR filter is a single cycle. (See 表 8 for latency of all filter settings). As illustrated in 图 65, the FIR filter section receives data from the second-stage sinc filter. The FIR filter section decimates the data to yield the output data rate of 20 SPS. A first-order variable-decimation averaging filter (sinc1) yields 10 SPS, 5 SPS, and 2.5 SPS.

As shown in 图 74 and 图 75, the FIR filter frequency response has a series of response nulls that are positioned close to 50 Hz and 60 Hz. The response nulls repeat near the harmonics of 50 Hz and 60 Hz.

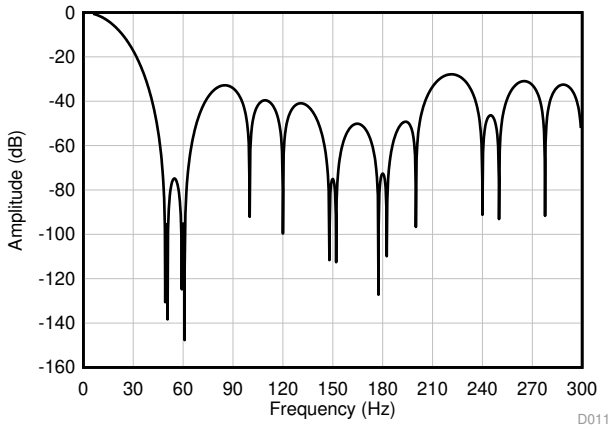

图 74. FIR Frequency Response (20 SPS)

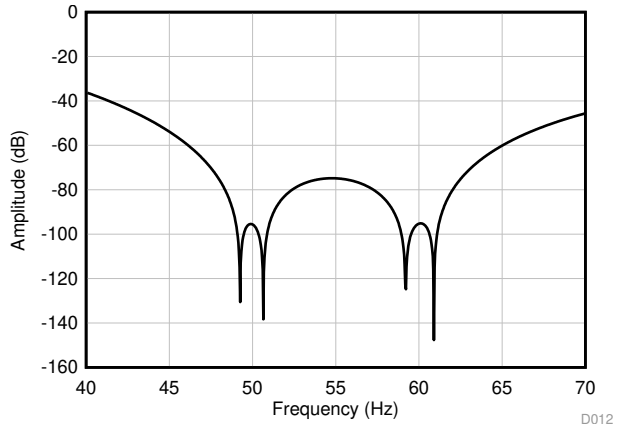

图 75. FIR Frequency Response Detail (20 SPS)

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图 76 shows the FIR filter response at 10 SPS. New frequency nulls are superimposed to the nulls in 图 74 as a result of the variable averager. The first of the combined response nulls occurs at 10 Hz. Additional nulls occur at folded frequencies around multiples of 20 Hz. The first of the 10 SPS folded null frequencies is shown in 图 76 at 10 Hz, 30 Hz, 70 Hz, 90 Hz, and so on.

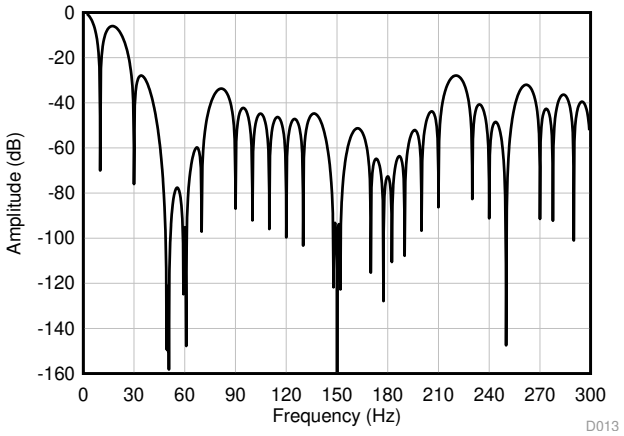

图 76. FIR Frequency Response (10 SPS)

Similar to the response of the sinc filter, the overall FIR filter frequency has a low-pass response that rolls off high frequencies. The response is such that the FIR filter limits the bandwidth of the input signal. The signal bandwidth depends on the output data rate. 表 6 lists the –3-dB filter bandwidth of the FIR filter. The total system bandwidth is the combined response of the digital filter, the PGA antialias filter, and external filters.

表 6. FIR Filter Bandwidth

DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)
2.5	1.2
5	2.4
10	4.7
20	13

9.3.8.3 50-Hz and 60-Hz Normal Mode Rejection

To reduce the effects of 50-Hz and 60-Hz noise interference, configure the data rate to reject noise occurring at 50 Hz and 60 Hz. 50-Hz and 60-Hz noise rejection depends on the filter type and order of the filter. 表 7 summarizes the 50-Hz and 60-Hz noise rejection versus data rate, filter type, and filter order. The table values are based on 2% and 6% tolerance of noise frequency to ADC clock frequency. For the sinc filter mode, 50-Hz and 60-Hz noise rejection is improved by increasing the filter order. Common-mode noise is also rejected at 50 Hz and 60 Hz.

表 7. 50-Hz and 60-Hz Normal Mode Rejection

DIGITAL FILTER AMPLITUDE (dB)					
DATA RATE (SPS)	FILTER TYPE	50 Hz (±2%)	60 Hz (±2%)	50 Hz (±6%)	60 Hz (±6%)
2.5	FIR	–113	–99	–88	–80
2.5	Sinc1	–36	–37	–40	–37
2.5	Sinc2	–72	–74	–80	–74
2.5	Sinc3	–108	–111	–120	–111
2.5	Sinc4	–144	–148	–160	–148
5	FIR	–111	–95	–77	–76
5	Sinc1	–34	–34	–30	–30
5	Sinc2	–68	–68	–60	–60
5	Sinc3	–102	–102	–90	–90
5	Sinc4	–136	–136	–120	–120
10	FIR	–111	–94	–73	–68
10	Sinc1	–34	–34	–25	–25
10	Sinc2	–68	–68	–50	–50
10	Sinc3	–102	–102	–75	–75
10	Sinc4	–136	–136	–100	–100
16.6	Sinc1	–34	–21	–24	–21
16.6	Sinc2	–68	–42	–48	–42
16.6	Sinc3	–102	–63	–72	–63
16.6	Sinc4	–136	–84	–96	–84
20	FIR	–95	–94	–66	–66
20	Sinc1	–18	–34	–18	–24
20	Sinc2	–36	–68	–36	–48
20	Sinc3	–54	–102	–54	–72
20	Sinc4	–72	–136	–72	–96
50	Sinc1	–34	–15	–24	–15
50	Sinc2	–68	–30	–48	–30
50	Sinc3	–102	–45	–72	–45
50	Sinc4	–136	–60	–96	–60
60	Sinc1	–13	–34	–12	–24
60	Sinc2	–27	–68	–24	–48
60	Sinc3	–40	–102	–36	–72
60	Sinc4	–53	–136	–48	–96

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9.4 Device Functional Modes

9.4.1 Conversion Control

The START pin or the START command controls the conversions. If using commands to control conversions, keep the START pin low to avoid contention between the pin and commands. Commands take affect on the 32nd falling SCLK edge. See the *Switching Characteristics* table for details on conversion control timing.

The ADC has two conversion control operating modes: continuous-conversion mode and pulse-conversion mode. The continuous-conversion mode performs conversions indefinitely until the user stops the conversions. Pulse-conversion mode performs one conversion and then stops. The CONVRT (bit 4 of the MODE1 register) programs the mode.

9.4.1.1 Continuous-Conversion Mode

This conversion mode performs continuous conversions until the user stops conversions. To start conversions, take the START pin high or send the START command. $\overline{\text{DRDY}}$ is driven high when the conversion is started. $\overline{\text{DRDY}}$ is driven low when the conversion data are ready. Conversion data are available to read at that time. Take the START pin low or send a STOP command to stop conversions. When conversions are stopped, the conversion in progress runs to completion. To restart a conversion that is in progress, toggle the START pin low-then-high or send a new START command.

9.4.1.2 Pulse-Conversion Mode

In pulse-conversion mode, the ADC performs one conversion when START is taken high or when the START command is sent. When the conversion completes, further conversions stop. The $\overline{\text{DRDY}}$ output is driven high to indicate the conversion is in progress and is driven low when the conversion data are ready. Conversion data are read at that time. To restart a conversion in progress, toggle the START pin low-then-high or send a new START command. Driving START low or sending the stop command does not interrupt the current conversion.

9.4.1.3 Conversion Latency

The digital filter averages data from the modulator to produce the conversion result. The discrete stages of the digital filter must have settled data to provide fully settled output data. The order and the decimation ratio of the digital filter determine the amount of data averaged that affects the latency of the conversion data. The FIR and sinc1 filter modes are zero latency because the ADC provides the conversion result in one conversion cycle. Latency time is an important consideration for data throughput in multiplexed applications.

表 8 lists the conversion latency values of the ADC. Conversion latency is defined as the time from the start of the first conversion by taking the START pin high or sending the start command to when the conversion data are ready. The ADC is designed to provide fully settled data under this condition. The conversion latency values listed in 表 8 include the programmable start-conversion delay equal to 50 µs before the digital filter starts, which also includes overhead time for final data processing. After the first conversion completes in continuous conversion mode, the period of the next conversions are equal to 1 / f_{DATA}. The first conversion latency time in auto-zero mode has twice the values listed in 表 8. The values listed in 表 8 are equal to the period of the next conversions.

Device Functional Modes (接下页)

表 8. Conversion Latency Time

DATA RATE (SPS)	CONVERSION LATENCY TIME ($t_{(STDR)}$ (1), ms)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	400.4	800.4	1,200	1,600	—	402.2
5	200.4	400.4	600.4	800.4	—	202.2
10	100.4	200.4	300.4	400.4	—	102.2
16.6	60.43	120.4	180.4	240.4	—	—
20	50.43	100.4	150.4	200.4	—	52.22
50	20.43	40.42	60.43	80.43	—	—
60	17.09	33.76	50.43	67.09	—	—
100	10.43	20.42	30.43	40.43	—	—
400	2.925	5.424	7.925	10.43	—	—
1200	1.258	2.091	2.925	3.758	—	—
2400	0.841	1.258	1.675	2.091	—	—
4800	0.633	0.841	1.050	1.258	—	—
7200	0.564	0.702	0.841	0.980	—	—
14400	—	—	—	—	0.423	—
19200	—	—	—	—	0.336	—
25600	—	—	—	—	0.271	—
40000	—	—	—	—	0.179	—

(1) Auto-zero mode off, conversion-start time delay = 50 µs (DELAY[3:0] = 0001). Actual conversion latency time can vary depending on the accuracy of f_{CLK}.

As shown in 图 77, if the input signal changes during the conversion phase, the conversion data are a mix of old and new data. After an unsynchronized input change, the number of conversion periods required to provide fully settled output data are calculated by dividing the conversion latency by the nominal period and then adding one additional conversion. In auto-zero mode, use twice the latency values plus one additional conversion.

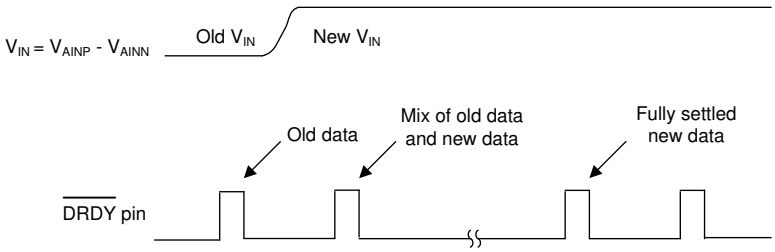

图 77. Input Change During Conversions

9.4.1.4 Start-Conversion Delay

At the start of a conversion, the ADC provides a programmable delay to allow for PGA settling time and to provide a delay for any external component settling effects. The default value is 50 µs and provides the settling time for the PGA antialiasing filter. Use additional delay time as needed to provide settling time for the effects of external components. The latency values listed in 表 8 are with a start-conversion delay value = 50 µs. As an alternative to this parameter, delay the start of conversion after the input and configuration changes.

9.4.2 Auto-Zero Mode

Auto-zero mode is a continuous calibration technique that provides low offset voltage and near-zero drift over time and temperature. Auto-zero mode is a form of chopping that covers the internal ADC signal chain. The ADC alternates the polarity of consecutive conversions by internally reversing the input signal. The digital filter subtracts the results of two reverse-polarity conversions to yield the final conversion data. The subtraction result removes the offset error. Auto-zero mode is available only for use with the AIN0 and AIN1 inputs. See the MODE1 register for details on how to program auto-zero mode.

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Auto-zero mode changes the data rate and the conversion latency time corresponding to the first conversion. The new data rate is equal to 1 divided by the latency values listed in 表 8. For example, when the ADC is programmed to 20 SPS and FIR mode, the new data rate is = 1 / 52.22 ms = 19.15 SPS. Regardless of the new data rate, the location of the digital filter frequency notches are unaltered. The latency time corresponding to the first conversion is equal to 2 × the latency time values listed in 表 8. Auto-zero mode reduces conversion noise by $\sqrt{2}$ because auto-zero mode effectively averages the data from two conversions.

9.4.3 Clock Mode

Operate the ADC with an external clock or with the internal oscillator. For external clock operation, apply the clock signal to CLKIN. The ADC detects the presence of the external clock and selects the clock automatically. As described in 表 9, the clock frequency depends on the data rate used. Be sure the external clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. For internal clock operation, connect CLKIN to DGND. Be aware of the accuracy of the internal oscillator as described in the *Electrical Characteristics* table. The internal oscillator begins operating immediately at device power-on. Read the CLOCK bit in the STATUS0 register to verify the clock mode.

表 9. External Clock vs Data Rate

DATA RATE	CLOCK FREQUENCY
2.5 SPS to 25600 SPS	7.3728 MHz
40000 SPS	10.24 MHz

9.4.4 Reset

The ADC is reset in three ways: automatic by power-on-reset, manually via the $\overline{\text{RESET}}$ pin, or by the RESET command.

When reset, the serial interface, conversion-control logic, digital filter, and register map values are reset. The RESET bit of the STATUS0 register is set after a reset occurs. Clear the bit to detect the next device reset. If the START pin is high after reset, the ADC immediately begins conversions.

9.4.4.1 Power-On Reset

After supply voltages cross the respective reset voltage thresholds at power-up, the ADC is reset and after 2^{16} f_{CLK} cycles the ADC is ready for communication. Until this time, $\overline{\text{DRDY}}$ is held low. $\overline{\text{DRDY}}$ is then driven high to indicate when ADC communication can begin. The conversion cycle starts 512 / f_{CLK} cycle after $\overline{\text{DRDY}}$ asserts high. 图 4 illustrates the power-on reset behavior.

9.4.4.2 Reset by Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of four f_{CLK} cycles, and then return the pin high. After reset, the conversion starts 512 / f_{CLK} cycles later. See 图 5 for $\overline{\text{RESET}}$ pin timing.

9.4.4.3 Reset by Command

Reset the ADC through the serial interface by the RESET command. Bring $\overline{\text{CS1}}$ high first to reset the serial interface to ensure the ADC is ready for the command. After reset, the conversion starts 512 / f_{CLK} cycles later. See 图 5 for the reset command timing.

9.4.5 Calibration

The ADC incorporates calibration registers and associated commands to calibrate offset and full-scale errors. Calibrate the ADC by using calibration commands, or calibrate by writing to the calibration registers directly (user calibration). To calibrate by command, send the offset or full-scale calibration commands. To user calibrate, write to the calibration registers with values based on the acquired conversion data. Perform the offset calibration operation before the full-scale calibration operation.

9.4.5.1 Offset and Full-Scale Calibration

Use the offset and full-scale (gain) registers to correct offset or full-scale errors, respectively. As illustrated in 图 78, the offset calibration register is subtracted from the output data before multiplication by the full-scale register, which is divided by 400000h. After the calibration operation, the final value of the output data is clipped to 24 bits.

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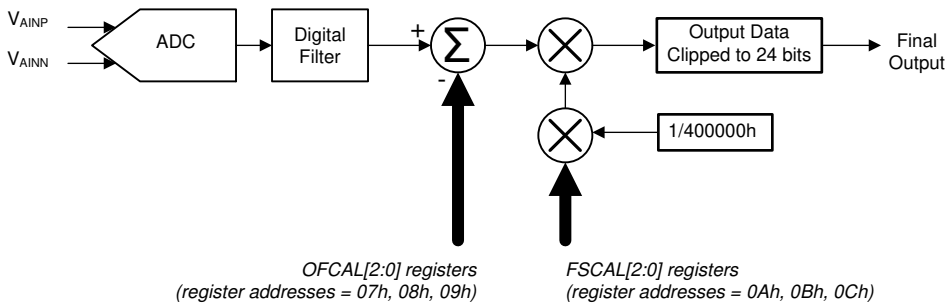

图 78. Calibration Block Diagram

公式 6 shows the internal calibration.

$$\text{Final Output Data} = (\text{Pre Data} - \text{OFCAL}[2:0]) \times \text{FSCAL}[2:0] / 400000\text{h} \quad (6)$$

9.4.5.1.1 Offset Calibration Registers

The offset calibration word, as listed in 表 10, is 24 bits consisting of three 8-bit registers. The offset value is subtracted from the conversion result. The offset value is in two's-complement format with a maximum positive value equal to 7FFFFFh and a maximum negative value equal to 800000h. A register value equal to 000000h has no offset correction. Although the calibration registers provide a wide range of offset values, the input signal cannot exceed ±106% of the precalibrated range; otherwise the ADC is overranged. 表 11 lists example values of the offset register.

表 10. Offset Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
OFCAL0	LSB	07h	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFCAL1	MID	08h	B15	B14	B13	B12	B11	B10	B9	B8
OFCAL2	MSB	09h	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

表 11. Offset Calibration Register Values

OFCAL[2:0] REGISTER VALUE	OFFSET CALIBRATED OUTPUT VALUE
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h

9.4.5.1.2 Full-Scale Calibration Registers

The full-scale calibration word, as listed in 表 12, is 24 bits consisting of three 8-bit registers. The full-scale calibration value is straight binary and normalized to a unity-gain at a value of 400000h. 表 13 lists register values for selected gain factors. Gain errors greater than unity are corrected by full-scale values less than 400000h. Although the calibration registers provide a wide range of possible values, the input signal must not exceed ±106% of the precalibrated input range; otherwise the ADC is overranged.

表 12. Full-Scale Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
FSCAL0	LSB	0Ah	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSCAL1	MID	0Bh	B15	B14	B13	B12	B11	B10	B9	B8
FSCAL2	MSB	0Ch	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

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表 13. Full-Scale Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1
3CCCCCh	0.95

9.4.5.2 Offset Calibration (OFSCAL)

The offset calibration command corrects offset errors. To calibrate offset errors, short the inputs to the ADC or to calibrate the system, short the signal inputs to the system. When the command is sent, the ADC averages 16 conversion results to reduce conversion noise for improved calibration accuracy. When calibration is complete, the ADC performs one conversion using the new calibration value. The new calibration value is written to the offset calibration register.

9.4.5.3 Full-Scale Calibration (GANCAL)

The full-scale calibration command corrects gain errors. To calibrate, apply a positive calibration voltage to the ADC, or apply the voltage to the signal inputs of the system, wait for the signal to settle, and then send the command. The ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. The ADC computes the full-scale calibration value so that the applied calibration voltage is scaled to an equal positive full-scale output code. The computed result is written to the calibration register. The ADC then performs one new conversion using the new calibration value.

9.4.5.4 Calibration Command Procedure

Use the following calibration procedure using the calibration commands. The register lock mode must be in the UNLOCK state prior to using the calibration commands. When calibrating at power-on, make sure the reference voltage has stabilized. Perform an offset calibration operation prior to full-scale calibration.

1. Select the desired input channel, gain, reference mode, and related ADC configurations as required.
2. Apply the appropriate calibration signal (zero or full-scale) to the ADC or system inputs.
3. Take the START pin high or send the START command to start conversions. $\overline{\text{DRDY}}$ is driven high.
4. Before the first conversion completes, send the appropriate calibration command. Keep $\overline{\text{CS1}}$ low; otherwise the command is cancelled. Do not send other commands during the calibration period.
5. The calibration time, as described in 表 14, depends on the data rate and digital filter mode. $\overline{\text{DRDY}}$ is driven low when calibration is complete. As a result, offset or full-scale calibration registers are updated with new values. New conversion data are available immediately using the new calibration value.

表 14. Calibration Time (ms)

DATA RATE (SPS)	FILTER MODE(1)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	6801	7601	8401	9201	—	6805
5	3401	3801	4201	4601	—	3405
10	1701	1901	2101	2300	—	1705
16.6	1021	1141	1261	1381	—	—
20	850.9	951	1051	1151	—	854.5
50	340.9	380.9	421	460.9	—	—
60	284.2	317.5	350.9	384.2	—	—
100	170.9	190.9	210.9	230.9	—	—
400	43.36	48.36	53.36	58.36	—	—
1200	15.02	16.69	18.36	20.02	—	—
2400	7.938	8.772	9.605	10.44	—	—
4800	4.397	4.813	5.230	5.647	—	—
7200	3.216	3.494	3.772	4.050	—	—
14400	—	—	—	—	1.892	—
19200	—	—	—	—	1.458	—
25600	—	—	—	—	1.133	—
40000	—	—	—	—	0.738	—

(1) Nominal clock frequency. Auto-zero mode disabled.

9.4.5.5 User Calibration Procedure

To user calibrate, apply the calibration voltage, acquire conversion data, and compute the calibration value. Write the computed value to the corresponding calibration registers. Before starting calibration, preset the offset and full-scale registers to 000000h and 400000h, respectively.

To offset calibrate, short the inputs to the system and average *n* number of the conversion data. Averaging conversion data reduces noise to increase calibration accuracy. Write the average value of the conversion data to the offset registers.

To gain calibrate using a full-scale calibration signal, temporarily reduce the full-scale register by 95% to avoid any output clipped codes (set FSCAL[2:0] to 3CCCCCh). Acquire *n* number of conversions and average the conversions to increase calibration accuracy. Compute the full-scale calibration value as shown in 公式 7:

Full-Scale Calibration Value = (Expected Code / Actual Code) × 400000h (7)

where:

- Expected code = 799998h using full-scale calibration signal and 95% precalibration scale factor

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9.5 Programming

9.5.1 Serial Interface

The SPI-compatible serial interface is used to read conversion data, configure the device registers, and control ADC operation. The CRC is used to validate error-free transmission of the input and output data flow. The serial interface consists of the following control signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/$\overline{DRDY}$. Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed on the SCLK rising edges; data are latched or read on the SCLK falling edges. Timing details of the SPI protocol are provided in 图 1 and 图 2.

9.5.1.1 Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)

The ADC consists of discrete PGA and ADC sections with each section selected for communication by separate chip-select inputs ($\overline{CS1}$ and $\overline{CS2}$). Most commands require the use of $\overline{CS1}$ to control the ADC section. However, for control of the PGA section, use $\overline{CS2}$ for register access commands at address 10h and above. Communicate to the device by taking either $\overline{CS1}$ or $\overline{CS2}$ low corresponding to the type of command and whether addressing the ADC or PGA registers.

$\overline{CS1}$ and $\overline{CS2}$ are active low inputs. In normal operation, take one chip-select input low at a time and keep that input low for the duration the command operation. Take the chip-select input high after the command operation completes. When the chip-select input is taken high, the serial interface resets and SCLK activity is ignored (thus blocking commands). When both chip-select inputs are high, DOUT/$\overline{DRDY}$ enters the high-impedance state. $\overline{CS1}$ must be low in order to poll the data-ready function provided by DOUT/$\overline{DRDY}$. $\overline{DRDY}$ remains active regardless of the state of the chip-select inputs.

9.5.1.2 Serial Clock (SCLK)

SCLK is the serial interface shift clock input that clocks data into and out of the device. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. Return SCLK low after the data operation completes. SCLK is a Schmidt-triggered input designed to provide noise immunity. Even though SCLK is noise resistant, keep SCLK noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. Use a series termination resistor at the SCLK drive pin to reduce ringing.

9.5.1.3 Data Input (DIN)

DIN is the serial interface data input. DIN inputs commands and register data to the device. Input data are latched on the falling edge of SCLK.

9.5.1.4 Data Output/Data Ready (DOUT/$\overline{DRDY}$)

The DOUT/$\overline{DRDY}$ pin is the serial interface data output. This pin also provides the conversion-data ready output. The function of the pin changes whether a read data (or read register) operation is in progress. With $\overline{CS1}$ low and when not reading register or conversion data, the pin indicates when data are ready by asserting low. For conversion data and register read operations, the function changes to data output. When the read operation is completed, the function changes to conversion-data ready. As DOUT, the data are updated on the SCLK rising edge and the data must therefore be latched on the SCLK falling edge. $\overline{CS1}$ must be low for DOUT/$\overline{DRDY}$ to provide the data-ready function. When both chip-select pins are high, DOUT/$\overline{DRDY}$ is in high-impedance mode (tri-state).

9.5.2 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ asserts low to indicate that new conversion data are ready for readback. The operation of $\overline{DRDY}$ depends on the mode (continuous or pulse) and whether or not the conversion data are retrieved.

9.5.2.1 $\overline{DRDY}$ in Continuous-Conversion Mode

In continuous-conversion mode, $\overline{DRDY}$ is driven high when conversions are started and is driven low when conversion data are ready. During data readback, $\overline{DRDY}$ is driven high, which indicates completion of the read operation. If the conversion data are not read, $\overline{DRDY}$ remains low and pulses high 16 f_{CLK} cycles prior to the next falling edge.

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To read back the current conversion data before the next conversion completes, send the read data command at least 16 f_{CLK} cycles prior to the $\overline{DRDY}$ falling edge. If the readback command is sent *less than* 16 f_{CLK} cycles prior to the $\overline{DRDY}$ falling edge, *either* the previous or new conversion data are provided. The timing of the command determines whether previous or new data are provided. In the event that previous data are provided, $\overline{DRDY}$ transitioning to low is suspended until after the read data operation completes. In this case, the DRDY bit of the STATUS0 byte is low to indicate that the previous data have already been read. In the event that new conversion data are provided, $\overline{DRDY}$ transitions low as normal. The DRDY bit of the STATUS0 byte is high to indicate new data are read. To ensure readback of new conversion data, wait until $\overline{DRDY}$ asserts low before starting the data read operation.

9.5.2.2 $\overline{DRDY}$ in Pulse-Conversion Mode

$\overline{DRDY}$ is driven high at conversion start and is driven low when the conversion data are ready. $\overline{DRDY}$ remains low until a new conversion is started.

图 79 shows $\overline{DRDY}$ operation with and without data retrieval in two conversion modes.

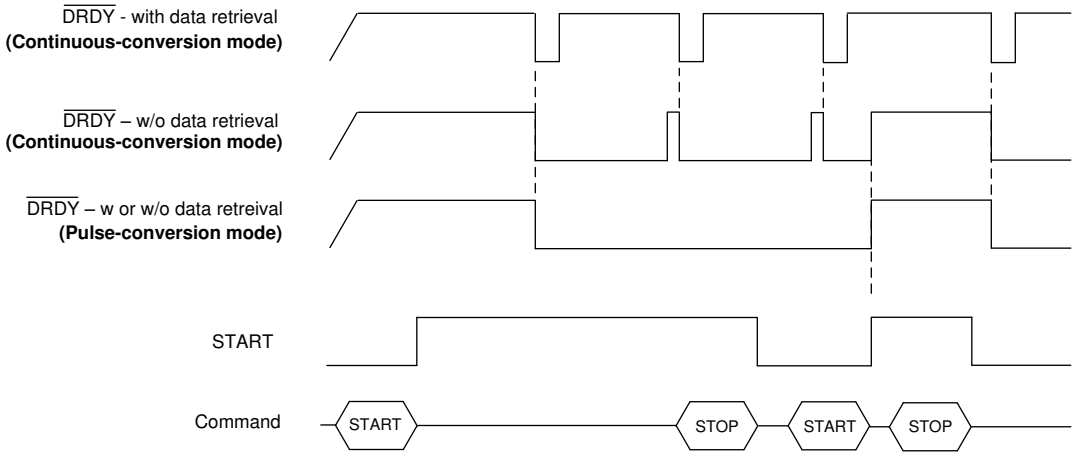

图 79. $\overline{DRDY}$ Operation

9.5.2.3 Data Ready by Software Polling

If desired, poll the DRDY bit in the STATUS word instead of polling the $\overline{DRDY}$ pin. In software poll mode, read the STATUS0 byte and poll the DRDY bit. If the bit is high, then conversion data are new from the last data read operation. If the bit is low, conversion data are not new from the last data read operation. In this case, the previous conversion data are returned. In order to avoid missing conversion data in continuos conversion mode, poll the bit at least as often as the period of the data rate.

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9.5.3 Conversion Data

Conversion data are read by the RDATA command. To read conversion data, take $\overline{CS1}$ low and issue the read data command. The conversion data field consists of an optional STATUS0 byte, three data bytes, and the CRC byte. The CRC byte is computed over the combined STATUS0 byte and three conversion data bytes. See the *RDATA Command* section for details on reading conversion data.

9.5.3.1 Status Byte (STATUS0)

The status byte contains information on the operating status of the ADC. The contents of the STATUS0 register byte is included with the conversion data by setting the STATENB bit of the MODE3 register. Alternatively, read the STATUS0 register directly by the register read command without having to read conversion data.

9.5.3.2 Conversion Data Format

The conversion data are 24 bits, in two's-complement format to represent positive and negative values. The data begins with the most significant bit (sign bit) first. The data are scaled so that V_{IN} = 0 V results in an ideal code value of 000000h, the positive full-scale input is equal to an ideal value of 7FFFFFh and the negative full-scale input is equal to an ideal code value of 800000h. 表 15 shows the code values. The data are clipped to 7FFFFFh and 800000h during positive and negative signal overdrive, respectively.

表 15. ADC Conversion Data Codes

DESCRIPTION	INPUT SIGNAL (V)	24-BIT CONVERSION DATA (1)
Positive full scale	≥ V_{REF} / Gain × (2^{23} – 1) / 2^{23}	7FFFFFh
1 LSB	V_{REF} / (Gain × 2^{23})	000001h
Zero scale	0	000000h
–1 LSB	–V_{REF} / (Gain × 2^{23})	FFFFFFh
Negative full scale	≤ –V_{REF} / Gain	800000h

(1) Ideal output code excluding noise, offset, gain, and linearity errors.

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9.5.4 Cyclic Redundancy Check (CRC)

Cyclic redundancy check (CRC) is an error detection byte that detects communication errors to and from the host and ADC. CRC is the division remainder of the payload data by the prescribed CRC polynomial. The payload data are 1, 2, 3, or 4 bytes depending on the data transfer operation.

The host computes the CRC over the two command bytes and appends the CRC to the command string (third byte). A fourth, zero-value byte completes the command field to the ADC. The ADC performs the CRC calculation and compares the result to the CRC transmitted by the host. If the host and ADC CRC values match, the command executes and the ADC responds by transmitting the valid CRC during the fourth byte of the command. If the CRC is error free and the operation is a data read, the ADC responds with a second CRC that is computed for the requested data byte payload. The response data payload is 1, 3, or 4 bytes depending on the type of operation.

If the host and ADC CRC values *do not* match, the command does not execute and the ADC responds with an *inverted* CRC value, calculated over the received command bytes. The inverted CRC is intended to signal the host of the failed operation. The host terminates transmission of further bytes to stop the command operation. The CRC1 bit is set in the STATUS0 register when a error pertaining to ADC registers occur. The STAT12 and CRC2 flags are set when an error pertaining to PGA registers occur.

The ADC is ready to accept the next command after all required bytes are transmitted when no CRC error occurs, or after a CRC error occurs when terminated at the end of the fourth command byte.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are: 100000111b.

The following is a general procedure to compute the CRC value:

1. Left shift the concatenated 1-, 2-, 3-, or 4-byte argument (if required) to create a new 40-bit data value (the starting data value). The shifted data are padded with ones to the right of the argument.
2. Align the MSB of the CRC polynomial (100000111) to the left-most, logic-one value of the data.
3. Perform an XOR operation on the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.
4. When the XOR result is less than 100000000b, the procedure ends, yielding the 8-bit CRC value. Otherwise, continue with the XOR operation shown in step 2 using the current data value. The number of loop iterations depends on the value of the initial data.

The following sections detail the input and output data of each command. In the descriptions that follow, these CRC mnemonics apply:

- **CRC-2**: Input the CRC of command bytes 1 and 2. Except for the WREG command, the byte 2 value is arbitrary.
- **Out CRC-1**: Output the CRC of one register data byte.
- **Out CRC-2:** Output the CRC of two command bytes, inverted value if an input CRC error is detected.
- **Out CRC-3:** Output the CRC of three conversion data bytes.
- **Out CRC-4:** Output the CRC of three conversion data bytes plus the STATUS0 byte.
- **Echo Byte 1:** Echo of received input byte 1.
- **Echo Byte 2:** Echo of received input byte 2.

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9.5.5 Commands

Commands are used to read conversion data, control the device, and read and write register data. 表 16 provides a list of commands and the corresponding command byte sequence. Only send the commands that are listed in 表 16.

The column labeled $\overline{CSx}$ shows the use of $\overline{CS1}$ or $\overline{CS2}$ for the particular command type. Most commands use $\overline{CS1}$. Only activate $\overline{CS2}$ to access register data at address 10h and above and to lock register data at address 10h and above. See the *Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)* section for details of chip-select operation.

表 16. Command Byte Summary

MNEMONIC	$\overline{CSx}$	DESCRIPTION	BYTE 1	BYTE 2(1)	BYTE 3	BYTE 4
CONTROL COMMANDS						
NOP	$\overline{CS1}$ or $\overline{CS2}$	No operation	00h	Arbitrary	CRC-2	00h
RESET	$\overline{CS1}$	Reset	06h	Arbitrary	CRC-2	00h
START	$\overline{CS1}$	Start conversion	08h	Arbitrary	CRC-2	00h
STOP	$\overline{CS1}$	Stop conversion	0Ah	Arbitrary	CRC-2	00h
READ DATA COMMAND						
RDATA	$\overline{CS1}$	Read conversion data	12h	Arbitrary	CRC-2	00h
CALIBRATION COMMANDS						
OFSCAL	$\overline{CS1}$	Offset calibration	16h	Arbitrary	CRC-2	00h
GANCAL	$\overline{CS1}$	Gain calibration	17h	Arbitrary	CRC-2	00h
REGISTER COMMANDS						
RREG	$\overline{CS1}$ or $\overline{CS2}$	Read register data	20h + rrh(2)	Arbitrary	CRC-2	00h
WREG	$\overline{CS1}$ or $\overline{CS2}$	Write register data	40h + rrh(2)	Register data	CRC-2	00h
PROTECTION COMMANDS						
LOCK	$\overline{CS1}$ or $\overline{CS2}$	Register data lock	F2h	Arbitrary	CRC-2	00h
UNLOCK	$\overline{CS1}$ or $\overline{CS2}$	Register data unlock	F5h	Arbitrary	CRC-2	00h

(1) Excluding the write-register command, the value of the second byte is arbitrary (any value) but *is* included in the CRC calculation.
(2) rrh = 5-bit register address.

9.5.5.1 General Command Format

图 80 shows an example register write operation to register address 02h (command opcode 42h). For this register address (02h), take $\overline{CS1}$ low. The first byte output from the ADC is always 0FFh. The host calculates the CRC of the two input command bytes. The Out CRC-2 byte is the ADC-calculated, output CRC based on the received command bytes. If the CRC values match, the command is executed beginning at the last SCLK of the fourth byte in the sequence. Forcing chip select high before the command completes results in command termination. Toggle chip select low-to-high between command operations.

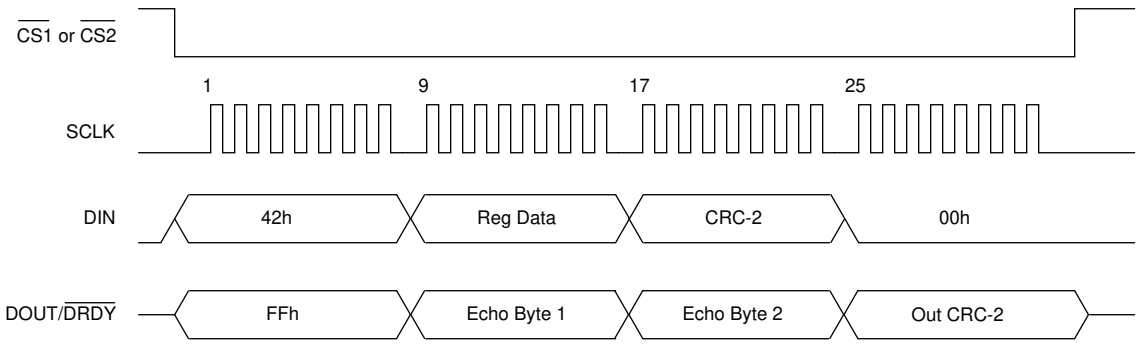

图 80. Register Write Command Sequence (Address = 02h)

The following sections detail the input and output byte sequence corresponding to each command. See the *Cyclic Redundancy Check (CRC)* section for the notation used for the CRC.

9.5.5.2 NOP Command

This command has no operation. Use the NOP command to validate the CRC response byte and error detection without affecting normal operation. 表 17 shows the NOP command byte sequence.

表 17. NOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	00h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.3 RESET Command

The RESET command resets the ADC operation and resets all registers to default. See the *Reset by Command* section for details. 表 18 lists the RESET command byte sequence.

表 18. RESET Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	06h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.4 START Command

This command starts a conversions. See the *Conversion Control* section for details. 表 19 lists the START command byte sequence.

表 19. START Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	08h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.5 STOP Command

This command is used to stop conversions. See the *Conversion Control* section for details. 表 20 lists the STOP command byte sequence.

表 20. STOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	0Ah	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.6 RDATA Command

This command reads conversion data. Because the data are buffered, the data can be read at any time during the conversion sequence. If data are read *near* the completion of the conversion phase, old or new conversion data are returned. See the *Data Ready (DRDY)* section for details.

The response data of the ADC varies in length depending on inclusion of the optional STATUS0 byte. See the *Conversion Data Format* section for details of the format of the conversion data. 表 21 and 图 81 describe the RDATA command byte sequence that includes the STATUS0 byte.

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表 21. RDATA Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
DIN	12h	Arbitrary	CRC-2	00h	00h	00h	00h	00h	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	STATUS0(1)	MSB data	MID data	LSB data	Out CRC-3 or Out CRC-4(2)

(1) Optional STATUS0 byte shown.
(2) Out CRC-4 (4-byte CRC = STATUS0 + data) if the STATUS0 byte is included in the data packet.

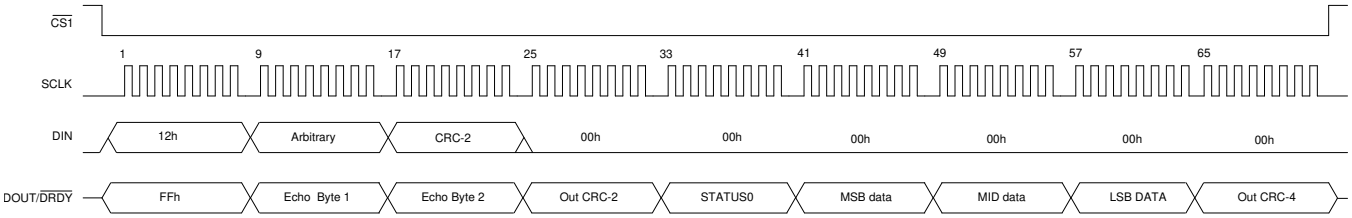

图 81. Conversion Data Read Operation

9.5.5.7 OFSCAL Command

This command is used for offset calibration. See the *Calibration* section for details. 表 22 lists the OFSCAL command byte sequence.

表 22. OFSCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	16h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.8 GANCAL Command

This command is used for gain calibration. See the *Calibration* section for details. 表 23 lists the GANCAL command byte sequence.

表 23. GANCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	17h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.9 RREG Command

Use the RREG command to read register data. Take $\overline{\text{CS1}}$ low to access registers within the ADC register block. Take $\overline{\text{CS2}}$ low to access registers within the PGA register block (see the *Register Map* section for the register block map). Register data are read one byte at a time using the RREG command for each operation. Add the register address (rrh) to the base opcode (20h) to complete the command byte (20h + rrh). 表 24 lists the RREG command byte sequence. The ADC responds with the register data byte, most significant bit first. Data for registers addressed outside the range is 00h. Out CRC-2 is the output CRC corresponding to the received command bytes. Out CRC-1 is the output CRC corresponding to the single register data byte.

表 24. RREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
DIN	20h + rrh	Arbitrary	CRC-2	00h	00h	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	Register data	Out CRC-1

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9.5.5.10 WREG Command

Use the WREG command to write register data. Take $\overline{CS1}$ low to access registers within the ADC register block. Take $\overline{CS2}$ low to access registers within the PGA register block (see the *Register Map* section for the register block map). The WREG command writes the register data one byte at a time using the WREG command for each operation. Add the register address (rrh) to the base opcode (40h) to complete the command byte (40h + rrh). 表 25 lists the WREG command byte sequence. Writing to certain registers results in conversion restart. 表 28 lists the affected registers. Do not write to registers outside the address range.

Register-write access is enabled and disabled by the UNLOCK and LOCK commands, respectively. The default mode is register UNLOCK. See the *LOCK Command* section.

表 25. WREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	40h + rrh	Register data	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.11 LOCK Command

Use the LOCK command to lock unintended write operations to the registers. Send the LOCK command using $\overline{CS1}$ to lock registers 00h to 0fh. Use $\overline{CS2}$ to lock registers 10h to 12h. Locking the registers disables register write access including the calibration registers. The default mode is unlocked. Register reads are allowed in LOCK mode. 表 26 lists the LOCK command byte sequence.

表 26. LOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F2h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.12 UNLOCK Command

Use the UNLOCK command to allow writing register data. Send the UNLOCK command using $\overline{CS1}$ to unlock registers 00h to 0fh. Use $\overline{CS2}$ to unlock registers 10h to 12h. Register unlock allows register write access including calibration registers. 表 27 lists the UNLOCK command byte sequence.

表 27. UNLOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F5h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

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9.6 Register Map

表 28 shows the device register map consisting of 19 one-byte registers. Collectively, the registers are used to configure the device to the desired operating mode. Access the registers by using the RREG and WREG commands (register-read and register-write, respectively). Data are accessed one register byte at a time for each command operation. The address of the register corresponds to using either $\overline{CS1}$ or $\overline{CS2}$ for the register command operation. The *CSx* column shows the correlation of $\overline{CS1}$ or $\overline{CS2}$ to the register address. Changing the data of certain registers results in a restart of conversions already in progress. The *Restart* column lists these registers.

表 28. Register Map Summary

ADDRESS	REGISTER	DEFAULT	RESTART	$\overline{CSx}$	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	6xh		$\overline{CS1}$	DEV_ID[3:0]				REV_ID1[3:0]			
01h	STATUS0	01h		$\overline{CS1}$	LOCK1	CRC1	0	STAT12	REFALM	DRDY	CLOCK	RESET
02h	MODE0	24h	Yes	$\overline{CS1}$	DR[4:0]					FILTER[2:0]		
03h	MODE1	01h	Yes	$\overline{CS1}$	0	0	AUTOZERO	CONVRT	DELAY[3:0]			
04h	MODE2	00h		$\overline{CS1}$	GPIO_CON[3:0]				GPIO_DIR[3:0]			
05h	MODE3	00h		$\overline{CS1}$	0	STATENB	0	0	GPIO_DAT[3:0]			
06h	REF	05h	Yes	$\overline{CS1}$	0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
07h	OFCAL0	00h		$\overline{CS1}$	OFC[7:0]							
08h	OFCAL1	00h		$\overline{CS1}$	OFC[15:8]							
09h	OFCAL2	00h		$\overline{CS1}$	OFC[23:16]							
0Ah	FSCAL0	00h		$\overline{CS1}$	FSC[7:0]							
0Bh	FSCAL1	00h		$\overline{CS1}$	FSC[15:8]							
0Ch	FSCAL2	40h		$\overline{CS1}$	FSC[23:16]							
0Dh	I_MUX	FFh		$\overline{CS1}$	I_MUX2[3:0]				I_MUX1[3:0]			
0Eh	I_MAG	00h		$\overline{CS1}$	I_MAG2[3:0]				I_MAG1[3:0]			
0Fh	RESERVED	00h		$\overline{CS1}$	00h							
10h	MODE4	50h		$\overline{CS2}$	0	MUX[2:0]			GAIN[3:0]			
11h	STATUS1	xxh		$\overline{CS2}$	PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
12h	STATUS2	0xh		$\overline{CS2}$	0	0	LOCK2	CRC2	REV_ID2[3:0]			

表 29 lists the access codes for the ADS125H02 registers.

表 29. ADS125H02 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R/W	R-W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.6.1 Device Identification (ID) Register (address = 00h) [reset = 6xh]

ID is shown in 图 82 and described in 表 30.

Return to Register Map Summary.

图 82. ID Register(1)

7	6	5	4	3	2	1	0
DEV_ID[3:0]				REV_ID1[3:0]			
R-6h				R-xh			

(1) Reset values are device dependent.

表 30. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DEV_ID[3:0]	R	6h	**Device ID** 0110 = ADS125H02
3:0	REV_ID1[3:0]	R	xh	**Revision ID1** There are two revision ID fields: REV_ID1 and REV_ID2. The revision IDs can change without notification.

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9.6.2 Main Status (STATUS0) Register (address = 01h) [reset = 01h]

STATUS0 is shown in 图 83 and described in 表 31.

Return to Register Map Summary.

图 83. STATUS0 Register

7	6	5	4	3	2	1	0
LOCK1	CRC1	0	STAT12	REFALM	DRDY	CLOCK	RESET
R-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-xh	R/W-1h

表 31. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOCK1	R	0h	**Register Write Lock1 Status** Indicates the register write lock status of register addresses 00h to 0Fh. See the *LOCK Command* section for details. 0: Registers 00h to 0Fh are not locked (default) 1: Registers 00h to 0Fh are locked See the STATUS2 register for the register lock status of register addresses 10h to 12h.
6	CRC1	R/W	0h	**CRC1 Error** Indicates if a CRC error occurred during commands when $\overline{CS1}$ is active. Write 0 to clear the CRC error. 0: No CRC error during commands using $\overline{CS1}$ 1: CRC error occurred during commands using $\overline{CS1}$ See the STATUS2 register for the CRC error status for commands using $\overline{CS2}$.
5	0	R	0h	**Reserved** Always write 0.
4	STAT12	R	0h	**STAT12 Error Flag** Indicates one or more error events have been logged in the STATUS1 or STATUS2 registers. Read the STATUS1 and STATUS2 registers to determine the error. This bit clears after all errors are cleared. 0: No error 1: Error logged to the STATUS1 or STATUS2 registers
3	REFALM	R	0h	**Reference Voltage Alarm** This bit sets when the reference voltage falls below < 0.4 V (typical). The alarm updates at each new conversion cycle (auto-reset). 0: No reference low alarm 1: Reference low alarm
2	DRDY	R	0h	**Data Ready** Indicates new conversion data. 0: Conversion data are not new since the last data read 1: Conversion data are new since the last data read
1	CLOCK	R	xh	**Clock** Indicates internal or external clock mode. The ADC automatically selects the clock mode. 0: ADC clock is internal 1: ADC clock is external

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表 31. STATUS0 Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
0	RESET	R/W	1h	**Reset** Indicates an ADC reset has occurred. Clear the bit to detect the next device reset. 0: No reset 1: Reset (default)

9.6.3 Mode 0 (MODE0) Register (address = 02h) [reset = 24h]

MODE0 is shown in 图 84 and described in 表 32.

Return to Register Map Summary.

图 84. MODE0 Register

7	6	5	4	3	2	1	0
DR[4:0]					FILTER[2:0]		
R/W-4h					R/W-4h		

表 32. MODE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	DR[4:0]	R/W	4h	**Data Rate** These bits select the data rate. 00000: 2.5 SPS 00001: 5 SPS 00010: 10 SPS 00011: 16.$\overline{6}$ SPS 00100: 20 SPS (default) 00101: 50 SPS 00110: 60 SPS 00111: 100 SPS 01000: 400 SPS 01001: 1200 SPS 01010: 2400 SPS 01011: 4800 SPS 01100: 7200 SPS 01101: 14400 SPS 01110: 19200 SPS 01111: 25600 SPS 10000 - 11111: 40 kSPS (f_{CLK} = 10.24 MHz)
2:0	FILTER[2:0]	R/W	4h	**Digital Filter** (see the *Digital Filter* section) These bits select the digital filter mode. 000: Sinc1 001: Sinc2 010: Sinc3 011: Sinc4 100: FIR (default) 101-111: Reserved

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9.6.4 Mode 1 (MODE1) Register (address = 03h) [reset = 01h]

MODE1 is shown in 图 85 and described in 表 33.

Return to Register Map Summary.

图 85. MODE1 Register

7	6	5	4	3	2	1	0
0	0	AUTOZERO	CONVRT	DELAY[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h			

表 33. MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	0	R/W	0h	**Reserved** Always write 0
5	AUTOZERO	R/W	0h	**Auto-Zero Mode** Select normal or auto-zero operating mods. See the *Auto-Zero Mode* section. 0: Normal mode (default) 1: Auto-zero mode
4	CONVRT	R/W	0h	**Conversion Mode** Select the ADC conversion mode. See the *Conversion Control* section. 0: Continuous conversion mode (default) 1: Pulse (one shot) conversion mode
3:0	DELAY[3:0]	R/W	1h	**Conversion Start Delay** Program the time delay at the start of conversion. See the *Start-Conversion Delay* section. 0000: 0 µs (not for 25600-SPS or 40000-SPS operation) 0001: 50 µs (default) 0010: 59 µs 0011: 67 µs 0100: 85 µs 0101: 119 µs 0110: 189 µs 0111: 328 µs 1000: 605 µs 1001: 1.16 ms 1010: 2.27 ms 1011: 4.49 ms 1100: 8.93 ms 1101: 17.8 ms 1110-1111: Reserved

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9.6.5 Mode 2 (MODE2) Register (address = 04h) [reset = 00h]

MODE2 is shown in 图 86 and described in 表 34.

Return to Register Map Summary.

图 86. MODE2 Register

7	6	5	4	3	2	1	0
GPIO_CON[3:0]				GPIO_DIR[3:0]			
R/W-0h				R/W-0h			

表 34. MODE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_CON[3]	R/W	0h	**GPIO[3] Pin Connection** Connect GPIO[3] to the GPIO3 pin. 0: GPIO[3] not connected to GPIO3 (default) 1: GPIO[3] connected to GPIO3
6	GPIO_CON[2]	R/W	0h	**GPIO[2] Pin Connection** Connect GPIO[2] to the GPIO2 pin. 0: GPIO[2] not connected to GPIO2 (default) 1: GPIO[2] connected to GPIO2
5	GPIO_CON[1]	R/W	0h	**GPIO[1] Pin Connection** Connect GPIO[1] to the REFN1/GPIO1 pin. 0: GPIO[1] not connected to REFN1/GPIO1 (default) 1: GPIO[1] connected to REFN1/GPIO1
4	GPIO_CON[0]	R/W	0h	**GPIO[0] Pin Connection** Connect GPIO[0] to the REFP1/GPIO0 pin. 0: GPIO[0] not connected to REFP1/GPIO0 (default) 1: GPIO[0] connected to REFP1/GPIO0
3	GPIO_DIR[3]	R/W	0h	**GPIO[3] Pin Direction** Configure GPIO[3] as a GPIO input or output to the GPIO3 pin. 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	GPIO_DIR[2]	R/W	0h	**GPIO[2] Pin Direction** Configure GPIO[2] as a GPIO input or output to the GPIO2 pin. 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	GPIO_DIR[1]	R/W	0h	**GPIO[1] Pin Direction** Configure GPIO[1] as a GPIO input or output to the REFN1/GPIO1 pin. 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	GPIO_DIR[0]	R/W	0h	**GPIO[0] Pin Direction** Configure GPIO[0] as a GPIO input or output to the REFP1/GPIO0 pin. 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

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9.6.6 Mode 3 (MODE3) Register (address = 05h) [reset = 00h]

MODE3 is shown in 图 87 and described in 表 35.

Return to Register Map Summary.

图 87. MODE3 Register

7	6	5	4	3	2	1	0
0	STATENB	0	0	GPIO_DAT[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

表 35. MODE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0h.
6	STATENB	R/W	0h	**STATUS0 Byte Enable** Enable the STATUS0 byte contents for inclusion during conversion data read operation. 0: Exclude STATUS0 byte during conversion data read (default) 1: Include STATUS0 byte during conversion data read
5:4	0	R/W	0h	**Reserved** Always write 0h.
3	GPIO_DAT[3]	R/W	0h	**GPIO[3] Data** Read or write the GPIO data on the GPIO3 pin. 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	GPIO_DAT[2]	R/W	0h	**GPIO[2] Data** Read or write the GPIO data on the GPIO2 pin. 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	GPIO_DAT[1]	R/W	0h	**GPIO[1] Data** Read or write the GPIO data on the REFN1/GPIO1 pin. 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	GPIO_DAT[0]	R/W	0h	**GPIO[0] Data** Read or write the GPIO data on the REFP1/GPIO0 pin. 0: GPIO[0] is low (default) 1: GPIO[0] is high

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9.6.7 Reference Configuration (REF) Register (address = 06h) [reset = 05h]

REF is shown in 图 88 and described in 表 36.

Return to Register Map Summary.

图 88. REF Register

7	6	5	4	3	2	1	0
0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-1h	

表 36. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	0	R/W	0h	**Reserved** Always write 0h.
4	REFENB	R/W	0h	**Internal Reference Enable** Enable the internal reference. 0: Internal reference disabled (default) 1: Internal reference enabled
3:2	RMUXP[1:0]	R/W	1h	**Reference Positive Input** (see the *Reference Voltage* section) Select the positive reference input. 00: Internal reference positive 01: AVDD (default) 10: REFP0 external 11: REFP1/GPIO0 external
1:0	RMUXN[1:0]	R/W	1h	**Reference Negative Input** (see the *Reference Voltage* section) Select the negative reference input. 00: Internal reference negative 01: AGND (default) 10: REFN0 external 11: REFN1/GPIO1 external

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9.6.8 Offset Calibration (OFCALx) Registers (address = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

OFCALx is shown in 图 89 and described in 表 37.

Return to Register Map Summary.

图 89. OFCAL0, OFCAL1, OFCAL2 Registers

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

表 37. OFCAL0, OFCAL1, OFCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration** These three registers are the 24-bit offset calibration word. The offset calibration is in two's-complement data format. The offset value is subtracted from the conversion result before the full-scale operation.

9.6.9 Full-Scale Calibration (FSCALx) Registers (address = 0Ah, 0Bh, 0Ch) [reset = 00h, 00h, 40h]

FSCALx is shown in 图 90 and described in 表 38.

Return to Register Map Summary.

图 90. FSCAL0, FSCAL1, FSCAL2 Registers

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSCAL[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSCAL[23:16]							
R/W-40h							

表 38. FSCAL0, FSCAL1, FSCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	FSCAL[23:0]	R/W	400000h	**Full-Scale Calibration** These three registers are the 24-bit full-scale calibration word. The full-scale calibration is in straight binary data format. The full-scale value is divided by 400000h and multiplied with the conversion data. The scaling operation occurs after the offset operation.

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9.6.10 Current Source Multiplexer (I_MUX) Register (address = 0Dh) [reset = FFh]

I_MUX is shown in 图 91 and described in 表 39.

Return to Register Map Summary.

图 91. I_MUX Register

7	6	5	4	3	2	1	0
I_MUX2[3:0]				I_MUX1[3:0]			
R/W-Fh				R/W-Fh			

表 39. I_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I_MUX2[3:0]	R/W	Fh	**Current Source 2 Output Multiplexer** These bits select the IDAC2 pin connection. 0000-0111: No connection 1000: Connect current source 2 to pin IDAC1 1001: Connect current source 2 to pin IDAC2 1010-1111: No connection (default = 1111)
3:0	I_MUX1[3:0]	R/W	Fh	**Current Source 1 Output Multiplexer** These bits select the IDAC1 pin connection. 0000-0111: No connection 1000: Connect current 1 to pin IDAC1 1001: Connect current 1 to pin IDAC2 1010-1111: No connection (default = 1111)

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9.6.11 Current Source Magnitude (I_MAG) Register (address = 0Eh) [reset = 00h]

I_MAG is shown in 图 92 and described in 表 40.

Return to Register Map Summary.

图 92. I_MAG Register

7	6	5	4	3	2	1	0
I_MAG2[3:0]				I_MAG1[3:0]			
R/W-0h				R/W-0h			

表 40. I_MAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I_MAG2[3:0]	R/W	0h	**Current Source 2 Magnitude** These bits select current source 2 magnitude. 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011-1111: Off
3:0	I_MAG1[3:0]	R/W	0h	**Current Source 1 Magnitude** These bits select current source 1 magnitude. 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011-1111: Off

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9.6.12 Reserved (RESERVED) Register (address = 0Fh) [reset = 00h]

RESERVED is shown in 图 93 and described in 表 41.

Return to Register Map Summary.

图 93. RESERVED Register

7	6	5	4	3	2	1	0
00h							
R/W-00h							

表 41. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	0	R	0h	**Reserved bits** Always write 00h.

9.6.13 MODE4 (MODE4) Register (address = 10h) [reset = 50h]

MODE4 is shown in 图 94 and described in 表 42.

Return to Register Map Summary.

图 94. MODE4 Register

7	6	5	4	3	2	1	0
0	MUX[2:0]			GAIN[3:0]			
R/W-0h	R/W-5h			R/W-0h			

表 42. MODE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0h	**Reserved** Always write 0h.
6:4	MUX[2:0]	R/W	5h	**Input Multiplexer** These bits set the input multiplexer control. 000: AIN1 – AIN0 001: AIN0 – AIN1 010: AIN1 – AINCOM 011: AIN0 – AINCOM 100: HV supply readback (HV_AVDD – HV_AVSS) / 36 101: Internal short to V_{COM} (HV_AVDD + HV_AVSS) / 2 (default) 110: Temperature sensor reading 111: Reserved (do not use)

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表 42. MODE4 Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
3:0	GAIN[3:0]	R/W	0h	**PGA Gain** These bits set the PGA gain setting. 0000: 0.125 (default) 0001: 0.1875 0010: 0.25 0011: 0.5 0100: 1 0101: 2 0110: 4 0111: 8 1000: 16 1001: 32 1010: 64 1011: 128 1100-1111: reserved

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9.6.14 PGA Alarm (STATUS1) Register (address = 11h) [reset = xxh]

STATUS1 is shown in 图 95 and described in 表 43.

Return to Register Map Summary.

图 95. STATUS1 Register

7	6	5	4	3	2	1	0
PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
R-xxh							

表 43. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGA_ONL	R	xh	**PGA Output Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
6	PGA_ONH	R	xh	**PGA Output Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
5	PGA_OPL	R	xh	**PGA Output Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
4	PGA_OPH	R	xh	**PGA Output Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
3	PGA_INL	R	xh	**PGA Input Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
2	PGA_INH	R	xh	**PGA Input Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
1	PGA_IPL	R	xh	**PGA Input Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
0	PGA_IPH	R	xh	**PGA Input Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active

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9.6.15 Status 2 (STATUS2) Register (address = 12h) [reset = 0xh]

STATUS2 is shown in 图 96 and described in 表 44.

Return to Register Map Summary.

图 96. STATUS2 Register

7	6	5	4	3	2	1	0
0	0	LOCK2	CRC2	REV_ID2[3:0]			
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-xh			

表 44. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	0	R/W	0h	**Reserved** Always write 0.
5	LOCK2	R	0h	**Register Write Lock2 Status** Indicates the register write lock status of registers 10h to 12h. See the *LOCK Command* section for details. 0: Registers 10h to 12h are not locked (default) 1: Registers 10h to 12h are locked See the STATUS2 register for the register write lock status of registers 00h to 0fh.
4	CRC2	R/W	0h	**CRC2 Error** Indicates if a CRC error occurred during commands with $\overline{CS2}$. The CRC error is latched until cleared by the user. Write 0 to clear the error. 0: No CRC error during commands with $\overline{CS2}$ 1: CRC error occurred during commands with $\overline{CS2}$
3:0	REV_ID2[3:0]	R	x	**Revision ID2** Revision ID 2 field. The revision ID1 and ID2 can change without notification.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Input Range

Linear operation of the PGA requires that the absolute input voltage does not exceed the specified range. The following example shows how to verify the absolute input voltage is within the valid range. In this example, the input signal is ±10 V with an arbitrary 15% overrange capability. The negative input lead of the sensor is connected to AGND. The ADC gain is 0.1875 using a 2.5-V reference voltage and ±15-V power supplies with 5% voltage tolerance. The summary of conditions to verify the ADC range are:

- $V_{(AINx\_MAX)}$ = 11.5 V
- $V_{(AINx\_MIN)}$ = –11.5 V
- $V_{(AINCOM)}$ = AGND
- HV_AVDD = 14.25 V
- HV_AVSS = –14.25 V
- Gain = 0.1875
- V_{REF} = 2.5 V

The evaluation of 公式 5 (for gain < 1) results in:

–11.75 V < –11.5 V and 11.5 V < **11.75 V**

The inequality is satisfied, and as a result, the absolute input voltage is within the ADC input range requirement.

10.1.2 Input Overload

The input overvoltage precautions as described in the *ESD Diodes* section. If an overvoltage condition occurs on an unused channel, the overvoltage channel may crosstalk to the measurement channel. One solution, as shown in 图 97, is to externally clamp the inputs with low-forward voltage diodes. The external diodes shunt the overvoltage current flow around the ADC inputs. Be aware of the reverse leakage current that can cause measurement errors.

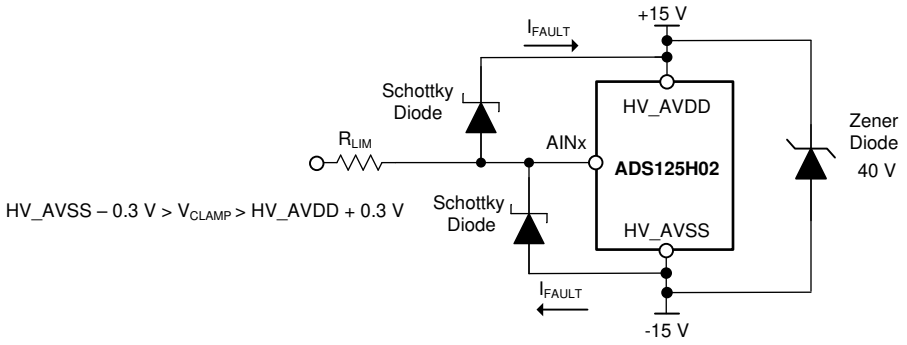

图 97. Optional Diode Clamps

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Application Information (接下页)

10.1.2.1 Input Signal Rate of Change (dV/dt)

A high dV/dt signal at the ADC input can lead to transient turn-on of the PGA inverse-parallel protection diodes (see 图 57 for details). Turn-on of the PGA diodes can result in current flow in the analog inputs that can cause a disturbance in the measurement channel. For example, a high dV/dt voltage can be generated at the output of a signal multiplexer after a channel selection, leading to a possible flow of transient currents through the ADC inputs. Filter the ADC input voltage to limit the rate of voltage change (dV/dt).

10.1.3 Unused Inputs and Outputs

- **Analog Inputs**

  To minimize input current leakage, connect unused analog inputs to AGND when operating the device with bipolar supplies, or connect unused inputs to AVDD when operating the device with a unipolar supply.
- **Analog Outputs**

  A capacitor is not required for REFOUT if the internal reference or the IDAC current sources are not used. Otherwise, connect a 10-µF capacitor between REFOUT and AGND.
- **Digital I/O**

  ADC operation is possible using only a subset of the digital I/O. Tie any unused digital inputs high or low (DVDD or DGND, as appropriate). Do not float (tri-state) the digital inputs or unpredictable operation can result. The following is a summary of digital I/O with optional connections:
  - **CLKIN:** Tie CLKIN to DGND to operate the ADC using the internal oscillator. The internal oscillator stops operation if CLKIN is connected to DVDD, resulting in loss of ADC functionality. Connect CLKIN to an external clock source to operate with an external clock.
  - **START:** Tie START low in order to control conversions entirely by command. Tie START high to free-run conversions when programmed to the continuous-conversion mode. Connect START to the host controller to control conversions directly by the pin.
  - **$\overline{\text{RESET}}$:** Tie $\overline{\text{RESET}}$ high if desired. An external RC reset on the $\overline{\text{RESET}}$ input pin is not necessary because the ADC resets at power on. The ADC can also be reset by the RESET command. Connect the $\overline{\text{RESET}}$ pin to the host controller to reset the ADC by hardware.
  - **$\overline{\text{DRDY}}$:** Indication of data ready is also provided by the DOUT/$\overline{\text{DRDY}}$ pin. $\overline{\text{CS1}}$ must be low to use DOUT/$\overline{\text{DRDY}}$ in the data-ready function. The indication of data ready is also achieved by polling the DRDY bit of the STATUS0 byte. For these methods, the connection of $\overline{\text{DRDY}}$ to the host controller is not necessary and the pin can be unconnected.
- **GPIO**

  Program unused GPIOs as outputs (default setting). If any GPIOs are programmed as inputs, the GPIO must not be allowed to float (unconnected), otherwise AVDD power-supply leakage current may result.

10.2 Typical Applications

10.2.1 ±10-V Analog Input Module

图 98 illustrates an example of the ADS125H02 used in a ±10-V analog input programmable logic controller (PLC) module. The inputs of the ADC are protected by external ESD diodes to provide system-level protection. A 100-MΩ resistor is used to pull the positive analog input to 15 V if the field-wiring connection is open or the transmitter has failed in open-circuit mode.

The signal from the transmitter is filtered to remove EMI and RFI interference when operated in noisy environments. The resistor also acts to limit the input current in the event of an input overvoltage, including if the module loses power with the signal present. The negative input signal is connected to AIN0, which is also connected to AGND. Connection to AGND is necessary if the sensor power supply is not referenced to the ADC ground.

The ADC measures the differential voltage between inputs AIN1 and AIN0. The input configuration is single-ended with the input voltage driven ±10 V relative to AIN0 (AGND).

Operation by internal reference requires a 10-µF capacitor connected to the REFOUT pin. Otherwise, apply the external reference voltage to REFP0 and REFN0. A 100-kΩ resistor biases the differential reference voltage to 0 V. The resistor provides the bias to allow the reference monitor to detect a failed or missing reference voltage that otherwise may be unnoticed.

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Typical Applications (接下页)

Because the excitation current sources and GPIOs are not used they are left unconnected.

The internal oscillator is selected by connecting the CLKIN input pin to ground. The serial interface and digital control lines of the ADC are connected to the host.

The zener diode clamps the high-voltage supply (HV_AVDD – HV_AVSS) to 40 V to provide overvoltage protection if an input signal is present with module power off.

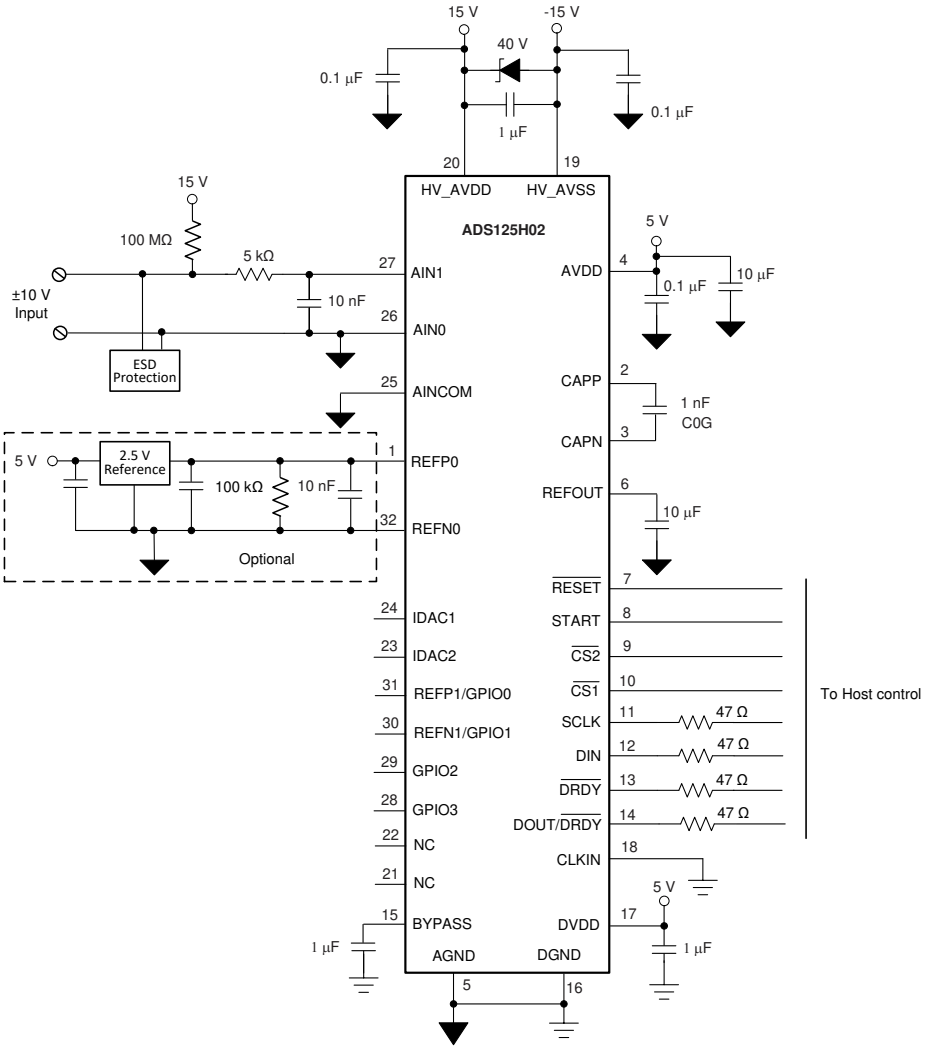

图 98. ±10-V Analog Input PLC Module

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Typical Applications (接下页)

10.2.1.1 Design Requirements

表 45 shows the design goals of the analog input PLC module. The ADC programmability allows various tradeoffs of sample rate, conversion noise, and conversion latency. 表 46 shows the design parameters of the analog input PLC module.

表 45. Design Goals

DESIGN GOAL	VALUE
Accuracy	±0.1%
Temperature range (internal module)	0°C to +105°C
Acquisition period	50 µs
Effective resolution	18 bits

表 46. Design Parameters

DESIGN PARAMETER	VALUE
Nominal signal range	±10 V
Extended range	±12 V
Input impedance	100 MΩ
Overvoltage rating	±35 V

10.2.1.2 Detailed Design Procedure

A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This example assumes the initial offset and gain (including reference voltage error) are user calibrated at T_A = 25°C. 表 47 shows the maximum drift error of the ADC over the 0°C to +105°C temperature range.

表 47. ADC Drift Error

PARAMETER		ERROR (0°C TO +105°C)
Offset drift error		0.00125%
Gain drift error		0.032%
Linearity error (over temperature)		0.001%
Reference drift error	ADS125H02 internal reference	0.16%
	REF5025IDGK external reference	0.024%
Total drift error	ADS125H02 internal reference	0.19425%
	REF5025IDGK external reference	0.05825%

As shown in 表 47, the largest error is from the internal voltage reference. The reference drift error is improved by using the REF5025IDGK external reference. Using the external reference, the total drift error is 0.05825%, which satisfies the 0.1% total error design goal.

The ADC gain is programmed to 0.1875. With a 2.5-V reference voltage, the ADC input range is ±2.5 V / 0.1875 = ±13.3 V. However, using ±15-V power supplies, the required headroom of the PGA limits the range to ±12.5 V (which excludes the tolerance of the ±15-V power supplies). The input range satisfies the extended range design target of ±12 V.

The 1-GΩ minimum input impedance of the ADC and the 100-MΩ external pullup resistor meets the input impedance goal of 100 MΩ. The input fault overvoltage requirement (35 V) is met by limiting the ADC input current to 10 mA. The external 5-kΩ input resistor limits the input current to 7 mA.

The data rate that meets the continuos conversion, 50-µs acquisition period is 25600 SPS (39 µs actual). If a precise 50-µs conversion period is desired, reduce the clock frequency to the ADC with an external clock source. The clock frequency that yields a 50-µs conversion period is 5.76 MHz.

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表 1 lists noise performance data under all combinations of gain, sample rate, and digital filter order. The specified conversion noise for the ADC configuration in this example is 100 μV_{RMS}. The effective resolution is derived by 公式 1, and calculates to: 3.32 log (26.6 V / 100 µV) = 18 bits.

10.2.1.3 Application Curves

图 99 shows 100,000 consecutive conversions over a four-second interval with the ADC inputs shorted using the ADC configuration given in this example. 100,000 conversions demonstrate the consistency of the ADC conversion results over time. The conversion noise in this example is 107 μV_{RMS}. The effective resolution calculates to 18 bits, which meets the design requirement.

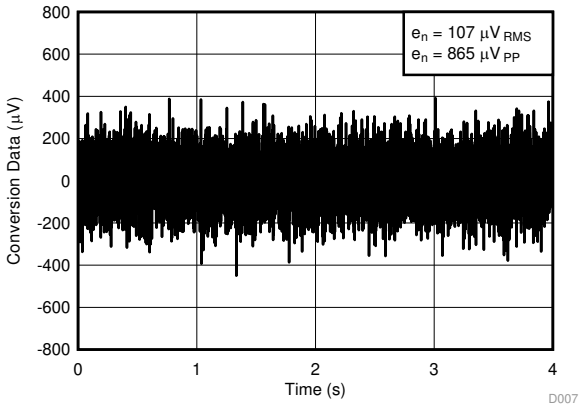

图 99. Conversion Noise

10.2.2 Thermocouple Input With High Common-Mode Voltage

The low noise and low drift performance, 50-Hz and 60-Hz noise rejection, and high common-mode voltage range of the ADS125H02 make the device suitable for multiple thermocouple inputs that have varying levels of common-mode voltage. The common-mode voltage can be AC (50-Hz or 60-Hz noise pickup) or DC caused by varying ground potentials encountered in industrial machinery. 图 100 shows a simplified application of an 8-input, isolated ground, thermocouple module using an external 8:1 differential input multiplexer. The GPIO of the ADS125H02 drives the mux select pins.

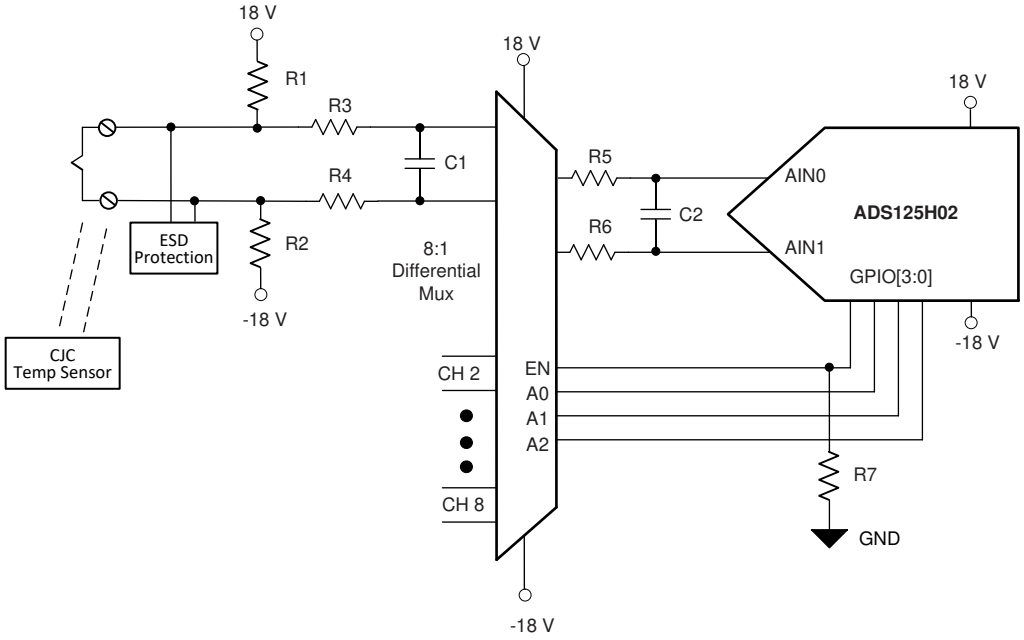

图 100. Thermocouple Input

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10.3 Initialization Setup

图 101 shows a general configuration and measurement procedure.

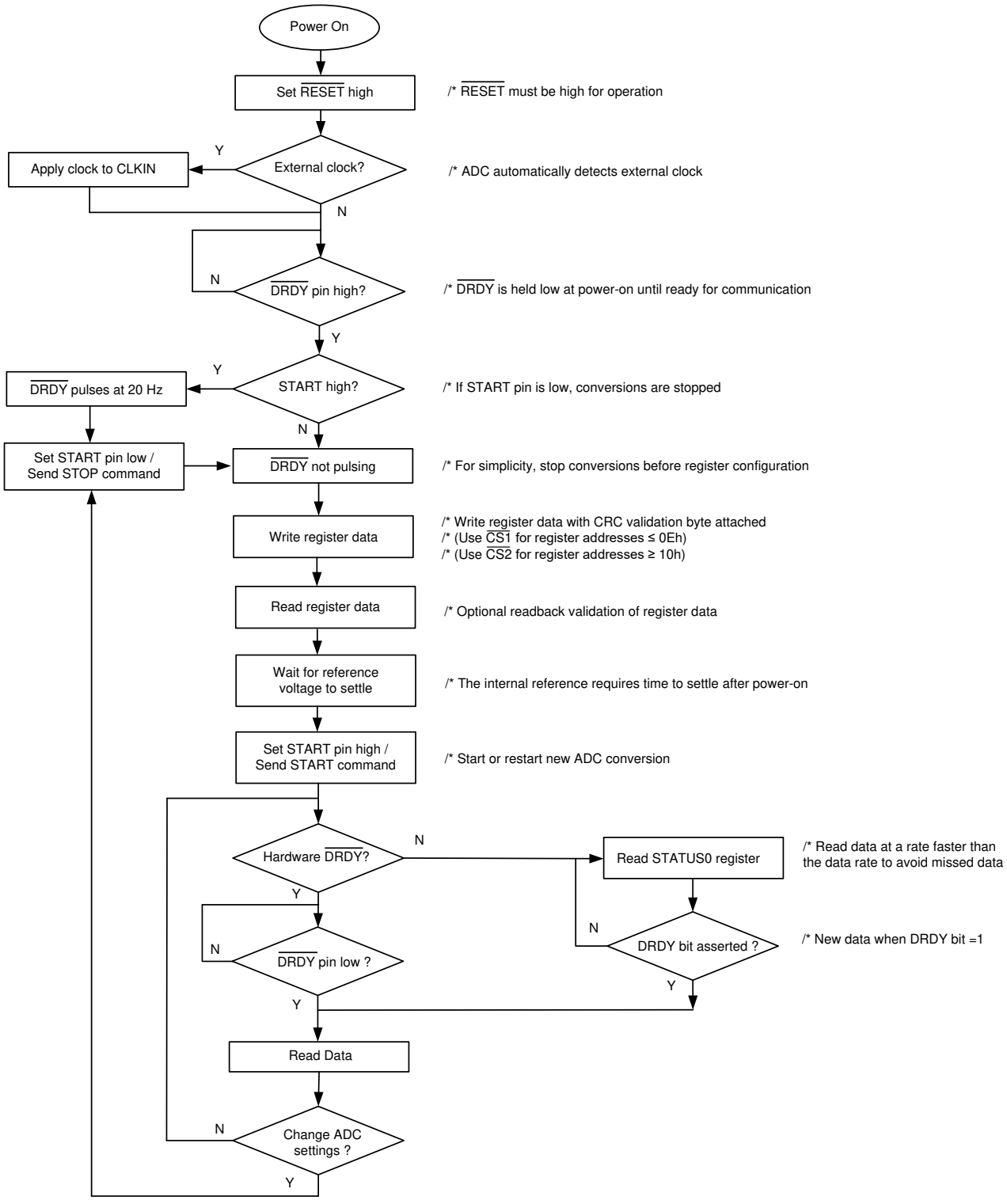

图 101. ADC Configuration and Measurement Procedure

11 Power Supply Recommendations

The ADC requires three analog power supplies (high-voltage supplies HV_AVDD and HV_AVSS, and low-voltage AVDD) and a digital power supply (DVDD). The high-voltage analog power-supply configuration is either bipolar (±5 V to ±18 V) or unipolar (10 V to 36 V). The AVDD power supply is 5 V. The digital supply range is 2.7 V to 5.25 V. AVDD and DVDD can be tied together as long as the 5-V power supply is free from noise and glitches that can affect conversion results. An internal low-dropout regulator (LDO) powers the digital core from the DVDD power supply. DVDD is the digital I/O voltage. Keep in mind that the GPIOs are referenced to AVDD and AGND voltage potentials.

Voltage ripple produced by switch-mode power supplies can interfere with the ADC conversion accuracy. Use LDOs at the switching regulator output to reduce power-supply ripple.

Inrush current is drawn from AVDD when the internal reference is enabled as a result of charging the 10-µF REFOUT capacitor. Observe the AVDD voltage under this condition and verify the supply does not drop below 4.5 V.

11.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve optimum performance. Power supplies must be decoupled close to the device supply pins. For the high voltage analog supply (HV_AVDD and HV_AVSS), place a 1-µF capacitor between the pins and place 0.1-µF capacitors from each supply to the ground plane. Connect 0.1-µF and 10-µF capacitors in parallel at AVDD to the ground plane. Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and equivalent series inductance (ESL) characteristics for power-supply decoupling purposes.

11.2 Analog Power-Supply Clamp

Circumstances must be evaluated when an input signal is present when the ADC is unpowered. When the input signal exceeds the forward voltage of the ESD diodes, the diodes conduct resulting in backdrive of the analog power-supply voltage through the internal ESD diodes. Backdriving the ADC power supply can also occur when the power-supply is on. The backdrive fault-current path is illustrated in 图 97. Depending on the power supply response during a backdrive condition, the ADC supply voltage rating may be exceeded. The ADC maximum-rated supply voltage must not be exceeded under any condition. One solution is to clamp the analog supply using a Zener diode placed across HV_AVSS and HV_AVDD.

11.3 Power-Supply Sequencing

The power supplies can be sequenced in any order, but do not allow analog or digital voltage inputs to exceed the respective analog or digital power supplies without limiting the input current.

11.4 5-V to ±15-V DC-DC Converter

图 102 illustrates a 5-V to ±15-V DC/DC converter for use with the device. The DC/DC converter generates ±15-V supply voltages from 5-V power. The SN6505B is a push-pull driver that drives the transformer primary from 5-V power. The typical switching frequency of the driver is 424 kHz, and when combined with the driver spread-spectrum clocking operation, reduces interference to the ADC as well as system-level EMI emissions. The secondary voltage of the 2:1 step-up transformer is half-wave rectified in a configuration that quadruples the 5-V primary voltage to generate output voltages of 20 V and –20 V. The rectified voltages are regulated by the TPS7A39 high-PSRR, dual positive and negative regulator to provide the ±15-V supply voltages.

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5-V to ±15-V DC-DC Converter (接下页)

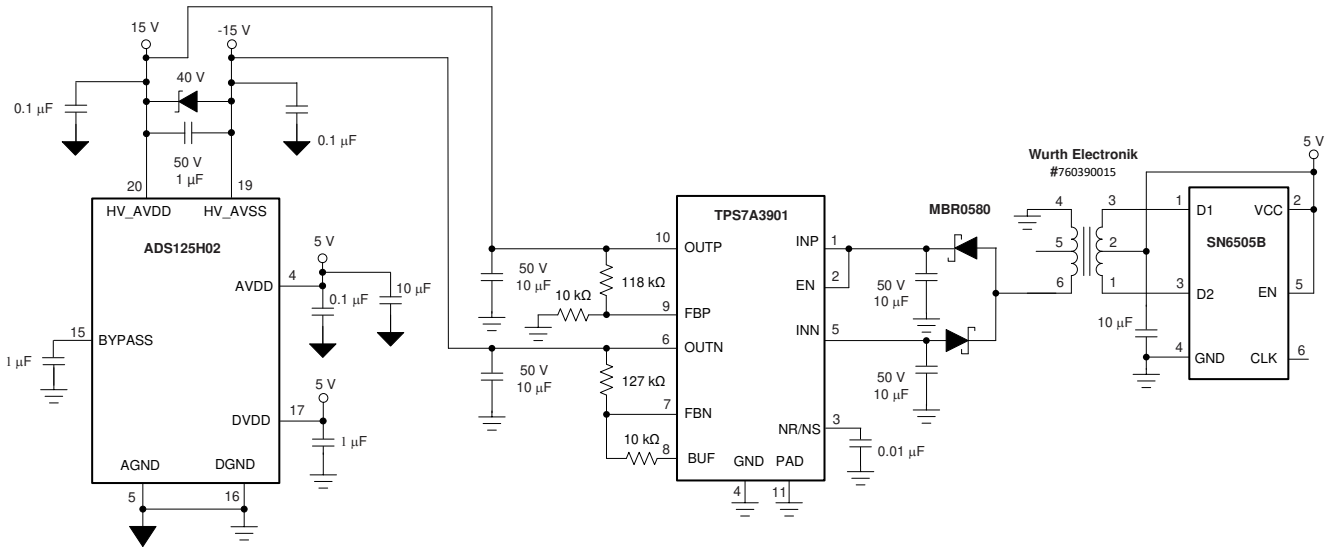

图 102. 5-V to ±15-V DC/DC Converter

12 Layout

12.1 Layout Guidelines

Good layout practices are crucial to realize the full performance of the ADC. Poor grounding can quickly degrade the noise performance. This section discusses layout recommendations that help provide the best results.

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on layout restrictions, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a single, direct connection to the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from the CAPP and CAPN pins, away from the REFOUT pin, and away from all analog inputs and associated components in order to minimize interference.

Because large capacitance on DOUT/$\overline{\text{DRDY}}$ can lead to increased ADC noise levels, minimize the length of the PCB trace. Use a series resistor or a buffer if long traces are used.

The internal reference output return is the AGND pin. To minimize coupling between the power supply and reference-return trace, route the traces separately; ideally, as a star connection to the AGND pin.

Use C0G capacitors on the analog inputs and for the CAPP to CAPN capacitor. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. The REFOUT pin requires a 10-µF capacitor and can be either ceramic or tantalum type. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections with multiple vias on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noisy conversion data.

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12.2 Layout Example

图 103 shows an example layout of the ADS125H02, requiring a minimum of three PCB layers. The example circuit is shown with bipolar supply operation (such as ±15 V) and using the internal reference. In this example, the inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, dedicate an additional inner layer for the power planes. In this example, the ADC is oriented in such a way to minimize crossover of the analog and digital signal traces.

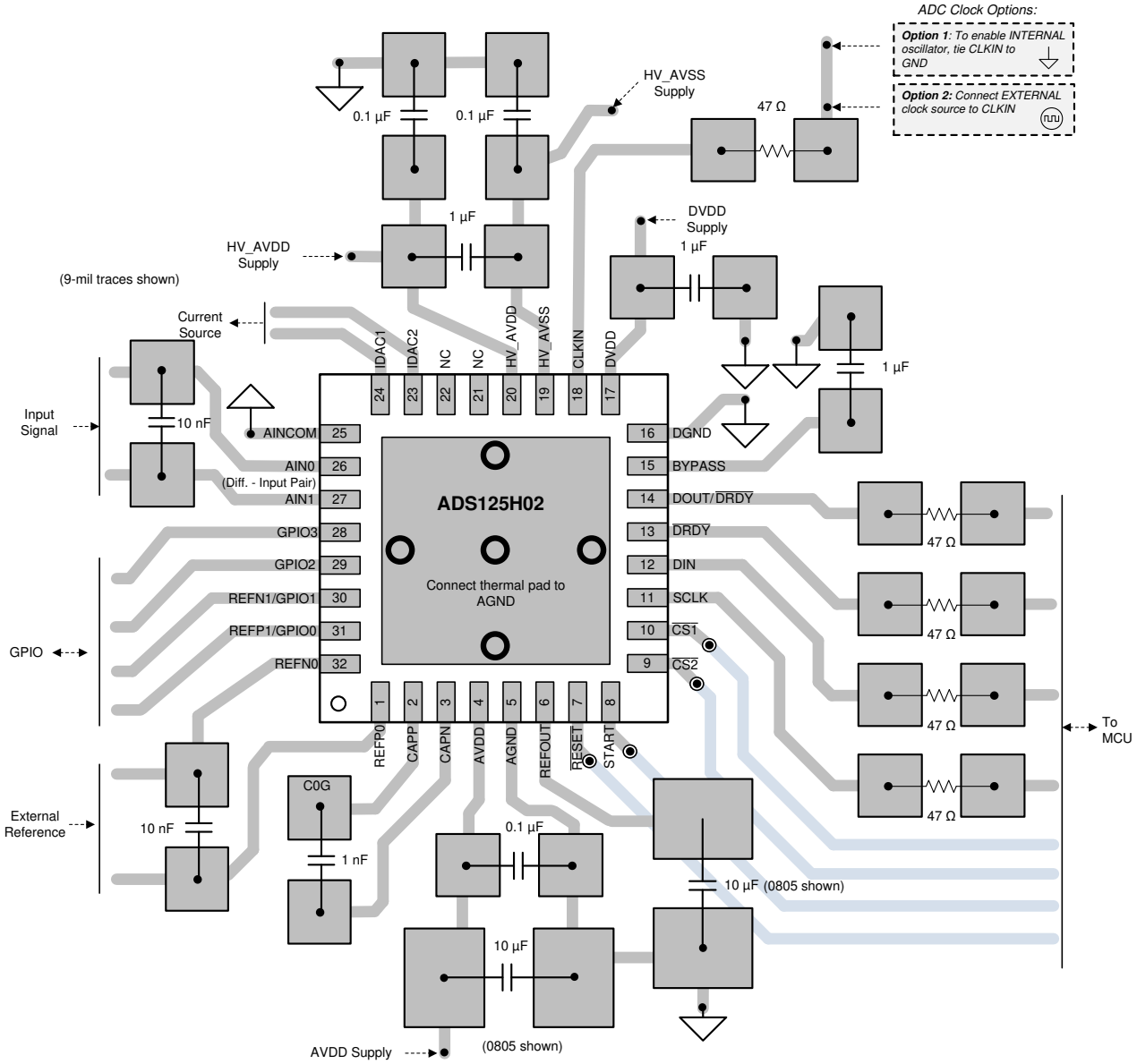

图 103. PCB Layout Example

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13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《REF50xx 低噪声、极低漂移、精密电压基准》数据表*
- 德州仪器 (TI)，*《用于隔离电源的 SN6505x 低噪声 1A 变压器驱动器》数据表*
- 德州仪器 (TI)，*《TPS7A39 双路、150mA、宽输入电压正负 LDO 稳压器》数据表*

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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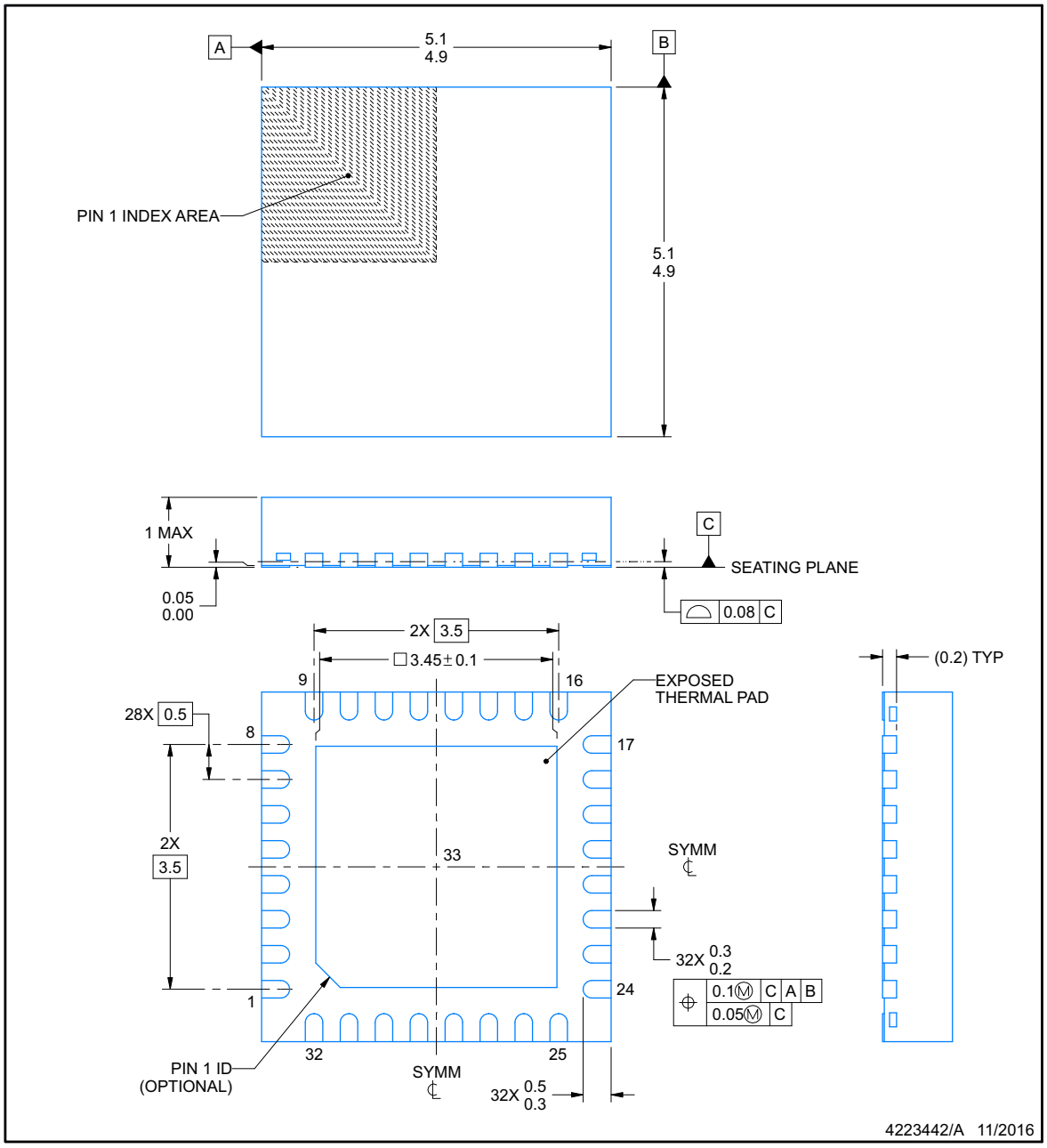
PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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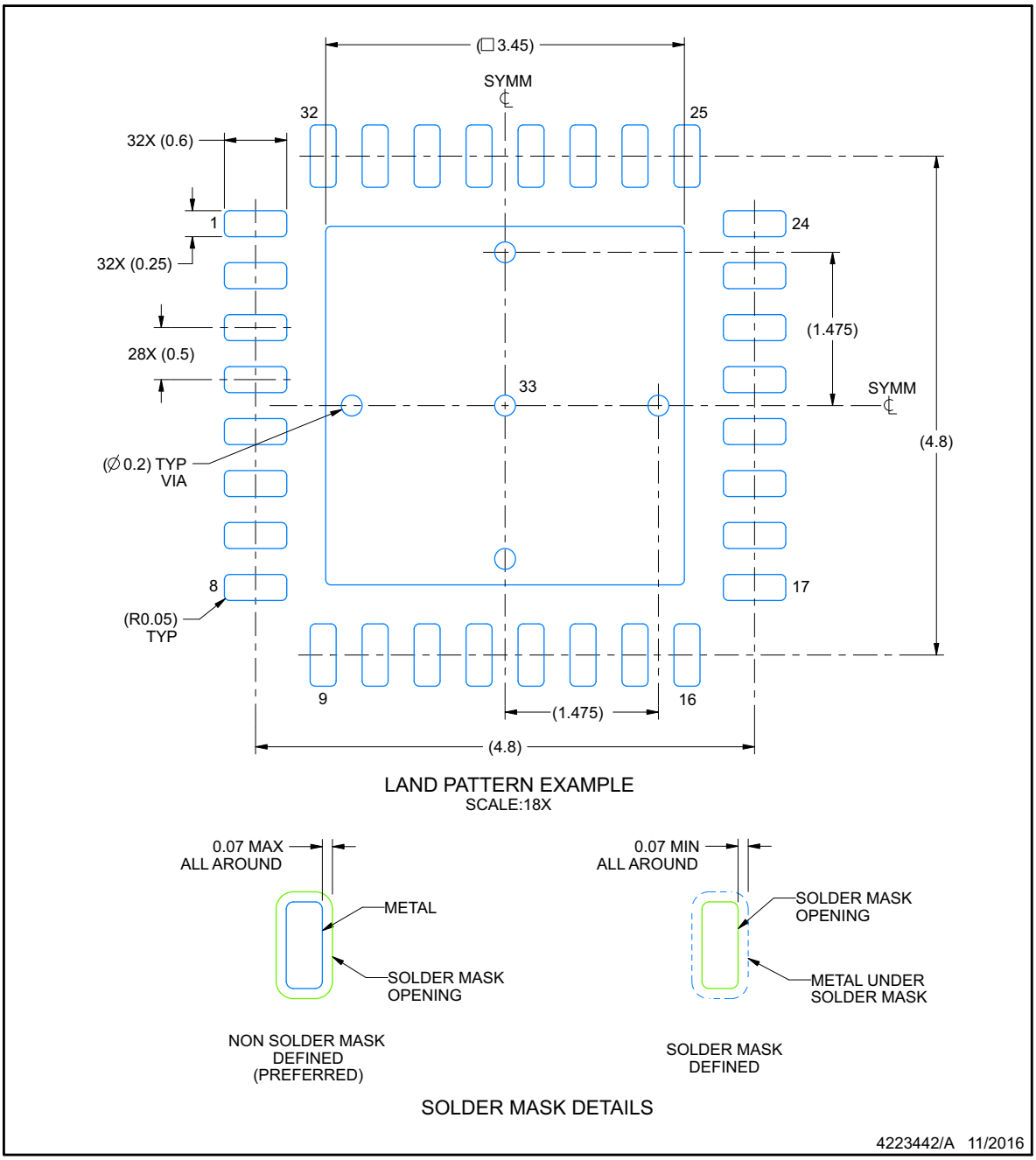
EXAMPLE BOARD LAYOUT

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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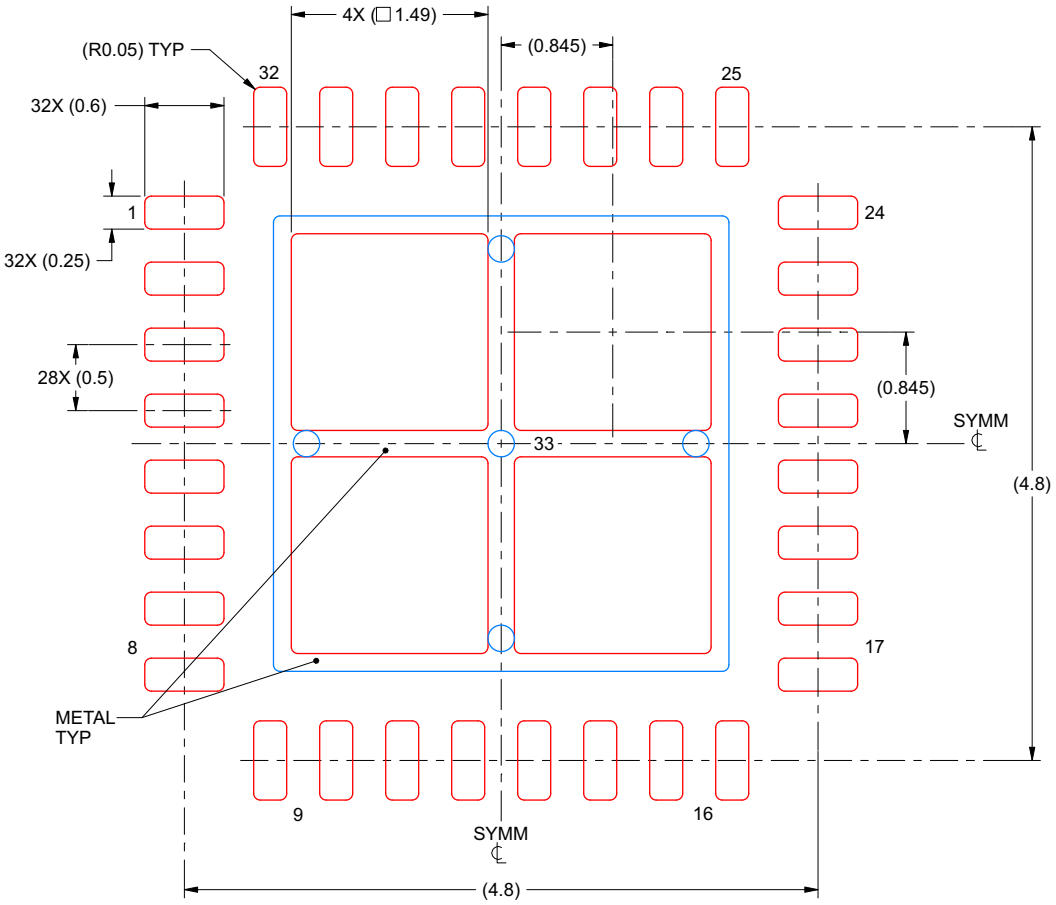
EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS125H02IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 125H02	Samples
ADS125H02IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 125H02	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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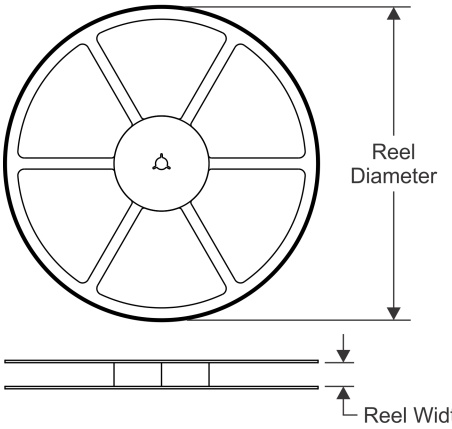
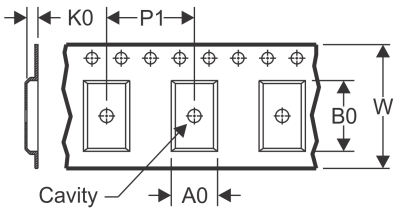
REEL DIMENSIONS

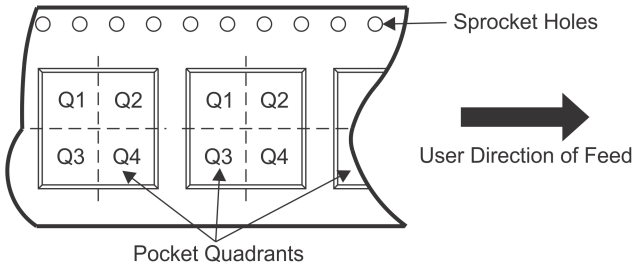


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

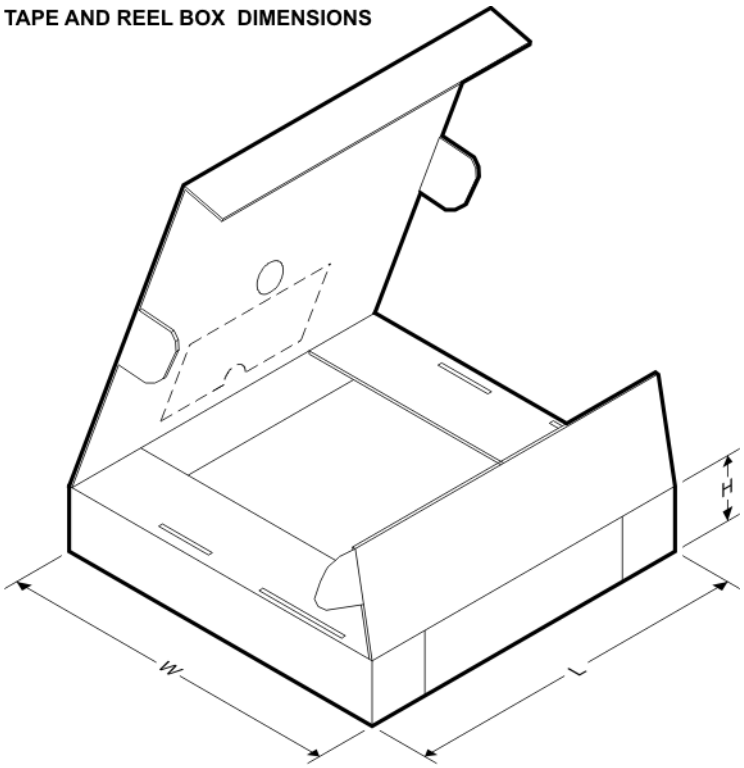
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS125H02IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS125H02IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS125H02IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS125H02IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

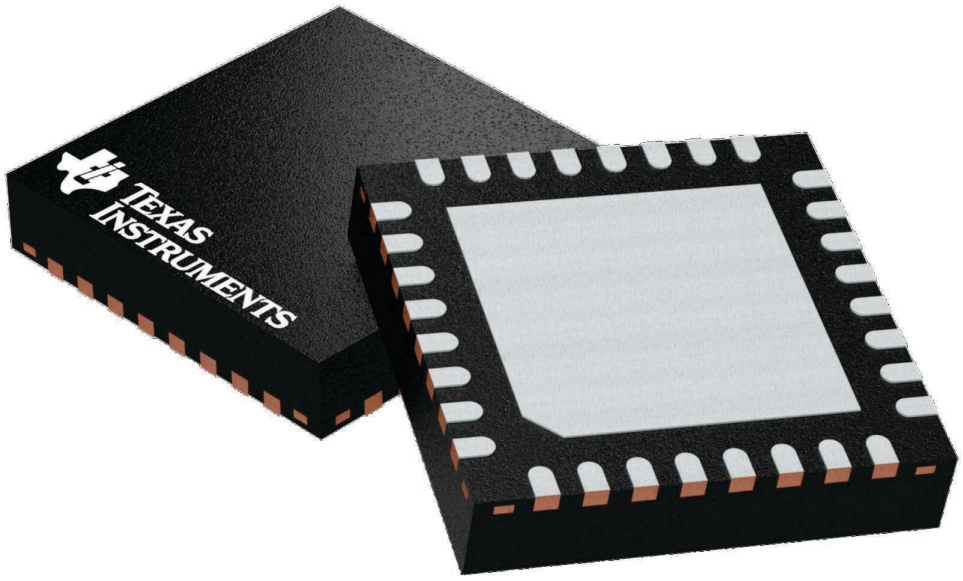
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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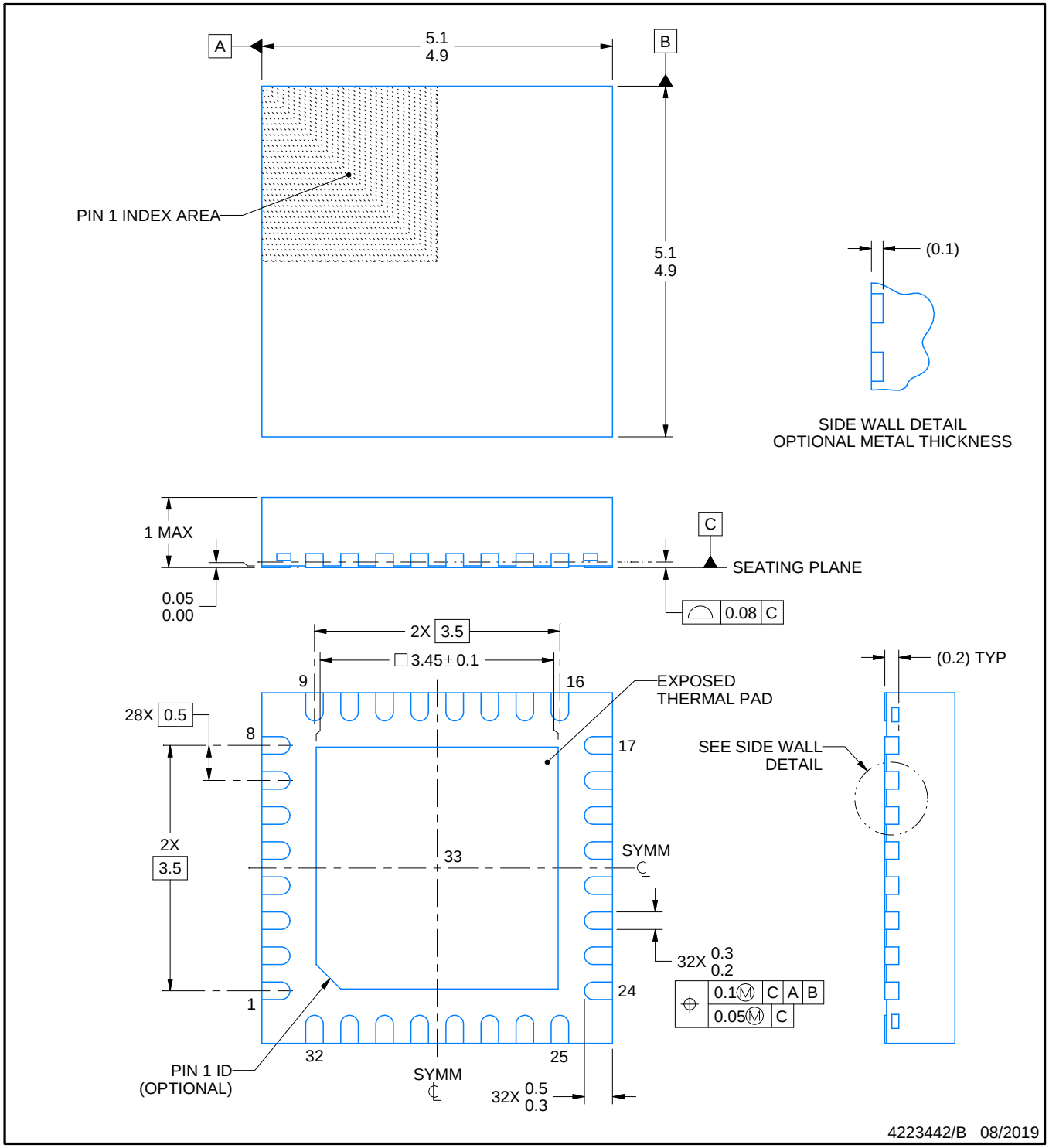
RHB0032E

PACKAGE OUTLINE

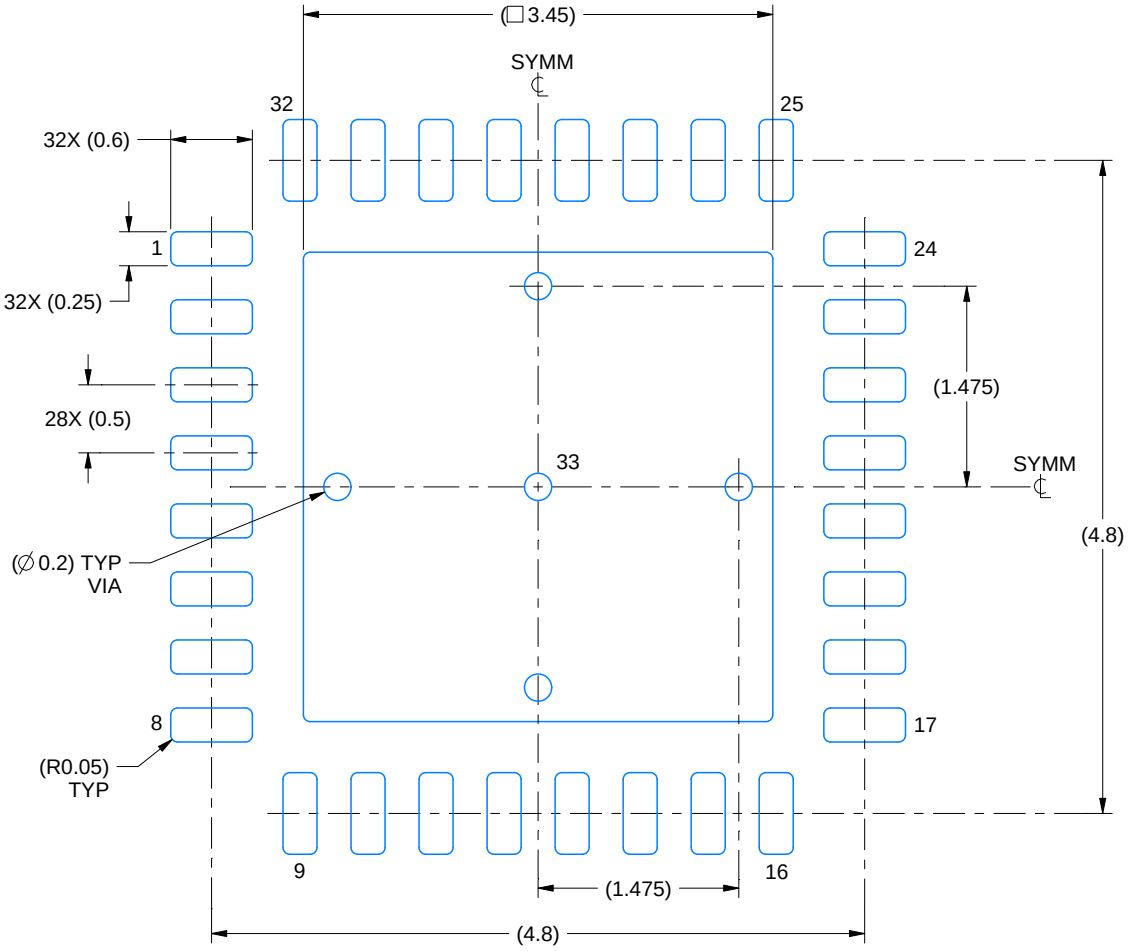
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

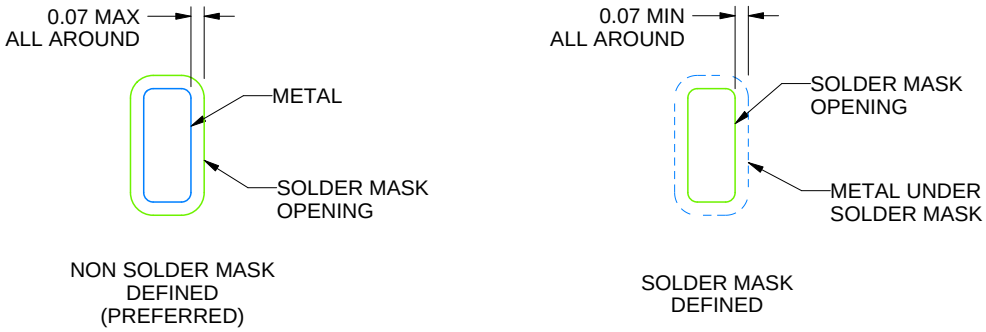


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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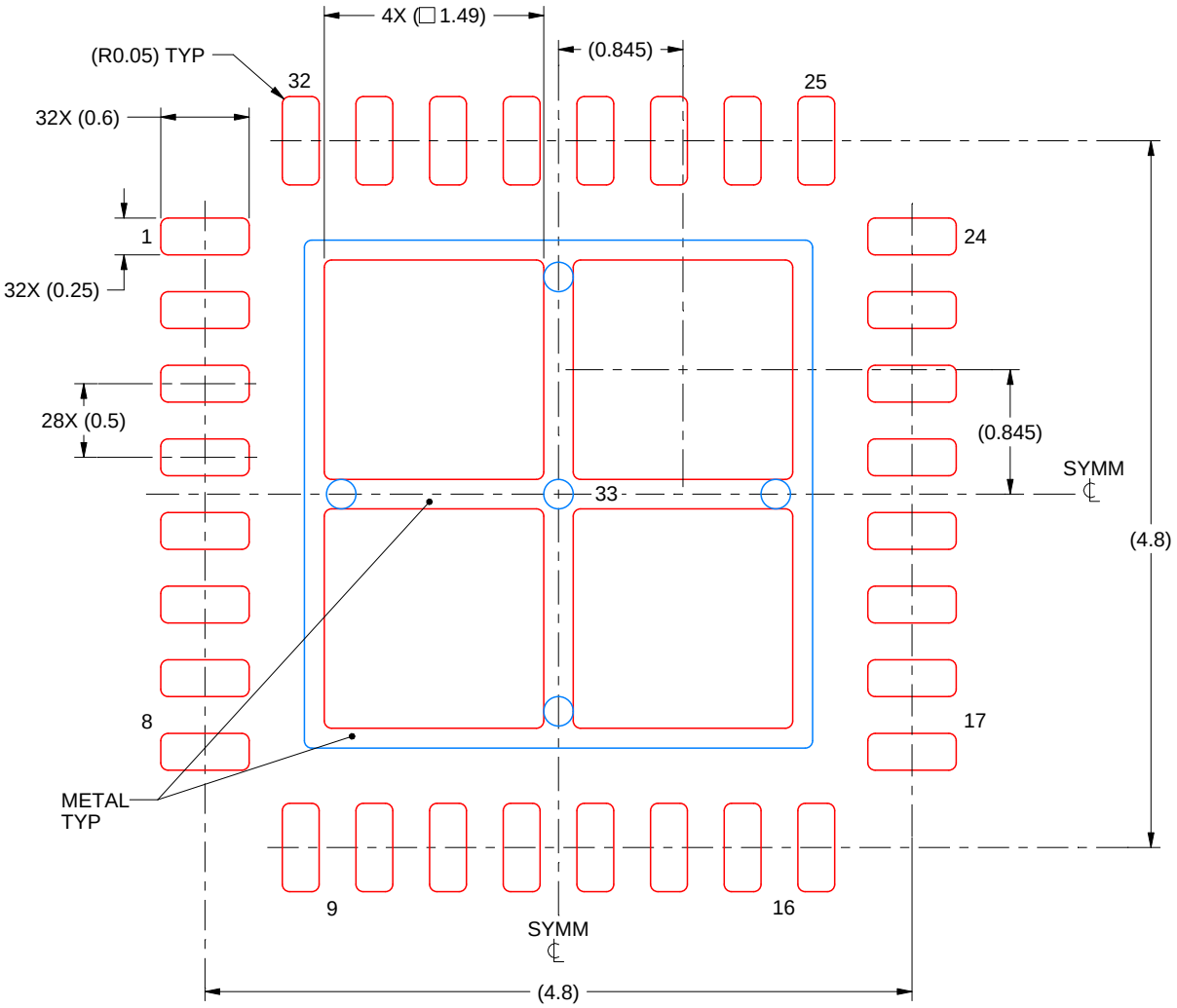
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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