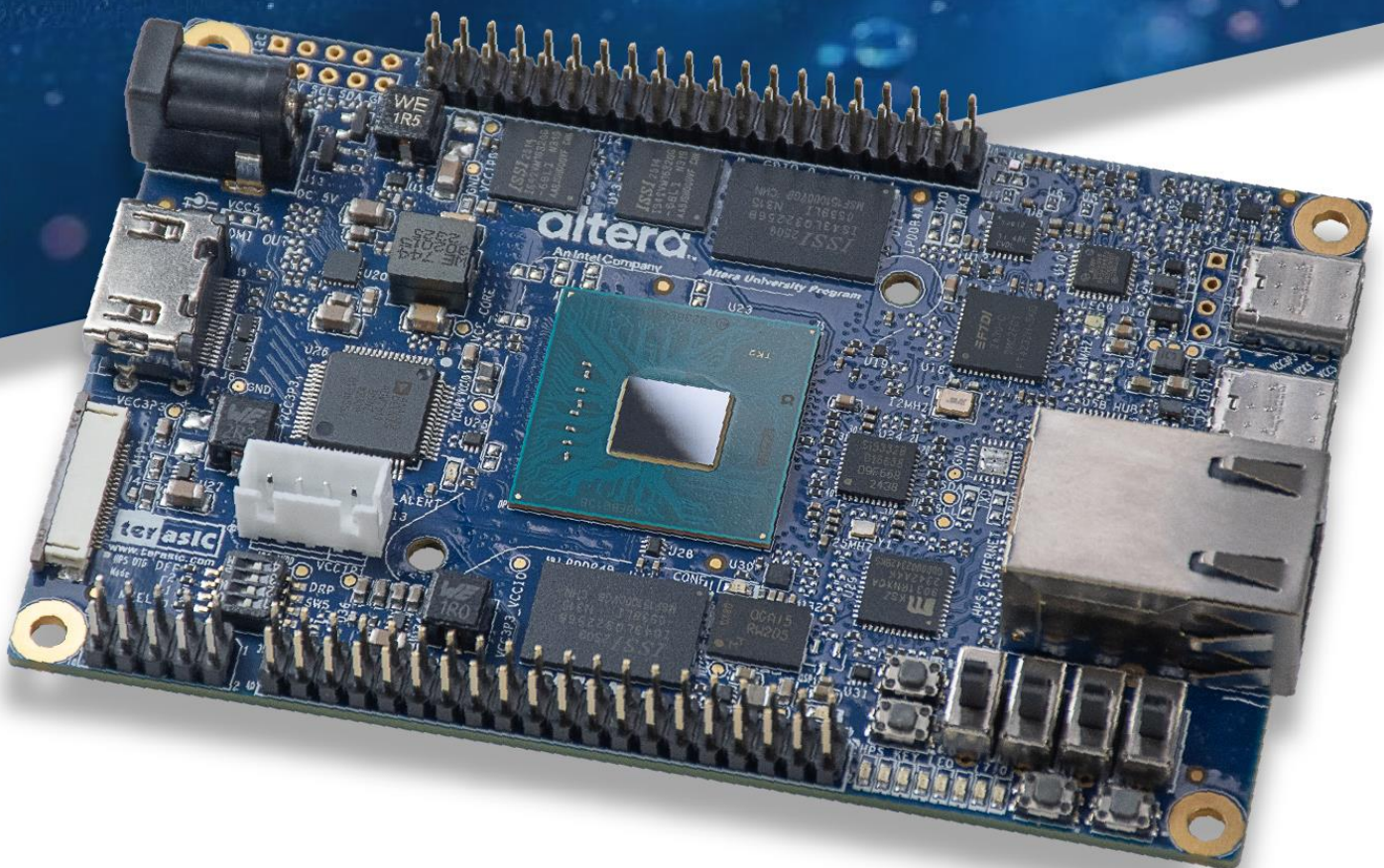


DE25-Nano Board

User Manual



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Chapter 1

DE25-Nano Board

The DE25-Nano board presents a robust hardware design platform built around the Agilex 5 SoC FPGA, which combines the ARM 2xA55 and 2xA76 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous reconfigurability paired with a high-performance, low-power processor system. Intel's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The DE25-Nano board is equipped with high-speed DDR4 memory, Ethernet networking, MIPI interface and much more that promise many exciting applications.

The DE25-Nano Development Kit contains all the tools needed to use the board in conjunction with a computer that runs the Windows 10/11.

1.1 Package Content

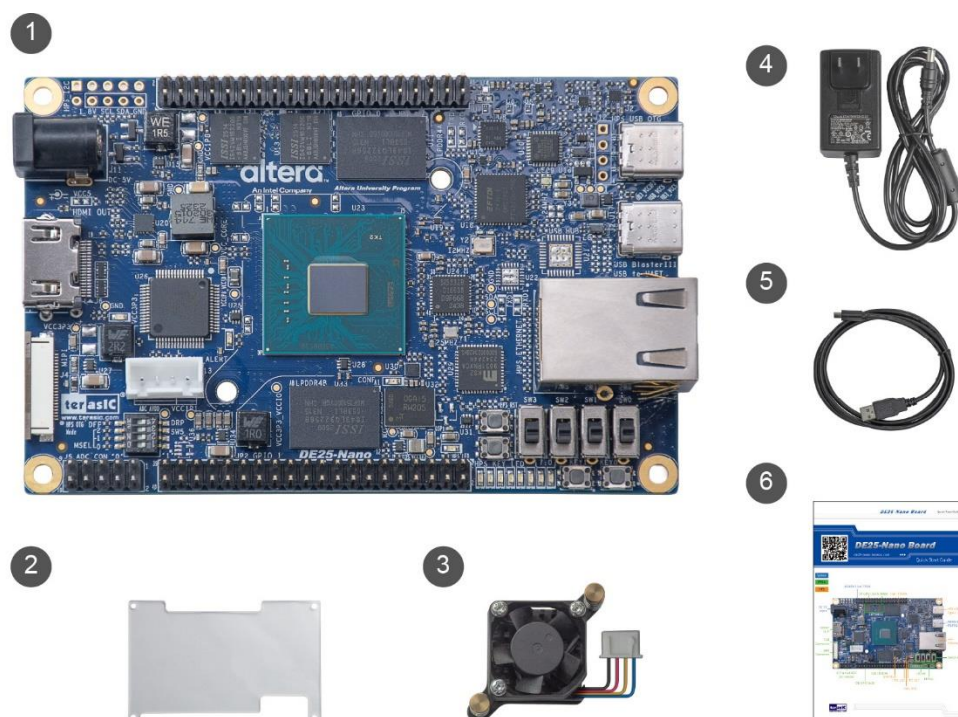


Figure 1-1 The DE25-Nano package contents

The DE25-Nano package includes:

1. DE25-Nano Board
2. Acrylic (Installed)

3. Active Heatsink (Installed)
4. 5V 4W Power Supply
5. USB Type-C Cable
6. Quick Start Guide

1.2 DE25-Nano System CD

The DE25-Nano System CD contains all the documents and supporting materials associated with DE25-Nano, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link: <http://DE25-Nano.terasic.com/cd/>.

The developers can create their Quartus project based on the **golden_top** Quartus project included in this CD. The **golde_top** Quartus project is placed in the folder: *Demonstration/FPGA/golden_top* .

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

- Terasic Technologies
- No.80, Fenggong Rd., Hukou Township, Hsinchu County, 303035 Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: <http://de25-nano.terasic.com>

Chapter 2

Introduction to the DE25-Nano Board

This chapter introduces the design and features of the board.

2.1 Layout and Components

Figure 2-1 shows a photograph of the board that illustrates its layout and the location of connectors and key components.

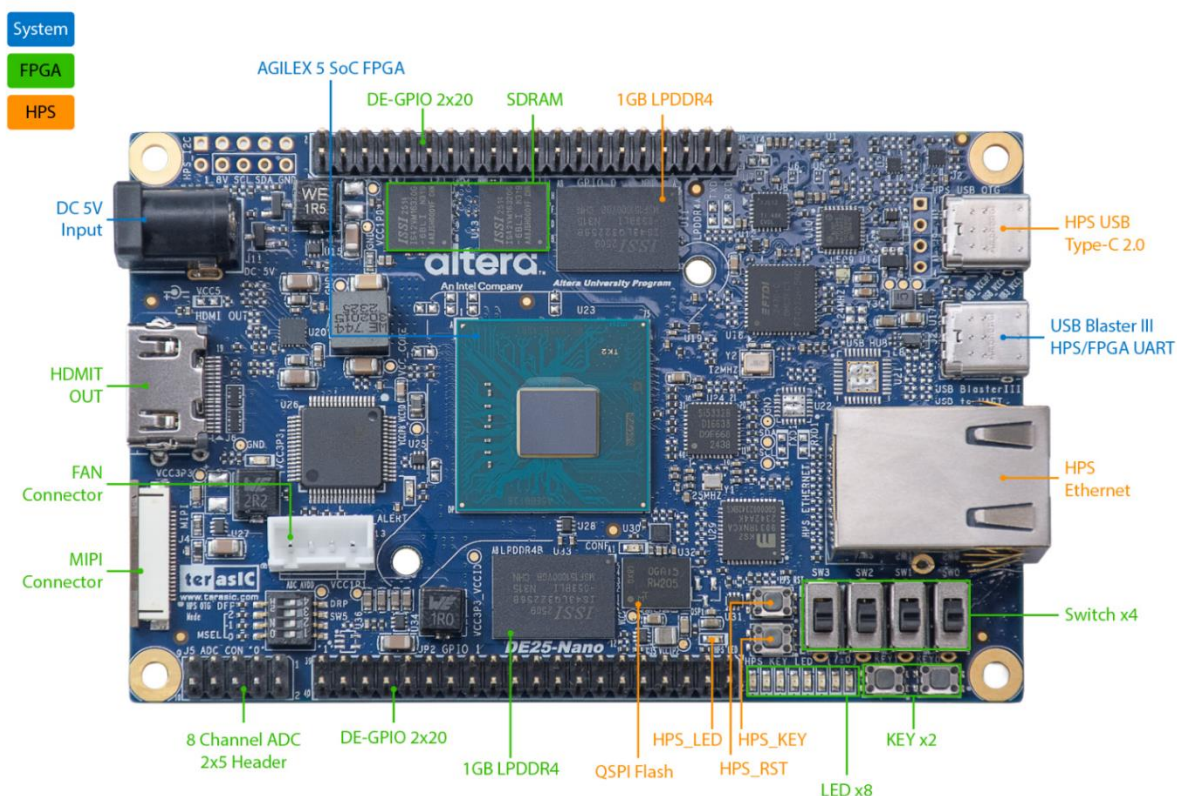


Figure 2-1 DE25-Nano development board (top view)

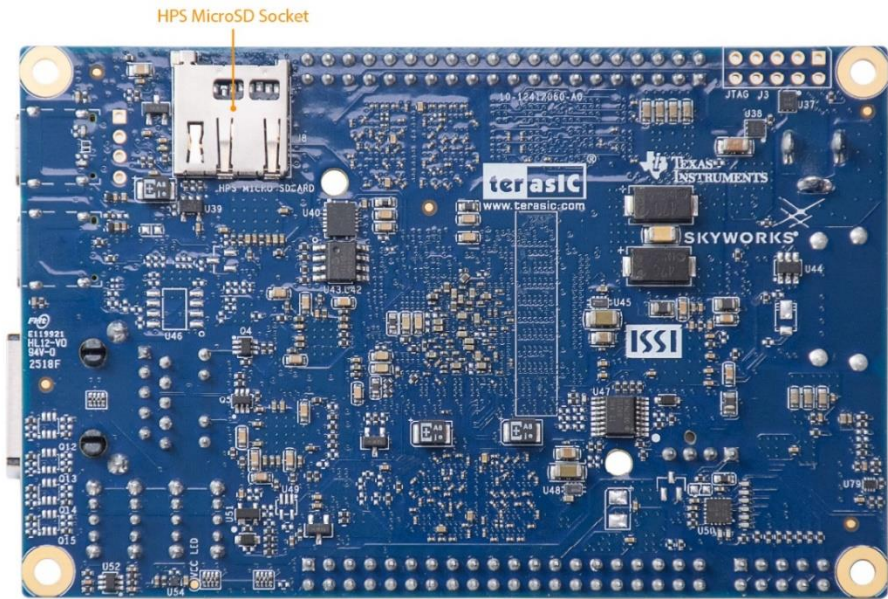


Figure 2-2 DE25-Nano development board (bottom view)

The DE25-Nano board has many features that allow users to implement a wide range of designed circuits, from simple circuits to multimedia projects.

The following hardware is provided on the board:

■ FPGA

- Agilx 5 SoC FPGA : A5EB013BB23BE4SR1(130K LEs)
- ASx4 128 Mbit QSPI Flash
- USB-Blaster III onboard for programming; JTAG Mode
- 128MB SDRAM (16-bit data bus)
- 1GB LPDDR4 (32-bit data bus)
- 4 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50 MHz clock sources from the clock generator
- HDMI 2.0 Output Port (Support 1080P)
- Two 40-pin expansion headers
- A/D converter, 4-pin SPI interface with FPGA
- One 2-lane MIPI Connector for Camera/Display

- One 2-pin UART Port via Type-C connector
- Integrated temperature sensor and fan controller

■ HPS (Hard Processor System)

- ARM Cortex Processor with 2× A55 and 2× A76 cores
- 1GB LPDDR4 (32-bit data bus), share with FPGA
- 1 Gigabit Ethernet PHY with RJ45 connector
- One USB 2.0 host with Type-C USB connector
- Micro SD card socket
- Integrated accelerometer sensor
- UART to USB, Type-C USB connector
- Cold reset button
- One user button and one user LED

2.2 Block Diagram of the DE25-Nano Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Agilex 5 SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

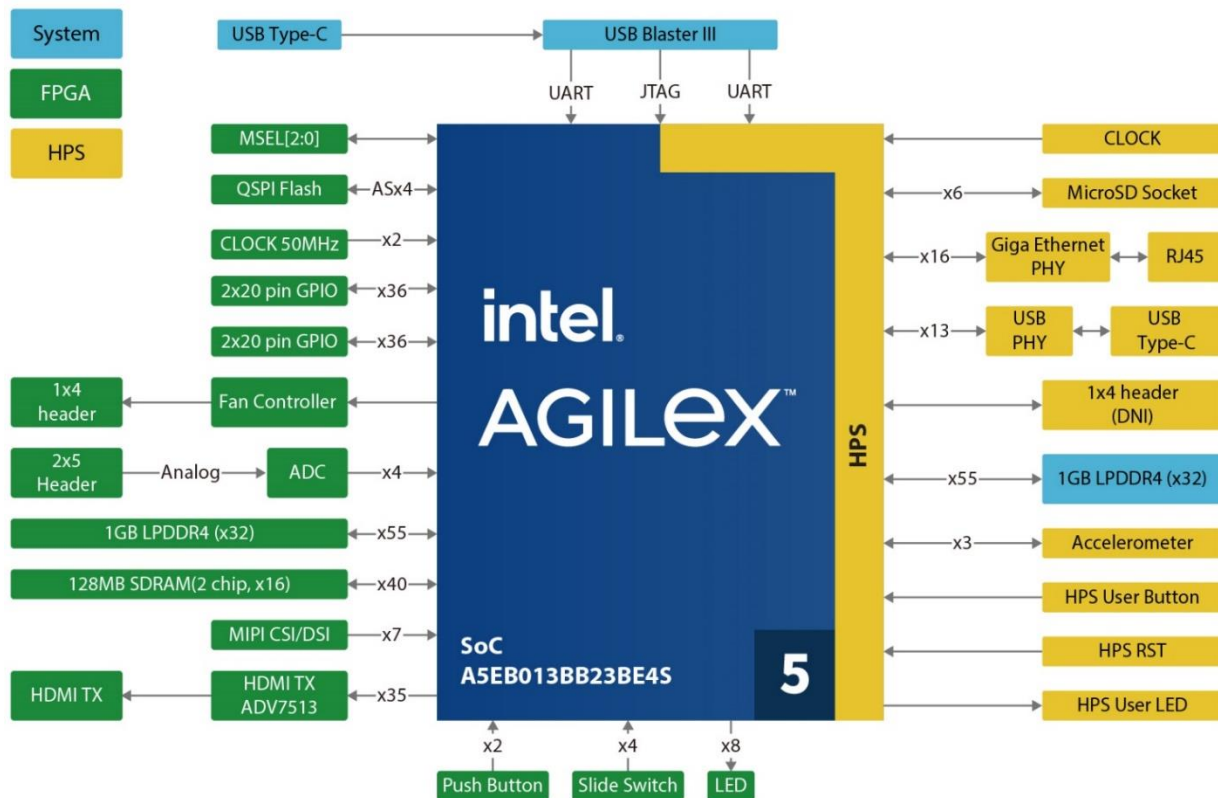


Figure 2-3 Block diagram of DE25-Nano

Detailed information about **Figure 2-3** are listed below.

FPGA Device

- Agilex™ 5 SoC FPGA : A5EB013BB23BE4SR1
- ARM Cortex Processor with 2×A55 and 2×A76
- 138K programmable logic elements
- 8.42 Mbit embedded memory
- 376 18-bit × 19-bit multipliers
- MIPI D-PHY v2.5

Configuration and Debug

- Support ASx4 Configure Mode with 128Mbits QSPI Flash
- Onboard USB-Blaster III (USB Type-C connector)

Memory Device

- 128MB (32M×16) SDRAM on FPGA
- 1GB (2×16M×32) LPDDR4 on FPGA
- 1GB (2×16M×32) LPDDR4 on HPS, shared with FPGA
- Micro SD card socket on HPS

Communication

- One USB 2.0 host port with Type-C USB connector
- UART to USB (Type-C USB connector)
- 10/100/1000 Ethernet

Connectors

- Two 40-pin DE-GPIO expansion headers
- One 10-pin ADC input header

Display

- HDMI 2.0 Output Port (Support 1080P)
- One MIPI connector with 2 data lanes

ADC

- Interface: SPI
- Fast throughput rate: 1MSPS
- Channel number: 8
- Resolution: 12-bit
- Analog input range : 0 ~ 3.4 V

Switches, Buttons, and Indicators

- 5 user buttons (FPGA ×4, HPS ×1)
- 4 user switches (FPGA ×4)
- 9 user LEDs (FPGA ×8, HPS × 1)
- 1 HPS reset buttons (HPS_Cold_RESET_n)

Sensors

- Accelerometer (G-Sensor) on HPS
- Temperature sensor on FPGA

Power

- 5V DC input

Using the DE25-Nano

This chapter provides instructions for using the board and describes its peripherals.

3.1 Settings of FPGA Configuration Mode

When the DE25-Nano board is powered on, the FPGA is configured from QSPI Flash or the HPS. The MSEL[2:0] switches are used to select the configuration scheme, implemented as a 4-pin DIP switch **SW5** on the DE25-Nano board, as shown in **Figure 3-1**.

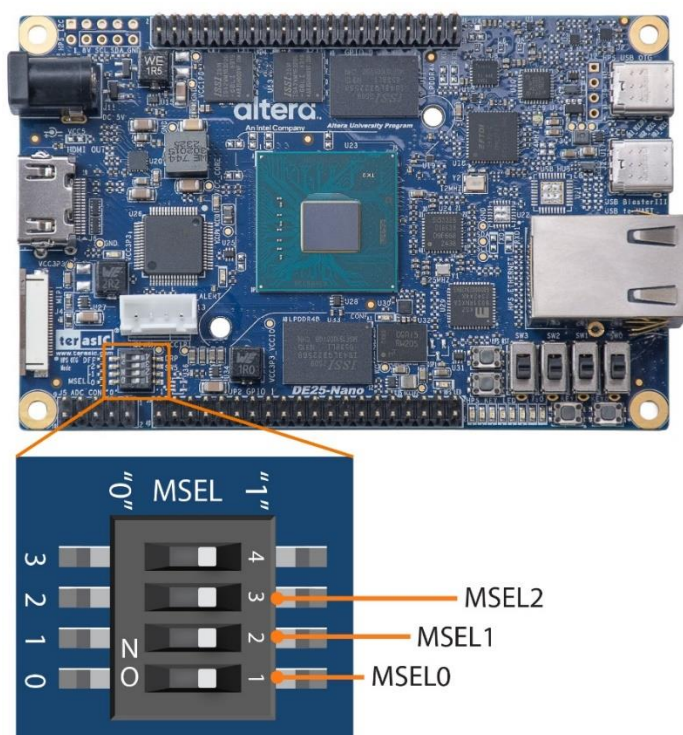


Figure 3-1 DIP switch (SW5) setting of Active Serial (AS) mode on DE25-Nano board

Table 3-1 shows the relation between MSEL[2:0] and DIP switch (SW5).

Table 3-1 FPGA Configuration Mode Switch (SW5)

Board Reference	Signal Name	Description	Default AS Mode
SW5.1	MSEL0	Use these pins to set the FPGA	OFF ("1")

SW5.2	MSEL1	Configuration scheme	ON ("0")
SW5.3	MSEL2		ON ("0")
SW5.4	N/A	N/A	N/A

Table 3-2 shows MSEL[2:0] setting of Active Serial (AS) Fast mode, which the default setting on the DE25-Nano. When the board is powered on, the FPGA is configured from QSPI Flash, which is pre-programmed with a default configuration.

Table 3-2 MSEL Pin Settings for FPGA Configure of DE25-Nano

<i>MSEL[2:0]</i>	<i>Configuration Scheme</i>	<i>Description</i>
001	AS Fast	FPGA configured from QSPI Flash (default)
111	JTAG	You can configure the FPGA using the dedicated JTAG interface and circuit.

3.2 Configuration of Agilex 5 SoC FPGA on DE25-Nano

There are two programming methods supported by DE25-Nano:

1. JTAG programming: This is named after the IEEE standards Joint Test Action Group. The configuration bitstream is downloaded directly to the Agilex 5 SoC FPGA. The FPGA will retain its current status as long as the power is applied to the board; the configuration information will be lost when the power is turned off.
2. AS programming: The other programming method is Active Serial configuration. The configuration bitstream is written to the quad serial configuration device (QSPI Flash), which provides non-volatile storage for the bit stream. The information is retained within QSPI Flash even if the DE25-Nano board is turned off. When the board is powered on, the configuration data in the QSPI Flash device is automatically loaded into the Agilex 5 SoC FPGA.

■ JTAG Chain on DE25-Nano Board

As shown in **Figure 3-2**, the DE25-Nano uses the on-board USB Blaster III (via USB Type-C) as the JTAG master. This circuit connects JTAG signals to the Agilex 5 SoC FPGA.

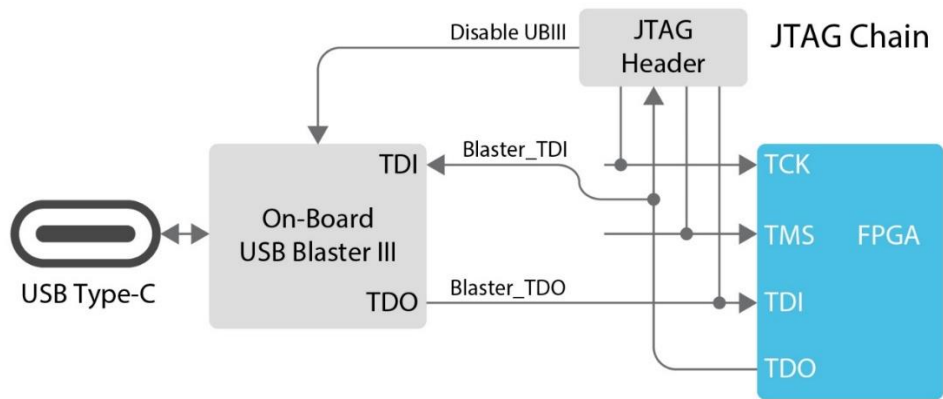


Figure 3-2 Block diagram of the JTAG chain

■ Configuring the FPGA in JTAG Mode

The following explains step-by-step how to program the FPGA in JTAG mode.

1. Make sure the Quartus Pro and the driver of USB Blaster III are installed on your Host.
2. Set the FPGA Configuration Mode Switch (SW5) to JTAG mode.
3. Connect the board's Type-C port to the host using a USB cable, and power up the board.
4. Open the Quartus Programmer tool, make sure the USB blaster III ("DE25-Nano[USB-x]") is found in "Hardware Setup.." tab.

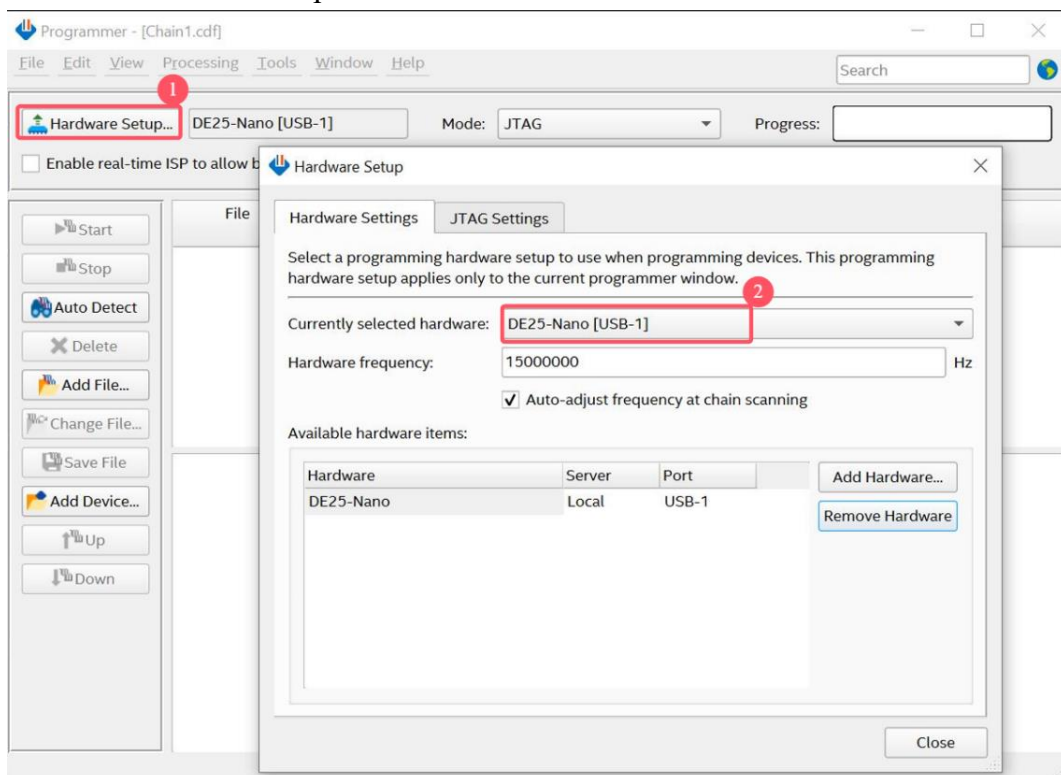


Figure 3-3 USB blaster III is found in Programmer

5. Open the Programmer and click “Auto Detect”, as shown in **Figure 3-4**

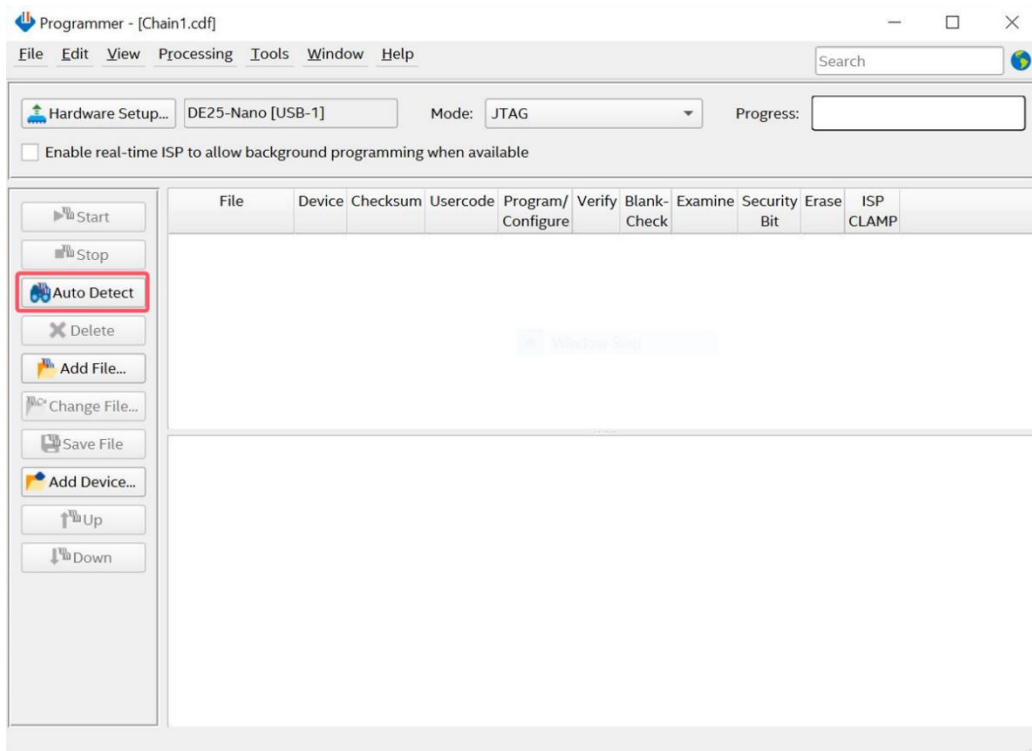


Figure 3-4 Detect FPGA device in JTAG mode

6. The Agilex 5 FPGA should be detected, as shown in **Figure 3-5**.

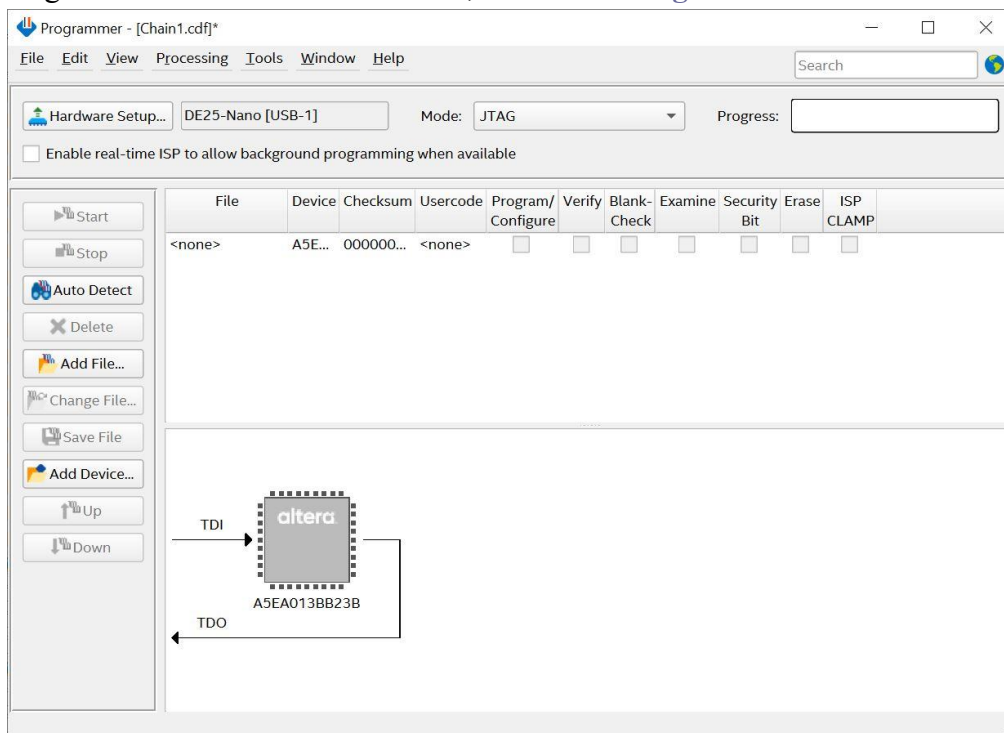


Figure 3-5 FPGA detected in Quartus programmer

7. Right click on the FPGA device and open the .sof file to be programmed, as shown in **Figure 3-6**.

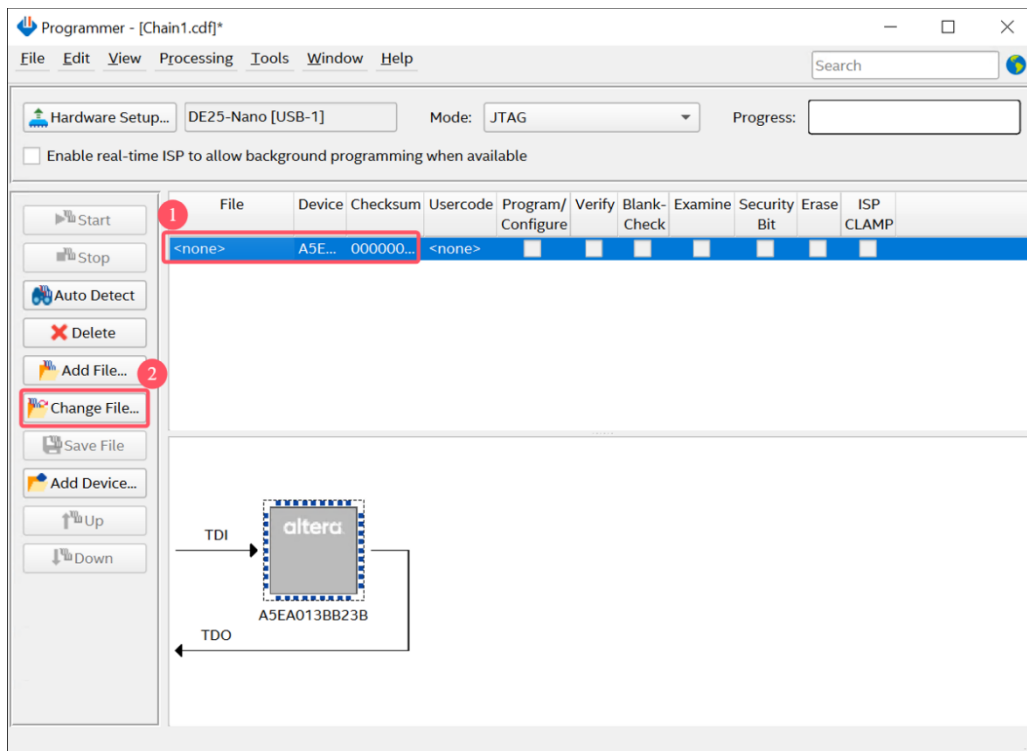


Figure 3-6 Open the .sof file to be programmed into the FPGA device

8. Select the .sof file to be programmed, as shown in **Figure 3-7**.

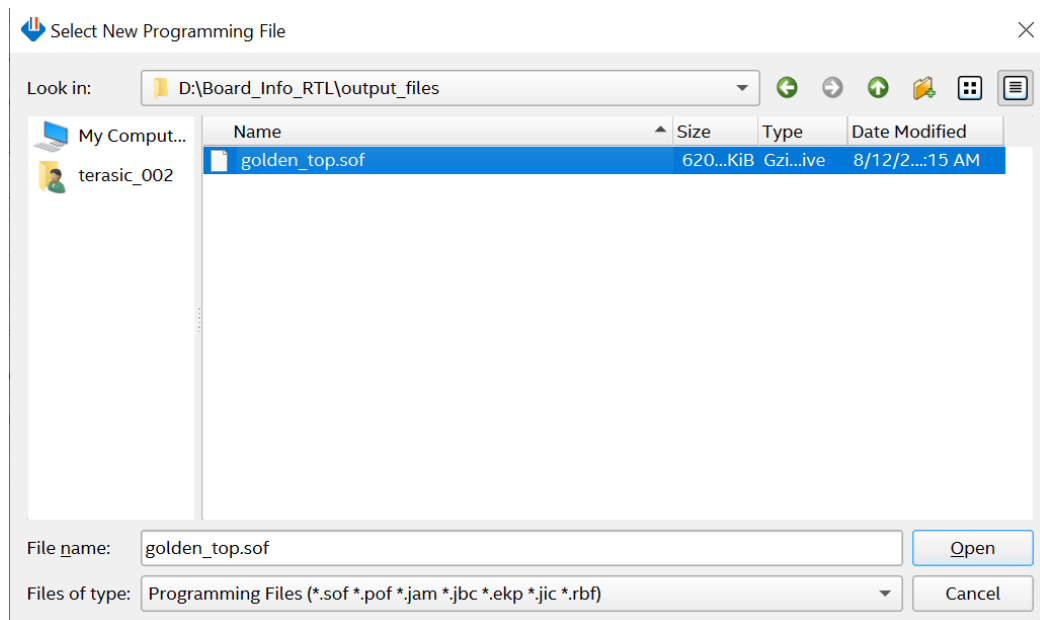


Figure 3-7 Select the .sof file to be programmed into the FPGA device

9. Click the “Program/Configure” checkbox and click “Start” button to download the .sof file

into the FPGA device, as shown in **Figure 3-8**.

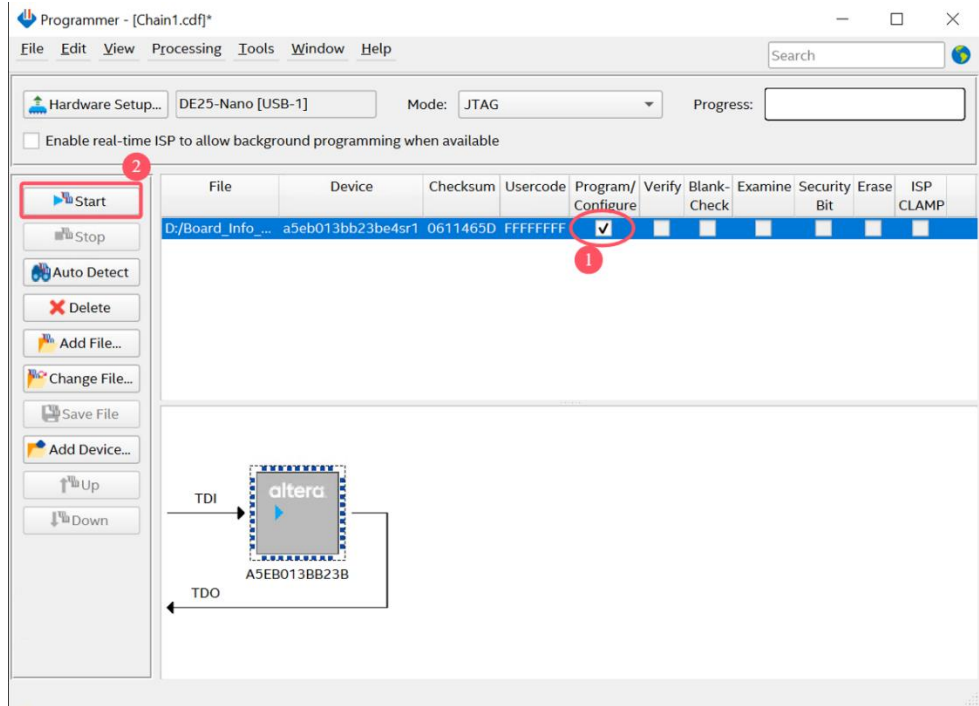


Figure 3-8 Program .sof file into the FPGA device

3.3 Board Status Elements

In addition to the LEDs that the FPGA can control, there are 6 indicators that indicate the board status (see **Figure 3-9**). **Table 3-3** shows the JTAG Blaster LED status (for USB blaster III) and its meaning. **Table 3-4** shows the status and description of other LEDs.

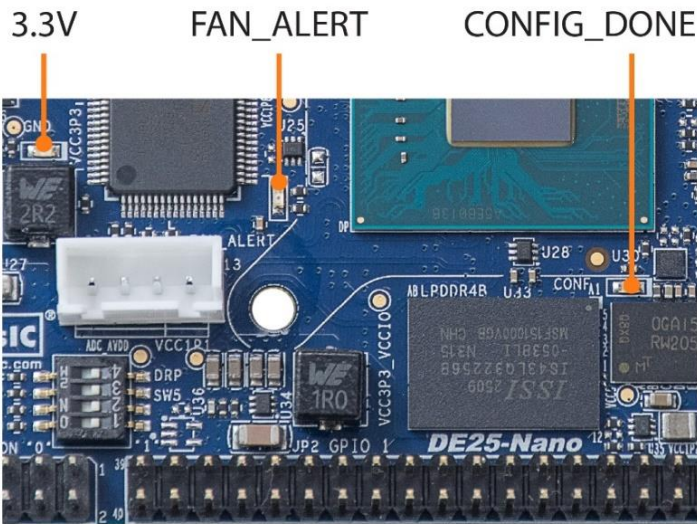


Figure 3-9 LED Indicators on the DE25-Nano

Table 3-3 JTAG blaster LED status

<i>Color</i>	<i>Meaning</i>
Off	No power / not connected / suspend mode
Blue	Connected, not in use
Green	Connected, an application is using JTAG, no traffic
Green flickering	Connected, data is moving through the JTAG interface
Purple flashing	Identify function has been triggered on this cable

Table 3-4 LED Indicators

<i>Board Reference</i>	<i>LED Name</i>	<i>Description</i>
LED11	3.3V	Illuminates when 3.3V power is active.
LED10	FPGA_CONF_DONE	Illuminates when FPGA configuration is complete and successful
D16	FAN_ALERT	Illuminates when the fan is abnormal, such as when the fan speed is different from expected

3.4 Board Reset Elements

The board provides two reset buttons for different system reset situations (see [Figure 3-10](#)). These buttons can reset the System HPS. [Table 3-5](#) lists the details.

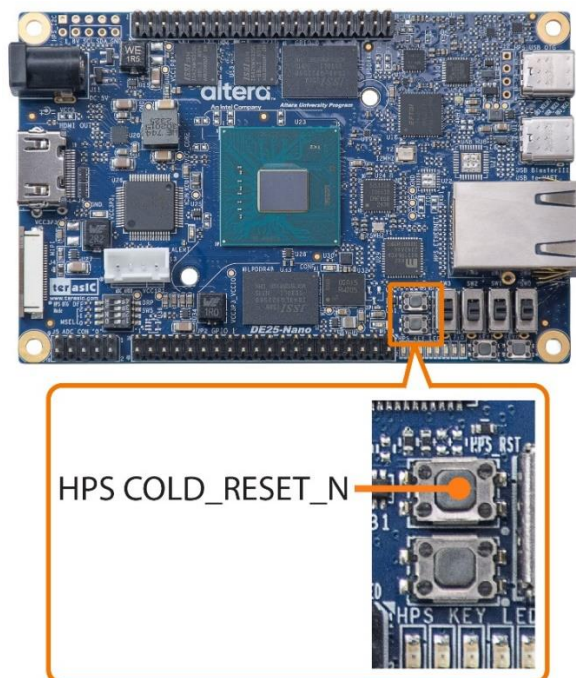


Figure 3-10 Reset buttons on DE25-Nano

Table 3-5 Description of the three Reset Buttons on the DE25-Nano

Board Reference	Signal Name	Description
KEY3	KEY_COLD_RESET_N	Cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset.

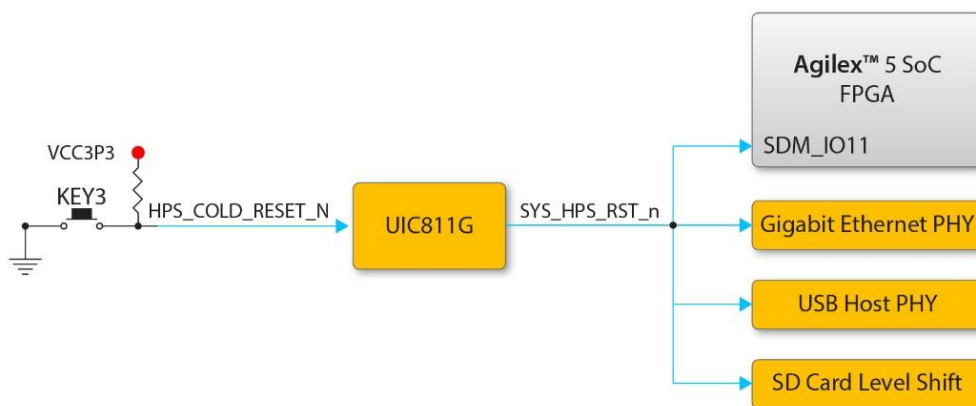


Figure 3-11 Block diagram of reset buttons the DE25-Nano

3.5 Clock Circuitry

Figure 3-12 shows the default frequency of all external clocks fed to the Agilex 5 SoC FPGA. A clock generator is used to distribute clock signals with low jitter. The three 50 MHz clock signals connected to the FPGA are used as clock sources for user logic. One 25 MHz clock signal is connected to HPS clock inputs, and the two 166.666MHz clocks are the reference clock for LPDDR4 A and LPDDR4 B interface. A 125 MHz clock is used for FPGA configuration and transceiver calibration bank (OSC_CLK1).

For peripheral devices, one 25 MHz clock is fed to the clock input of Gigabit Ethernet PHY. Two 24 MHz clock signals are connected to the clock inputs of the USB Host/OTG PHY and USB hub controller. The pin assignments of clock inputs to FPGA I/O pins are listed in **Table 3-6**.

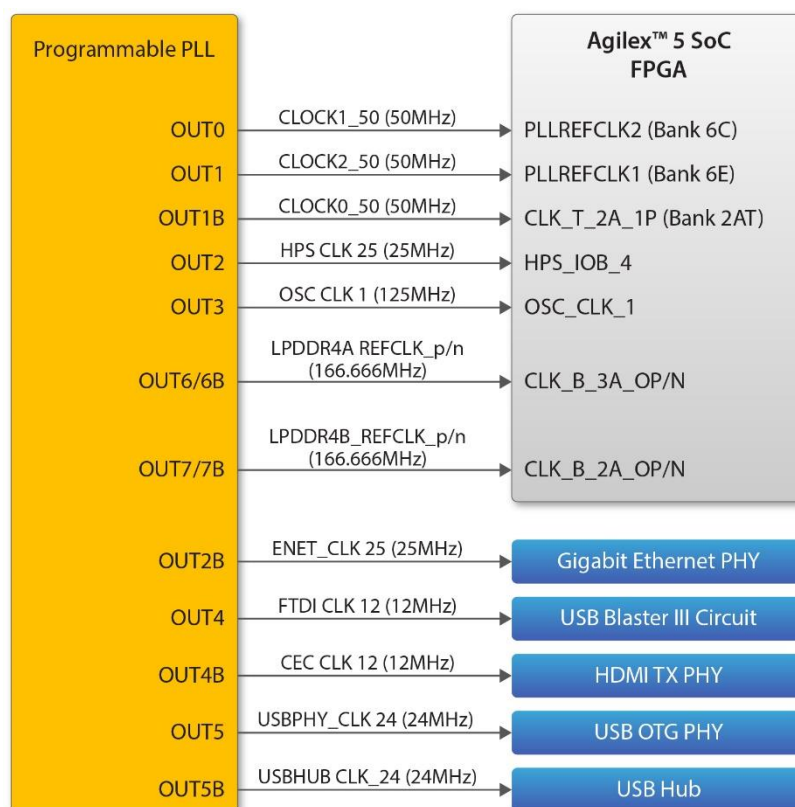


Figure 3-12 Block diagram of the clock distribution on the DE25-Nano

Table 3-6 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
CLOCK0_50	PIN_DJ35	50 MHz clock input	1.1V
CLOCK1_50	PIN_V16	50 MHz clock input	3.3-V LVCMOS
CLOCK2_50	PIN_BF23	50 MHz clock input	3.3-V LVCMOS
HPS_CLK_25	PIN_AN67	25 MHz clock input	1.8V
LPDDR4A_REFCLK_P	PIN_B55	166.666MHz clock input	1.1V TRUE DIFFERENTIAL SIGNALING
LPDDR4B_REFCLK_P	PIN_DK39	166.666MHz clock input	1.1V TRUE DIFFERENTIAL SIGNALING

3.6 I2C Bus

There are many devices controlled by the I2C interface on the DE25-Nano board, such as the MIPI module, HDMI TX PHY and accelerometer. The devices on the board are connected to the HPS and

FPGA I2C bus independently as shown in **Figure 3-13**. The pin assignment of the I2C bus is listed in **Table 3-7**.

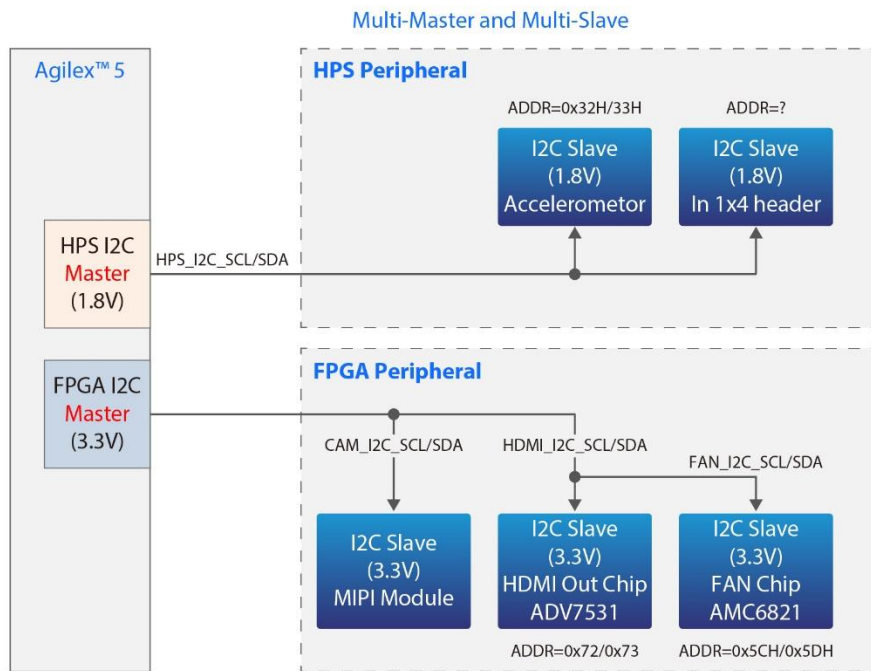


Figure 3-13 Control mechanism for the I2C multiplexer

Table 3-7 I2C Bus Pin Assignments

Signal Name	FPGA Pin No.	Description	I/O Standard
HDMI_I2C_SCL	PIN_BT1	HDMI TX I2C Clock	3.3V LVCMOS
HDMI_I2C_SDA	PIN_BW2	HDMI TX I2C Data	3.3V LVCMOS
CAM_I2C_SCL	PIN_BP2	MIPI Module I2C Clock	3.3V LVCMOS
CAM_I2C_SDA	PIN_BP1	MIPI Module I2C Data	3.3V LVCMOS
HPS_I2C_SCL	PIN_N72	I2C Clock of the first HPS I2C controller	1.8V
HPS_I2C_SDA	PIN_L75	I2C Data of the first HPS I2C controller	1.8V

3.7 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor these interfaces with user logic in the FPGA.

3.7.1 User Push-buttons, Switches and LEDs

The board has two push-buttons connected to the FPGA, as shown in **Figure 3-14**. A Schmitt trigger circuit acts as a switch debouncer in **Figure 3-15** for the connected buttons. The two buttons named

KEY0 and KEY1 coming out of the Schmitt trigger device are connected directly to the Agilex 5 SoC FPGA. Each push-button generates a low logic level when it is pressed (Active low). Since the push-buttons are debounced, they can be used as reset inputs in a circuit.

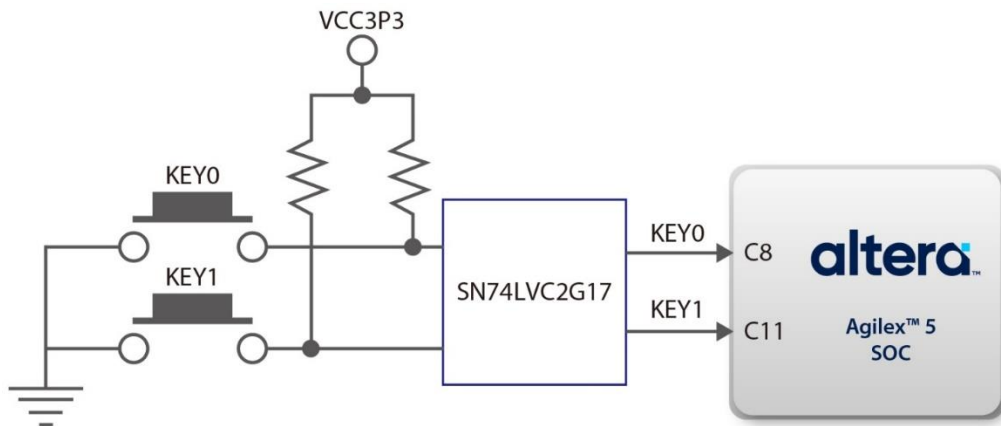


Figure 3-14 Connections between the push-buttons and the Agilex 5 SoC FPGA

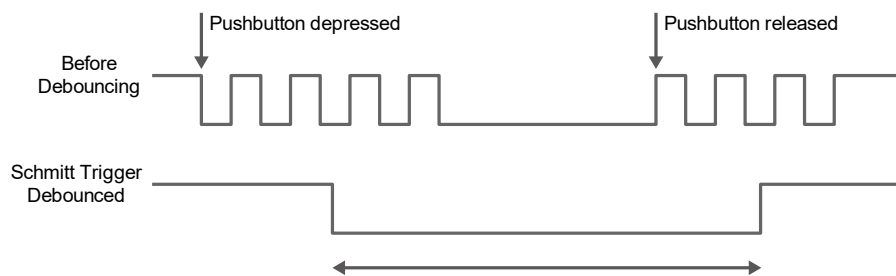


Figure 3-15 Switch debouncing

There are four slide switches connected to the FPGA, as shown in [Figure 3-16](#). These switches are not debounced and may be used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it sends a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is sent to the FPGA.



Figure 3-16 Connections between the slide switches and the Agilex 5 SoC FPGA

There are also eight user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the Agilex 5 SoC FPGA; driving its associated pin to a “**low**” logic level turn the LED “**on**”. **Figure 3-17** shows the connections between LEDs and Agilex 5 SoC FPGA. **Table 3-8**, **Table 3-9** and **Table 3-10** list the pin assignment of user push-buttons, switches, and LEDs.



Figure 3-17 Connections between the LEDs and the Agilex 5 SoC FPGA

Table 3-8 Pin Assignments of Slide Switches

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
SW[0]	PIN_DK24	Slide Switch[0]	1.1V
SW[1]	PIN_DD24	Slide Switch[1]	1.1V

SW[2]	PIN_DD27	Slide Switch[2]	1.1V
SW[3]	PIN_DF27	Slide Switch[3]	1.1V

Table 3-9 Pin Assignments of Push-buttons

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
KEY[0]	PIN_C8	Push-button[0]	3.3-V LVCMOS
KEY[1]	PIN_C11	Push-button[1]	3.3-V LVCMOS

Table 3-10 Pin Assignments of LEDs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
LED[0]	PIN_DF35	LED [0]	1.1V
LED[1]	PIN_DJ32	LED [1]	1.1V
LED[2]	PIN_DN22	LED [2]	1.1V
LED[3]	PIN_DP23	LED [3]	1.1V
LED[4]	PIN_DN25	LED [4]	1.1V
LED[5]	PIN_DP25	LED [5]	1.1V
LED[6]	PIN_DJ27	LED [6]	1.1V
LED[7]	PIN_DP30	LED [7]	1.1V

3.7.2 2x20 GPIO Expansion Header

The board has two 40-pin expansion headers. Each header has 36 user pins connected directly to the Agilix 5 SoC FPGA. It also includes DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. The maximum power consumption allowed for a daughter card connected to one GPIO ports is shown in [Table 3-11](#).

Table 3-11 Voltage and Max. Current Limit of Expansion Header(s)

<i>Supplied Voltage</i>	<i>Max. Current Limit</i>
5V	1A
3.3V	1.5A

[Figure 3-18](#) shows the I/O distribution of the GPIO headers.

[Table 3-12](#) shows the pin assignment of the GPIO headers.

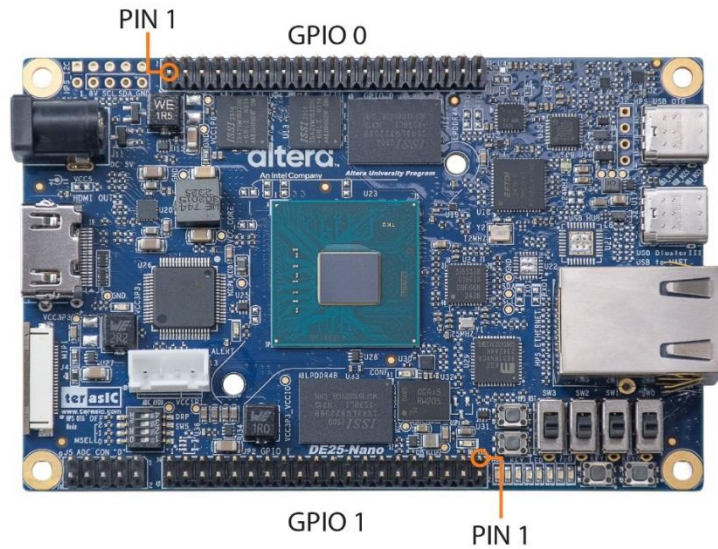


Figure 3-18 Connections between the GPIO header and Agilex 5 SoC FPGA

GPIO 0 (JP1)										GPIO 1 (JP2)									
PIN_H16	GPIO_0[0]	1		2	GPIO_0[1]	PIN_Y1	PIN_BV14	GPIO_1[0]	1		2	GPIO_1[1]	PIN_CG26						
PIN_C2	GPIO_0[2]	3		4	GPIO_0[3]	PIN_P1	PIN_DM2	GPIO_1[2]	3		4	GPIO_1[3]	PIN_CD23						
PIN_Y2	GPIO_0[4]	5		6	GPIO_0[5]	PIN_U2	PIN_CG23	GPIO_1[4]	5		6	GPIO_1[5]	PIN_CE14						
PIN_L1	GPIO_0[6]	7		8	GPIO_0[7]	PIN_F2	PIN_CA23	GPIO_1[6]	7		8	GPIO_1[7]	PIN_CH16						
PIN_P2	GPIO_0[8]	9		10	GPIO_0[9]	PIN_B3	PIN_CV16	GPIO_1[8]	9		10	GPIO_1[9]	PIN_CH14						
5V		11		12	GND			5V	11		12	GND							
PIN_H4	GPIO_0[10]	13		14	GPIO_0[11]	PIN_H14	PIN_CR6	GPIO_1[10]	13		14	GPIO_1[11]	PIN_CH11						
PIN_C6	GPIO_0[12]	15		16	GPIO_0[13]	PIN_H6	PIN_CV6	GPIO_1[12]	15		16	GPIO_1[13]	PIN_CR14						
PIN_B5	GPIO_0[14]	17		18	GPIO_0[15]	PIN_H11	PIN_CR19	GPIO_1[14]	17		18	GPIO_1[15]	PIN_CR11						
PIN_C14	GPIO_0[16]	19		20	GPIO_0[17]	PIN_B10	PIN_CV19	GPIO_1[16]	19		20	GPIO_1[17]	PIN_CV11						
PIN_A15	GPIO_0[18]	21		22	GPIO_0[19]	PIN_A10	PIN_CV14	GPIO_1[18]	21		22	GPIO_1[19]	PIN_DJ3						
PIN_B17	GPIO_0[20]	23		24	GPIO_0[21]	PIN_B15	PIN_DF3	GPIO_1[20]	23		24	GPIO_1[21]	PIN_DN2						
PIN_AH16	GPIO_0[22]	25		26	GPIO_0[23]	PIN_A13	PIN_CV4	GPIO_1[22]	25		26	GPIO_1[23]	PIN_DD3						
PIN_AE19	GPIO_0[24]	27		28	GPIO_0[25]	PIN_C19	PIN_CE11	GPIO_1[24]	27		28	GPIO_1[25]	PIN_CE8						
3.3V		29		30	GND			3.3V	29		30	GND							
PIN_H19	GPIO_0[26]	31		32	GPIO_0[27]	PIN_AH19	PIN_DE1	GPIO_1[26]	31		32	GPIO_1[27]	PIN_DH1						
PIN_R19	GPIO_0[28]	33		34	GPIO_0[29]	PIN_R14	PIN_DH2	GPIO_1[28]	33		34	GPIO_1[29]	PIN_CH4						
PIN_V19	GPIO_0[30]	35		36	GPIO_0[31]	PIN_V14	PIN_DC2	GPIO_1[30]	35		36	GPIO_1[31]	PIN_DC1						
PIN_AG31	GPIO_0[32]	37		38	GPIO_0[33]	PIN_AL31	PIN_BV19	GPIO_1[32]	37		38	GPIO_1[33]	PIN_CE6						
PIN_AL37	GPIO_0[34]	39		40	GPIO_0[35]	PIN_AL34	PIN_BV11	GPIO_1[34]	39		40	GPIO_1[35]	PIN_BV16						

Table 3-12 Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_0[0]	PIN_H16	GPIO Connection 0[0]	3.3V
GPIO_0[1]	PIN_Y1	GPIO Connection 0[1]	3.3V

GPIO_0[2]	PIN_C2	GPIO Connection 0[2]	3.3V
GPIO_0[3]	PIN_P1	GPIO Connection 0[3]	3.3V
GPIO_0[4]	PIN_Y2	GPIO Connection 0[4]	3.3V
GPIO_0[5]	PIN_U2	GPIO Connection 0[5]	3.3V
GPIO_0[6]	PIN_L1	GPIO Connection 0[6]	3.3V
GPIO_0[7]	PIN_F2	GPIO Connection 0[7]	3.3V
GPIO_0[8]	PIN_P2	GPIO Connection 0[8]	3.3V
GPIO_0[9]	PIN_B3	GPIO Connection 0[9]	3.3V
GPIO_0[10]	PIN_H4	GPIO Connection 0[10]	3.3V
GPIO_0[11]	PIN_H14	GPIO Connection 0[11]	3.3V
GPIO_0[12]	PIN_C6	GPIO Connection 0[12]	3.3V
GPIO_0[13]	PIN_H6	GPIO Connection 0[13]	3.3V
GPIO_0[14]	PIN_B5	GPIO Connection 0[14]	3.3V
GPIO_0[15]	PIN_H11	GPIO Connection 0[15]	3.3V
GPIO_0[16]	PIN_C14	GPIO Connection 0[16]	3.3V
GPIO_0[17]	PIN_B10	GPIO Connection 0[17]	3.3V
GPIO_0[18]	PIN_A15	GPIO Connection 0[18]	3.3V
GPIO_0[19]	PIN_A10	GPIO Connection 0[19]	3.3V
GPIO_0[20]	PIN_B17	GPIO Connection 0[20]	3.3V
GPIO_0[21]	PIN_B15	GPIO Connection 0[21]	3.3V
GPIO_0[22]	PIN_AH16	GPIO Connection 0[22]	3.3V
GPIO_0[23]	PIN_A13	GPIO Connection 0[23]	3.3V
GPIO_0[24]	PIN_AE19	GPIO Connection 0[24]	3.3V
GPIO_0[25]	PIN_C19	GPIO Connection 0[25]	3.3V
GPIO_0[26]	PIN_H19	GPIO Connection 0[26]	3.3V
GPIO_0[27]	PIN_AH19	GPIO Connection 0[27]	3.3V
GPIO_0[28]	PIN_R19	GPIO Connection 0[28]	3.3V
GPIO_0[29]	PIN_R14	GPIO Connection 0[29]	3.3V
GPIO_0[30]	PIN_V19	GPIO Connection 0[30]	3.3V

GPIO_0[31]	PIN_V14	GPIO Connection 0[31]	3.3V
GPIO_0[32]	PIN_AG31	GPIO Connection 0[32]	3.3V
GPIO_0[33]	PIN_AL31	GPIO Connection 0[33]	3.3V
GPIO_0[34]	PIN_AL37	GPIO Connection 0[34]	3.3V
GPIO_0[35]	PIN_AL34	GPIO Connection 0[35]	3.3V
GPIO_1[0]	PIN_BV14	GPIO Connection 1[0]	3.3V
GPIO_1[1]	PIN_CG26	GPIO Connection 1[1]	3.3V
GPIO_1[2]	PIN_DM2	GPIO Connection 1[2]	3.3V
GPIO_1[3]	PIN_CD23	GPIO Connection 1[3]	3.3V
GPIO_1[4]	PIN_CG23	GPIO Connection 1[4]	3.3V
GPIO_1[5]	PIN_CE14	GPIO Connection 1[5]	3.3V
GPIO_1[6]	PIN_CA23	GPIO Connection 1[6]	3.3V
GPIO_1[7]	PIN_CH16	GPIO Connection 1[7]	3.3V
GPIO_1[8]	PIN_CV16	GPIO Connection 1[8]	3.3V
GPIO_1[9]	PIN_CH14	GPIO Connection 1[9]	3.3V
GPIO_1[10]	PIN_CR6	GPIO Connection 1[10]	3.3V
GPIO_1[11]	PIN_CH11	GPIO Connection 1[11]	3.3V
GPIO_1[12]	PIN_CV6	GPIO Connection 1[12]	3.3V
GPIO_1[13]	PIN_CR14	GPIO Connection 1[13]	3.3V
GPIO_1[14]	PIN_CR19	GPIO Connection 1[14]	3.3V
GPIO_1[15]	PIN_CR11	GPIO Connection 1[15]	3.3V
GPIO_1[16]	PIN_CV19	GPIO Connection 1[16]	3.3V
GPIO_1[17]	PIN_CV11	GPIO Connection 1[17]	3.3V
GPIO_1[18]	PIN_CV14	GPIO Connection 1[18]	3.3V
GPIO_1[19]	PIN_DJ3	GPIO Connection 1[19]	3.3V
GPIO_1[20]	PIN_DF3	GPIO Connection 1[20]	3.3V
GPIO_1[21]	PIN_DN2	GPIO Connection 1[21]	3.3V
GPIO_1[22]	PIN_CV4	GPIO Connection 1[22]	3.3V
GPIO_1[23]	PIN_DD3	GPIO Connection 1[23]	3.3V

GPIO_1[24]	PIN_CE11	GPIO Connection 1[24]	3.3V
GPIO_1[25]	PIN_CE8	GPIO Connection 1[25]	3.3V
GPIO_1[26]	PIN_DE1	GPIO Connection 1[26]	3.3V
GPIO_1[27]	PIN_DH1	GPIO Connection 1[27]	3.3V
GPIO_1[28]	PIN_DH2	GPIO Connection 1[28]	3.3V
GPIO_1[29]	PIN_CH4	GPIO Connection 1[29]	3.3V
GPIO_1[30]	PIN_DC2	GPIO Connection 1[30]	3.3V
GPIO_1[31]	PIN_DC1	GPIO Connection 1[31]	3.3V
GPIO_1[32]	PIN_BV19	GPIO Connection 1[32]	3.3V
GPIO_1[33]	PIN_CE6	GPIO Connection 1[33]	3.3V
GPIO_1[34]	PIN_BV11	GPIO Connection 1[34]	3.3V
GPIO_1[35]	PIN_BV16	GPIO Connection 1[35]	3.3V

3.7.3 HDMI Output

The development board provides a high performance HDMI transmitter via the Analog Devices ADV7513, which incorporates HDMI v1.4 features, including 3D video support and 165MHz support for all video formats up to 1080p and UXGA. The ADV7513 is controlled via a serial I2C bus interface, which is connected to pins on the Agilex 5 SoC FPGA. A schematic diagram of the audio circuitry is shown in **Figure 3-19**. Detailed information on using the ADV7513 HDMI TX is available on the manufacturer's website, or under the Datasheets\HDMI folder in the DE25-Nano System CD.

Table 3-13 lists the HDMI Interface pin assignments and signal names relative to the FPGA.

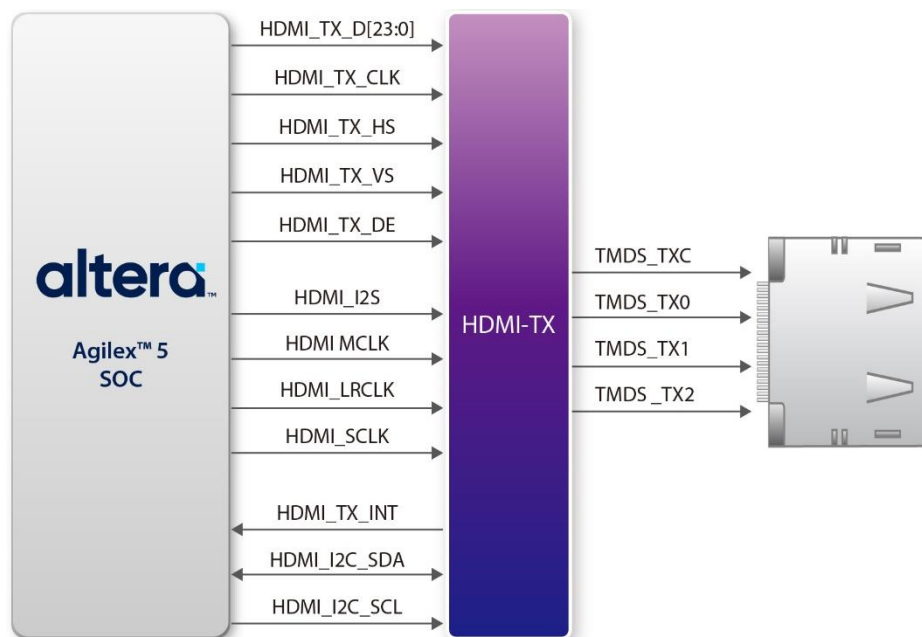


Figure 3-19 Connections between the FPGA and HDMI Transmitter Chip

Table 3-13 Pin Assignment of HDMI

Signal Name	FPGA Pin No.	Description	I/O Standard
HDMI_TX_D0	PIN_AV19	Video Data bus	3.3V
HDMI_TX_D1	PIN_AT11	Video Data bus	3.3V
HDMI_TX_D2	PIN_BE11	Video Data bus	3.3V
HDMI_TX_D3	PIN_AV14	Video Data bus	3.3V
HDMI_TX_D4	PIN_AT19	Video Data bus	3.3V
HDMI_TX_D5	PIN_AT14	Video Data bus	3.3V
HDMI_TX_D6	PIN_AV16	Video Data bus	3.3V
HDMI_TX_D7	PIN_AV11	Video Data bus	3.3V
HDMI_TX_D8	PIN_BH11	Video Data bus	3.3V
HDMI_TX_D9	PIN_BE14	Video Data bus	3.3V
HDMI_TX_D10	PIN_BE19	Video Data bus	3.3V
HDMI_TX_D11	PIN_BH14	Video Data bus	3.3V
HDMI_TX_D12	PIN_BV6	Video Data bus	3.3V
HDMI_TX_D13	PIN_BJ23	Video Data bus	3.3V
HDMI_TX_D14	PIN_BV4	Video Data bus	3.3V

HDMI_TX_D15	PIN_BU23	Video Data bus	3.3V
HDMI_TX_D16	PIN_BH16	Video Data bus	3.3V
HDMI_TX_D17	PIN_DA1	Video Data bus	3.3V
HDMI_TX_D18	PIN_BH19	Video Data bus	3.3V
HDMI_TX_D19	PIN_CP2	Video Data bus	3.3V
HDMI_TX_D20	PIN_CM1	Video Data bus	3.3V
HDMI_TX_D21	PIN_DA2	Video Data bus	3.3V
HDMI_TX_D22	PIN_CP1	Video Data bus	3.3V
HDMI_TX_D23	PIN_CU2	Video Data bus	3.3V
HDMI_TX_CLK	PIN_DJ24	Video Clock	3.3V
HDMI_TX_DE	PIN_CJ2	Data Enable Signal for Digital Video.	3.3V
HDMI_TX_HS	PIN_BR11	Horizontal Synchronization	3.3V
HDMI_TX_VS	PIN_BR14	Vertical Synchronization	3.3V
HDMI_TX_INT	PIN_CF2	Interrupt Signal	3.3V
HDMI_I2S	PIN_CB2	I2S Channel 0 Audio Data Input	3.3V
HDMI_MCLK	PIN_CF1	Audio Reference Clock Input	3.3V
HDMI_LRCLK	PIN_BR6	Audio Left/Right Channel Signal Input	3.3V
HDMI_SCLK	PIN_BW1	I2S Audio Clock Input	3.3V
FPGA_I2C_SCL	PIN_BT1	FPGA I2C Clock	3.3V
FPGA_I2C_SDA	PIN_BW2	FPGA I2C Data	3.3V

3.7.4 LPDDR4 Memory

The board supports two independent banks of LPDDR4 device (LPDDR4A and LPDDR4B). Each LPDDR4 bank can support 32-bit 1GB LPDDR. The I/O bank where LPDDR4A is located can implement the Intel Agilex 5 FPGA EMIF IP with the Hard Processor Subsystem (HPS). If no HPS EMIF IP is used in a system, the LPDDR4A bank can be used for the EMIF IP of the FPGA. The LPDDR4A and LPDDR4B on the board can run at a clock frequency of 1866MHz.

Figure 3-20 shows the connections between the LPDDR4 and the Agilex 5 SoC FPGA. **Table 3-14** lists the pin assignments of the LPDDR4 and their I/O standards.

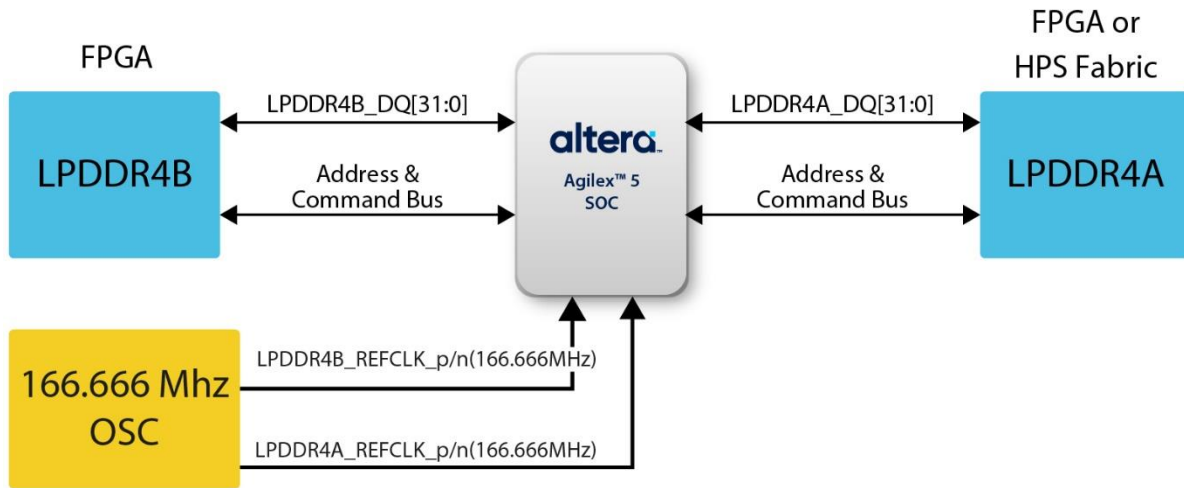


Figure 3-20 Connections between FPGA and LPDDR4

Table 3-14 Pin Assignment of LPDDR4A Memory

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4A_CA[0]	PIN_B66	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4A_CA[1]	PIN_A68	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4A_CA[2]	PIN_B68	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4A_CA[3]	PIN_A70	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4A_CA[4]	PIN_B63	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4A_CA[5]	PIN_A66	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4A_DM[0]	PIN_J59	Data Mask[0]	1.1-V LVSTL
LPDDR4A_DM[1]	PIN_T59	Data Mask[1]	1.1-V LVSTL
LPDDR4A_DM[2]	PIN_J27	Data Mask[2]	1.1-V LVSTL
LPDDR4A_DM[3]	PIN_A25	Data Mask[3]	1.1-V LVSTL
LPDDR4A_CKE	PIN_A61	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4A_CK	PIN_J42	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_CK_n	PIN_G42	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_CS_n	PIN_B58	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4A_DQ[0]	PIN_T62	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4A_DQ[1]	PIN_T56	LPDDR4 Data[1]	1.1-V LVSTL

LPDDR4A_DQ[2]	PIN_G56	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4A_DQ[3]	PIN_E56	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4A_DQ[4]	PIN_G65	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4A_DQ[5]	PIN_J65	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4A_DQ[6]	PIN_M56	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4A_DQ[7]	PIN_M62	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4A_DQ[8]	PIN_W62	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4A_DQ[9]	PIN_M65	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4A_DQ[10]	PIN_M51	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4A_DQ[11]	PIN_T51	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4A_DQ[12]	PIN_AB48	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4A_DQ[13]	PIN_W48	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4A_DQ[14]	PIN_T65	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4A_DQ[15]	PIN_AB62	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4A_DQ[16]	PIN_G24	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4A_DQ[17]	PIN_E24	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4A_DQ[18]	PIN_J35	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4A_DQ[19]	PIN_T32	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4A_DQ[20]	PIN_M32	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4A_DQ[21]	PIN_T24	LPDDR4 Data[21]	1.1-V LVSTL
LPDDR4A_DQ[22]	PIN_G35	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4A_DQ[23]	PIN_M24	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4A_DQ[24]	PIN_A22	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4A_DQ[25]	PIN_A23	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4A_DQ[26]	PIN_A33	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4A_DQ[27]	PIN_B33	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4A_DQ[28]	PIN_B30	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4A_DQ[29]	PIN_A36	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4A_DQ[30]	PIN_A20	LPDDR4 Data[30]	1.1-V LVSTL

LPDDR4A_DQ[31]	PIN_B22	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4A_DQS_n[0]	PIN_E62	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[1]	PIN_W56	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[2]	PIN_E32	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[3]	PIN_A30	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[0]	PIN_G62	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[1]	PIN_AB56	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[2]	PIN_G32	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[3]	PIN_B28	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_RESET_N	PIN_M48	LPDDR4 Reset	1.1-V LVSTL
LPDDR4A_RZQ	PIN_T48	External reference ball for output drive calibration	1.1V
LPDDR4A_REFCLK_p	PIN_B55	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

Table 3-15 Pin Assignment of LPDDR4B Memory

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4B_CA[0]	PIN_DJ51	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4B_CA[1]	PIN_DF51	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4B_CA[2]	PIN_DD51	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4B_CA[3]	PIN_DD48	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4B_CA[4]	PIN_DK48	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4B_CA[5]	PIN_DJ48	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4B_DM[0]	PIN_DJ59	Data Mask[0]	1.1-V LVSTL
LPDDR4B_DM[1]	PIN_DP66	Data Mask[1]	1.1-V LVSTL

LPDDR4B_DM[2]	PIN_DP10	Data Mask[2]	1.1-V LVSTL
LPDDR4B_DM[3]	PIN_DJ12	Data Mask[3]	1.1-V LVSTL
LPDDR4B_CKE	PIN_DJ42	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4B_CK	PIN_DP47	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CK_n	PIN_DN45	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CS_n	PIN_DD42	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4B_DQ[0]	PIN_DJ65	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4B_DQ[1]	PIN_DF65	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4B_DQ[2]	PIN_DD59	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4B_DQ[3]	PIN_DJ56	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4B_DQ[4]	PIN_DD56	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4B_DQ[5]	PIN_DK56	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4B_DQ[6]	PIN_DD65	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4B_DQ[7]	PIN_DD62	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4B_DQ[8]	PIN_DN73	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4B_DQ[9]	PIN_DN74	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4B_DQ[10]	PIN_DP60	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4B_DQ[11]	PIN_DN58	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4B_DQ[12]	PIN_DN61	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4B_DQ[13]	PIN_DP61	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4B_DQ[14]	PIN_DN68	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4B_DQ[15]	PIN_DP70	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4B_DQ[16]	PIN_DN10	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4B_DQ[17]	PIN_DN17	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4B_DQ[18]	PIN_DP20	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4B_DQ[19]	PIN_DN20	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4B_DQ[20]	PIN_DP7	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4B_DQ[21]	PIN_DP22	LPDDR4 Data[21]	1.1-V LVSTL

LPDDR4B_DQ[22]	PIN_DN3	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4B_DQ[23]	PIN_DN7	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4B_DQ[24]	PIN_DD9	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4B_DQ[25]	PIN_DD12	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4B_DQ[26]	PIN_DJ21	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4B_DQ[27]	PIN_DD21	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4B_DQ[28]	PIN_DF21	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4B_DQ[29]	PIN_DD18	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4B_DQ[30]	PIN_DJ9	LPDDR4 Data[30]	1.1-V LVSTL
LPDDR4B_DQ[31]	PIN_DK9	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4B_DQS_n[0]	PIN_DJ62	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[1]	PIN_DN66	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[2]	PIN_DN15	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[3]	PIN_DJ18	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[0]	PIN_DK62	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[1]	PIN_DP68	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[2]	PIN_DP15	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[3]	PIN_DK18	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_RESET_N	PIN_DN55	LPDDR4 Reset	1.1-V LVSTL
LPDDR4B_RZQ	PIN_DP58	External reference ball for output drive calibration	1.1V
LPDDR4B_REFCLK_p	PIN_DK39	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

3.7.5 SDRAM Memory

The board features 128MB of SDRAM with two 64MB (32M×16) SDRAM chip. The chip connects to the FPGA with 16 data lines, 13 address lines and control lines. This chip uses the 1.8V LVCMOS signaling standard. Connections between the FPGA and SDRAM are shown in **Figure 3-21**, and the pin assignment is listed in **Table 3-16**.

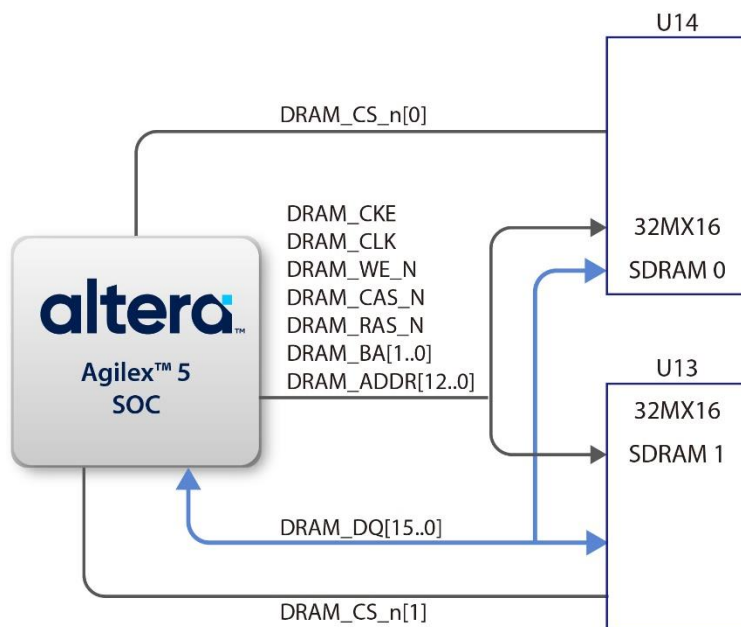


Figure 3-21 Connections between the FPGA and SDRAM

Table 3-16 Pin Assignment of SDRAM

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
DRAM_ADDR[0]	PIN_AC1	SDRAM Address[0]	1.8V
DRAM_ADDR[1]	PIN_AH6	SDRAM Address[1]	1.8V
DRAM_ADDR[2]	PIN_AC2	SDRAM Address[2]	1.8V
DRAM_ADDR[3]	PIN_R8	SDRAM Address[3]	1.8V
DRAM_ADDR[4]	PIN_AE11	SDRAM Address[4]	1.8V
DRAM_ADDR[5]	PIN_AH14	SDRAM Address[5]	1.8V
DRAM_ADDR[6]	PIN_V4	SDRAM Address[6]	1.8V
DRAM_ADDR[7]	PIN_AG26	SDRAM Address[7]	1.8V
DRAM_ADDR[8]	PIN_AG23	SDRAM Address[8]	1.8V
DRAM_ADDR[9]	PIN_V11	SDRAM Address[9]	1.8V
DRAM_ADDR[10]	PIN_BE8	SDRAM Address[10]	1.8V

DRAM_ADDR[11]	PIN_R6	SDRAM Address[11]	1.8V
DRAM_ADDR[12]	PIN_AH11	SDRAM Address[12]	1.8V
DRAM_DQ[0]	PIN_AU1	SDRAM Data[0]	1.8V
DRAM_DQ[1]	PIN_AJ1	SDRAM Data[1]	1.8V
DRAM_DQ[2]	PIN_BA1	SDRAM Data[2]	1.8V
DRAM_DQ[3]	PIN_AP1	SDRAM Data[3]	1.8V
DRAM_DQ[4]	PIN_AM2	SDRAM Data[4]	1.8V
DRAM_DQ[5]	PIN_BL1	SDRAM Data[5]	1.8V
DRAM_DQ[6]	PIN_AJ2	SDRAM Data[6]	1.8V
DRAM_DQ[7]	PIN_AP2	SDRAM Data[7]	1.8V
DRAM_DQ[8]	PIN_BH4	SDRAM Data[8]	1.8V
DRAM_DQ[9]	PIN_AH4	SDRAM Data[9]	1.8V
DRAM_DQ[10]	PIN_BH6	SDRAM Data[10]	1.8V
DRAM_DQ[11]	PIN_AU2	SDRAM Data[11]	1.8V
DRAM_DQ[12]	PIN_BE6	SDRAM Data[12]	1.8V
DRAM_DQ[13]	PIN_BD2	SDRAM Data[13]	1.8V
DRAM_DQ[14]	PIN_BG2	SDRAM Data[14]	1.8V
DRAM_DQ[15]	PIN_BL2	SDRAM Data[15]	1.8V
DRAM_BA[0]	PIN_AT6	SDRAM Bank Address[0]	1.8V
DRAM_BA[1]	PIN_AV4	SDRAM Bank Address[1]	1.8V
DRAM_LDQM	PIN_BD1	SDRAM byte Data Mask[0]	1.8V
DRAM_UDQM	PIN_AT8	SDRAM byte Data Mask[1]	1.8V
DRAM_RAS_N	PIN_V6	SDRAM Row Address Strobe	1.8V
DRAM_CAS_N	PIN_AE6	SDRAM Column Address Strobe	1.8V
DRAM_CKE	PIN_AE8	SDRAM Clock Enable	1.8V
DRAM_CLK	PIN_R11	SDRAM Clock	1.8V
DRAM_WE_N	PIN_AV6	SDRAM Write Enable	1.8V
DRAM_CS_N[0]	PIN_AF1	SDRAM Chip Select	1.8V
DRAM_CS_N[1]	PIN_AE14	SDRAM Chip Select	1.8V

3.7.6 A/D Converter and 2x5 Header

The DE25-Nano features the TI TLA2518, an 8-channel, multiplexed, 12-bit successive approximation register (SAR) analog-to-digital converter capable of sampling rates up to 1MSPS. The analog input range for all input channels extends from 0 V to 3.4V (default setting is 3.4V, it can be modified to 5.1 V). The flexible SPI interface allows the external serial output data clock (SCLK) to operate at frequencies up to 60MHz. The ADC can be configured to accept eight single-ended analog input signals at ADC_IN0 through ADC_IN7. Alternatively, these pins can be reconfigured as digital inputs or outputs in GPIO mode. These eight signals are routed to a 2×5 header, as shown in **Figure 3-22**.

More information about the A/D converter chip is available in its datasheet, which can be found on the manufacturer's website or in the directory \datasheet\ADC of the DE25-Nano system CD.

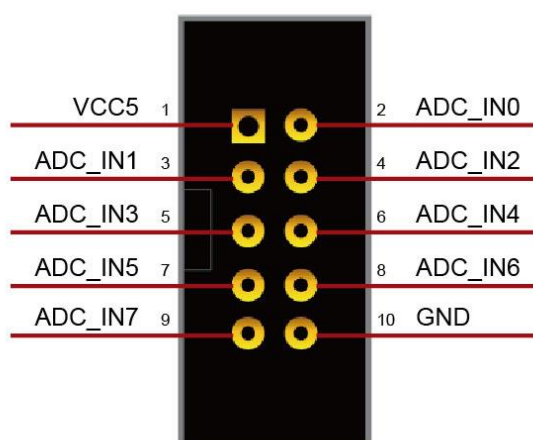


Figure 3-22 Signals of the 2x5 Header

Figure 3-23 shows the connections between the FPGA, 2×5 header, and the A/D converter. **Table 3-17** shows the pin assignment of the A/D converter.

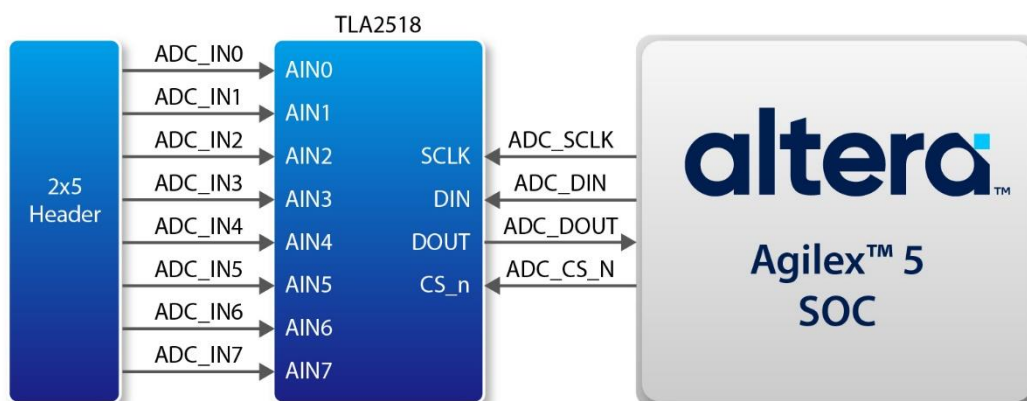


Figure 3-23 Connections between the FPGA, 2x5 header and the A/D converter

Table 3-17 Pin Assignment of ADC

Signal Name	FPGA Pin No.	Description	I/O Standard
ADC_CS_n	PIN_CE19	Conversion Start	3.3V
ADC_SDO	PIN_CH19	Digital data input	3.3V
ADC_SDI	PIN_CR8	Digital data output	3.3V
ADC_SCK	PIN_CH6	Digital clock output	3.3V

3.7.7 MIPI Connector

The Agilex 5 devices offer a native mobile industry processor interface (MIPI) D-PHY. This support complies with MIPI D-PHY version 2.5 and allows transmission or reception of data with MIPI D-PHY interfaces. It provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

The board provides a 22-pin FPC connector (1 clock lane and 2 data lanes), allowing users to connect MIPI interface cameras and display devices through a FPC cable (see **Figure 3-24**). Users can use this connector and camera cable to connect to devices such as Raspberry Pi camera modules. In addition, it can also be connected with a display device such as a Raspberry Pi MIPI display module.

Figure 3-25 shows the connections between the FPGA and the 22-pin MIPI connector. **Table 3-18** shows the pin assignments of the 22-pin MIPI connector.

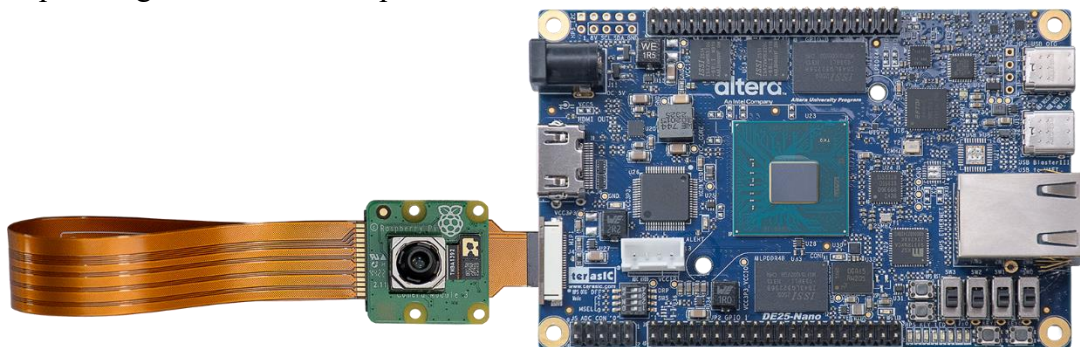


Figure 3-24 MIPI camera module connects to the board via cable

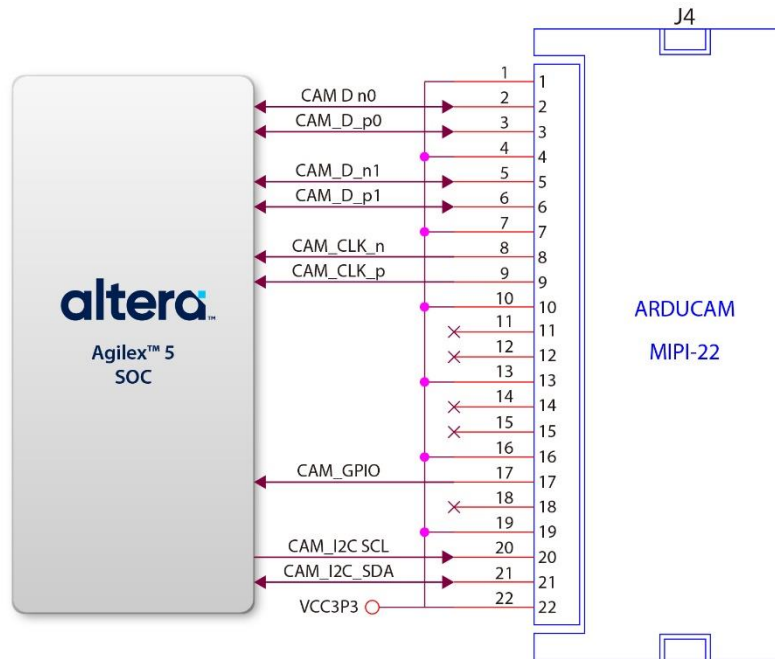


Figure 3-25 Connections between the FPGA and the 22-pin MIPI connector

Table 3-18 Pin Assignment of 22-pin MIPI connector

Signal Name	FPGA Pin No.	Description	I/O Standard
CAM_CLK_P	PIN_DP33	MIPI Clock positive	DPHY
CAM_CLK_N	PIN_DN30	MIPI Clock negative	DPHY
CAM_D_P[0]	PIN_DP36	MIPI Data 0 positive	DPHY
CAM_D_P[1]	PIN_DP38	MIPI Data 1 positive	DPHY
CAM_D_N[0]	PIN_DN33	MIPI Data 0 negative	DPHY
CAM_D_N[1]	PIN_DN38	MIPI Data 1 negative	DPHY
CAM_I2C_SCL	PIN_BP2	I2C clock	3.3V
CAM_I2C_SDA	PIN_BP1	I2C data	3.3V
CAM_GPIO	PIN_BR8	GPIO signal	3.3V
CAM_RZQ1	PIN_DD35	External reference ball for output drive calibration	1.1V

3.8 Peripherals Connected to the Hard Processor System

This section introduces the interfaces connected to the HPS section of the Agilex 5 SoC FPGA. Users can access these interfaces via the HPS processors.

3.8.1 User Push-buttons and LEDs

Like the FPGA, the HPS is directly connected to its own pushbutton and LED through its GPIO interface, which can be read or written from code running on the HPS processors.

Table 3-19 gives the pin assignment of all the LEDs, switches, and push-buttons.

Table 3-19 Pin Assignment of LEDs, Switches and Push-buttons

Signal Name	HPS GPIO	FPGA Pin No.	Function
HPS_KEY	GPIO1_IO16	PIN_F75	I/O
HPS_LED	GPIO1_IO17	PIN_AD71	I/O

3.8.2 Gigabit Ethernet

The board supports Gigabit Ethernet communication through an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports an RGMII MAC interface. **Figure 3-26** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

The pin assignment associated with the Gigabit Ethernet interface is listed in **Table 3-20**. More information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, is available on the manufacturer's website.

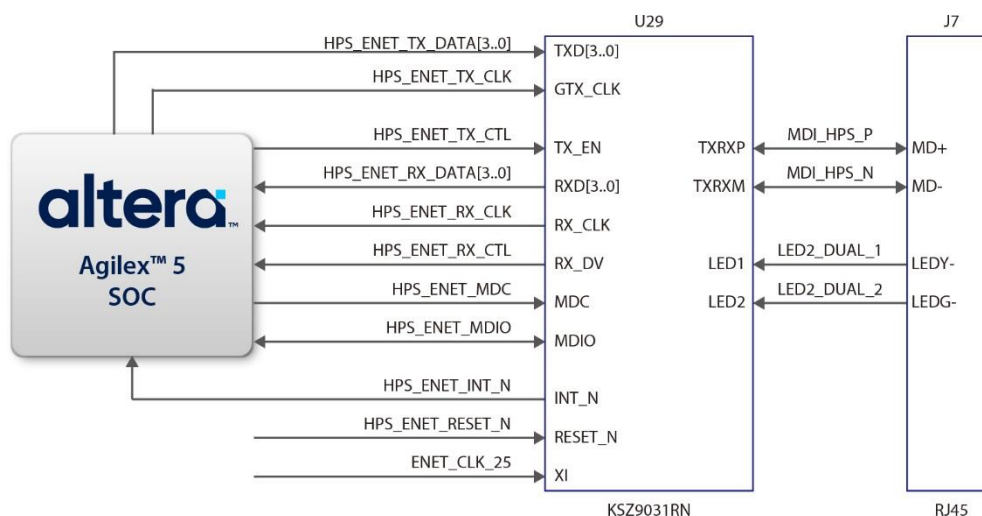


Figure 3-26 Connections between the HPS and Gigabit Ethernet

Table 3-20 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_ENET_TX_CTL	PIN_BL74	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_BG74	GMII and MII transmit data[0]	1.8V

HPS_ENET_TX_DATA[1]	PIN_AP75	GMII and MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_BD75	GMII and MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_AM74	GMII and MII transmit data[3]	1.8V
HPS_ENET_TX_CLK	PIN_BP75	GMII and MII transmit clock	1.8V
HPS_ENET_RX_CTL	PIN_AP74	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_BD74	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_AN71	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_AJ74	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_AJ75	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_BL75	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_C74	Management Data	1.8V
HPS_ENET_MDC	PIN_D71	Management Data Clock Reference	1.8V

There are two LEDs, green LED (LEDG) and yellow LED (LEDY), which report the status of Ethernet PHY (KSZ9031RNI). The LED control signals are connected to the LEDs on the RJ45 connector. The state and definition of LEDG and LEDY are listed in [Table 3-21](#). For instance, the LEDG light indicates the connection from the board to the Gigabit Ethernet interface has been established.

Table 3-21 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

3.8.3 UART to USB

The board provides a UART interface for users to communicate and transfer data with the FPGA and HPS through the host. The interface is implemented via the FT4232H chip in the USB Blaster III circuit. Connecting a USB cable between the DE25-Nano's Type-C port and the host enables both USB Blaster III and HPS UART functions.

Figure 3-27 shows the connections between the FPGA (HPS), FT4232H chip, and the USB Type-C connector. **Table 3-22** lists the pin assignments of the UART interface connected to the HPS.

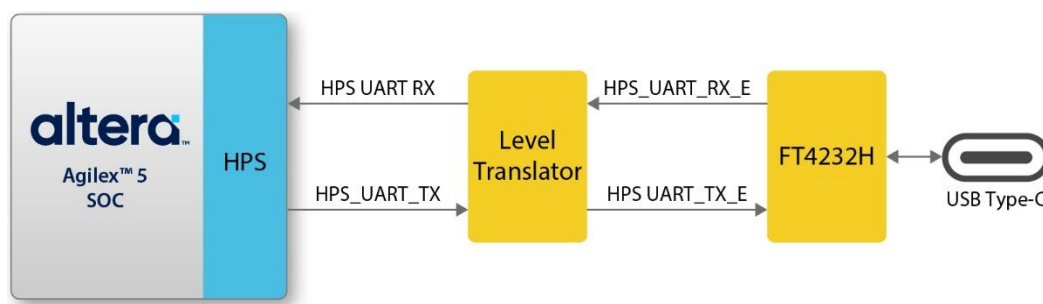


Figure 3-27 Connections between the HPS and FT4232H Chip

Table 3-22 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_AD72	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_N71	HPS UART Transmitter	1.8V

3.8.4 Micro SD Card Socket

The board supports a Micro SD card interface with 4 data lines. It serves not only as an external storage for the HPS but also as an alternative boot option for the DE25-Nano board. **Figure 3-28** shows the signals connected between the HPS and the Micro SD card socket.

Table 3-23 lists the pin assignment of Micro SD card socket to the HPS.

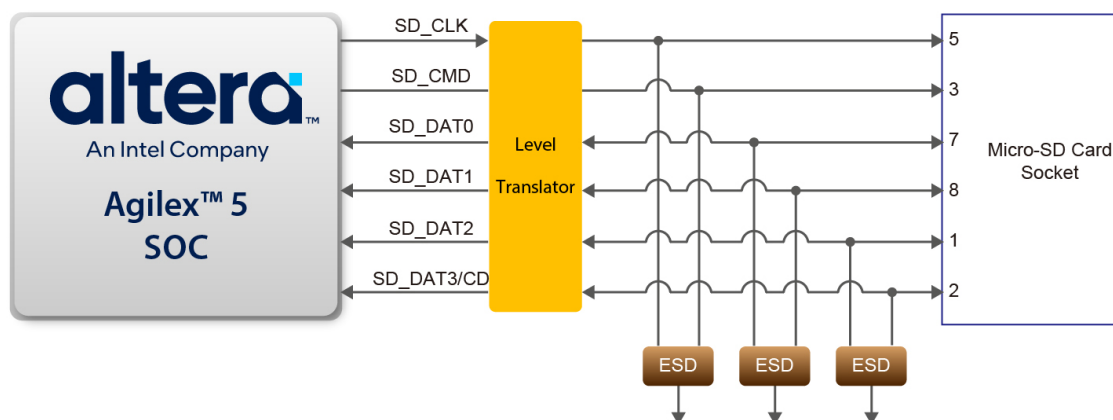


Figure 3-28 Connections between the FPGA and SD card socket

Table 3-23 Pin Assignment of Micro SD Card Socket

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_SD_CLK	PIN_AC74	HPS SD Clock	1.8V
HPS_SD_CMD	PIN_AK69	HPS SD Command Line	1.8V
HPS_SD_DATA[0]	PIN_AF75	HPS SD Data[0]	1.8V
HPS_SD_DATA[1]	PIN_AC75	HPS SD Data[1]	1.8V
HPS_SD_DATA[2]	PIN_AN64	HPS SD Data[2]	1.8V
HPS_SD_DATA[3]	PIN_Y74	HPS SD Data[3]	1.8V

3.8.5 USB 2.0 OTG

The board provides USB interfaces using the SMSC USB3320 controller. A SMSC USB3320 device in a 32-pin QFN package device is used to interface to a single Type-C USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Type-C USB interface. **Figure 3-29** shows the connections of USB PTG PHY to the HPS. **Table 3-24** lists the pin assignment of the USB OTG PHY to the HPS.

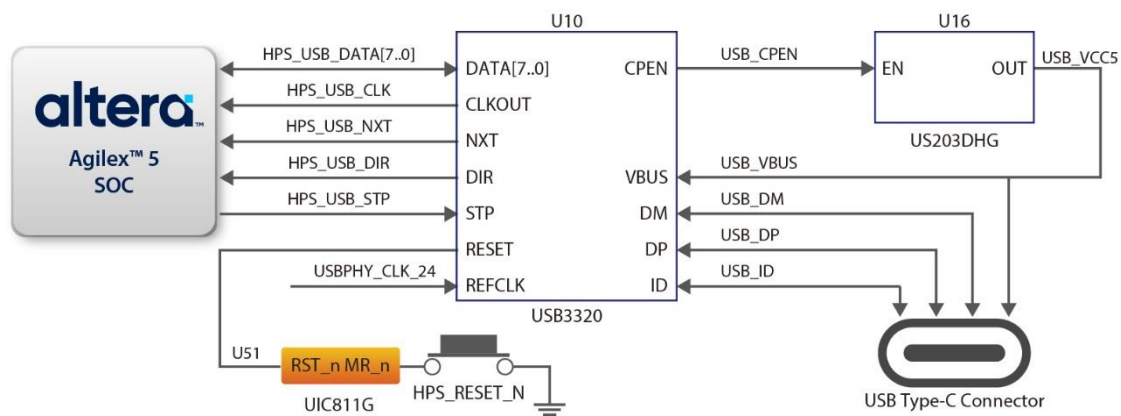


Figure 3-29 Connections between the HPS and USB OTG PHY

Table 3-24 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLK	PIN_BC64	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_AN72	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_AY69	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_BC71	HPS USB_DATA[2]	1.8V

HPS_USB_DATA[3]	PIN_AU74	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_AY71	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_AU75	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_BC72	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_BP74	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_AY67	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_BA75	Throttle the Data	1.8V
HPS_USB_STP	PIN_BC67	Stop Data Stream on the Bus	1.8V

3.8.6 Accelerometer (G-sensor)

The board comes with a digital accelerometer sensor module (LIS2DW12), commonly known as a G-sensor. This G-sensor is a small, thin, ultra-low-power-consumption 3-axis accelerometer with high-resolution measurement. Digitized output is formatted in 16-bit two's complement and can be accessed through an I2C interface. The I2C address of the G-sensor is 0x32H/0x33H. More information about this chip can be found in its datasheet, which is available on the manufacturer's website or in the \Datasheet folder of the DE25-Nano system CD. **Figure 3-30** shows the connections between the HPS and the G-sensor. **Table 3-25** lists the pin assignments of the G-sensor to the HPS.

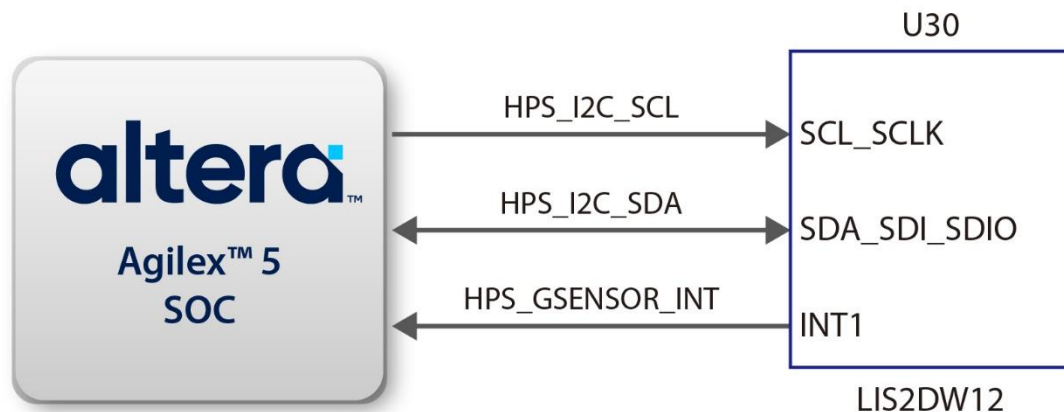


Figure 3-30 Connections between Agilex 5 SoC FPGA and G-Sensor

Table 3-25 Pin Assignment of G-sensor

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_GSENSOR_INT	PIN_Y75	HPS GSENSOR Interrupt Output	1.8V
HPS_I2C_SCL	PIN_N72	HPS I2C Clock	1.8V
HPS_I2C_SDA	PIN_L75	HPS I2C Data	1.8V

Chapter 4

DE25-Nano System Builder

This chapter describes how users can create a custom design project with the tool named DE25-Nano System Builder.

4.1 Introduction

The DE25-Nano System Builder is a Windows-based utility. It is designed to help users create a Quartus project for DE25-Nano within minutes. The generated Quartus project files include:

- Quartus project file (.qpf)
- Quartus setting file (.qsf)
- Top-level design file (.v)
- Synopsis design constraints file (.sdc)
- Pin assignment document (.htm)

The above files generated by the DE25-Nano System Builder can also prevent occurrence of situations that are prone to compilation error when users manually edit the top-level design file or place pin assignment. The common mistakes that users encounter are:

- Board is damaged due to incorrect bank voltage setting or pin assignment.
- Board is malfunctioned because of wrong device chosen, declaration of pin location or direction is incorrect or forgotten.
- Performance degradation due to improper pin assignment.

4.2 General Design Flow

This section provides an introduction to the design flow of building a Quartus project for DE25-Nano under the DE25-Nano System Builder. The design flow is illustrated in **Figure 4-1**.

The DE25-Nano System Builder will generate two major files, a top-level design file (.v) and a Quartus setting file (.qsf) after users launch the DE25-Nano System Builder and create a new project according to their design requirements.

The top-level design file contains a top-level Verilog HDL wrapper for users to add their own design/logic. The Quartus setting file contains information such as FPGA device type, top-level pin assignment, and the I/O standard for each user-defined I/O pin.

Finally, the Quartus programmer is used to download .sof file to the development board via JTAG interface.

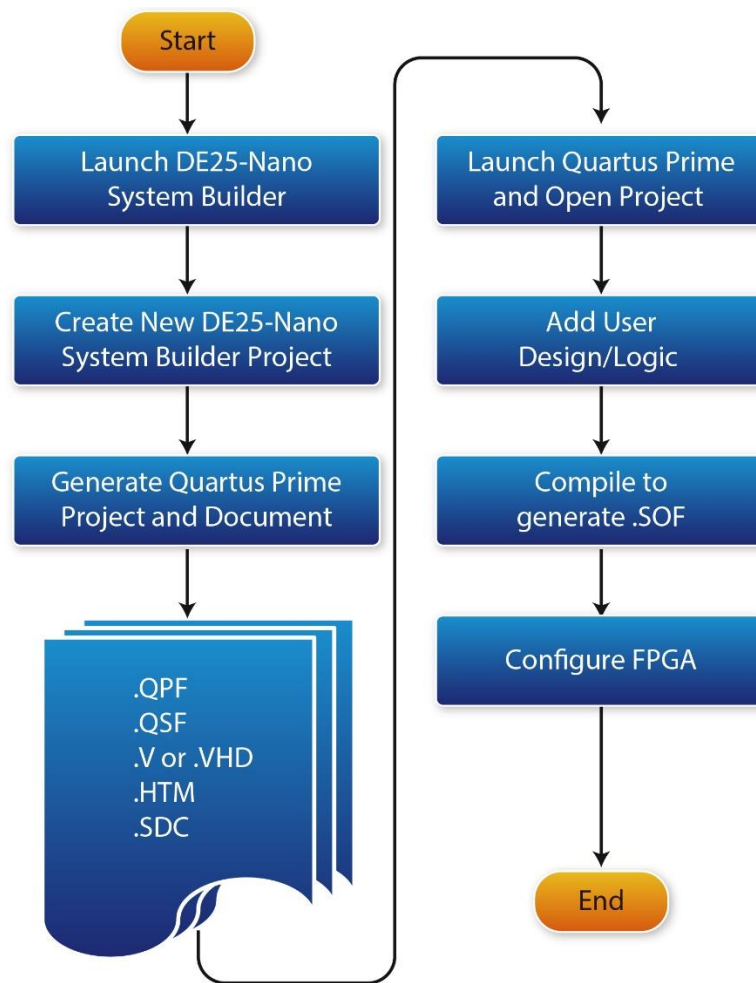


Figure 4-1 Design flow of building a project from the beginning to the end

4.3 Using the DE25-Nano System Builder

This section provides the procedures in details on how to use the DE25-Nano System Builder.

■ Install and Launch the DE25-Nano System Builder

The DE25-Nano System Builder is located in the directory Tools\SystemBuilder of the DE25-Nano System CD. Users can copy the entire folder to a host computer without installing the utility. A window will pop up, as shown in **Figure 4-2**, after executing the DE25-Nano SystemBuilder.exe on the host computer.

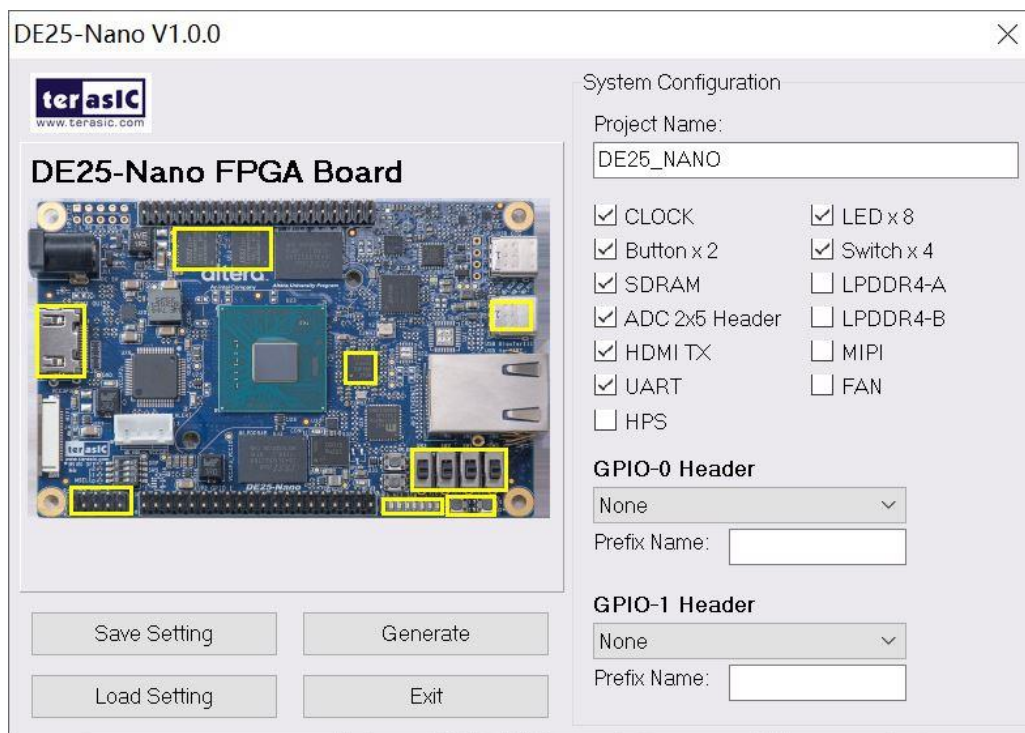


Figure 4-2 The GUI of DE25-Nano System Builder

■ Enter Project Name

Enter the project name in the circled area, as shown in [Figure 4-3](#).

The project name typed in will be assigned automatically as the name of your top-level design entity.

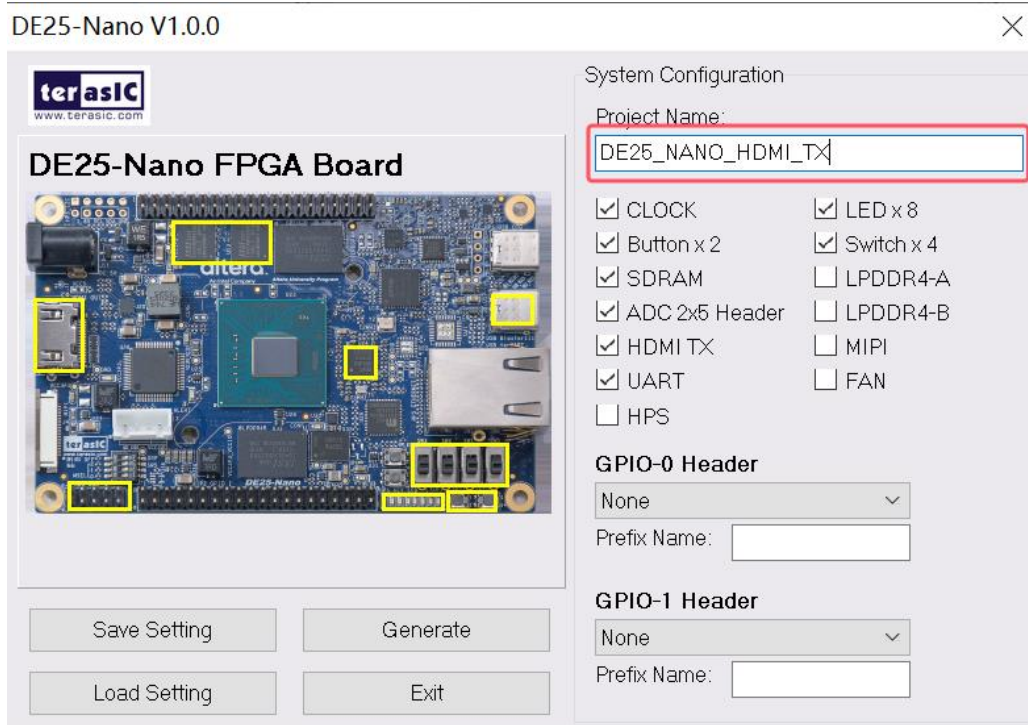


Figure 4-3 Enter the project name

■ System Configuration

Users are given the flexibility in the System Configuration to include their choice of components in the project, as shown in **Figure 4-4**. Each component onboard is listed and users can enable or disable one or more components at will. If a component is enabled, the DE25-Nano System Builder will automatically generate its associated pin assignment, including the pin name, pin location, pin direction, and I/O standard.

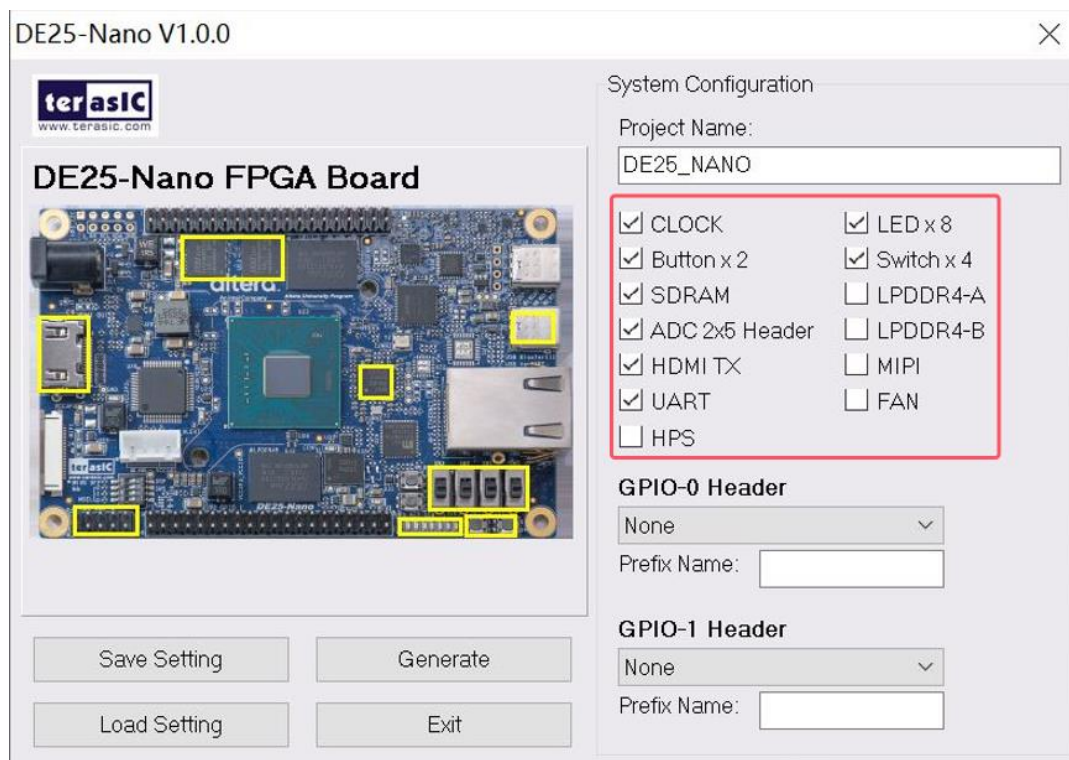


Figure 4-4 System configuration group

■ GPIO Expansion

If users connect any Terasic GPIO-based daughter card to the GPIO connector(s) on DE25-Nano, the DE25-Nano System Builder can generate a project that include the corresponding module, as shown in **Figure 4-5**. It will also generate the associated pin assignment automatically, including pin name, pin location, pin direction, and I/O standard.

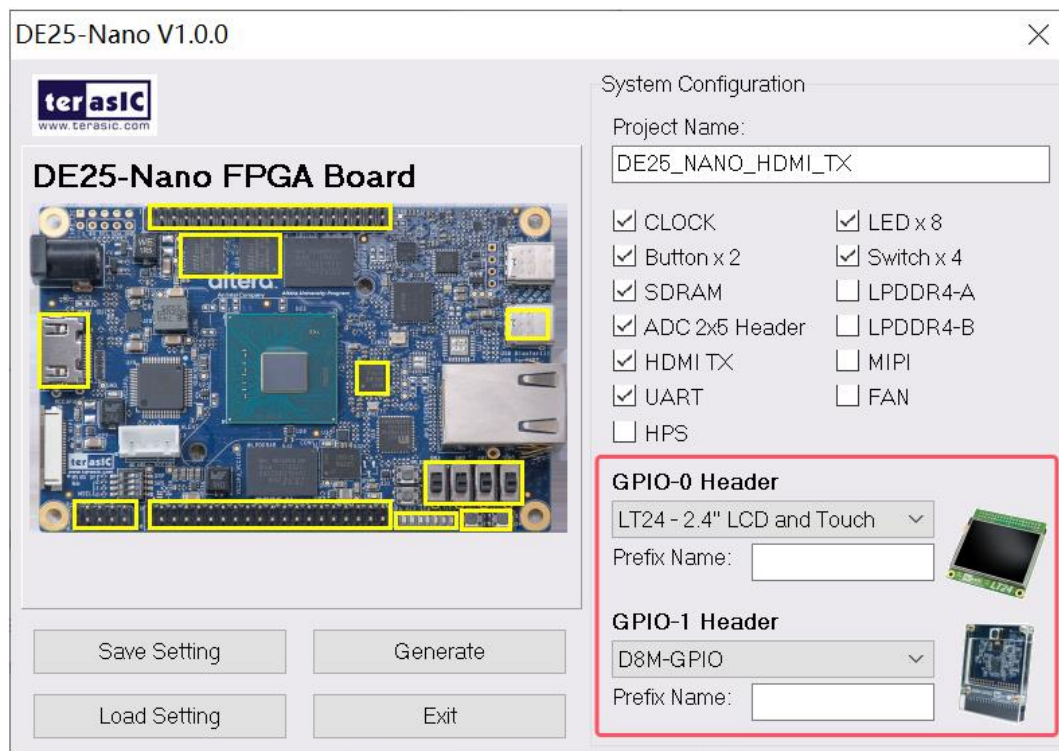


Figure 4-5 GPIO expansion group

The “Prefix Name” is an optional feature that denote the pin name of the daughter card assigned in your design. Users may leave this field blank.

■ Project Setting Management

The DE25-Nano System Builder also provides the option to load a setting or save users’ current board configuration in .cfg file, as shown in **Figure 4-6**.

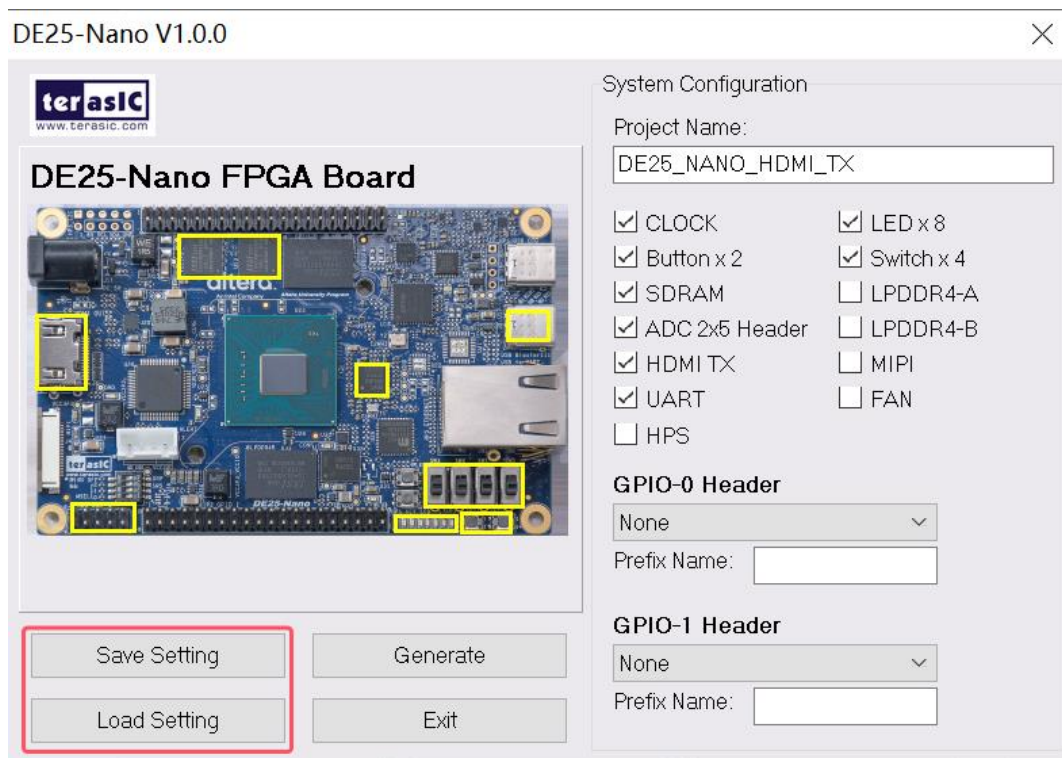


Figure 4-6 Project Settings

■ Project Generation

When users press the Generate button, the DE25-Nano System Builder will generate the corresponding Quartus files and documents, as listed in [Table 4-1](#):

Table 4-1 Files generated by the DE25-Nano System Builder

No.	Filename	Description
1	<Project name>.v	Top level Verilog HDL file for Quartus
2	<Project name>.qpf	Quartus Project File
3	<Project name>.qsf	Quartus Setting File
4	<Project name>.sdc	Synopsis Design Constraints file for Quartus
5	<Project name>.htm	Pin Assignment Document

Users can add custom logic into the project in Quartus and compile the project to generate the SRAM Object File (.sof).

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