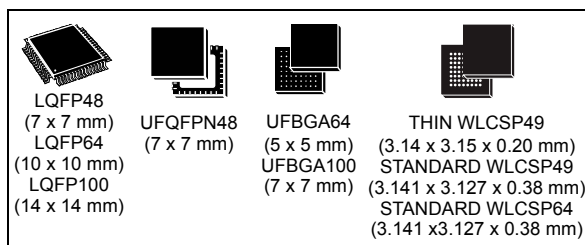


Ultra-low-power Arm[®] Cortex[®]-M4 32-bit MCU+FPU, 100DMIPS,
256KB Flash, 64KB SRAM, USB FS, LCD, analog, audio, AES

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
 - 1.71 V to 3.6 V power supply
 - -40 °C to 85/105/125 °C temperature range
 - 200 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
 - 8 nA Shutdown mode (5 wakeup pins)
 - 28 nA Standby mode (5 wakeup pins)
 - 280 nA Standby mode with RTC
 - 1.0 µA Stop 2 mode, 1.28 µA with RTC
 - 84 µA/MHz run mode
 - Batch acquisition mode (BAM)
 - 4 µs wakeup from Stop mode
 - Brown out reset (BOR)
 - Interconnect matrix
- Core: Arm[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS and DSP instructions
- Performance benchmark
 - 1.25 DMIPS/MHz (Drystone 2.1)
 - 273.55 CoreMark[®] (3.42 CoreMark/MHz @ 80 MHz)
- Energy benchmark
 - 347 ULPMark™ CP score
 - 121 ULPMark™ PP score
- Clock Sources
 - 4 to 48 MHz crystal oscillator
 - 32 kHz crystal oscillator for RTC (LSE)
 - Internal 16 MHz factory-trimmed RC (±1%)
 - Internal low-power 32 kHz RC (±5%)
 - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
 - Internal 48 MHz with clock recovery
 - 2 PLLs for system clock, USB, audio, ADC



- Up to 83 fast I/Os, most 5 V-tolerant
- RTC with HW calendar, alarms and calibration
- LCD 8× 40 or 4× 44 with step-up converter
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 11x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 2x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Memories
 - 256 KB single bank Flash, proprietary code readout protection
 - 64 KB of SRAM including 16 KB with hardware parity check
 - Quad SPI memory interface
- Rich analog peripherals (independent supply)
 - 1x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
 - 2x 12-bit DAC output channels, low-power sample and hold
 - 1x operational amplifier with built-in PGA
 - 2x ultra-low-power comparators
- AES: 128/256-bit key encryption hardware accelerator
- 17x communication interfaces
 - USB 2.0 full-speed crystal less solution with LPM and BCD
 - 1x SAI (serial audio interface)
 - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
 - 4x USARTs (ISO 7816, LIN, IrDA, modem)
 - 1x LPUART (Stop 2 wake-up)

- 3x SPIs (and 1x Quad SPI)
- CAN (2.0B Active) and SDMMC interface
- SWPMI single wire protocol master I/F
- IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™
- All packages are ECOPACK2® compliant

Contents

1	Introduction	12
2	Description	13
3	Functional overview	17
3.1	Arm® Cortex®-M4 core with FPU	17
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	17
3.3	Memory protection unit	17
3.4	Embedded Flash memory	18
3.5	Embedded SRAM	19
3.6	Firewall	19
3.7	Boot modes	20
3.8	Cyclic redundancy check calculation unit (CRC)	20
3.9	Power supply management	20
3.9.1	Power supply schemes	20
3.9.2	Power supply supervisor	22
3.9.3	Voltage regulator	23
3.9.4	Low-power modes	23
3.9.5	Reset mode	31
3.9.6	VBAT operation	31
3.10	Interconnect matrix	32
3.11	Clocks and startup	34
3.12	General-purpose inputs/outputs (GPIOs)	37
3.13	Direct memory access controller (DMA)	37
3.14	Interrupts and events	38
3.14.1	Nested vectored interrupt controller (NVIC)	38
3.14.2	Extended interrupt/event controller (EXTI)	38
3.15	Analog to digital converter (ADC)	39
3.15.1	Temperature sensor	39
3.15.2	Internal voltage reference (VREFINT)	40
3.15.3	VBAT battery voltage monitoring	40
3.16	Digital to analog converter (DAC)	40

3.17	Voltage reference buffer (VREFBUF)	41
3.18	Comparators (COMP)	42
3.19	Operational amplifier (OPAMP)	42
3.20	Touch sensing controller (TSC)	42
3.21	Liquid crystal display controller (LCD)	43
3.22	Random number generator (RNG)	43
3.23	Advanced encryption standard hardware accelerator (AES)	43
3.24	Timers and watchdogs	44
3.24.1	Advanced-control timer (TIM1)	45
3.24.2	General-purpose timers (TIM2, TIM15, TIM16)	46
3.24.3	Basic timers (TIM6 and TIM7)	46
3.24.4	Low-power timer (LPTIM1 and LPTIM2)	46
3.24.5	Infrared interface (IRTIM)	47
3.24.6	Independent watchdog (IWDG)	47
3.24.7	System window watchdog (WWDG)	47
3.24.8	SysTick timer	47
3.25	Real-time clock (RTC) and backup registers	48
3.26	Inter-integrated circuit interface (I ² C)	49
3.27	Universal synchronous/asynchronous receiver transmitter (USART) ...	50
3.28	Low-power universal asynchronous receiver transmitter (LPUART) ...	51
3.29	Serial peripheral interface (SPI)	52
3.30	Serial audio interfaces (SAI)	52
3.31	Single wire protocol master interface (SWPMI)	53
3.32	Controller area network (CAN)	53
3.33	Secure digital input/output and MultiMediaCards Interface (SDMMC) ...	54
3.34	Universal serial bus (USB)	54
3.35	Clock recovery system (CRS)	55
3.36	Quad SPI memory interface (QUADSPI)	55
3.37	Development support	56
3.37.1	Serial wire JTAG debug port (SWJ-DP)	56
3.37.2	Embedded Trace Macrocell™	56
4	Pinouts and pin description	57
5	Memory mapping	83

6	Electrical characteristics	87
6.1	Parameter conditions	87
6.1.1	Minimum and maximum values	87
6.1.2	Typical values	87
6.1.3	Typical curves	87
6.1.4	Loading capacitor	87
6.1.5	Pin input voltage	87
6.1.6	Power supply scheme	88
6.1.7	Current consumption measurement	89
6.2	Absolute maximum ratings	89
6.3	Operating conditions	92
6.3.1	General operating conditions	92
6.3.2	Operating conditions at power-up / power-down	93
6.3.3	Embedded reset and power control block characteristics	93
6.3.4	Embedded voltage reference	96
6.3.5	Supply current characteristics	98
6.3.6	Wakeup time from low-power modes and voltage scaling transition times	118
6.3.7	External clock source characteristics	121
6.3.8	Internal clock source characteristics	126
6.3.9	PLL characteristics	133
6.3.10	Flash memory characteristics	134
6.3.11	EMC characteristics	135
6.3.12	Electrical sensitivity characteristics	136
6.3.13	I/O current injection characteristics	137
6.3.14	I/O port characteristics	138
6.3.15	NRST pin characteristics	143
6.3.16	Extended interrupt and event controller input (EXTI) characteristics	144
6.3.17	Analog switches booster	144
6.3.18	Analog-to-Digital converter characteristics	145
6.3.19	Digital-to-Analog converter characteristics	158
6.3.20	Voltage reference buffer characteristics	163
6.3.21	Comparator characteristics	165
6.3.22	Operational amplifiers characteristics	166
6.3.23	Temperature sensor characteristics	169
6.3.24	V _{BAT} monitoring characteristics	170
6.3.25	LCD controller characteristics	171

6.3.26	Timer characteristics	172
6.3.27	Communication interfaces characteristics	173
7	Package information	186
7.1	LQFP100 package information	186
7.2	UFBGA100 package information	190
7.3	LQFP64 package information	193
7.4	UFBGA64 package information	195
7.5	STANDARD WLCSP64 package information	198
7.6	STANDARD WLCSP49 package information	201
7.7	THIN WLCSP49 package information	204
7.8	LQFP48 package information	207
7.9	UFQFPN48 package information	211
7.10	Thermal characteristics	214
7.10.1	Reference document	214
7.10.2	Selecting the product temperature range	215
8	Ordering information	217
9	Revision history	218

List of tables

Table 1.	STM32L443xx family device features and peripheral counts	14
Table 2.	Access status versus readout protection level and execution modes.	18
Table 3.	STM32L443xx modes overview	24
Table 4.	Functionalities depending on the working mode.	29
Table 5.	STM32L443xx peripherals interconnect matrix	32
Table 6.	DMA implementation	37
Table 7.	Temperature sensor calibration values.	40
Table 8.	Internal voltage reference calibration values	40
Table 9.	Timer feature comparison.	44
Table 10.	I2C implementation.	49
Table 11.	STM32L443xx USART/LPUART features	50
Table 12.	SAI implementation.	53
Table 13.	Legend/abbreviations used in the pinout table	61
Table 14.	STM32L443xx pin definitions	61
Table 15.	Alternate function AF0 to AF7.	72
Table 16.	Alternate function AF8 to AF15.	77
Table 17.	STM32L443xx memory map and peripheral register boundary addresses	84
Table 18.	Voltage characteristics	89
Table 19.	Current characteristics	90
Table 20.	Thermal characteristics.	91
Table 21.	General operating conditions	92
Table 22.	Operating conditions at power-up / power-down	93
Table 23.	Embedded reset and power control block characteristics.	94
Table 24.	Embedded internal voltage reference.	96
Table 25.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)	99
Table 26.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable	100
Table 27.	Current consumption in Run and Low-power run modes, code with data processing running from SRAM1	101
Table 28.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)	102
Table 29.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable	103
Table 30.	Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1	103
Table 31.	Current consumption in Sleep and Low-power sleep modes, Flash ON	104
Table 32.	Current consumption in Low-power sleep modes, Flash in power-down	105
Table 33.	Current consumption in Stop 2 mode	105
Table 34.	Current consumption in Stop 1 mode	108
Table 35.	Current consumption in Stop 0	110
Table 36.	Current consumption in Standby mode	111
Table 37.	Current consumption in Shutdown mode	112
Table 38.	Current consumption in VBAT mode	114
Table 39.	Peripheral current consumption	116
Table 40.	Low-power mode wakeup timings	119
Table 41.	Regulator modes transition times	120
Table 42.	Wakeup time using USART/LPUART.	120

Table 43.	High-speed external user clock characteristics	121
Table 44.	Low-speed external user clock characteristics	122
Table 45.	HSE oscillator characteristics	123
Table 46.	LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)	124
Table 47.	HSI16 oscillator characteristics	126
Table 48.	MSI oscillator characteristics	128
Table 49.	HSI48 oscillator characteristics	131
Table 50.	LSI oscillator characteristics	132
Table 51.	PLL, PLLSAI1 characteristics	133
Table 52.	Flash memory characteristics	134
Table 53.	Flash memory endurance and data retention	134
Table 54.	EMS characteristics	135
Table 55.	EMI characteristics	136
Table 56.	ESD absolute maximum ratings	136
Table 57.	Electrical sensitivities	137
Table 58.	I/O current injection susceptibility	137
Table 59.	I/O static characteristics	138
Table 60.	Output voltage characteristics	140
Table 61.	I/O AC characteristics	141
Table 62.	NRST pin characteristics	143
Table 63.	EXTI Input Characteristics	144
Table 64.	Analog switches booster characteristics	144
Table 65.	ADC characteristics	145
Table 66.	Maximum ADC RAIN	147
Table 67.	ADC accuracy - limited test conditions 1	149
Table 68.	ADC accuracy - limited test conditions 2	151
Table 69.	ADC accuracy - limited test conditions 3	153
Table 70.	ADC accuracy - limited test conditions 4	155
Table 71.	DAC characteristics	158
Table 72.	DAC accuracy	161
Table 73.	VREFBUF characteristics	163
Table 74.	COMP characteristics	165
Table 75.	OPAMP characteristics	166
Table 76.	TS characteristics	169
Table 77.	V _{BAT} monitoring characteristics	170
Table 78.	V _{BAT} charging characteristics	170
Table 79.	LCD controller characteristics	171
Table 80.	TIMx characteristics	172
Table 81.	IWDG min/max timeout period at 32 kHz (LSI)	172
Table 82.	WWDG min/max timeout value at 80 MHz (PCLK)	173
Table 83.	I2C analog filter characteristics	173
Table 84.	SPI characteristics	174
Table 85.	Quad SPI characteristics in SDR mode	177
Table 86.	QUADSPI characteristics in DDR mode	178
Table 87.	SAI characteristics	180
Table 88.	SD / MMC dynamic characteristics, VDD=2.7 V to 3.6 V	182
Table 89.	eMMC dynamic characteristics, VDD = 1.71 V to 1.9 V	183
Table 90.	USB electrical characteristics	184
Table 91.	SWPMI electrical characteristics	185
Table 92.	LQFP - 100 pins, 14 x 14 mm low-profile quad flat package mechanical data	187
Table 93.	UFPGA - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid	

	array package mechanical data	190
Table 94.	UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)	191
Table 95.	LQFP - 64 pins, 10 x 10 mm low-profile quad flat package mechanical data	193
Table 96.	UFBGA – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data	196
Table 97.	UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)	197
Table 98.	STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package mechanical data	198
Table 99.	STANDARD WLCSP64 recommended PCB design rules (0.35 mm pitch)	200
Table 100.	STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package mechanical data	202
Table 101.	STANDARD WLCSP49 recommended PCB design rules (0.4 mm pitch)	203
Table 102.	THIN WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale mechanical data	204
Table 103.	THIN WLCSP49 recommended PCB design rules	206
Table 104.	LQFP - 48 pins, 7 x 7 mm low-profile quad flat package mechanical data	208
Table 105.	UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	212
Table 106.	Package thermal characteristics	214
Table 107.	STM32L443xx ordering information scheme	217
Table 108.	Document revision history	218

List of figures

Figure 1.	STM32L443xx block diagram	16
Figure 2.	Power supply overview	21
Figure 3.	Power-up/down sequence	22
Figure 4.	Clock tree	36
Figure 5.	Voltage reference buffer	41
Figure 6.	STM32L443Vx LQFP100 pinout ⁽¹⁾	57
Figure 7.	STM32L443Vx UFBGA100 ballout ⁽¹⁾	58
Figure 8.	STM32L443Rx LQFP64 pinout ⁽¹⁾	58
Figure 9.	STM32L443Rx UFBGA64 ballout ⁽¹⁾	59
Figure 10.	STM32L443Rx WLCSP64 pinout ⁽¹⁾	59
Figure 11.	STM32L443Cx WLCSP49 pinout ⁽¹⁾	59
Figure 12.	STM32L443Cx LQFP48 pinout ⁽¹⁾	60
Figure 13.	STM32L443Cx UFQFPN48 pinout ⁽¹⁾	60
Figure 14.	STM32L443xx memory map	83
Figure 15.	Pin loading conditions	87
Figure 16.	Pin input voltage	87
Figure 17.	Power supply scheme	88
Figure 18.	Current consumption measurement scheme	89
Figure 19.	VREFINT versus temperature	97
Figure 20.	High-speed external clock source AC timing diagram	121
Figure 21.	Low-speed external clock source AC timing diagram	122
Figure 22.	Typical application with an 8 MHz crystal	124
Figure 23.	Typical application with a 32.768 kHz crystal	125
Figure 24.	HSI16 frequency versus temperature	127
Figure 25.	Typical current consumption versus MSI frequency	131
Figure 26.	HSI48 frequency versus temperature	132
Figure 27.	I/O input characteristics	139
Figure 28.	I/O AC characteristics definition ⁽¹⁾	143
Figure 29.	Recommended NRST pin protection	144
Figure 30.	ADC accuracy characteristics	156
Figure 31.	Typical connection diagram using the ADC	157
Figure 32.	12-bit buffered / non-buffered DAC	160
Figure 33.	SPI timing diagram - slave mode and CPHA = 0	175
Figure 34.	SPI timing diagram - slave mode and CPHA = 1	176
Figure 35.	SPI timing diagram - master mode	176
Figure 36.	Quad SPI timing diagram - SDR mode	179
Figure 37.	Quad SPI timing diagram - DDR mode	179
Figure 38.	SAI master timing waveforms	181
Figure 39.	SAI slave timing waveforms	182
Figure 40.	SDIO high-speed mode	183
Figure 41.	SD default mode	184
Figure 42.	LQFP - 100 pins, 14 x 14 mm low-profile quad flat package outline	186
Figure 43.	LQFP - 100 pins, 14 x 14 mm low-profile quad flat recommended footprint	188
Figure 44.	LQFP100 marking (package top view)	189
Figure 45.	UFBGA - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	190
Figure 46.	UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid	

	array package recommended footprint	191
Figure 47.	UFBGA100 marking (package top view)	192
Figure 48.	LQFP - 64 pins, 10 x 10 mm low-profile quad flat package outline.	193
Figure 49.	LQFP - 64 pins, 10 x 10 mm low-profile quad flat package recommended footprint.	194
Figure 50.	LQFP64 marking (package top view)	195
Figure 51.	UFBGA – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline	195
Figure 52.	UFBGA64 – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint	196
Figure 53.	UFBGA64 marking (package top view)	197
Figure 54.	STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package outline	198
Figure 55.	STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package recommended footprint	199
Figure 56.	STANDARD WLCSP64 marking (package top view)	200
Figure 57.	STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package outline	201
Figure 58.	STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package recommended footprint	202
Figure 59.	STANDARD WLCSP49 marking (package top view)	203
Figure 60.	WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale package outline.	204
Figure 61.	THIN WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale recommended footprint.	205
Figure 62.	THIN WLCSP49 marking (package top view).	206
Figure 63.	LQFP - 48 pins, 7 x 7 mm low-profile quad flat package outline.	207
Figure 64.	LQFP - 48 pins, 7 x 7 mm low-profile quad flat package recommended footprint.	209
Figure 65.	LQFP48 marking (package top view)	210
Figure 66.	UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.	211
Figure 67.	UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint	212
Figure 68.	UFQFPN48 marking (package top view)	213
Figure 69.	LQFP64 P _D max vs. T _A	216

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L443xx microcontrollers.

This document should be read in conjunction with the STM32L41x, STM32L42x, STM32L43x, STM32L44x, STM32L45x, STM32L46x reference manual (RM0394). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Arm^{®(a)} Cortex[®]-M4 core, please refer to the Cortex[®]-M4 Technical Reference Manual, available from the www.arm.com website.



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2 Description

The STM32L443xx devices are the ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L443xx devices embed high-speed memories (256 Kbyte of Flash memory, 64 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L443xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, two DAC channels, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces.

- Three I2Cs
- Three SPIs
- Three USARTs and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB full-speed device crystal less
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L443xx devices embed AES hardware accelerator.

The STM32L443xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators, and 3.3 V dedicated supply input for USB. A VBAT input allows to backup the RTC and backup registers.

The STM32L443xx family offers eight packages from 48 to 100-pin packages.

Table 1. STM32L443xx family device features and peripheral counts

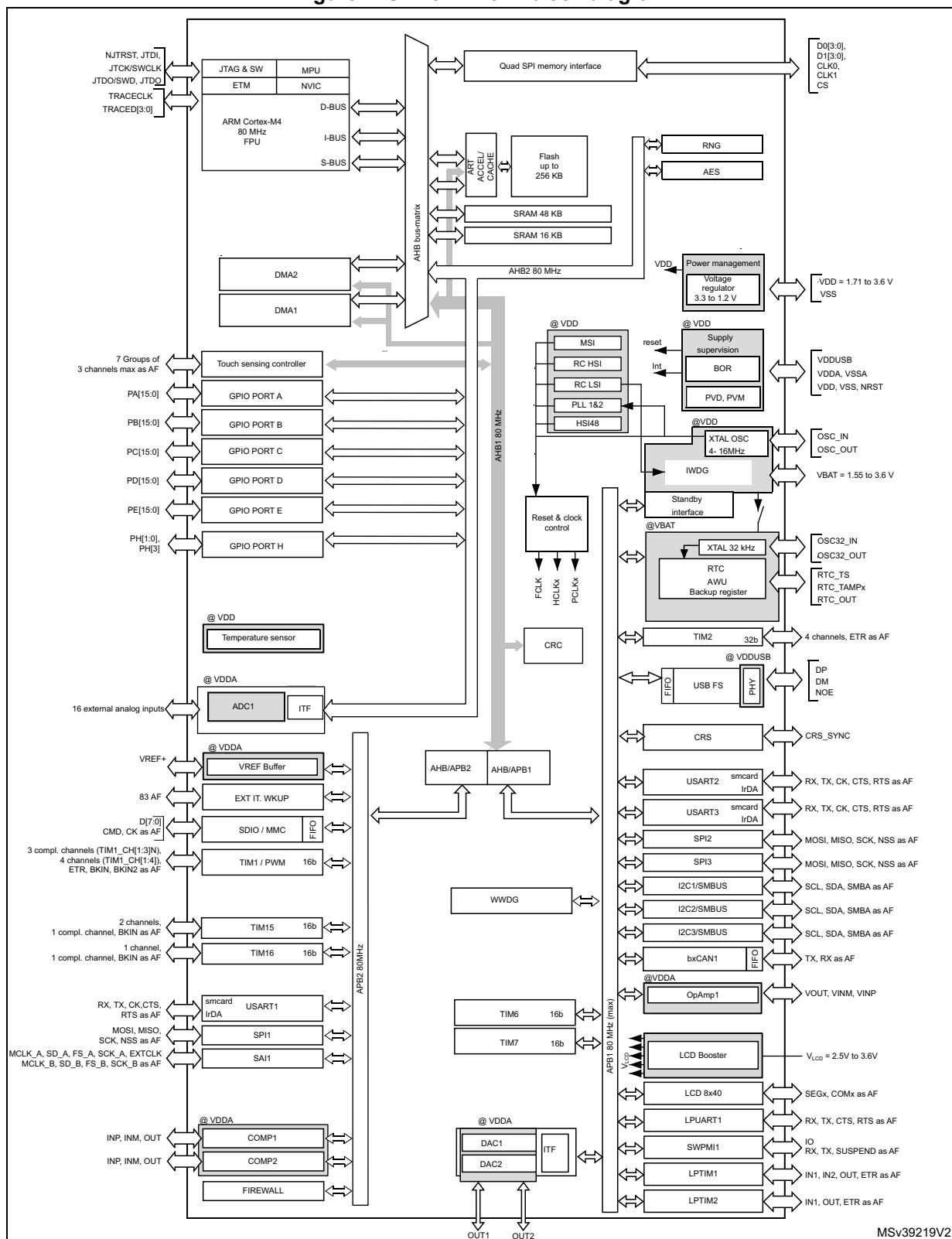
Peripheral		STM32L443Vx	STM32L443Rx	STM32L443Cx
Flash memory		256KB		
SRAM		64KB		
Quad SPI		Yes		
Timers	Advanced control	1 (16-bit)		
	General purpose	2 (16-bit) 1 (32-bit)		
	Basic	2 (16-bit)		
	Low -power	2 (16-bit)		
	SysTick timer	1		
	Watchdog timers (independent, window)	2		
Comm. interfaces	SPI	3		
	I ² C	3		
	USART	3		
	LPUART	1		
	SAI	1		
	CAN	1		
	USB FS	Yes		
	SDMMC	Yes	No	
SWPMI	Yes			
RTC		Yes		
Tamper pins		3	2	2
LCD COM x SEG		Yes 8x40 or 4x44	Yes 8x28 or 4x32	Yes 4x19
Random generator		Yes		
AES		Yes		
GPIOs		83	52	38 or 39 ⁽¹⁾
Wakeup pins		5	4	3
Capacitive sensing Number of channels		21	12	6
12-bit ADC Number of channels		1 16	1 16	1 10
12-bit DAC channels		2		
Internal voltage reference buffer		Yes	No	
Analog comparator		2		
Operational amplifiers		1		

Table 1. STM32L443xx family device features and peripheral counts (continued)

Peripheral	STM32L443Vx	STM32L443Rx	STM32L443Cx
Max. CPU frequency	80 MHz		
Operating voltage	1.71 to 3.6 V		
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	WLCSP49 LQFP48 UFQFPN48

1. For WLCSP49 package.

Figure 1. STM32L443xx block diagram



Note: *AF: alternate function on I/O pins.*

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L443xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L443xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L443xx devices feature 256 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 128 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 2. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽¹⁾	No	No	N/A ⁽¹⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes ⁽¹⁾	No	No	No ⁽¹⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L443xx devices feature 64 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 48 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 16 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

This memory is also mapped at address 0x2000 C000, offering a contiguous address space with the SRAM1 (16 Kbyte aliased by bit band)

This block is accessed through the ICode/DCode buses for maximum performance. These 16 Kbyte SRAM can also be retained in Standby mode.

The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
 - Code segment (located in Flash or SRAM1 if defined as executable protected area)
 - Non-volatile data segment (located in Flash)
 - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
 - Code segment: up to 1024 Kbyte with granularity of 256 bytes
 - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
 - Volatile data segment: up to 48 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB FS in Device mode through DFU (device firmware upgrade).

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

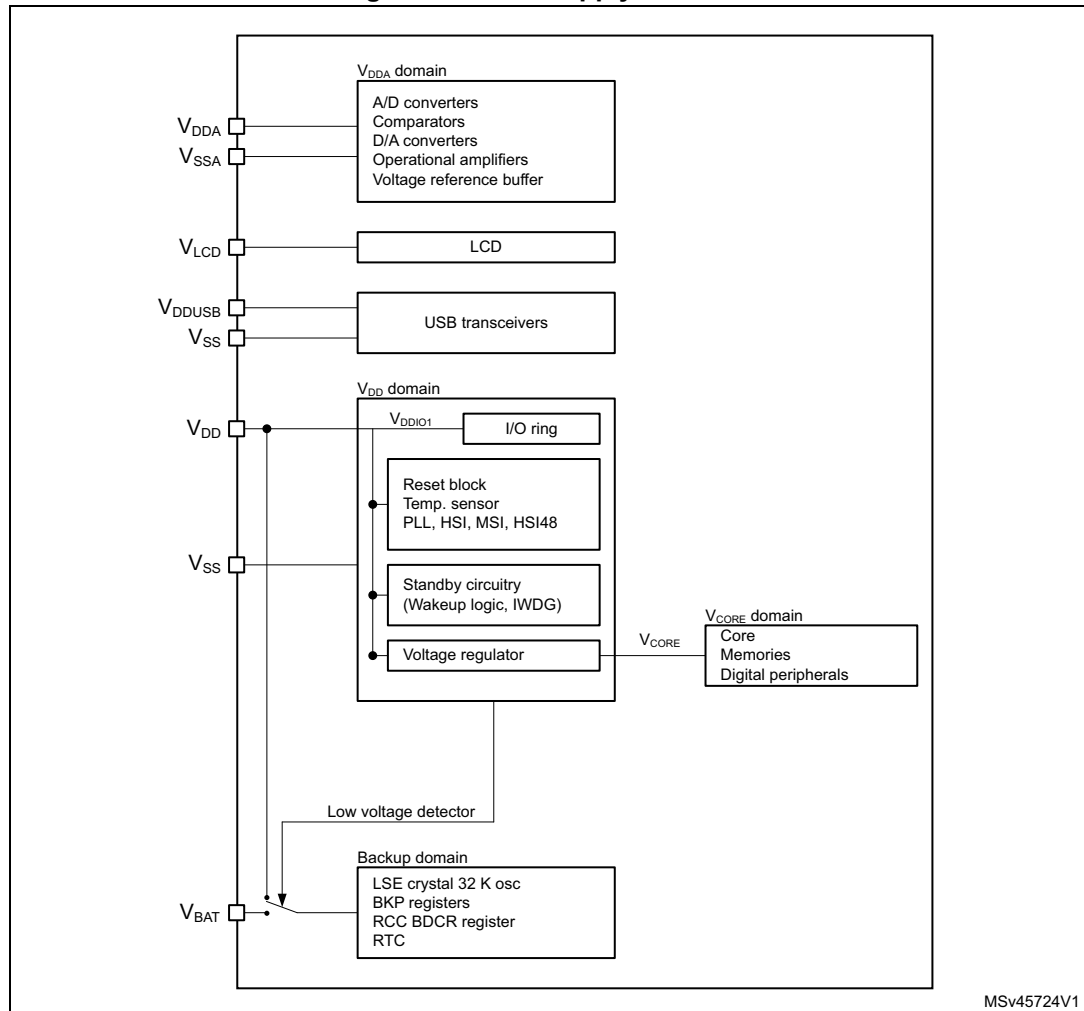
- $V_{DD} = 1.71$ to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- $V_{DDA} = 1.62$ V (ADCs/COMP) / 1.8 (DAC/OPAMP) to 3.6 V: external analog power supply for ADCs, DAC, OPAMPs, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- $V_{DDUSB} = 3.0$ to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- $V_{LCD} = 2.5$ to 3.6 V: the LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
- $V_{BAT} = 1.55$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} or V_{DDUSB} are not used, these supplies should preferably be shorted to V_{DD} .

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to [Table 18: Voltage characteristics](#)).

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1} , with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview

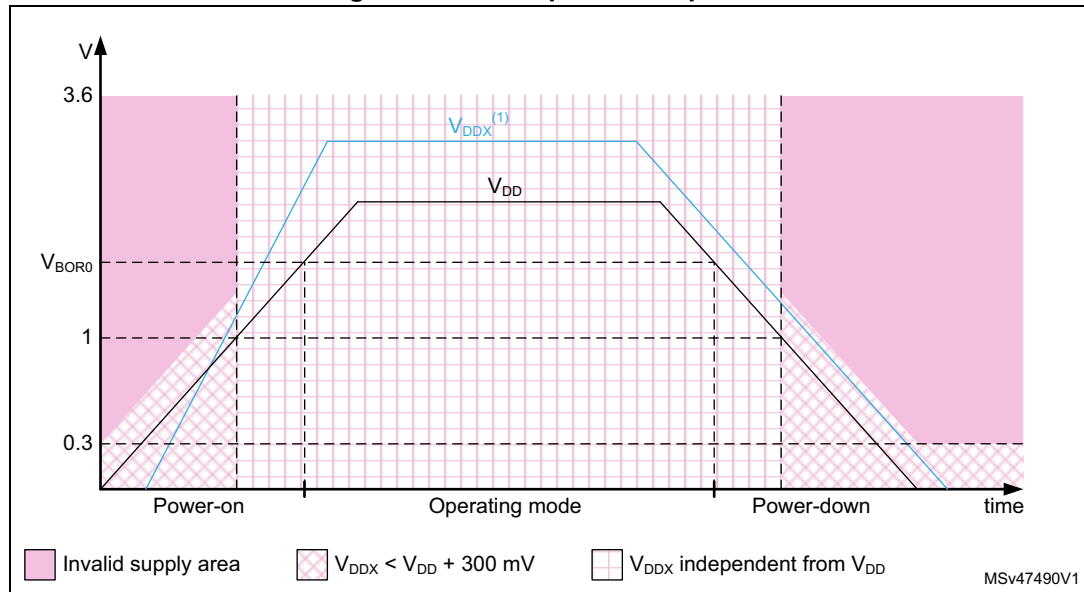


During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA} , V_{DDUSB} , V_{LCD}) must remain below $V_{DD} + 300$ mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 3. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA} , V_{DDUSB} , V_{LCD} .

3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes. The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA} , V_{DDUSB} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 16 Kbyte SRAM2 in Standby with SRAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L443xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The V_{CORE} can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L443xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

Table 3. STM32L443xx modes overview

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source
Run	MR range 1	Yes	ON ⁽⁴⁾	ON	Any	All	N/A
	MR range2					All except USB_FS, RNG	
LPRun	LPR	Yes	ON ⁽⁴⁾	ON	Any except PLL	All except USB_FS, RNG	N/A
Sleep	MR range 1	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any	All	Any interrupt or event
	MR range2					All except USB_FS, RNG	
LPSleep	LPR	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any except PLL	All except USB_FS, RNG	Any interrupt or event
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) USARTx (x=1...3) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) USB_FS ⁽⁸⁾ SWPMI1 ⁽⁹⁾
	MR Range 2						



Table 3. STM32L443xx modes overview (continued)

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) USARTx (x=1...3) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) USB_FS ⁽⁸⁾ SWPMI1 ⁽⁹⁾
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1

Table 3. STM32L443xx modes overview (continued)

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source
Standby	LPR	Power ed Off	Off	SRAM 2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx) ⁽¹⁰⁾ BOR, RTC, IWDG
	OFF			Power ed Off			
Shutdown	OFF	Power ed Off	Off	Power ed Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull- down ⁽¹¹⁾	Reset pin 5 I/Os (WKUPx) ⁽¹⁰⁾ RTC

1. LPR means Main regulator is OFF and Low-power regulator is ON.

2. All peripherals can be active or clock gated to save power consumption.

3. Typical current at $V_{DD} = 1.8\text{ V}$, 25°C . Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 2, LPRun/LPSleep.

4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.

5. The SRAM1 and SRAM2 clocks can be gated on or off independently.

6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received

7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.

8. USB_FS wakeup by resume from suspend and attach detection protocol event.

9. SWPMI1 wakeup by resume from suspend.

10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.

11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the SH

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run mode**

This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep mode**

This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2 modes**

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the V_{CORE} domain is put in a lower leakage mode.

Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

The brown-out reset (BOR) always remains active in Standby mode.

The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in Standby mode, supplied by the low-power Regulator (Standby with SRAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown mode**

The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

The system clock after wakeup is MSI at 4 MHz.

Table 4. Functionalities depending on the working mode⁽¹⁾

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (256 KB)	O ⁽²⁾	O ⁽²⁾	O ⁽²⁾	O ⁽²⁾	-	-	-	-	-	-	-	-	-
SRAM1 (48 KB)	Y	Y ⁽³⁾	Y	Y ⁽³⁾	Y	-	Y	-	-	-	-	-	-
SRAM2 (16 KB)	Y	Y ⁽³⁾	Y	Y ⁽³⁾	Y	-	Y	-	O ⁽⁴⁾	-	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator RC48	O	O	-	-	-	-	-	-	-	-	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed Internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
LCD	O	O	O	O	O	O	O	O	-	-	-	-	-

Table 4. Functionalities depending on the working mode⁽¹⁾ (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
USB FS	O ⁽⁸⁾	O ⁽⁸⁾	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3)	O	O	O	O	O ⁽⁶⁾	O ⁽⁶⁾	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O ⁽⁶⁾	O ⁽⁶⁾	O ⁽⁶⁾	O ⁽⁶⁾	-	-	-	-	-
I2Cx (x=1,2)	O	O	O	O	O ⁽⁷⁾	O ⁽⁷⁾	-	-	-	-	-	-	-
I2C3	O	O	O	O	O ⁽⁷⁾	O ⁽⁷⁾	O ⁽⁷⁾	O ⁽⁷⁾	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SWPMI1	O	O	O	O	-	O	-	-	-	-	-	-	-
SAIx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O ⁽⁸⁾	O ⁽⁸⁾	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-

Table 4. Functionalities depending on the working mode⁽¹⁾ (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9) 5 pins (10)	(11) 5 pins (10)	-	-	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.10 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 5. STM32L443xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DAC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
TIM15/TIM16	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y ⁽¹⁾	-
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y ⁽¹⁾	-
All clocks sources (internal and external)	TIM2 TIM15, 16	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM15,16	Timer break	Y	Y	Y	Y	-	-

Table 5. STM32L443xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y ⁽¹⁾
	ADCx DAC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.11 Clocks and startup

The clock controller (see [Figure 4](#)) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

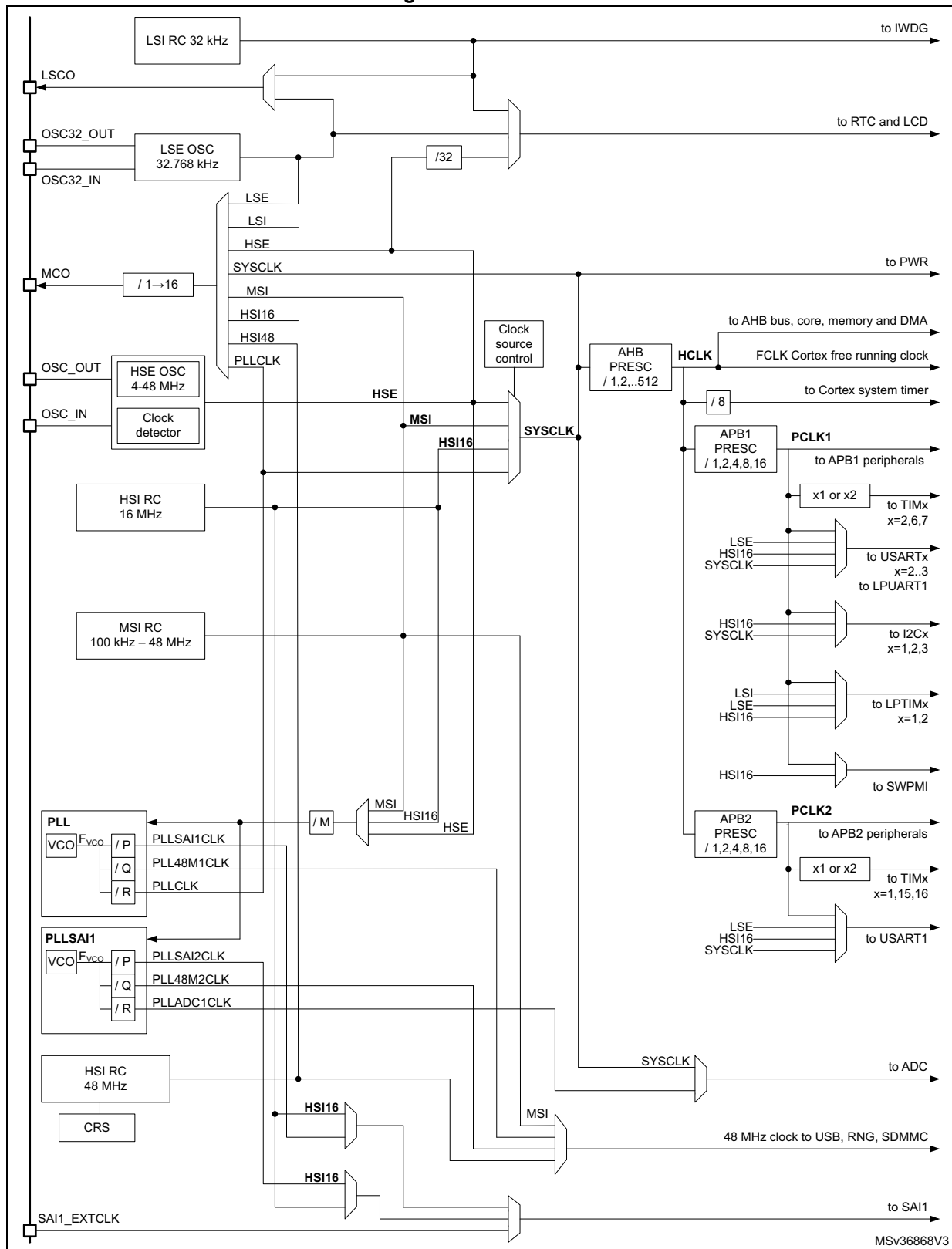
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
 - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
 - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than $\pm 0.25\%$ accuracy. In this mode the MSI can feed the USB device. The MSI can supply a PLL.
 - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **RC48 with clock recovery system (HSI48):** internal RC48 MHz clock source can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
 - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is $\pm 5\%$ accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Two PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
 - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
 - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

Figure 4. Clock tree



3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to [Table 6: DMA implementation](#) for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 6. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 67 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 37 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

3.15 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
 - Down to 18.75 ns sampling time
 - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1_OUT1 and DAC1_OUT2.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
 - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
 - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
 - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
 - ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
 - Results stored into data register or in RAM with DMA controller support
 - Data pre-processing: left/right alignment and per channel offset compensation
 - Built-in oversampling unit for enhanced SNR
 - Channel-wise programmable sampling time
 - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
 - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.15.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC1_IN0 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.16 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L443xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DAC and also as voltage reference for external components through the VREF+ pin.

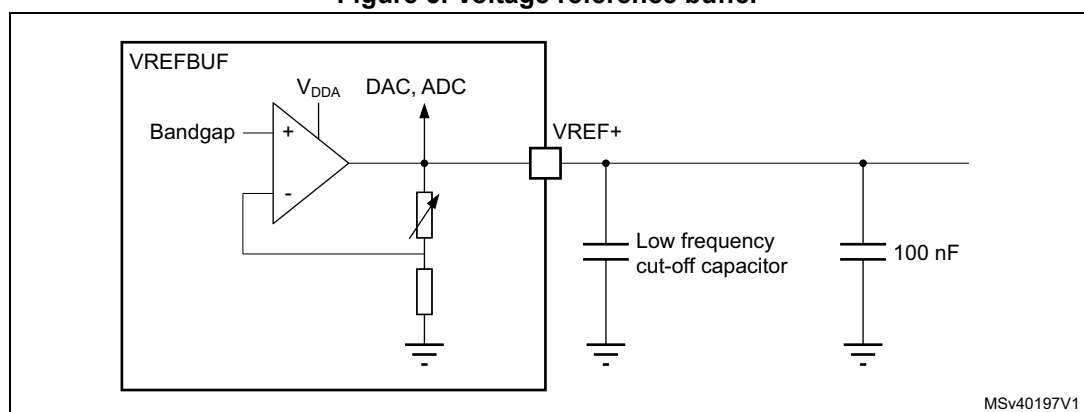
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 5. Voltage reference buffer



3.18 Comparators (COMP)

The STM32L443xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.19 Operational amplifier (OPAMP)

The STM32L443xx embeds one operational amplifier with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 21 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.21 Liquid crystal display controller (LCD)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD} . This converter can be deactivated, in which case the VLCD pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Integrated voltage output buffers for higher LCD driving capability
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.22 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.23 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator can be used to both encipher and

decipher data using AES algorithm.

The AES peripheral supports:

- Encryption/Decryption using AES Rijndael Block Cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported.
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer.
- Register access supporting 32-bit data width only.
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode.
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outgoing data.
- Suspend a message if another message with a higher priority needs to be processed

3.24 Timers and watchdogs

The STM32L443xx includes one advanced control timers, up to five general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 9. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1

Table 9. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
General-purpose	TIM16	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.24.1 Advanced-control timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in [Section 3.24.2](#)) using the same architecture, so the advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.24.2 General-purpose timers (TIM2, TIM15, TIM16)

There are up to three synchronizable general-purpose timers embedded in the STM32L443xx (see [Table 9](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2

It is a full-featured general-purpose timer:

TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler.

This timer features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. It can work with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

It has independent DMA request generation and support quadrature encoder.

- TIM15 and 16

They are general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel

- TIM16 has 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

3.24.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.24.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
 - Internal clock sources: LSE, LSI, HSI16 or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.24.5 Infrared interface (IRTIM)

The STM32L443xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM15 and TIM16 output channels to generate output signal waveforms on IR_OUT pin.

3.24.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.24.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.24.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.25 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.26 Inter-integrated circuit interface (I²C)

The device embeds three I2C. Refer to [Table 10: I2C implementation](#) for the features implementation.

The I²C bus interface handles communications between the microcontroller and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
 - Slave and master modes, multimaster capability
 - Standard-mode (Sm), with a bitrate up to 100 kbit/s
 - Fast-mode (Fm), with a bitrate up to 400 kbit/s
 - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
 - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
 - Programmable setup and hold times
 - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
 - Hardware PEC (Packet Error Checking) generation and verification with ACK control
 - Address resolution protocol (ARP) support
 - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to [Figure 4: Clock tree](#).
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 10. I2C implementation

I2C features ⁽¹⁾	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

1. X: supported

3.27 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L443xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3) to wake up the MCU from Stop mode using baudrates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 11. STM32L443xx USART/LPUART features

USART modes/features ⁽¹⁾	USART1	USART2	USART3	LPUART1
Hardware flow control for modem	X	X	X	X
Continuous communication using DMA	X	X	X	X
Multiprocessor communication	X	X	X	X
Synchronous mode	X	X	X	-
Smartcard mode	X	X	X	-
Single-wire half-duplex communication	X	X	X	X
IrDA SIR ENDEC block	X	X	X	-
LIN mode	X	X	X	-
Dual clock domain	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	X
Receiver timeout interrupt	X	X	X	-
Modbus communication	X	X	X	-
Auto baud rate detection	X (4 modes)			-
Driver Enable	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits			

1. X = supported.

3.28 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.29 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.30 Serial audio interfaces (SAI)

The device embeds 1 SAI. Refer to [Table 12: SAI implementation](#) for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
 - Overrun and underrun detection.
 - Anticipated frame synchronization signal detection in slave mode.
 - Late frame synchronization signal detection in slave mode.
 - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
 - Errors.
 - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 12. SAI implementation

SAI features	Support ⁽¹⁾
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/Mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO Size	X (8 Word)
SPDIF	X

1. X: supported

3.31 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.32 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s
- Transmission
 - Three transmit mailboxes
 - Configurable transmit priority
- Reception
 - Two receive FIFOs with three stages
 - 14 Scalable filter banks
 - Identifier list feature
 - Configurable FIFO overrun
- Time-triggered communication option
 - Disable automatic retransmission mode
 - 16-bit free running timer
 - Time Stamp sent in last two data bytes
- Management
 - Maskable interrupts
 - Software-efficient mailbox mapping at a unique address space

3.33 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.34 Universal serial bus (USB)

The STM32L443xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in

automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.35 Clock recovery system (CRS)

The STM32L443xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.36 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

The Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- Dual-flash mode, where 8 bits can be sent/received simultaneously by accessing two flash memories in parallel.
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
 - Instruction phase
 - Address phase
 - Alternate bytes phase
 - Dummy cycles phase
 - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.37 Development support

3.37.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

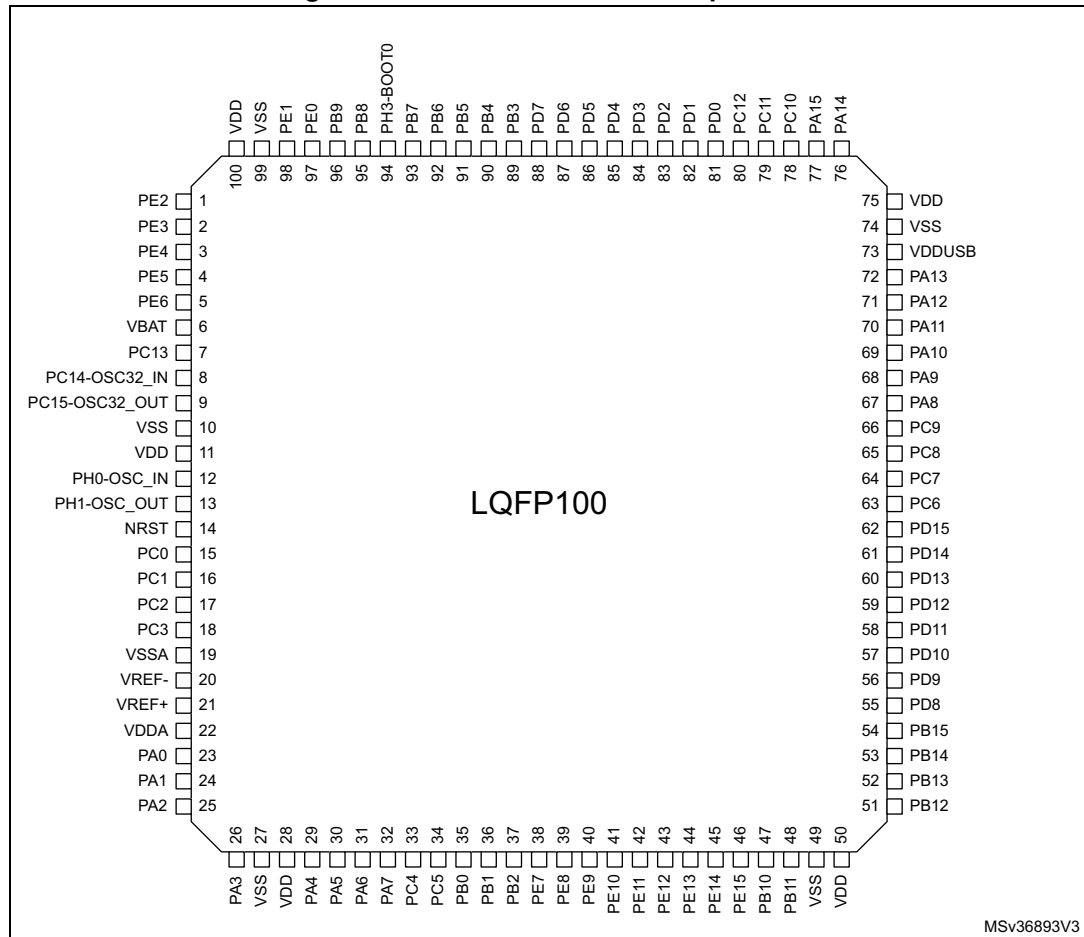
3.37.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell™ provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L443xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell™ operates with third party debugger software tools.

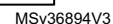
4 Pinouts and pin description

Figure 6. STM32L443Vx LQFP100 pinout⁽¹⁾



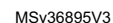
1. The above figure shows the package top view.

Figure 7. STM32L443Vx UFBGA100 ballout⁽¹⁾



1. The above figure shows the package top view.

Figure 8. STM32L443Rx LQFP64 pinout⁽¹⁾



1. The above figure shows the package top view.

Figure 9. STM32L443Rx UFBGA64 ballout⁽¹⁾

	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN	PC13	PB9	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PB8	PH3-BOOT0	PD2	PC11	PC10	PA12
C	PH0-OSC_IN	VSS	PB7	PB5	PC12	PA10	PA9	PA11
D	PH1-OSC_OUT	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	NRST	PC1	PC0	VDD	VDDUSB	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

MSv36896V3

1. The above figure shows the package top view.

Figure 10. STM32L443Rx WLCSP64 pinout⁽¹⁾

	1	2	3	4	5	6	7	8
A	VDDUSB	PA15	PC12	PD2	PB3	PB7	VSS	VDD
B	VSS	PA14	PC11	PB4	PB6	PB9	VBAT	PC13
C	PA12	PA13	PC10	PB5	PH3-BOOT0	PB8	PC15-OSC32_OUT	PC14-OSC32_IN
D	PA9	PA10	PA11	PC4	PC0	NRST	PH1-OSC_OUT	PH0-OSC_IN
E	PC7	PC9	PA8	PC5	PA4	PC3	PC2	PC1
F	PC6	PB15	PC8	PB0	PA5	PA2	PA0	VSSA/VREF-
G	PB14	PB13	PB12	PB2	PA6	PA3	PA1	VDDA/VREF+
H	VDD	VSS	PB11	PB10	PB1	PA7	VDD	VSS

MSv38084V3

1. The above figure shows the package top view.

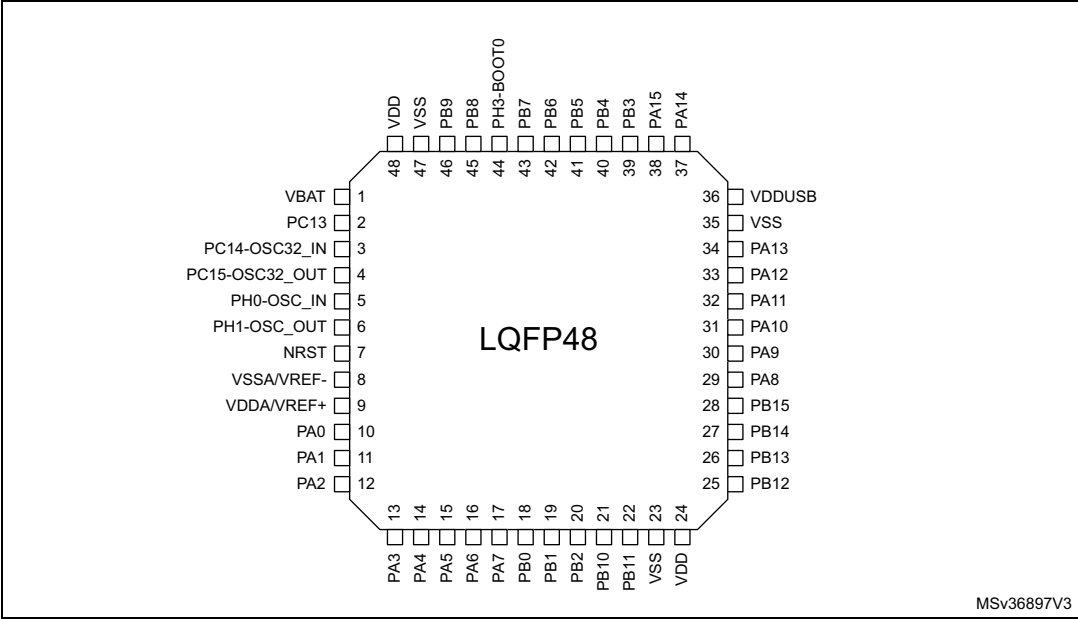
Figure 11. STM32L443Cx WLCSP49 pinout⁽¹⁾

	1	2	3	4	5	6	7
A	VDDUSB	PA14	PB3	PB4	PH3-BOOT0	VSS	VDD
B	VSS	PA13	PA15	PB5	PB8	VBAT	PC13
C	PA11	PA10	PA12	PB6	PB9	PC15-OSC32_OUT	PC14-OSC32_IN
D	PA8	PA9	PB15	PB7	NRST	PH1-OSC_OUT	PH0-OSC_IN
E	PB14	PB13	PB10	PA3	PA2	PC3	VSSA/VREF-
F	PB12	PB11	PA7	PA6	PA5	PA0	VDDA/VREF+
G	VDD	VSS	PB2	PB1	PB0	PA4	PA1

MSv38085V3

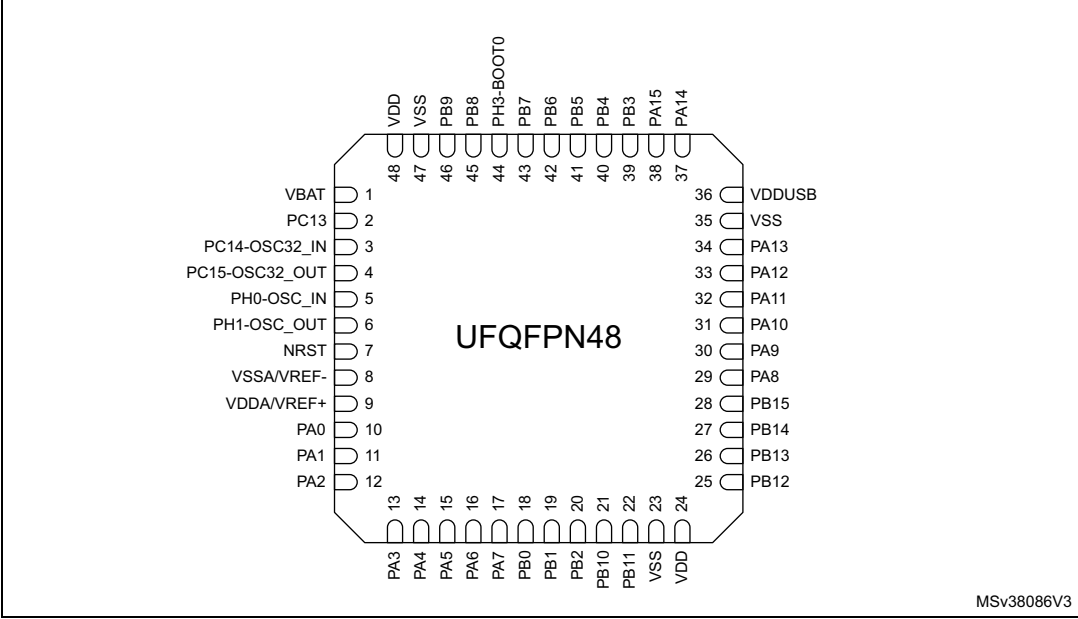
1. The above figure shows the package top view.

Figure 12. STM32L443Cx LQFP48 pinout⁽¹⁾



1. The above figure shows the package top view.

Figure 13. STM32L443Cx UFQFPN48 pinout⁽¹⁾



1. The above figure shows the package top view.

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f ⁽¹⁾	I/O, Fm+ capable
		_l ⁽²⁾	I/O, with LCD function supplied by V _{LCD}
		_u ⁽³⁾	I/O, with USB function supplied by V _{DDUSB}
		_a ⁽⁴⁾	I/O, with Analog switch function supplied by V _{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in [Table 14](#) are: FT_f, FT_fa, FT_fl, FT_fla.

2. The related I/O structures in [Table 14](#) are: FT_l, FT_fl, FT_lu.

3. The related I/O structures in [Table 14](#) are: FT_u, FT_lu.

4. The related I/O structures in [Table 14](#) are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.

Table 14. STM32L443xx pin definitions

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	1	B2	PE2	I/O	FT_l	-	TRACECK, TSC_G7_IO1, LCD_SEG38, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	2	A1	PE3	I/O	FT_l	-	TRACED0, TSC_G7_IO2, LCD_SEG39, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TRACED1, TSC_G7_IO3, SAI1_FS_A, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WL CSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TRACED2, TSC_G7_IO4, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TRACED3, SAI1_SD_A, EVENTOUT	RTC_TAMP3/ WKUP3
1	1	B6	B7	1	B2	6	E2	VBAT	S	-	-	-	-
2	2	B7	B8	2	A2	7	C1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
3	3	C7	C8	3	A1	8	D1	PC14- OSC32_I N (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	4	C6	C7	4	B1	9	E1	PC15- OSC32_ OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	10	F2	VSS	S	-	-	-	-
-	-	-	-	-	-	11	G2	VDD	S	-	-	-	-
5	5	D7	D8	5	C1	12	F1	PH0- OSC_ IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	D6	D7	6	D1	13	G1	PH1- OSC_OU T (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	7	D5	D6	7	E1	14	H2	NRST	I/O	RST	-	-	-
-	-	-	D5	8	E3	15	H1	PC0	I/O	FT fla	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, EVENTOUT	ADC1_IN1
-	-	-	E8	9	E2	16	J2	PC1	I/O	FT fla	-	LPTIM1_OUT, I2C3_SDA, LPUART1_TX, LCD_SEG19, EVENTOUT	ADC1_IN2
-	-	-	E7	10	F2	17	J3	PC2	I/O	FT la	-	LPTIM1_IN2, SPI2_MISO, LCD_SEG20, EVENTOUT	ADC1_IN3
-	-	E6	E6	11	G1	18	K2	PC3	I/O	FT a	-	LPTIM1_ETR, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	-	-	-	19	J1	VSSA	S	-	-	-	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	20	K1	VREF-	S	-	-	-	-
8	8	E7	F8	12	F1	-	-	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	-	22	M1	VDDA	S	-	-	-	-
9	9	F7	G8	13	H1	-	-	VDDA/ VREF+	S	-	-	-	-
10	10	F6	F7	14	G2	23	L2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM, ADC1_IN5, RTC_TAMP2/ WKUP1
11	11	G7	G7	15	H2	24	M2	PA1	I/O	FT_la	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP, ADC1_IN6
12	12	E5	F6	16	F3	25	K3	PA2	I/O	FT_la	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG1, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4/LSCO
13	13	E4	G6	17	G3	26	L3	PA3	I/O	TT_la	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, LCD_SEG2, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	-	H8	18	C2	27	E3	VSS	S	-	-	-	-
-	-	-	H7	19	D2	28	H3	VDD	S	-	-	-	-
14	14	G6	E5	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
15	15	F5	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10, DAC1_OUT2

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
16	16	F4	G5	22	G4	31	L4	PA6	I/O	FT_la	-	TIM1_BKIN, SPI1_MISO, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, COMP1_OUT/TIM1_BKIN _COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
17	17	F3	H6	23	H4	32	M4	PA7	I/O	FT fla	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, COMP2_OUT, EVENTOUT	ADC1_IN12
-	-	-	D4	24	H5	33	K5	PC4	I/O	FT_la	-	USART3_TX, LCD_SEG22, EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	E4	25	H6	34	L5	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
18	18	G5	F4	26	F5	35	M5	PB0	I/O	FT_la	-	TIM1_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
19	19	G4	H5	27	G5	36	M6	PB1	I/O	FT_la	-	TIM1_CH3N, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
20	20	G3	G4	28	G6	37	L6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, LCD_VLCD, EVENTOUT	COMP1_INP
-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, SAI1_FS_B, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WL CSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, EVENTOUT	-
21	21	E3	H4	29	G7	47	L10	PB10	I/O	FT_fl	-	TIM2_CH3, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
22	22	F2	H3	30	H7	48	L11	PB11	I/O	FT_fl	-	TIM2_CH4, I2C2_SDA, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
23	23	G2	H2	31	D6	49	F12	VSS	S	-	-	-	-
24	24	G1	H1	32	E6	50	G12	VDD	S	-	-	-	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WL CSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
25	25	F1	G3	33	H8	51	L12	PB12	I/O	FT_I	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
26	26	E2	G2	34	G8	52	K12	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SWPMI1_TX, SAI1_SCK_A, TIM15_CH1N, EVENTOUT	-
27	27	E1	G1	35	F8	53	K11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C2_SDA, SPI2_MISO, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI1_MCLK_A, TIM15_CH1, EVENTOUT	-
28	28	D3	F2	36	F7	54	K10	PB15	I/O	FT_I	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI1_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	55	K9	PD8	I/O	FT_I	-	USART3_TX, LCD_SEG28, EVENTOUT	-
-	-	-	-	-	-	56	K8	PD9	I/O	FT_I	-	USART3_RX, LCD_SEG29, EVENTOUT	-
-	-	-	-	-	-	57	J12	PD10	I/O	FT_I	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WL CSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	58	J11	PD11	I/O	FT_I	-	USART3_CTS, TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	-	-	59	J10	PD12	I/O	FT_I	-	USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	-	-	60	H12	PD13	I/O	FT_I	-	TSC_G6_IO4, LCD_SEG33, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	61	H11	PD14	I/O	FT_I	-	LCD_SEG34, EVENTOUT	-
-	-	-	-	-	-	62	H10	PD15	I/O	FT_I	-	LCD_SEG35, EVENTOUT	-
-	-	-	F1	37	F6	63	E12	PC6	I/O	FT_I	-	TSC_G4_IO1, LCD_SEG24, SDMMC1_D6, EVENTOUT	-
-	-	-	E1	38	E7	64	E11	PC7	I/O	FT_I	-	TSC_G4_IO2, LCD_SEG25, SDMMC1_D7, EVENTOUT	-
-	-	-	F3	39	E8	65	E10	PC8	I/O	FT_I	-	TSC_G4_IO3, LCD_SEG26, SDMMC1_D0, EVENTOUT	-
-	-	-	E2	40	D8	66	D12	PC9	I/O	FT_I	-	TSC_G4_IO4, USB_NOE, LCD_SEG27, SDMMC1_D1, EVENTOUT	-
29	29	D1	E3	41	D7	67	D11	PA8	I/O	FT_I	-	MCO, TIM1_CH1, USART1_CK, LCD_COM0, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	30	D2	D1	42	C7	68	D10	PA9	I/O	FT_fl	-	TIM1_CH2, I2C1_SCL, USART1_TX, LCD_COM1, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
31	31	C2	D2	43	C6	69	C12	PA10	I/O	FT_fl	-	TIM1_CH3, I2C1_SDA, USART1_RX, USB_CRD_SYNC, LCD_COM2, SAI1_SD_A, EVENTOUT	-
32	32	C1	D3	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, CAN1_RX, USB_DM, TIM1_BKIN2_COMP1, EVENTOUT	COMP1_OUT
33	33	C3	C1	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, USB_DP, EVENTOUT	-
34	34	B2	C2	46	A8	72	A11	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, USB_NOE, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-
35	35	B1	B1	47	D5	-	-	VSS	S	-	-	-	-
36	36	A1	A1	48	E5	73	C11	VDD USB	S	-	-	-	-
-	-	-	-	-	-	74	F11	VSS	S	-	-	-	-
-	-	-	-	-	-	75	G11	VDD	S	-	-	-	-
37	37	A2	B2	49	A7	76	A10	PA14 (JTCK-SWCLK)	I/O	FT	(3)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SWPMI1_RX, SAI1_FS_B, EVENTOUT	-
38	38	B3	A2	50	A6	77	A9	PA15 (JTDI)	I/O	FT_I	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, TSC_G3_IO1, LCD_SEG17, SWPMI1_SUSPEND, EVENTOUT	-
-	-	-	C3	51	B7	78	B11	PC10	I/O	FT_I	-	SPI3_SCK, USART3_TX, TSC_G3_IO2, LCD_COM4/LCD_SEG28/ LCD_SEG40, SDMMC1_D2, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	B3	52	B6	79	C10	PC11	I/O	FT_I	-	SPI3_MISO, USART3_RX, TSC_G3_IO3, LCD_COM5/LCD_SEG29/ LCD_SEG41, SDMMC1_D3, EVENTOUT	-
-	-	-	A3	53	C5	80	B10	PC12	I/O	FT_I	-	SPI3_MOSI, USART3_CK, TSC_G3_IO4, LCD_COM6/LCD_SEG30/ LCD_SEG42, SDMMC1_CK, EVENTOUT	-
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	SPI2_NSS, CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK, CAN1_TX, EVENTOUT	-
-	-	-	A4	54	B5	83	C8	PD2	I/O	FT_I	-	USART3_RTS_DE, TSC_SYNC, LCD_COM7/LCD_SEG31/ LCD_SEG43, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	SPI2_MISO, USART2_CTS, QUADSPI_BK2_NCS, EVENTOUT	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	SPI2_MOSI, USART2_RTS_DE, QUADSPI_BK2_IO0, EVENTOUT	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, EVENTOUT	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX, QUADSPI_BK2_IO2, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, QUADSPI_BK2_IO3, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
39	39	A3	A5	55	A5	89	A8	PB3 (JTDO- TRACE SWO)	I/O	FT_la	(3)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, EVENTOUT	COMP2_INM
40	40	A4	B4	56	A4	90	A7	PB4 (NJTRST)	I/O	FT fla	(3)	NJTRST, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, EVENTOUT	COMP2_INP
41	41	B4	C4	57	C4	91	C5	PB5	I/O	FT_I	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
42	42	C4	B5	58	D3	92	B5	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP
43	43	D4	A6	59	C3	93	B4	PB7	I/O	FT fla	-	LPTIM1_IN2, I2C1_SDA, USART1_RX, TSC_G2_IO4, LCD_SEG21, EVENTOUT	COMP2_INM, PVD_IN
44	44	A5	C5	60	B4	94	A4	PH3/ BOOT0	I/O	FT	-	EVENTOUT	BOOT0
45	45	B5	C6	61	B3	95	A3	PB8	I/O	FT fl	-	I2C1_SCL, CAN1_RX, LCD_SEG16, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
46	46	C5	B6	62	A3	96	B3	PB9	I/O	FT fl	-	IR_OUT, I2C1_SDA, SPI2_NSS, CAN1_TX, LCD_COM3, SDMMC1_D5, SAI1_FS_A, EVENTOUT	-

Table 14. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	97	C3	PE0	I/O	FT_I	-	LCD_SEG36, TIM16_CH1, EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT_I	-	LCD_SEG37, EVENTOUT	-
47	47	A6	A7	63	D4	99	D3	VSS	S	-	-	-	-
48	48	A7	A8	64	E4	100	C4	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0394 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 15. Alternate function AF0 to AF7⁽¹⁾

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2
Port A	PA0	-	TIM2_CH1	-	-	-	-
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK
	PA2	-	TIM2_CH3	-	-	-	-
	PA3	-	TIM2_CH4	-	-	-	-
	PA4	-	-	-	-	-	SPI1_NSS
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK
	PA6	-	TIM1_BKIN	-	-	-	SPI1_MISO
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI
	PA8	MCO	TIM1_CH1	-	-	-	-
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2
Port B	PB0	-	TIM1_CH2N	-	-	-	SPI1_NSS
	PB1	-	TIM1_CH3N	-	-	-	-
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-
	PB3	JTDO- TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO
Port B	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	-
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	-
	PB8	-	-	-	-	I2C1_SCL	-
	PB9	-	IR_OUT	-	-	I2C1_SDA	SPI2_NSS
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK
	PB14	-	TIM1_CH2N	-	-	I2C2_SDA	SPI2_MISO
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-
	PC1	-	LPTIM1_OUT	-	-	I2C3_SDA	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI
	PC4	-	-	-	-	-	-
	PC5	-	-	-	-	-	-
	PC6	-	-	-	-	-	-
	PC7	-	-	-	-	-	-
	PC8	-	-	-	-	-	-
	PC9	-	-	-	-	-	-
	PC10	-	-	-	-	-	-
Port C	PC11	-	-	-	-	-	-
	PC12	-	-	-	-	-	-
	PC13	-	-	-	-	-	-
	PC14	-	-	-	-	-	-
	PC15	-	-	-	-	-	-

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2
Port D	PD0	-	-	-	-	-	SPI2_NSS
	PD1	-	-	-	-	-	SPI2_SCK
	PD2	-	-	-	-	-	-
	PD3	-	-	-	-	-	SPI2_MISO
	PD4	-	-	-	-	-	SPI2_MOSI
	PD5	-	-	-	-	-	-
	PD6	-	-	-	-	-	-
	PD7	-	-	-	-	-	-
	PD8	-	-	-	-	-	-
	PD9	-	-	-	-	-	-
	PD10	-	-	-	-	-	-
	PD11	-	-	-	-	-	-
	PD12	-	-	-	-	-	-
	PD13	-	-	-	-	-	-
	PD14	-	-	-	-	-	-
	PD15	-	-	-	-	-	-
Port E	PE0	-	-	-	-	-	-

Table 15. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2
Port E	PE1	-	-	-	-	-	-
	PE2	TRACECK	-	-	-	-	-
	PE3	TRACED0	-	-	-	-	-
	PE4	TRACED1	-	-	-	-	-
	PE5	TRACED2	-	-	-	-	-
	PE6	TRACED3	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-
	PE9	-	TIM1_CH1	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI
Port H	PH0	-	-	-	-	-	-
	PH1	-	-	-	-	-	-
	PH3	-	-	-	-	-	-

1. Please refer to [Table 16](#) for AF8 to AF15.

Table 16. Alternate function AF8 to AF15⁽¹⁾

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port A	PA0	-	-	-	-	COMP1_OUT	SAI1_EXTCLK
	PA1	-	-	-	LCD_SEG0	-	-
	PA2	LPUART1_TX	-	QUADSPI_ BK1_NCS	LCD_SEG1	COMP2_OUT	-
	PA3	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A
	PA4	-	-	-	-	-	SAI1_FS_B
	PA5	-	-	-	-	-	-
	PA6	LPUART1_CTS	-	QUADSPI_ BK1_IO3	LCD_SEG3	TIM1_BKIN_ COMP2	-
	PA7	-	-	QUADSPI_ BK1_IO2	LCD_SEG4	COMP2_OUT	-
	PA8	-	-	-	LCD_COM0	SWPMI1_IO	SAI1_SCK_A
	PA9	-	-	-	LCD_COM1	-	SAI1_FS_A
	PA10	-	-	USB_CRD_ SYNC	LCD_COM2	-	SAI1_SD_A
	PA11	-	CAN1_RX	USB_DM	-	TIM1_BKIN2_ COMP1	-
	PA12	-	CAN1_TX	USB_DP	-	-	-
	PA13	-	-	USB_NOE	-	SWPMI1_TX	SAI1_SD_B
	PA14	-	-	-	-	SWPMI1_RX	SAI1_FS_B
	PA15	-	TSC_G3_IO1	-	LCD_SEG17	SWPMI1_ SUSPEND	-

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port B	PB0	-	-	QUADSPI_ BK1_IO1	LCD_SEG5	COMP1_OUT	SAI1_EXTCLK
	PB1	LPUART1_RTS _DE	-	QUADSPI_ BK1_IO0	LCD_SEG6	-	-
	PB2	-	-	-	LCD_VLCD	-	-
	PB3	-	-	-	LCD_SEG7	-	SAI1_SCK_B
	PB4	-	TSC_G2_IO1	-	LCD_SEG8	-	SAI1_MCLK_
	PB5	-	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B
	PB6	-	TSC_G2_IO3	-	-	-	SAI1_FS_B
	PB7	-	TSC_G2_IO4	-	LCD_SEG21	-	-
	PB8	-	CAN1_RX	-	LCD_SEG16	SDMMC1_D4	SAI1_MCLK_
	PB9	-	CAN1_TX	-	LCD_COM3	SDMMC1_D5	SAI1_FS_A
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A
	PB11	LPUART1_TX	-	QUADSPI_ BK1_NCS	LCD_SEG11	COMP2_OUT	-
	PB12	LPUART1_RTS _DE	TSC_G1_IO1	-	LCD_SEG12	SWPMI1_IO	SAI1_FS_A
	PB13	LPUART1_CTS	TSC_G1_IO2	-	LCD_SEG13	SWPMI1_TX	SAI1_SCK_A
	PB14	-	TSC_G1_IO3	-	LCD_SEG14	SWPMI1_RX	SAI1_MCLK_
	PB15	-	TSC_G1_IO4	-	LCD_SEG15	SWPMI1_ SUSPEND	SAI1_SD_A


Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port C	PC0	LPUART1_RX	-	-	LCD_SEG18	-	-
	PC1	LPUART1_TX	-	-	LCD_SEG19	-	-
	PC2	-	-	-	LCD_SEG20	-	-
Port C	PC3	-	-	-	LCD_VLCD	-	SAI1_SD_A
	PC4	-	-	-	LCD_SEG22	-	-
	PC5	-	-	-	LCD_SEG23	-	-
	PC6	-	TSC_G4_IO1	-	LCD_SEG24	SDMMC1_D6	-
	PC7	-	TSC_G4_IO2	-	LCD_SEG25	SDMMC1_D7	-
	PC8	-	TSC_G4_IO3	-	LCD_SEG26	SDMMC1_D0	-
	PC9	-	TSC_G4_IO4	USB_NOE	LCD_SEG27	SDMMC1_D1	-
	PC10	-	TSC_G3_IO2	-	LCD_COM4/ LCD_SEG28/ LCD_SEG40	SDMMC1_D2	-
	PC11	-	TSC_G3_IO3	-	LCD_COM5/ LCD_SEG29/ LCD_SEG41	SDMMC1_D3	-
	PC12	-	TSC_G3_IO4	-	LCD_COM6/ LCD_SEG30/ LCD_SEG42	SDMMC1_CK	-
	PC13	-	-	-	-	-	-
	PC14	-	-	-	-	-	-
	PC15	-	-	-	-	-	-

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port D	PD0	-	CAN1_RX	-	-	-	-
	PD1	-	CAN1_TX	-	-	-	-
	PD2	-	TSC_SYNC	-	LCD_COM7/ LCD_SEG31/ LCD_SEG43	SDMMC1_ CMD	-
Port D	PD3	-	-	QUADSPI_BK2_ NCS	-	-	-
	PD4	-	-	QUADSPI_BK2_ IO0	-	-	-
	PD5	-	-	QUADSPI_BK2_ IO1	-	-	-
	PD6	-	-	QUADSPI_BK2_ IO2	-	-	SAI1_SD_A
	PD7	-	-	QUADSPI_BK2_ IO3	-	-	-
	PD8	-	-	-	LCD_SEG28	-	-
	PD9	-	-	-	LCD_SEG29	-	-
	PD10	-	TSC_G6_IO1	-	LCD_SEG30	-	-
	PD11	-	TSC_G6_IO2	-	LCD_SEG31	-	-
	PD12	-	TSC_G6_IO3	-	LCD_SEG32	-	-
	PD13	-	TSC_G6_IO4	-	LCD_SEG33	-	-
	PD14	-	-	-	LCD_SEG34	-	-
	PD15	-	-	-	LCD_SEG35	-	-


Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port E	PE0	-	-	-	LCD_SEG36	-	-
	PE1	-	-	-	LCD_SEG37	-	-
	PE2	-	TSC_G7_IO1	-	LCD_SEG38	-	SAI1_MCLK_A
	PE3	-	TSC_G7_IO2	-	LCD_SEG39	-	SAI1_SD_B
	PE4	-	TSC_G7_IO3	-	-	-	SAI1_FS_A
Port E	PE5	-	TSC_G7_IO4	-	-	-	SAI1_SCK_A
	PE6	-	-	-	-	-	SAI1_SD_A
	PE7	-	-	-	-	-	SAI1_SD_B
	PE8	-	-	-	-	-	SAI1_SCK_E
	PE9	-	-	-	-	-	SAI1_FS_B
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	-	SAI1_MCLK_I
	PE11	-	TSC_G5_IO2	QUADSPI_BK1_NCS	-	-	-
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	-	-
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	-	-
	PE14	-	-	QUADSPI_BK1_IO2	-	-	-
	PE15	-	-	QUADSPI_BK1_IO3	-	-	-

Table 16. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1
Port H	PH0	-	-	-	-	-	-
	PH1	-	-	-	-	-	-
	PH3	-	-	-	-	-	-

1. Please refer to [Table 15](#) for AF0 to AF7.

5 Memory mapping

Figure 14. STM32L443xx memory map

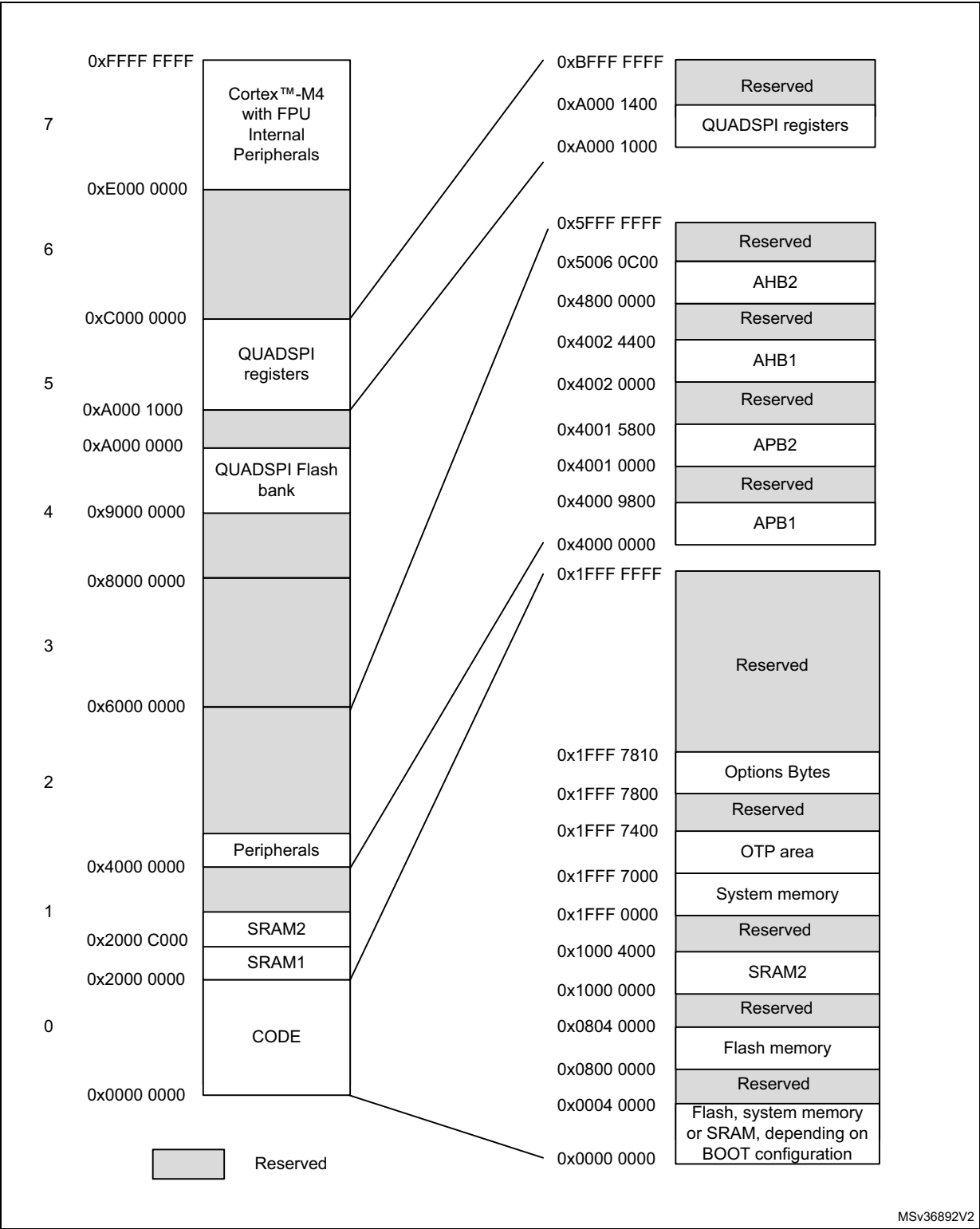


Table 17. STM32L443xx memory map and peripheral register boundary addresses⁽¹⁾

Bus	Boundary address	Size(bytes)	Peripheral
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5006 0400 - 0x5006 07FF	158 KB	Reserved
	0x5006 0000 - 0x5006 03FF	1 KB	AES
	0x5004 0400 - 0x5005 FFFF	158 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	Reserved
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1400 - 0x4800 1BFF	2 KB	Reserved
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1

Table 17. STM32L443xx memory map and peripheral register boundary addresses⁽¹⁾
(continued)

Bus	Boundary address	Size(bytes)	Peripheral
APB2	0x4001 5800 - 0x4001 FFFF	42 KB	Reserved
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4800 - 0x4000 53FF	3 KB	Reserved
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
APB2	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800 - 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG

Table 17. STM32L443xx memory map and peripheral register boundary addresses⁽¹⁾
(continued)

Bus	Boundary address	Size(bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	USB SRAM
	0x4000 6800 - 0x4000 6BFF	1 KB	USB FS
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00 - 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
APB1	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 1800 - 0x4000 23FF	3 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0400 - 0x4000 0FFF	3 KB	Reserved
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = V_{DDA} = 3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

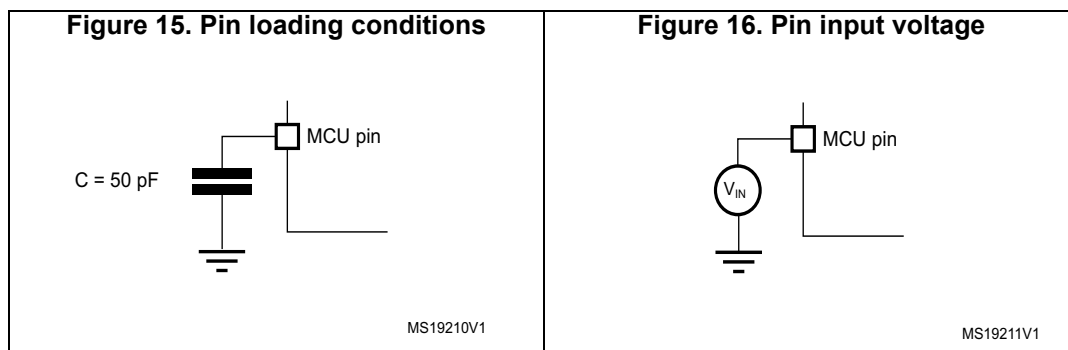
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 15](#).

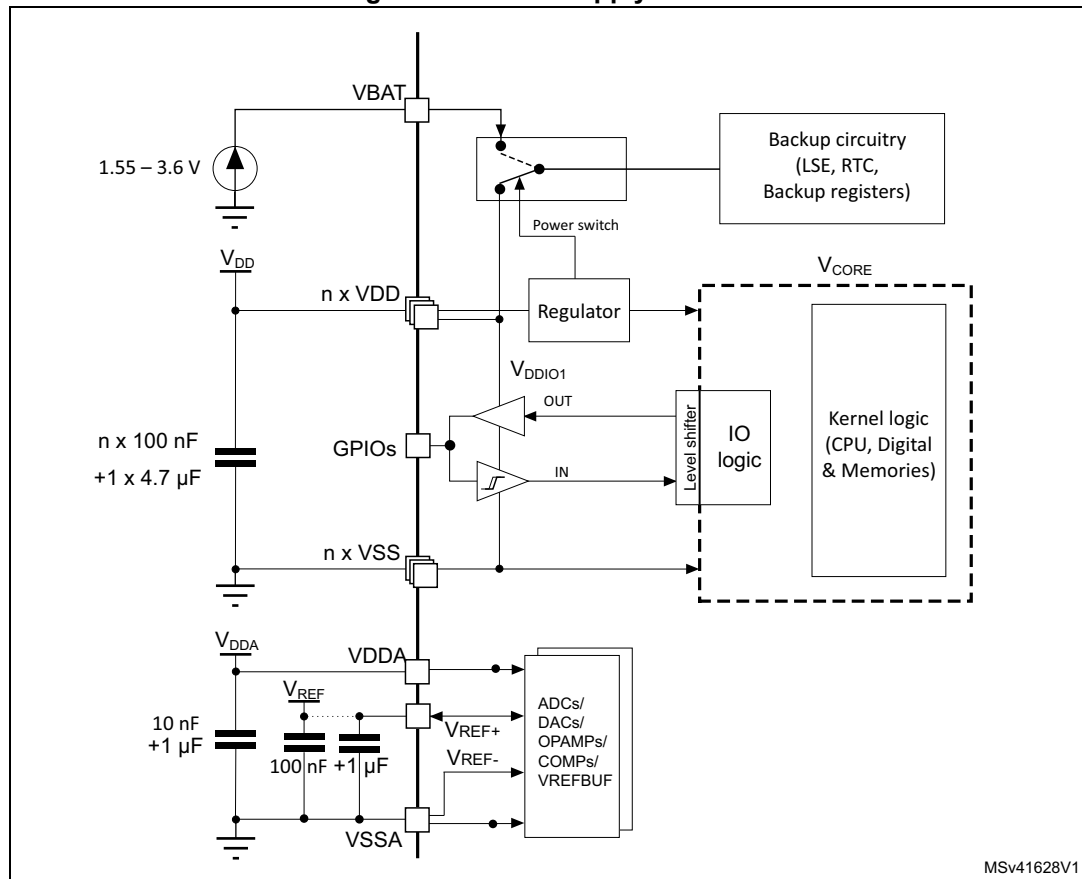
6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 16](#).



6.1.6 Power supply scheme

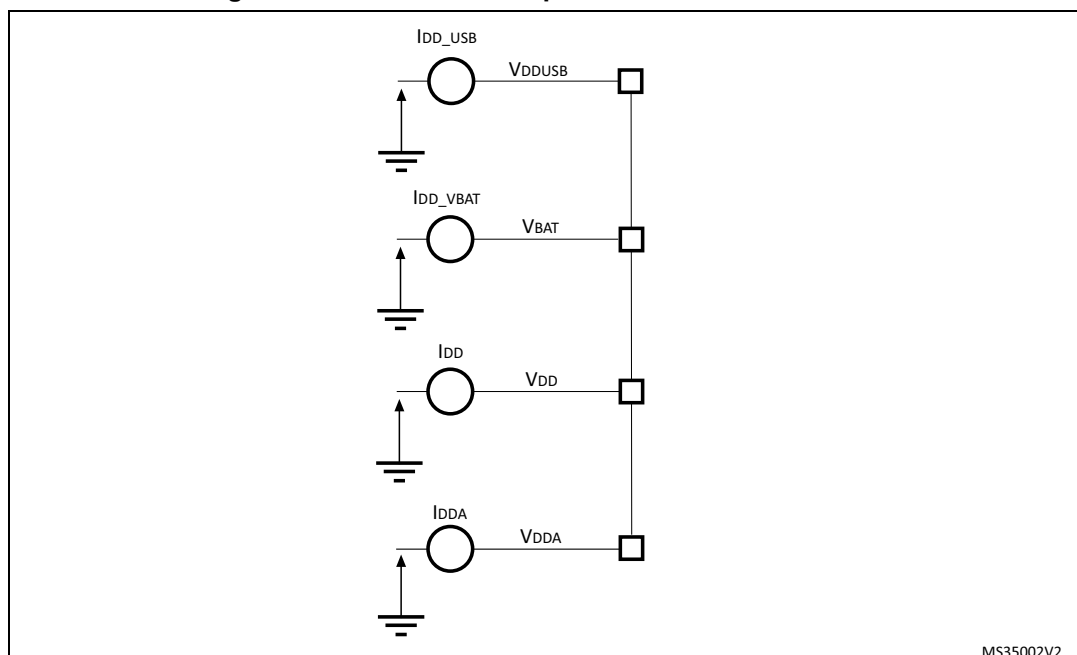
Figure 17. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



The I_{DD_ALL} parameters given in [Table 25](#) to [Table 37](#) represent the total MCU consumption including the current supplying V_{DD} , V_{DDA} , V_{DDUSB} and V_{BAT} .

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 18: Voltage characteristics](#), [Table 19: Current characteristics](#) and [Table 20: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 18. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{BAT})	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT_XXX pins	$V_{SS}-0.3$	$\min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 4.0^{(3)(4)}$	V
	Input voltage on TT_XX pins	$V_{SS}-0.3$	4.0	
	Input voltage on any other pins	$V_{SS}-0.3$	4.0	

Table 18. Voltage characteristics⁽¹⁾ (continued)

Symbol	Ratings	Min	Max	Unit
$ \Delta V_{DDX} $	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins ⁽⁵⁾	-	50	mV

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB} , V_{LCD} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 19: Current characteristics](#) for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$\Sigma I_{V_{DD}}$	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	140	mA
$\Sigma I_{V_{SS}}$	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	140	
$I_{V_{DD}(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{V_{SS}(PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	100	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	100	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0 ⁽⁴⁾	
	Injected current on PA4, PA5	-5/0	
$\Sigma I_{INJ(PIN)} $	Total injected current (sum of all I/Os and control pins) ⁽⁵⁾	25	

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOX}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 18: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma |I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	V
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	$V_{DDIOx}+0.3$	V
		All I/O except TT_xx	-0.3	$\text{Min}(\text{Min}(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCP})+3.6 \text{ V}, 5.5 \text{ V})^{(2)(3)}$	
P_D	Power dissipation at $T_A = 85^\circ\text{C}$ for suffix 6 or $T_A = 105^\circ\text{C}$ for suffix 7 ⁽⁴⁾	LQFP100	-	476	mW
		LQFP64	-	444	
		LQFP48	-	350	
		UFBGA100	-	350	
		UFBGA64	-	307	
		UFQFPN48	-	606	
		WLCSP64	-	434	
		WLCSP49	-	416	
P_D	Power dissipation at $T_A = 125^\circ\text{C}$ for suffix 3 ⁽⁴⁾	LQFP100	-	119	mW
		LQFP64	-	111	
		LQFP48	-	88	
		UFBGA100	-	88	
		UFBGA64	-	77	
		UFQFPN48	-	151	
		WLCSP64	-	109	
		WLCSP49	-	104	

Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T _A	Ambient temperature for the suffix 6 version	Maximum power dissipation	−40	85	°C
		Low-power dissipation ⁽⁵⁾	−40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	−40	105	
		Low-power dissipation ⁽⁵⁾	−40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	−40	125	
		Low-power dissipation ⁽⁵⁾	−40	130	
T _J	Junction temperature range	Suffix 6 version	−40	105	°C
		Suffix 7 version	−40	125	
		Suffix 3 version	−40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between Min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see [Section 7.10: Thermal characteristics](#)).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.10: Thermal characteristics](#)).

6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 22](#) are derived from tests performed under the ambient temperature condition summarized in [Table 21](#).

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t _{VDD}	V _{DD} rise time rate	-	0	∞	μs/V
	V _{DD} fall time rate		10	∞	
t _{VDDA}	V _{DDA} rise time rate	-	0	∞	
	V _{DDA} fall time rate		10	∞	
t _{VDDUSB}	V _{DDUSB} rise time rate	-	0	∞	
	V _{DDUSB} fall time rate		10	∞	

The requirements for power-up/down sequence specified in [Section 3.9.1: Power supply schemes](#) must be respected.

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature conditions summarized in [Table 21: General operating conditions](#).

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
$t_{RSTTEMPO}^{(2)}$	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	μs
$V_{BOR0}^{(2)}$	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
$I_{DD}^{(3)}$ (BOR_PVD) ⁽²⁾	BOR ⁽³⁾ (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	μA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V

Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1) (2)	PVM1 consumption from V_{DD}	-	-	0.2	-	μA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	μA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

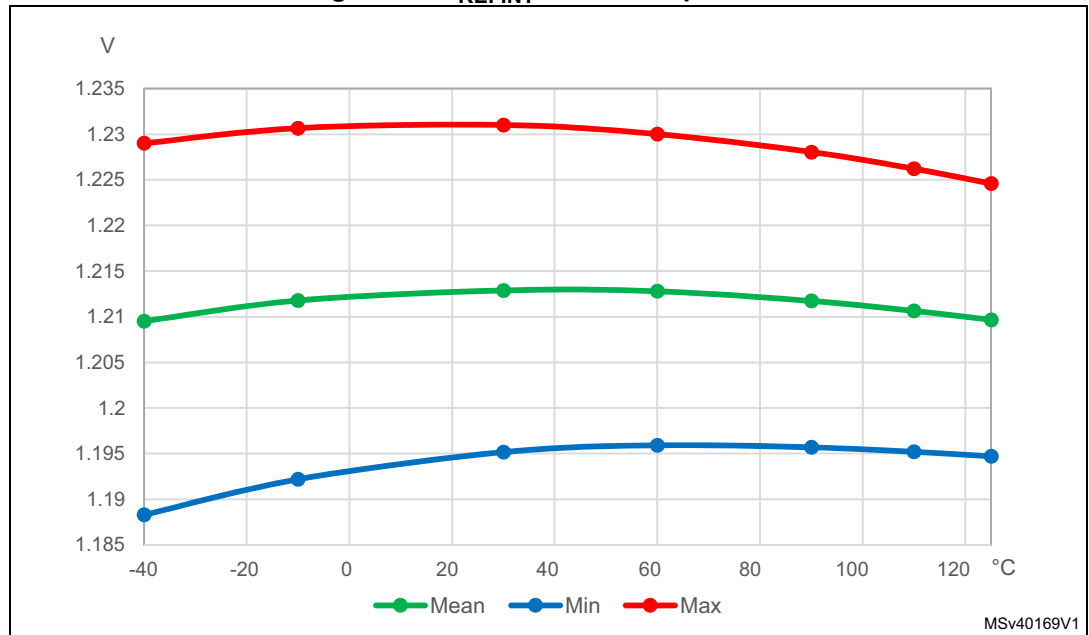
6.3.4 Embedded voltage reference

The parameters given in [Table 24](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +130\text{ }^{\circ}\text{C}$	1.182	1.212	1.232	V
$t_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽²⁾	-	-	μs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12 ⁽²⁾	μs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20 ⁽²⁾	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V}$	-	5	7.5 ⁽²⁾	mV
T_{Coeff}	Temperature coefficient	$-40\text{ }^{\circ}\text{C} < T_A < +130\text{ }^{\circ}\text{C}$	-	30	50 ⁽²⁾	ppm/ $^{\circ}\text{C}$
A_{Coeff}	Long term stability	1000 hours, $T = 25\text{ }^{\circ}\text{C}$	-	300	1000 ⁽²⁾	ppm
$V_{DDCcoeff}$	Voltage coefficient	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	250	1200 ⁽²⁾	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 19. V_{REFINT} versus temperature

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 18: Current consumption measurement scheme](#).

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0394 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in [Table 25](#) to [Table 38](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).



Table 25. Current consumption in Run and Low-power run modes, code with data protection running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (Run)	Supply current in Run mode	f _{HCLK} = f _{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.37	2.38	2.44	2.52	2.66	2.7	2.7
				16 MHz	1.5	1.52	1.57	1.64	1.79	1.7	1.7
				8 MHz	0.81	0.82	0.87	0.94	1.08	0.9	0.9
				4 MHz	0.46	0.47	0.52	0.59	0.73	0.5	0.5
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	0.3
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	0.2
			Range 1	100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	0.1
				80 MHz	8.53	8.56	8.64	8.74	8.92	9.5	9.5
				72 MHz	7.7	7.73	7.8	7.9	8.08	8.6	8.6
				64 MHz	6.86	6.9	6.97	7.06	7.23	7.7	7.7
				48 MHz	5.13	5.16	5.23	5.32	5.49	5.8	5.8
				32 MHz	3.46	3.48	3.55	3.64	3.8	3.9	3.9
				24 MHz	2.63	2.64	2.71	2.79	2.96	3.0	3.0
				16 MHz	1.8	1.81	1.87	1.96	2.12	2.0	2.0
I _{DD_ALL} (LPRun)	Supply current in Low-power run mode	f _{HCLK} = f _{MSI} all peripherals disable	2 MHz	211	230	280	355	506	273.8	273.8	
			1 MHz	117	134	179	254	404	154.7	154.7	
			400 kHz	58.5	70.4	116	189	338	80.2	80.2	
			100 kHz	30	41.1	85.2	159	308	46.5	46.5	

1. Guaranteed by characterization results, unless otherwise specified.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (Run)	Supply current in Run mode	f _{HCLK} = f _{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.66	2.68	2.73	2.81	2.96	3.0	4.0
				16 MHz	1.88	1.9	1.94	2.02	2.17	2.1	3.0
				8 MHz	1.05	1.06	1.11	1.18	1.33	1.2	2.0
				4 MHz	0.6	0.62	0.66	0.73	0.87	0.7	1.0
				2 MHz	0.36	0.37	0.34	0.48	0.62	0.4	0.5
				1 MHz	0.23	0.25	0.25	0.36	0.5	0.3	0.4
				100 kHz	0.12	0.14	0.17	0.25	0.39	0.1	0.2
			Range 1	80 MHz	8.56	8.61	8.69	8.79	8.97	9.6	12.0
				72 MHz	7.74	7.79	7.86	7.96	8.14	8.7	11.0
				64 MHz	7.63	7.68	7.75	7.85	8.04	8.6	10.0
				48 MHz	6.36	6.4	6.48	6.58	6.76	7.2	9.0
				32 MHz	4.56	4.6	4.66	4.76	4.93	5.2	7.0
				24 MHz	3.45	3.48	3.54	3.64	3.8	3.9	5.0
				16 MHz	2.48	2.51	2.56	2.65	2.82	2.8	4.0
I _{DD_ALL} (LPRun)	Supply current in Low-power run	f _{HCLK} = f _{MSI} all peripherals disable		2 MHz	310	317	364	440	593	375.3	470
				1 MHz	157	173	226	296	448	204.8	260
				400 kHz	72.6	89	130	206	356	99.7	125
				100 kHz	32.3	46	89.7	164	314	52.4	65

1. Guaranteed by characterization results, unless otherwise specified.

**Table 27. Current consumption in Run and Low-power run modes, code with data running from SRAM1**

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	
I _{DD_ALL} (Run)	Supply current in Run mode	f _{HCLK} = f _{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.42	2.43	2.49	2.56	2.71	2.7	
				16 MHz	1.54	1.55	1.6	1.67	1.82	1.7	
				8 MHz	0.82	0.84	0.88	0.95	1.1	0.9	
				4 MHz	0.47	0.48	0.52	0.59	0.73	0.5	
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	
				100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	
			Range 1	80 MHz	8.63	8.68	8.74	8.84	9.01	9.5	
				72 MHz	7.79	7.83	7.9	7.99	8.17	8.6	
				64 MHz	6.95	6.99	7.05	7.15	7.32	7.7	
				48 MHz	5.19	5.22	5.29	5.38	5.55	5.8	
				32 MHz	3.51	3.53	3.6	3.68	3.85	3.9	
				24 MHz	2.66	2.68	2.74	2.83	2.99	3.0	
				16 MHz	1.82	1.84	1.89	1.98	2.14	2.0	
I _{DD_ALL} (LPRun)	Supply current in low-power run mode	f _{HCLK} = f _{MSI} all peripherals disable FLASH in power-down	2 MHz	205	228	275	352	501	276.5		
			1 MHz	111	126	175	248	397	151.3		
			400 kHz	49.2	62.7	108	181	330	73.3		
			100 kHz	21.5	33.3	76.6	151	299	36.4		

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 $f_{HCLK} = 26$ MHz	Reduced code ⁽¹⁾	2.37	mA	91	$\mu A/MHz$
				Coremark	2.69		103	
				Dhrystone 2.1	2.74		105	
				Fibonacci	2.58		99	
				While(1)	2.30		88	
			Range 1 $f_{HCLK} = 80$ MHz	Reduced code ⁽¹⁾	8.53	mA	107	$\mu A/MHz$
				Coremark	9.68		121	
				Dhrystone 2.1	9.76		122	
				Fibonacci	9.27		116	
				While(1)	8.20		103	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz all peripherals disable		Reduced code ⁽¹⁾	211	μA	106	$\mu A/MHz$
				Coremark	251		126	
				Dhrystone 2.1	269		135	
				Fibonacci	230		115	
				While(1)	286		143	

1. Reduced code used for characterization results provided in [Table 25](#), [Table 26](#), [Table 27](#).

Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 $f_{HCLK} = 26$ MHz	Reduced code ⁽¹⁾	2.66	mA	102	$\mu A/MHz$
				Coremark	2.44		94	
				Dhrystone 2.1	2.46		95	
				Fibonacci	2.27		87	
				While(1)	2.20		84.6	
			Range 1 $f_{HCLK} = 80$ MHz	Reduced code ⁽¹⁾	8.56	mA	107	$\mu A/MHz$
				Coremark	8.00		100	
				Dhrystone 2.1	7.98		100	
				Fibonacci	7.41		93	
				While(1)	7.83		98	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz all peripherals disable		Reduced code ⁽¹⁾	310	μA	155	$\mu A/MHz$
				Coremark	342		171	
				Dhrystone 2.1	324		162	
				Fibonacci	324		162	
				While(1)	384		192	

1. Reduced code used for characterization results provided in [Table 25](#), [Table 26](#), [Table 27](#).

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 $f_{HCLK} = 26$ MHz	Reduced code ⁽¹⁾	2.42	mA	93	$\mu A/MHz$
				Coremark	2.18		84	
				Dhrystone 2.1	2.40		92	
				Fibonacci	2.40		92	
				While(1)	2.29		88	
			Range 1 $f_{HCLK} = 80$ MHz	Reduced code ⁽¹⁾	8.63	mA	108	$\mu A/MHz$
				Coremark	7.76		97	
				Dhrystone 2.1	8.55		107	
				Fibonacci	8.56		107	
				While(1)	8.12		102	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz all peripherals disable		Reduced code ⁽¹⁾	205	μA	103	$\mu A/MHz$
				Coremark	188		94	
				Dhrystone 2.1	222		111	
				Fibonacci	204		102	
				While(1)	211		106	

1. Reduced code used for characterization results provided in [Table 25](#), [Table 26](#), [Table 27](#).

Table 31. Current consumption in Sleep and Low-power sleep modes, Flash

Symbol	Parameter	Conditions			TYP					25 °C	55 °C
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C		
I _{DD,ALL} (Sleep)	Supply current in sleep mode,	f _{HCLK} = f _{HSE} up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	
I _{DD,ALL} (LPSleep)	Supply current in low-power sleep mode	f _{HCLK} = f _{MSI} all peripherals disable		2 MHz	71.8	80.7	125	200	350	91.1	1
				1 MHz	45.0	57.3	101	176	325	63.2	
				400 kHz	27.0	40.7	84.6	158	308	43.9	
				100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	

1. Guaranteed by characterization results, unless otherwise specified.

Table 32. Current consumption in Low-power sleep modes, Flash in power

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	f _{HCLK} = f _{MSI} all peripherals disable		2 MHz	58.7	70.7	103.2	153.7	248.5	80	55
				1 MHz	39.4	47.2	79.3	129.6	224.8	53	40
				400 kHz	20.8	30.8	62.1	112.5	207.8	35	25
				100 kHz	14.3	23.1	55.1	105.7	201.5	27	18

1. Guaranteed by characterization results, unless otherwise specified.

Table 33. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP						
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled	1.8 V	1	2.54	8.74	19.8	43.4	2.0	1.5
			2.4 V	1.02	2.59	8.89	20.2	44.3	2.1	1.6
			3 V	1.06	2.67	9.11	20.7	45.5	2.1	1.6
			3.6 V	1.23	2.88	9.56	21.6	47.3	2.3	1.8
		LCD enabled ⁽²⁾ clocked by LSI	1.8 V	1.31	2.87	9.03	20	43.1	2.6	2.0
			2.4 V	1.36	2.96	9.22	20.4	44.1	2.8	2.2
			3 V	1.45	3.08	9.24	20.4	45.5	2.9	2.3
			3.6 V	1.69	3.4	10.1	22.1	47.9	3.1	2.5



Table 33. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	1.8 V	1.3	2.82	9.02	20.1	43.6	2.5	
			2.4 V	1.39	2.95	9.24	20.5	44.6	2.8	
			3 V	1.5	3.11	9.55	21.1	45.8	3.0	
			3.6 V	1.76	3.42	10.1	22.1	47.8	3.3	
		RTC clocked by LSI, LCD enabled ⁽²⁾	1.8 V	1.41	2.96	9.13	20.1	43.3	2.8	
			2.4 V	1.49	3.08	9.35	20.5	44.2	3.0	
			3 V	1.61	3.25	9.41	20.5	45.6	3.2	
			3.6 V	1.91	3.63	10.3	22.3	48.1	3.5	
		RTC clocked by LSE bypassed at 32768Hz, LCD disabled	1.8 V	1.36	2.9	9.1	20.1	43.7	-	
			2.4 V	1.48	3.09	9.44	20.8	45	-	
			3 V	1.83	3.67	10.4	22.3	47.3	-	
			3.6 V	3.58	6.17	13.9	26.6	53	-	
		RTC clocked by LSE quartz ⁽⁴⁾ in low drive mode, LCD disabled	1.8 V	1.28	2.81	9.13	20.8	-	-	
			2.4 V	1.39	2.93	9.34	21.3	-	-	
			3 V	1.59	3.1	9.64	21.8	-	-	
			3.6 V	1.86	3.45	10.2	22.8	-	-	
I _{DD_ALL} (wakeup from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See ⁽⁵⁾ .	3 V	1.85	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See ⁽⁵⁾ .	3 V	1.52	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See ⁽⁵⁾ .	3 V	1.54	-	-	-	-	-	



1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD} .
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 40: Low-power mode](#).

Table 34. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					25 °C
		-	-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD_ALL} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	4.34	12.4	43.6	96.4	204	9.3
				2.4 V	4.35	12.5	43.8	97	205	9.4
				3 V	4.41	12.6	44.1	97.7	207	9.5
				3.6 V	4.56	12.9	44.8	98.9	210	9.7
		-	LCD enabled ⁽²⁾ clocked by LSI	1.8 V	4.68	12.7	43.9	96.7	204	9.1
				2.4 V	4.7	12.8	44.2	97.3	205	9.7
				3 V	4.88	12.6	44.5	98	206	10.2
				3.6 V	5.1	13.4	45.3	99.6	270	10.6
		RTC clocked by LSI	LCD disabled	1.8 V	4.63	12.7	43.9	96.8	205	9.9
				2.4 V	4.78	12.8	44.2	97.4	206	10.1
				3 V	4.93	13	44.6	98.1	207	10.4
				3.6 V	5.05	13.4	45.3	99.5	210	10.8
			LCD enabled ⁽²⁾	1.8 V	4.82	12.9	44	96.8	204	10.2
				2.4 V	4.93	13	44.3	97.4	205	10.4
				3 V	5.05	12.7	44.7	98.1	206	10.7
				3.6 V	5.31	13.7	45.6	99.9	210	11.1
I _{DD_ALL} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	4.7	12.8	44	96.9	205	-
				2.4 V	4.95	13	44.4	97.6	206	-
				3 V	5.33	13.6	45.4	99.1	209	-
				3.6 V	6.91	16.1	48.8	103	216	-
		RTC clocked by LSE quartz ⁽³⁾ in low drive mode	LCD disabled	1.8 V	4.76	12.3	43.7	99.1	-	-
				2.4 V	4.95	12.4	43.8	99.3	-	-
				3 V	5.1	12.6	44.1	99.6	-	-
				3.6 V	5.65	13	44.8	101	-	-

**Table 34. Current consumption in Stop 1 mode (continued)**

Symbol	Parameter	Conditions			TYP					25 °C
		-	-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD_ALL} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See ⁽⁴⁾ .		3 V	1.14	-	-	-	-	-
		Wakeup clock MSI = 4 MHz, voltage Range 2. See ⁽⁴⁾ .		3 V	1.22	-	-	-	-	-
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See ⁽⁴⁾ .		3 V	1.20	-	-	-	-	-

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 40: Low-power mode](#).

**Table 35. Current consumption in Stop 0**

Symbol	Parameter	Conditions	TYP						
		V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C
I _{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	108	119	158	221	347	133	136
		2.4 V	110	121	160	223	349	136	139
		3 V	111	123	161	224	352	139	142
		3.6 V	114	125	163	227	355	142	145

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 36. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP						
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	
I _{DD_ALL} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	27.7	144	758	2 072	5 425	119	
			2.4 V	50.9	187	892	2 408	6 247	183	
			3 V	90.2	253	1 090	2 884	7 409	225	
			3.6 V	253	459	1 474	3 575	8 836	292	
		with independent watchdog	1.8 V	216	-	-	-	-	-	
			2.4 V	342	-	-	-	-	-	
			3 V	416	-	-	-	-	-	
			3.6 V	551	-	-	-	-	-	
I _{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	287	407	989	2 230	5 396	585	
			2.4 V	386	526	1 201	2 638	6 274	811	
			3 V	513	679	1 478	3 167	7 414	1022	
			3.6 V	771	978	1 963	3 992	9 039	1284	
		RTC clocked by LSI, with independent watchdog	1.8 V	342	-	-	-	-	-	
			2.4 V	521	-	-	-	-	-	
			3 V	655	-	-	-	-	-	
			3.6 V	865	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768Hz	1.8 V	142	126	865	2 220	5 650	-	
			2.4 V	249	219	1 090	2 660	6 600	-	
			3 V	404	364	1 410	3 260	7 850	-	
			3.6 V	742	670	2 000	4 230	9 700	-	
		RTC clocked by LSE quartz ⁽³⁾ in low drive mode	1.8 V	281	423	1 046	2 410	5 700	-	
			2.4 V	388	548	1 268	2 847	6 564	-	
			3 V	535	715	1 565	3 420	7 694	-	
			3.6 V	836	1 048	2 081	4 311	9 338	-	

Table 36. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					25 °C	55 °C
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C		
I _{DD_ALL} (SRAM2) ⁽⁴⁾	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	173	349	1 009	2 158	4 542	249	
			2.4 V	174	345	1 015	2 163	4 535	271	
			3 V	178	350	1 019	2 148	4 419	277	
			3.6 V	184	352	1 033	2 208	4 610	293	
I _{DD_ALL} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See ⁽⁵⁾ .	3 V	1.23	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 40: Low-power mode](#).

Table 37. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					25 °C	55 °C
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C		
I _{DD_ALL} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	7.82	190	386	1 286	3 854	25.0	
			2.4 V	23	229	485	1 517	4 431	34.9	
			3 V	44.3	290	634	1 878	5 310	70.1	
			3.6 V	212	397	977	2 516	6 656	119.1	

Table 37. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					25 °C	5
		-	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C		
I _{DD_ALL} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	63	133	522	1 490	4 270	-	-
			2.4 V	165	253	710	1 830	4 980	-	-
			3 V	316	423	990	2 340	6 050	-	-
			3.6 V	649	787	1 530	3 220	7 710	-	-
	RTC clocked by LSE quartz ⁽²⁾ in low drive mode		1.8 V	203	293	700	1 675	-	-	-
			2.4 V	303	411	880	2 001	-	-	-
			3 V	448	567	1 136	2 479	-	-	-
			3.6 V	744	887	1 609	3 256	-	-	-
I _{DD_ALL} (wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See ⁽³⁾ .	3 V	0.780	-	-	-	-	-	-

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 40: Low-power mode](#).

Table 38. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					25 °C	5
		-	V _{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C		
I _{DD VBAT} (VBAT)	Backup domain supply current	RTC disabled	1.8 V	2	12	66	193	540	5	
			2.4 V	1	12	73	217	600	6	
			3 V	5	16	92	266	731	12.5	
			3.6 V	6	30	161	459	1 269	15	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	154	175	247	430	-	-	
			2.4 V	228	246	335	542	-	-	
			3 V	316	340	459	714	-	-	
			3.6 V	419	462	684	1 140	-	-	
		RTC enabled and clocked by LSE quartz ⁽²⁾	1.8 V	256	297	385	558	823	-	
			2.4 V	345	381	477	673	906	-	
			3 V	455	495	603	836	1 085	-	
			3.6 V	591	642	824	1 207	1 733	-	

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading ca

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 59: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 39: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 39](#). The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
 - when the peripheral is clocked on
 - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 18: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 39](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 39. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix ⁽¹⁾	3.2	2.9	3.1	μA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	AES	1.7	1.5	1.6	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA ⁽²⁾	1.7	1.4	1.6	
	GPIOB ⁽²⁾	1.6	1.3	1.6	
	GPIOC ⁽²⁾	1.7	1.5	1.6	
	GPIOD ⁽²⁾	1.8	1.6	1.7	
	GPIOE ⁽²⁾	1.7	1.6	1.6	
	GPIOH ⁽²⁾	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	N/A	N/A	
	RNG clock domain	0.5	N/A	N/A	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge ⁽³⁾	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	

Table 39. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	DAC1	2.4	1.8	2.2	$\mu\text{A}/\text{MHz}$
	RTCA	1.7	1.1	2.1	
	CRS	0.3	0.3	0.6	
	USB FS independent clock domain	2.9	N/A	N/A	
	USB FS clock domain	2.3	N/A	N/A	
	I2C1 independent clock domain	3.5	2.8	3.4	
	I2C1 clock domain	1.1	0.9	1.0	
	I2C2 independent clock domain	3.5	3.0	3.4	
	I2C2 clock domain	1.1	0.7	0.9	
	I2C3 independent clock domain	2.9	2.3	2.5	
	I2C3 clock domain	0.9	0.4	0.8	
	LCD	0.9	0.6	0.8	
	LPUART1 independent clock domain	1.9	1.6	1.8	
	LPUART1 clock domain	0.6	0.6	0.6	
	LPTIM1 independent clock domain	2.9	2.4	2.8	
	LPTIM1 clock domain	0.8	0.4	0.7	
	LPTIM2 independent clock domain	3.1	2.7	3.9	
	LPTIM2 clock domain	0.8	0.7	0.8	
	OPAMP	0.4	0.2	0.4	
	PWR	0.4	0.1	0.4	
	SPI2	1.8	1.6	1.6	
	SPI3	1.7	1.3	1.6	
	SWPMI1 independent clock domain	1.9	1.6	1.9	
	SWPMI1 clock domain	0.9	0.7	0.8	
	TIM2	6.2	5.0	5.9	
	TIM6	1.0	0.6	0.9	
	TIM7	1.0	0.6	0.6	
	USART2 independent clock domain	4.1	3.6	3.8	
	USART2 clock domain	1.3	0.9	1.1	

Table 39. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	USART3 independent clock domain	4.3	3.5	4.2	$\mu\text{A}/\text{MHz}$
	USART3 clock domain	1.5	1.1	1.3	
	WWDG	0.5	0.5	0.5	
	All APB1 on	51.5	35.5	48.6	
APB2	AHB to APB2 ⁽⁴⁾	1.0	0.9	0.9	
	FW	0.2	0.2	0.2	
	SAI1 independent clock domain	2.3	1.8	1.9	
	SAI1 clock domain	2.1	1.8	2.0	
	SDMMC1 independent clock domain	4.7	3.9	3.9	
	SDMMC1 clock domain	2.5	1.9	1.9	
	SPI1	1.8	1.6	1.7	
	SYSCFG/VREFBUF/COMP	0.6	0.5	0.6	
	TIM1	8.1	6.5	7.6	
	TIM15	3.7	3.0	3.4	
	TIM16	2.7	2.1	2.6	
	USART1 independent clock domain	4.8	4.2	4.6	
	USART1 clock domain	1.5	1.3	1.7	
	All APB2 on	24.2	19.9	22.6	
ALL		100.9	77.1	94.8	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A...H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in [Table 40](#) are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 40. Low-power mode wakeup timings⁽¹⁾

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		6	8.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	3.8	5.7	μs
			Wakeup clock HSI16 = 16 MHz	4.1	6.9	
		Range 2	Wakeup clock MSI = 24 MHz	4.07	6.2	
			Wakeup clock HSI16 = 16 MHz	4.1	6.8	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 4 MHz	8.45	11.8	
			Wakeup clock MSI = 48 MHz	1.5	2.9	
		Range 2	Wakeup clock HSI16 = 16 MHz	2.4	2.76	
			Wakeup clock MSI = 24 MHz	2.4	3.48	
			Wakeup clock HSI16 = 16 MHz	2.4	2.76	
			Wakeup clock MSI = 4 MHz	8.16	10.94	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.34	7.86	μs
			Wakeup clock HSI16 = 16 MHz	6.84	8.23	
		Range 2	Wakeup clock MSI = 24 MHz	6.74	8.1	
			Wakeup clock HSI16 = 16 MHz	6.89	8.21	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 4 MHz	10.47	12.1	
			Wakeup clock MSI = 48 MHz	4.7	5.97	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.9	6.92	
			Wakeup clock MSI = 24 MHz	5.4	6.51	
			Wakeup clock HSI16 = 16 MHz	5.9	6.92	
			Wakeup clock MSI = 4 MHz	11.1	12.2	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	16.4	17.73	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			17.3	18.82	

Table 40. Low-power mode wakeup timings⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.02	9.24	μs
			Wakeup clock HSI16 = 16 MHz	7.66	8.95	
		Range 2	Wakeup clock MSI = 24 MHz	8.5	9.54	
			Wakeup clock HSI16 = 16 MHz	7.75	8.95	
			Wakeup clock MSI = 4 MHz	12.06	13.16	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.45	6.79	
			Wakeup clock HSI16 = 16 MHz	6.9	7.98	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	7.36	
			Wakeup clock HSI16 = 16 MHz	6.9	7.9	
			Wakeup clock MSI = 4 MHz	13.1	13.31	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	12.2	18.35	μs
			Wakeup clock MSI = 4 MHz	19.14	25.8	
$t_{WUSTBY\text{ SRAM2}}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	12.1	18.3	μs
			Wakeup clock MSI = 4 MHz	19.2	25.87	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	261.5	315.7	μs

1. Guaranteed by characterization results.

Table 41. Regulator modes transition times⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode ⁽²⁾	Code run with MSI 2 MHz	5	7	μs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2 ⁽³⁾	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.

2. Time until REGLPF flag is cleared in PWR_SR2.

3. Time until VOSF flag is cleared in PWR_SR2.

Table 42. Wakeup time using USART/LPUART⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI16	Stop 0 mode	-	1.7	μs
		Stop 1 mode and Stop 2 mode	-	8.5	

1. Guaranteed by design.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

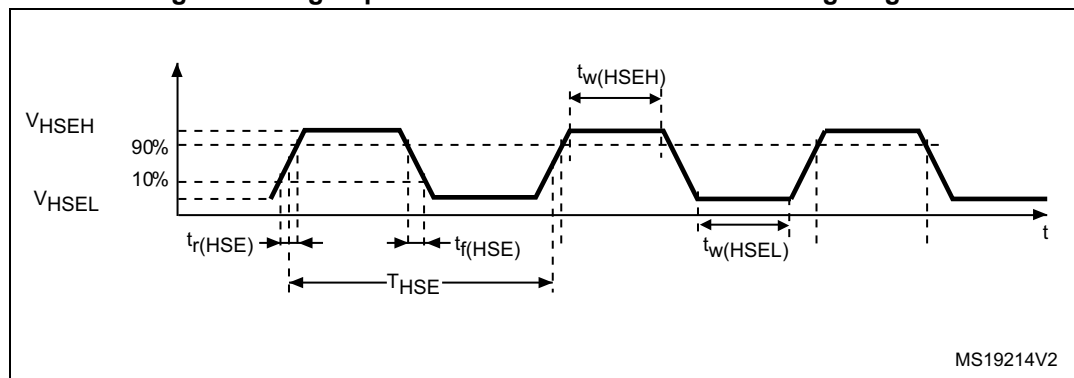
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 20: High-speed external clock source AC timing diagram](#).

Table 43. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSE_ext}}$	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7 V_{\text{DDIOx}}$	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3 V_{\text{DDIOx}}$	
$t_{\text{w(HSEH)}}$ $t_{\text{w(HSEL)}}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 20. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

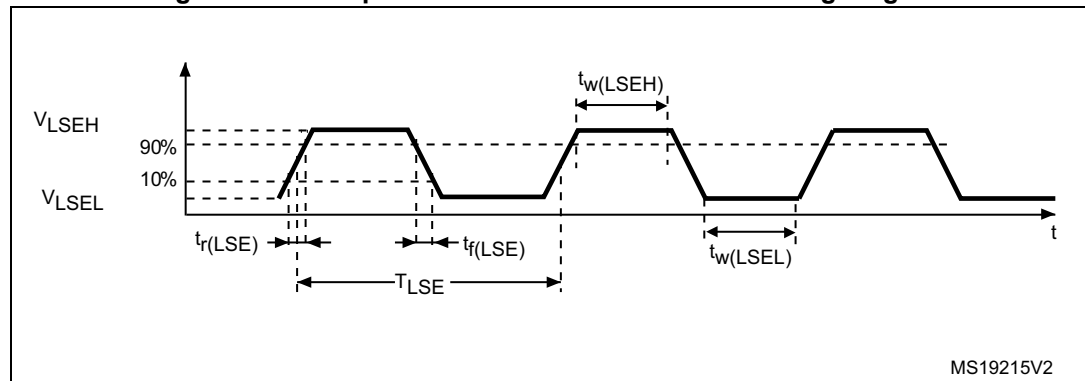
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 21](#).

Table 44. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7 V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 45](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 45. HSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
$I_{DD(HSE)}$	HSE current consumption	During startup ⁽³⁾	-	-	5.5	mA
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$	-	0.44	-	
		$V_{DD} = 3\text{ V}$, $R_m = 45\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$	-	0.45	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 5\text{ pF}@48\text{ MHz}$	-	0.68	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@48\text{ MHz}$	-	0.94	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 20\text{ pF}@48\text{ MHz}$	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.

2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

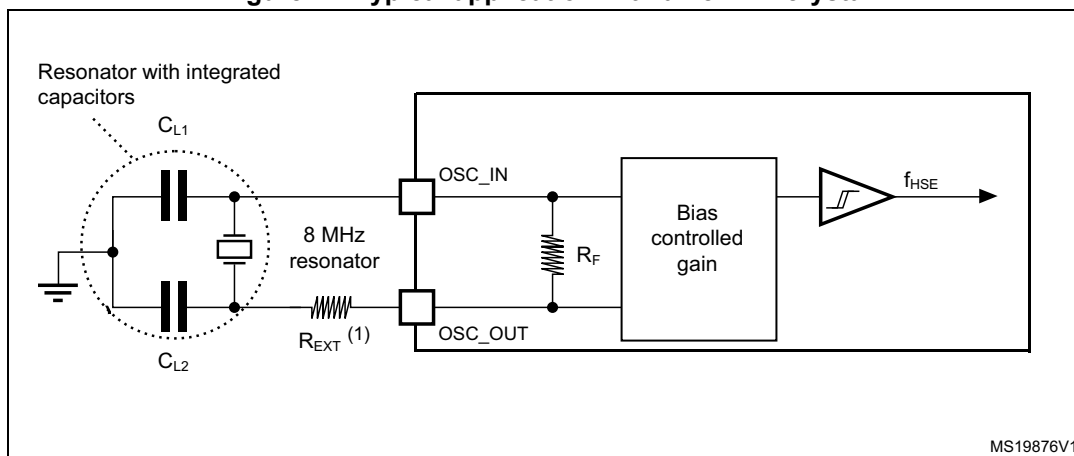
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 22](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 46](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

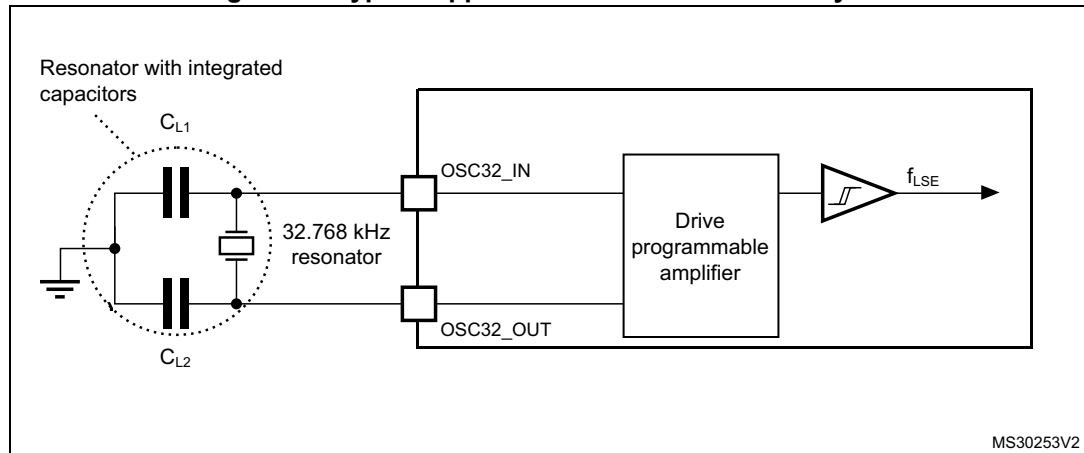
Table 46. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{m_{critmax}}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 23. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between $OSC32_IN$ and $OSC32_OUT$ and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in [Table 47](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#). The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

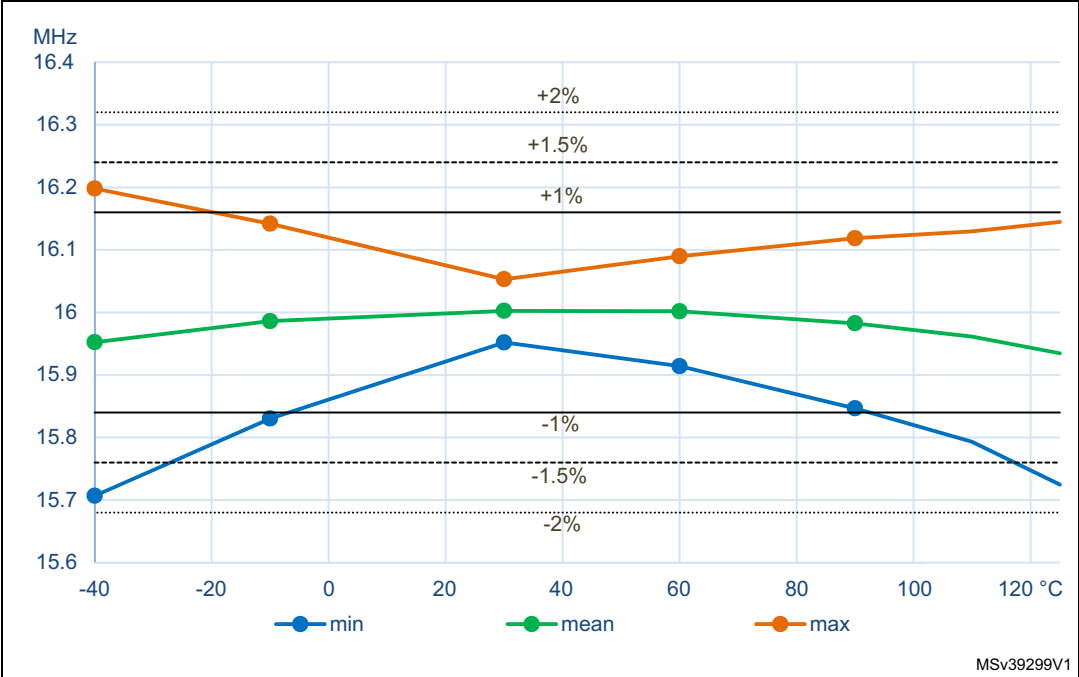
Table 47. HSI16 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	$V_{\text{DD}}=3.0\text{ V}$, $T_{\text{A}}=30\text{ }^{\circ}\text{C}$	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
$\text{DuCy}(\text{HSI16})^{(2)}$	Duty Cycle	-	45	-	55	%
$\Delta_{\text{Temp}}(\text{HSI16})$	HSI16 oscillator frequency drift over temperature	$T_{\text{A}}=0\text{ to }85\text{ }^{\circ}\text{C}$	-1	-	1	%
		$T_{\text{A}}=-40\text{ to }125\text{ }^{\circ}\text{C}$	-2	-	1.5	%
$\Delta_{\text{VDD}}(\text{HSI16})$	HSI16 oscillator frequency drift over V_{DD}	$V_{\text{DD}}=1.62\text{ V to }3.6\text{ V}$	-0.1	-	0.05	%
$t_{\text{su}}(\text{HSI16})^{(2)}$	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
$t_{\text{stab}}(\text{HSI16})^{(2)}$	HSI16 oscillator stabilization time	-	-	3	5	μs
$I_{\text{DD}}(\text{HSI16})^{(2)}$	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Figure 24. HSI16 frequency versus temperature



Multi-speed internal (MSI) RC oscillator

Table 48. MSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at $V_{\text{DD}}=3\text{ V}$ and $T_{\text{A}}=30\text{ }^{\circ}\text{C}$	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{\text{TEMP}}(\text{MSI})^{(2)}$	MSI oscillator frequency drift over temperature	MSI mode	$T_{\text{A}} = -0\text{ to }85\text{ }^{\circ}\text{C}$	-3.5	-	3	%
			$T_{\text{A}} = -40\text{ to }125\text{ }^{\circ}\text{C}$	-8	-	6	

Table 48. MSI oscillator characteristics⁽¹⁾ (continued)

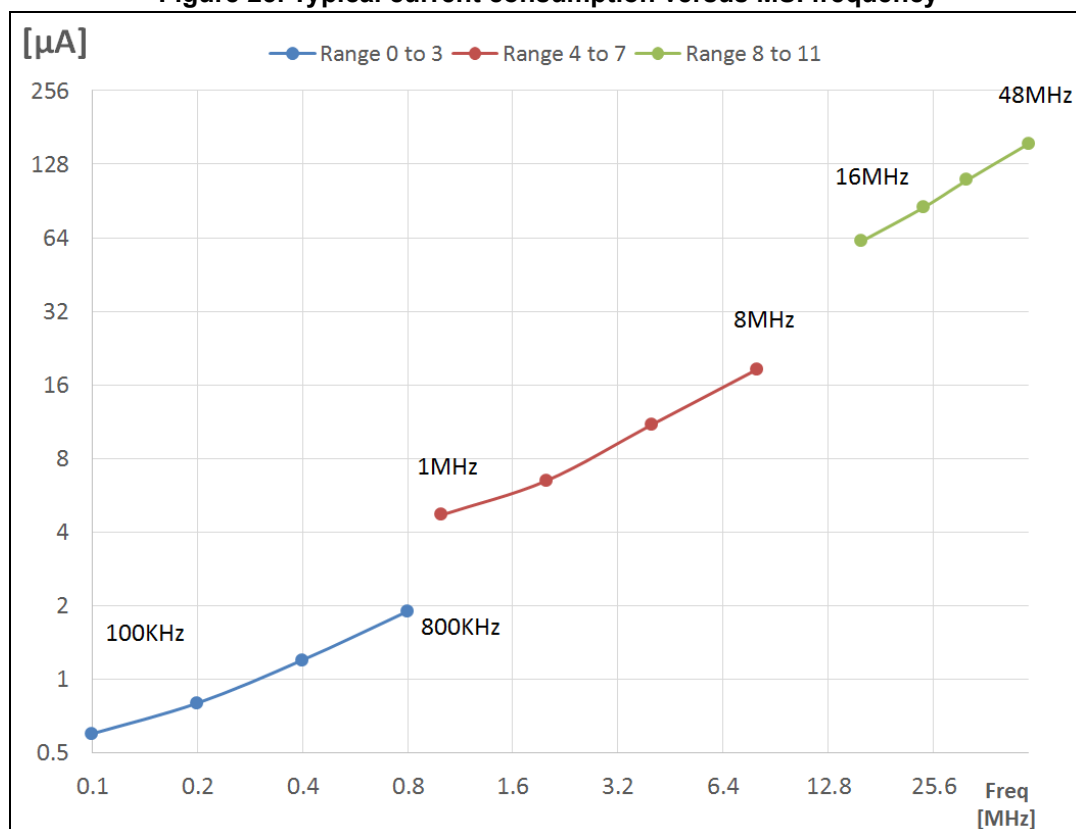
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta V_{DD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	$V_{DD}=1.62$ V to 3.6 V	-1.2	-	0.5	%
				$V_{DD}=2.4$ V to 3.6 V	-0.5	-		
			Range 4 to 7	$V_{DD}=1.62$ V to 3.6 V	-2.5	-	0.7	
				$V_{DD}=2.4$ V to 3.6 V	-0.8	-		
			Range 8 to 11	$V_{DD}=1.62$ V to 3.6 V	-5	-	1	
				$V_{DD}=2.4$ V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode ⁽³⁾	MSI mode	$T_A = -40$ to 85 °C		-	1	2	%
			$T_A = -40$ to 125 °C		-	2	4	
P_USB Jitter(MSI) ⁽⁶⁾	Period jitter for USB clock ⁽⁴⁾	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI) ⁽⁶⁾	Medium term jitter for USB clock ⁽⁵⁾	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI) ⁽⁶⁾	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI) ⁽⁶⁾	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 48. MSI oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD}(MSI)^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1
			Range 1	-	-	0.8	1.2
			Range 2	-	-	1.2	1.7
			Range 3	-	-	1.9	2.5
			Range 4	-	-	4.7	6
			Range 5	-	-	6.5	9
			Range 6	-	-	11	15
			Range 7	-	-	18.5	25
			Range 8	-	-	62	80
			Range 9	-	-	85	110
			Range 10	-	-	110	130
			Range 11	-	-	155	190

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.
5. Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.
For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.
For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Figure 25. Typical current consumption versus MSI frequency



High-speed internal 48 MHz (HSI48) RC oscillator

Table 49. HSI48 oscillator characteristics⁽¹⁾

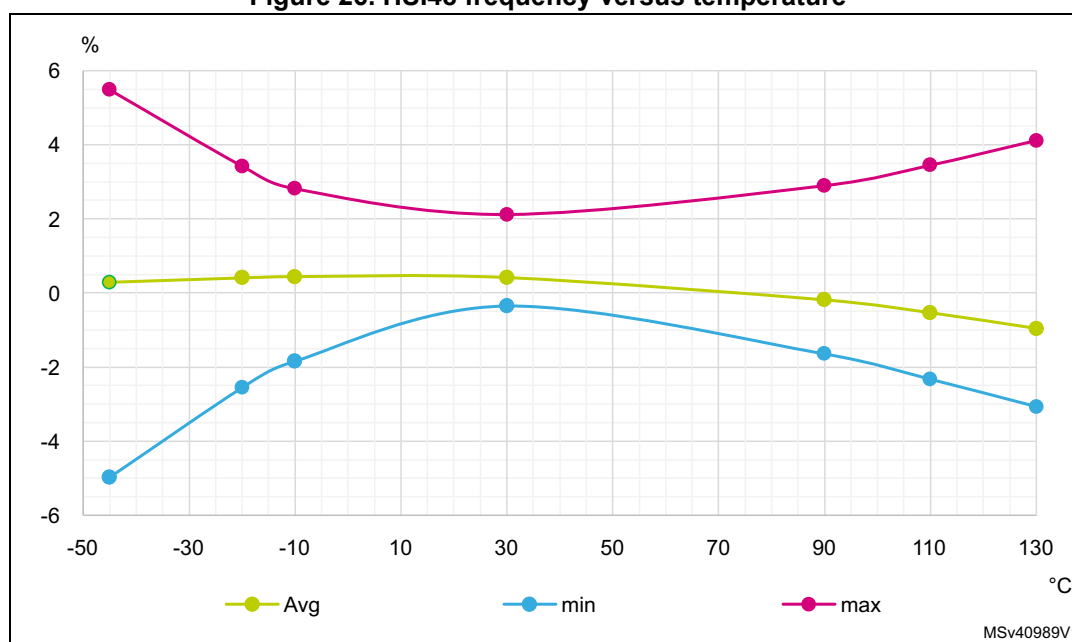
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	$V_{\text{DD}}=3.0\text{V}$, $T_{\text{A}}=30^{\circ}\text{C}$	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11 ⁽²⁾	0.18 ⁽²⁾	%
USER TRIM COVERAGE	HSI48 user trimming coverage	± 32 steps	± 3 ⁽³⁾	± 3.5 ⁽³⁾	-	%
DuCy(HSI48)	Duty Cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
$\text{ACC}_{\text{HSI48_REL}}$	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	$V_{\text{DD}} = 3.0\text{ V to } 3.6\text{ V}$, $T_{\text{A}} = -15\text{ to } 85^{\circ}\text{C}$	-	-	± 3 ⁽³⁾	%
		$V_{\text{DD}} = 1.65\text{ V to } 3.6\text{ V}$, $T_{\text{A}} = -40\text{ to } 125^{\circ}\text{C}$	-	-	± 4.5 ⁽³⁾	
$\text{D}_{\text{VDD}}(\text{HSI48})$	HSI48 oscillator frequency drift with V_{DD}	$V_{\text{DD}} = 3\text{ V to } 3.6\text{ V}$	-	0.025 ⁽³⁾	0.05 ⁽³⁾	%
		$V_{\text{DD}} = 1.65\text{ V to } 3.6\text{ V}$	-	0.05 ⁽³⁾	0.1 ⁽³⁾	
$t_{\text{su}}(\text{HSI48})$	HSI48 oscillator start-up time	-	-	2.5 ⁽²⁾	6 ⁽²⁾	μs
$I_{\text{DD}}(\text{HSI48})$	HSI48 oscillator power consumption	-	-	340 ⁽²⁾	380 ⁽²⁾	μA

Table 49. HSI48 oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _T jitter	Next transition jitter Accumulated jitter on 28 cycles ⁽⁴⁾	-	-	+/-0.15 ⁽²⁾	-	ns
P _T jitter	Paired transition jitter Accumulated jitter on 56 cycles ⁽⁴⁾	-	-	+/-0.25 ⁽²⁾	-	ns

1. V_{DD} = 3 V, T_A = -40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 26. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 50. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	LSI Frequency	V _{DD} = 3.0 V, T _A = 30 °C	31.04	-	32.96	kHz
		V _{DD} = 1.62 to 3.6 V, T _A = -40 to 125 °C	29.5	-	34	
t _{SU} (LSI) ⁽²⁾	LSI oscillator start-up time	-	-	80	130	μs
t _{STAB} (LSI) ⁽²⁾	LSI oscillator stabilization time	5% of final frequency	-	125	180	μs
I _{DD} (LSI) ⁽²⁾	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in [Table 51](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 51. PLL, PLLSAI1 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽²⁾	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.0968	-	80	MHz
		Voltage scaling Range 2	3.0968	-	26	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	μs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	$\pm ps$
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on V_{DD} ⁽¹⁾	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 2 PLLs.

6.3.10 Flash memory characteristics

Table 52. Flash memory characteristics⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	μs
$t_{\text{prog_row}}$	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
$t_{\text{prog_page}}$	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
$t_{\text{prog_bank}}$	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 μs)	-	
		Erase mode	7 (for 41 μs)	-	

1. Guaranteed by design.

Table 53. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N_{END}	Endurance	$T_{\text{A}} = -40$ to $+105$ °C	10	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_{\text{A}} = 85$ °C	30	Years
		1 kcycle ⁽²⁾ at $T_{\text{A}} = 105$ °C	15	
		1 kcycle ⁽²⁾ at $T_{\text{A}} = 125$ °C	7	
		10 kcycles ⁽²⁾ at $T_{\text{A}} = 55$ °C	30	
		10 kcycles ⁽²⁾ at $T_{\text{A}} = 85$ °C	15	
		10 kcycles ⁽²⁾ at $T_{\text{A}} = 105$ °C	10	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 54](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 80\text{ MHz}$, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 80\text{ MHz}$, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{HSE}/f_{HCLK}]$	Unit
				8 MHz/ 80 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.6\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-8	dB μ V
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	5	
			1 GHz to 2 GHz	8	
			EMI Level	2.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts $\times$ (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^{\circ}\text{C}$, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ }^{\circ}\text{C}$, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 57. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 58](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 58. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5, PE8, PE9, PE10, PE11, PE12	-5	N/A ⁽²⁾	mA
	Injected current on PE8, PE9, PE10, PE11, PE12	-0	N/A ⁽²⁾	
	Injected current on PA4, PA5 pins	-5	0	

1. Guaranteed by characterization results.

2. Injection is not possible.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the conditions summarized in [Table 21: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant.

Table 59. I/O static characteristics

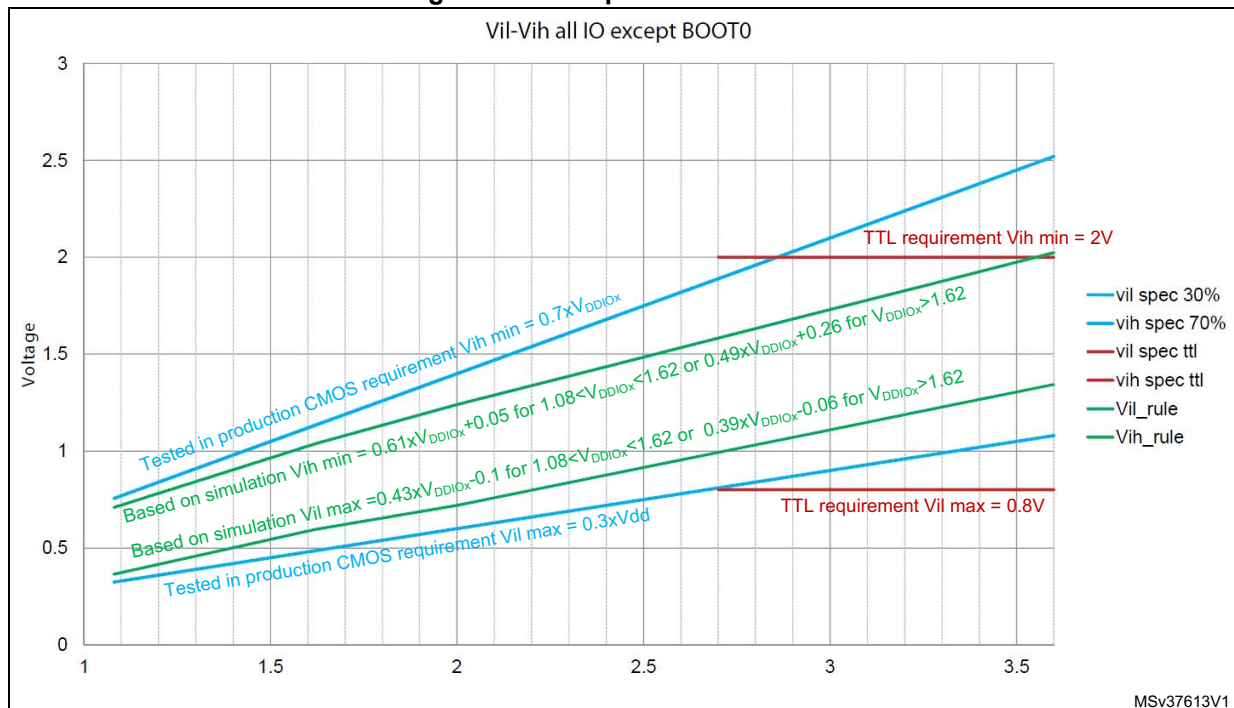
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}^{(1)}$	I/O input low level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	-	$0.3 \times V_{DDIOx}^{(2)}$	V
	I/O input low level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	-	$0.39 \times V_{DDIOx} - 0.06^{(3)}$	
	I/O input low level voltage	$1.08\text{ V} < V_{DDIOx} < 1.62\text{ V}$	-	-	$0.43 \times V_{DDIOx} - 0.1^{(3)}$	
$V_{IH}^{(1)}$	I/O input high level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	$0.7 \times V_{DDIOx}^{(2)}$	-	-	V
	I/O input high level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	$0.49 \times V_{DDIOx} + 0.26^{(3)}$	-	-	
	I/O input high level voltage	$1.08\text{ V} < V_{DDIOx} < 1.62\text{ V}$	$0.61 \times V_{DDIOx} + 0.05^{(3)}$	-	-	
$V_{hys}^{(3)}$	TT_xx, FT_XXX and NRST I/O input hysteresis	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	200	-	mV
$I_{lkg}^{(4)}$	FT_xx input leakage current ⁽³⁾⁽⁵⁾	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(6)(7)}$	-	-	± 100	nA
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1\text{ V}^{(6)(7)}$	-	-	650	
		$\text{Max}(V_{DDXXX}) + 1\text{ V} < V_{IN} \leq 5.5\text{ V}^{(6)(7)}$	-	-	200	
	FT_u and PC3 I/Os	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(6)(7)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1\text{ V}^{(6)(7)}$	-	-	$2500^{(3)}$	
		$\text{Max}(V_{DDXXX}) + 1\text{ V} < V_{IN} \leq 5.5\text{ V}^{(6)(7)}$	-	-	250	
	TT_xx input leakage current	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(6)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} < 3.6\text{ V}^{(6)}$	-	-	$2000^{(3)}$	
R_{PU}	Weak pull-up equivalent resistor ⁽⁸⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor ⁽⁸⁾	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to [Figure 27: I/O input characteristics](#).
2. Tested in production.
3. Guaranteed by design.
4. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:

$$I_{\text{Total_leak_max}} = 10 \mu\text{A} + [\text{number of IOs where } V_{\text{IN}} \text{ is applied on the pad}] \times I_{\text{kg}}(\text{Max}).$$
5. All FT_xx GPIOs except FT_u and PC3 I/Os.
6. $\text{Max}(V_{\text{DDXXX}})$ is the maximum value of all the I/O supplies.
7. To sustain a voltage higher than $\text{Min}(V_{\text{DD}}, V_{\text{DDA}}, V_{\text{DDUSB}}, V_{\text{LCD}}) + 0.3 \text{ V}$, the internal Pull-up and Pull-Down resistors must be disabled.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 27](#) for standard I/Os, and in [Figure 27](#) for 5 V tolerant I/Os.

Figure 27. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to $\pm 8 \text{ mA}$, and sink or source up to $\pm 20 \text{ mA}$ (with a relaxed $V_{\text{OL}}/V_{\text{OH}}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 18: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 18: Voltage characteristics](#)).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 60. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.45	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.45$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	$0.35 \times V_{DDIOx}$	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$0.65 \times V_{DDIOx}$	-	
$V_{OLFM+}^{(3)}$	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
		$ I_{IO} = 10 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.4	
		$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 18: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 28](#) and [Table 61](#), respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 61. I/O AC characteristics⁽¹⁾⁽²⁾

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	5	MHz
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	1	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	0.1	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	10	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	1.5	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	25	ns
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	52	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	140	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	17	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	37	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	25	MHz
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	10	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	1	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	50	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	15	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	9	ns
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	16	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	40	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	4.5	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	9	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	21	

Table 61. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

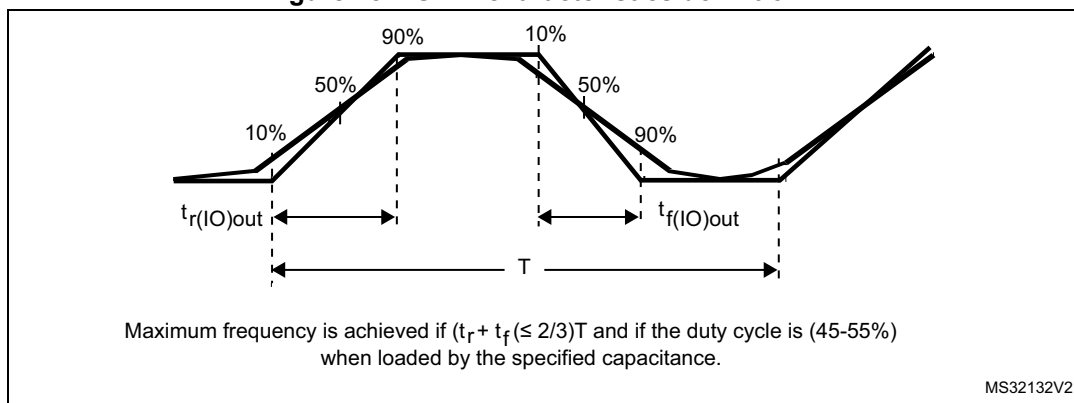
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	50	MHz
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	25	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	5	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	100 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	37.5	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	5.8	ns
			C=50 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	11	
			C=50 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	28	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	5	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	120 ⁽³⁾	MHz
			C=30 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	50	
			C=30 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	10	
			C=10 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	180 ⁽³⁾	
			C=10 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	75	
			C=10 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V _{DDIOx} ≤ 3.6 V	-	3.3	ns
			C=30 pF, 1.62 V ≤ V _{DDIOx} ≤ 2.7 V	-	6	
			C=30 pF, 1.08 V ≤ V _{DDIOx} ≤ 1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V ≤ V _{DDIOx} ≤ 3.6 V	-	1	MHz
	Tf	Output fall time ⁽⁴⁾		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0394 reference manual for a description of GPIO Port configuration register.

2. Guaranteed by design.

3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.

4. The fall time is defined between 70% and 30% of the output waveform accordingly to I²C specification.

Figure 28. I/O AC characteristics definition⁽¹⁾

1. Refer to [Table 61: I/O AC characteristics](#).

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

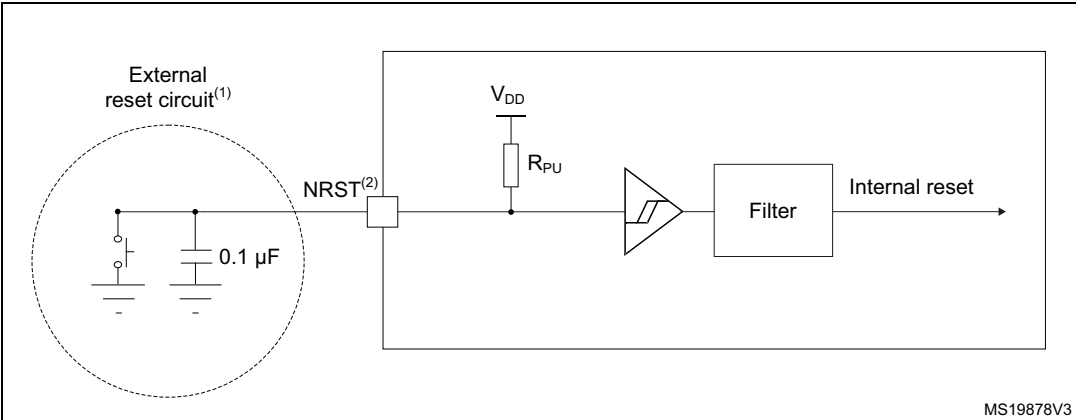
Table 62. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_F(NRST)$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	350	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 29. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 62: NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 63. EXTI Input Characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.17 Analog switches booster

Table 64. Analog switches booster characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for $1.62\text{ V} \leq V_{DD} \leq 2.0\text{ V}$	-	-	250	µA
	Booster consumption for $2.0\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	-	-	500	
	Booster consumption for $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	900	

1. Guaranteed by design.

6.3.18 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in [Table 65](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 21: General operating conditions](#).

Note: It is recommended to perform a calibration after each power-up.

Table 65. ADC characteristics^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
$V_{\text{REF}+}$	Positive reference voltage	$V_{\text{DDA}} \geq 2 \text{ V}$	2	-	V_{DDA}	V
		$V_{\text{DDA}} < 2 \text{ V}$	V_{DDA}			V
$V_{\text{REF}-}$	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	80	MHz
		Range 2	0.14	-	26	
f_{s}	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	MSPS
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	$f_{\text{ADC}} = 80 \text{ MHz}$ Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{\text{ADC}}$
V_{CMIN}	Input common mode	Differential mode	$(V_{\text{REF}+} + V_{\text{REF}-})/2 - 0.18$	$(V_{\text{REF}+} + V_{\text{REF}-})/2$	$(V_{\text{REF}+} + V_{\text{REF}-})/2 + 0.18$	V
$V_{\text{AIN}}^{(3)}$	Conversion voltage range ⁽²⁾	-	0	-	$V_{\text{REF}+}$	V
R_{AIN}	External input impedance	-	-	-	50	k Ω
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	$f_{\text{ADC}} = 80 \text{ MHz}$	1.45			μs
		-	116			$1/f_{\text{ADC}}$

Table 65. ADC characteristics^{(1) (2)} (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	$f_{ADC} = 80 \text{ MHz}$	0.03125	-	8.00625	μs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 80 \text{ MHz}$ Resolution = 12 bits	0.1875	-	8.1625	μs
		Resolution = 12 bits	$t_s + 12.5$ cycles for successive approximation = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	$f_s = 5 \text{ Msps}$	-	730	830	μA
		$f_s = 1 \text{ Msps}$	-	160	220	
		$f_s = 10 \text{ ksps}$	-	16	50	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	$f_s = 5 \text{ Msps}$	-	130	160	μA
		$f_s = 1 \text{ Msps}$	-	30	40	
		$f_s = 10 \text{ ksps}$	-	0.6	2	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	$f_s = 5 \text{ Msps}$	-	260	310	μA
		$f_s = 1 \text{ Msps}$	-	60	70	
		$f_s = 10 \text{ ksps}$	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4 \text{ V}$). It is disable when $V_{DDA} \geq 2.4 \text{ V}$.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package. Refer to [Section 4: Pinouts and pin description](#) for further details.

The maximum value of R_{AIN} can be found in [Table 66: Maximum ADC RAIN](#).

Table 66. Maximum ADC $R_{AIN}^{(1)(2)}$

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels ⁽³⁾	Slow channels ⁽⁴⁾
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.

2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 67. ADC accuracy - limited test conditions 1⁽¹⁾(2)(3)

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	5	LSB
			Slow channel (max speed)	-	4	5	
		Differential	Fast channel (max speed)	-	3.5	4.5	
			Slow channel (max speed)	-	3.5	4.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	2.5	
			Slow channel (max speed)	-	1	2.5	
		Differential	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	4.5	
			Slow channel (max speed)	-	2.5	4.5	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
		Differential	Fast channel (max speed)	-	1	2	
			Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.4	10.5	-	bits
			Slow channel (max speed)	10.4	10.5	-	
		Differential	Fast channel (max speed)	10.8	10.9	-	
			Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	64.4	65	-	dB
			Slow channel (max speed)	64.4	65	-	
		Differential	Fast channel (max speed)	66.8	67.4	-	
			Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
		Differential	Fast channel (max speed)	67	68	-	
			Slow channel (max speed)	67	68	-	

Table 67. ADC accuracy - limited test conditions 1⁽¹⁾(2)(3) (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency $\leq$ 80 MHz, Sampling rate $\leq$ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, $T_A = 25$ °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 68. ADC accuracy - limited test conditions 2⁽¹⁾(2)(3)

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	6.5	LSB
			Slow channel (max speed)	-	4	6.5	
		Differential	Fast channel (max speed)	-	3.5	5.5	
			Slow channel (max speed)	-	3.5	5.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	4.5	
			Slow channel (max speed)	-	1	5	
		Differential	Fast channel (max speed)	-	1.5	3	
			Slow channel (max speed)	-	1.5	3	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	6	
			Slow channel (max speed)	-	2.5	6	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	3.5	
			Slow channel (max speed)	-	1.5	3.5	
		Differential	Fast channel (max speed)	-	1	3	
			Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10	10.5	-	bits
			Slow channel (max speed)	10	10.5	-	
		Differential	Fast channel (max speed)	10.7	10.9	-	
			Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	62	65	-	dB
			Slow channel (max speed)	62	65	-	
		Differential	Fast channel (max speed)	66	67.4	-	
			Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	64	66	-	
			Slow channel (max speed)	64	66	-	
		Differential	Fast channel (max speed)	66.5	68	-	
			Slow channel (max speed)	66.5	68	-	

Table 68. ADC accuracy - limited test conditions 2⁽¹⁾(2)(3) (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency $\leq$ 80 MHz, Sampling rate $\leq$ 5.33 Msps, $2\text{ V} \leq V_{DDA}$	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{ V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$. No oversampling.

Table 69. ADC accuracy - limited test conditions 3⁽¹⁾⁽²⁾⁽³⁾

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
			Slow channel (max speed)	-	4.5	6.5	
		Differential	Fast channel (max speed)	-	4.5	7.5	
			Slow channel (max speed)	-	4.5	5.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	2	5	
			Slow channel (max speed)	-	2.5	5	
		Differential	Fast channel (max speed)	-	2	3.5	
			Slow channel (max speed)	-	2.5	3	
EG	Gain error	Single ended	Fast channel (max speed)	-	4.5	7	
			Slow channel (max speed)	-	3.5	6	
		Differential	Fast channel (max speed)	-	3.5	4	
			Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1.2	1.5	
			Slow channel (max speed)	-	1.2	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	3	3.5	
			Slow channel (max speed)	-	2.5	3.5	
		Differential	Fast channel (max speed)	-	2	2.5	
			Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10	10.4	-	bits
			Slow channel (max speed)	10	10.4	-	
		Differential	Fast channel (max speed)	10.6	10.7	-	
			Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	62	64	-	dB
			Slow channel (max speed)	62	64	-	
		Differential	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	63	65	-	
			Slow channel (max speed)	63	65	-	
		Differential	Fast channel (max speed)	66	67	-	
			Slow channel (max speed)	66	67	-	

Table 69. ADC accuracy - limited test conditions 3⁽¹⁾(2)(3) (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency $\leq$ 80 MHz, Sampling rate $\leq$ 5.33 Msps, $1.65\text{ V} \leq V_{\text{DDA}} = V_{\text{REF+}} \leq 3.6\text{ V}$, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{\text{DDA}} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{\text{DDA}} < 2.4\text{ V}$). It is disable when $V_{\text{DDA}} \geq 2.4\text{ V}$. No oversampling.

Table 70. ADC accuracy - limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	5	5.4	LSB
			Slow channel (max speed)	-	4	5	
		Differential	Fast channel (max speed)	-	4	5	
			Slow channel (max speed)	-	3.5	4.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	2	4	
			Slow channel (max speed)	-	2	4	
		Differential	Fast channel (max speed)	-	2	3.5	
			Slow channel (max speed)	-	2	3.5	
EG	Gain error	Single ended	Fast channel (max speed)	-	4	4.5	
			Slow channel (max speed)	-	4	4.5	
		Differential	Fast channel (max speed)	-	3	4	
			Slow channel (max speed)	-	3	4	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	2.5	3	
			Slow channel (max speed)	-	2.5	3	
		Differential	Fast channel (max speed)	-	2	2.5	
			Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.2	10.5	-	bits
			Slow channel (max speed)	10.2	10.5	-	
		Differential	Fast channel (max speed)	10.6	10.7	-	
			Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	63	65	-	dB
			Slow channel (max speed)	63	65	-	
		Differential	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	64	65	-	
			Slow channel (max speed)	64	65	-	
		Differential	Fast channel (max speed)	66	67	-	
			Slow channel (max speed)	66	67	-	

Table 70. ADC accuracy - limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾ (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V _{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
		Differential	Fast channel (max speed)	-	-73	-72		
			Slow channel (max speed)	-	-73	-72		

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
- The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{ V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$. No oversampling.

Figure 30. ADC accuracy characteristics

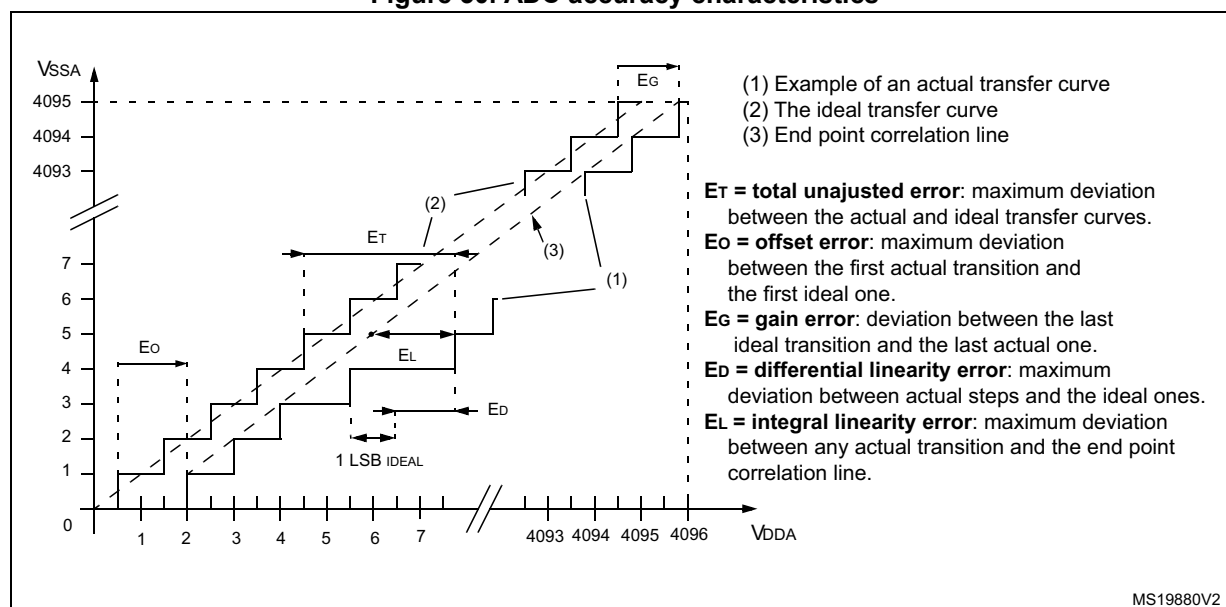
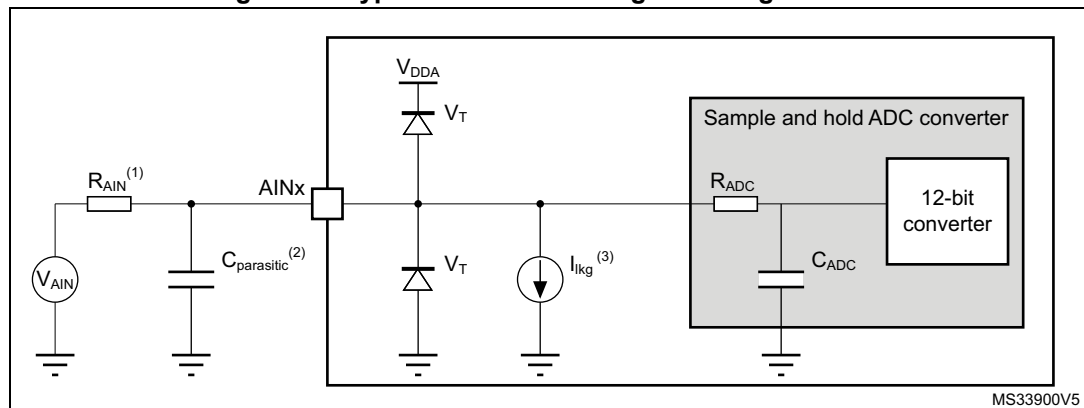


Figure 31. Typical connection diagram using the ADC



1. Refer to [Table 65: ADC characteristics](#) for the values of R_{AIN} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to [Table 59: I/O static characteristics](#) for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to [Table 59: I/O static characteristics](#) for the values of I_{lkg} .

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 17: Power supply scheme](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.19 Digital-to-Analog converter characteristics

Table 71. DAC characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	3.6	V
		Other modes		1.80	-		
$V_{\text{REF+}}$	Positive reference voltage	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
$V_{\text{REF-}}$	Negative reference voltage	-		V_{SSA}			
R_{L}	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	k Ω
			connected to V_{DDA}	25	-	-	
R_{O}	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	k Ω
R_{BON}	Output impedance sample and hold mode, output buffer ON	$V_{\text{DD}} = 2.7\text{ V}$		-	-	2	k Ω
		$V_{\text{DD}} = 2.0\text{ V}$		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	$V_{\text{DD}} = 2.7\text{ V}$		-	-	16.5	k Ω
		$V_{\text{DD}} = 2.0\text{ V}$		-	-	18.0	
C_{L}	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	μF
$V_{\text{DAC_OUT}}$	Voltage on DAC1_OUTx output	DAC output buffer ON		0.2	-	$V_{\text{REF+}} - 0.2$	V
		DAC output buffer OFF		0	-	$V_{\text{REF+}}$	
t_{SETTLING}	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC1_OUTx reaches final value $\pm 0.5\text{ LSB}$, $\pm 1\text{ LSB}$, $\pm 2\text{ LSB}$, $\pm 4\text{ LSB}$, $\pm 8\text{ LSB}$)	Normal mode DAC output buffer ON $CL \leq 50\text{ pF}$, $RL \geq 5\text{ k}\Omega$	$\pm 0.5\text{ LSB}$	-	1.7	3	μs
			$\pm 1\text{ LSB}$	-	1.6	2.9	
			$\pm 2\text{ LSB}$	-	1.55	2.85	
			$\pm 4\text{ LSB}$	-	1.48	2.8	
			$\pm 8\text{ LSB}$	-	1.4	2.75	
		Normal mode DAC output buffer OFF, $\pm 1\text{ LSB}$, $CL = 10\text{ pF}$		-	2	2.5	
$t_{\text{WAKEUP}}^{(2)}$	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value $\pm 1\text{ LSB}$	Normal mode DAC output buffer ON $CL \leq 50\text{ pF}$, $RL \geq 5\text{ k}\Omega$		-	4.2	7.5	μs
		Normal mode DAC output buffer OFF, $CL \leq 10\text{ pF}$		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON $CL \leq 50\text{ pF}$, $RL = 5\text{ k}\Omega$, DC		-	-80	-28	dB

Table 71. DAC characteristics⁽¹⁾ (continued)

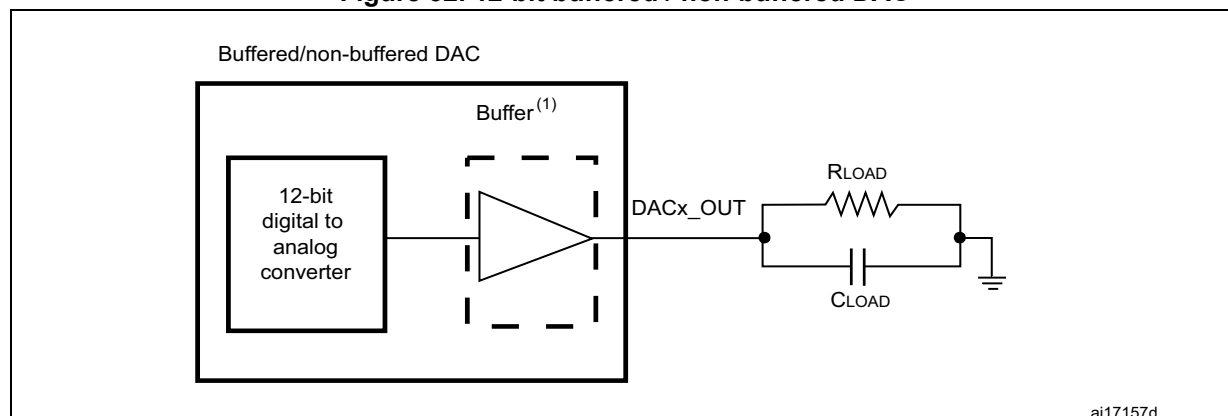
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC1_OUTx for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	μs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DAC1_OUTx reaches final value ±1LSB)	DAC1_OUTx pin connected	DAC output buffer ON, C _{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C _{SH} = 100 nF	-	10.5	18	
		DAC1_OUTx pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	μs
I_{leak}	Output leakage current	Sample and hold mode, DAC1_OUTx pin connected		-	-	_(3)	nA
C_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	μs
V_{offset}	Middle code offset for 1 trim code step	$V_{REF+} = 3.6\text{ V}$		-	1500	-	μV
		$V_{REF+} = 1.8\text{ V}$		-	750	-	
$I_{DDA(DAC)}$	DAC consumption from V _{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	μA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C _{SH} = 100 nF		-	315 × Ton/(Ton + Toff) (4)	670 × Ton/(Ton + Toff) (4)	

Table 71. DAC characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDV}(DAC)$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	μA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, $C_{SH} = 100$ nF, worst case		-	$185 \times \frac{T_{on}}{T_{on} + T_{off}}$ (4)	$400 \times \frac{T_{on}}{T_{on} + T_{off}}$ (4)	
		Sample and hold mode, buffer OFF, $C_{SH} = 100$ nF, worst case		-	$155 \times \frac{T_{on}}{T_{on} + T_{off}}$ (4)	$205 \times \frac{T_{on}}{T_{on} + T_{off}}$ (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to [Table 59: I/O static characteristics](#).
4. T_{on} is the Refresh phase duration. T_{off} is the Hold phase duration. Refer to RM0394 reference manual for more details.

Figure 32. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 72. DAC accuracy⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity ⁽²⁾	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity ⁽³⁾	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800 ⁽³⁾	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V _{REF+} = 3.6 V	-	-	±12	
			V _{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001 ⁽⁴⁾	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V _{REF+} = 3.6 V	-	-	±5	
			V _{REF+} = 1.8 V	-	-	±7	
Gain	Gain error ⁽⁵⁾	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 72. DAC accuracy⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFFF when buffer is OFF, and from code giving 0.2 V and ($V_{REF+} - 0.2$) V when buffer is ON.

6.3.20 Voltage reference buffer characteristics

Table 73. VREFBUF characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046 ⁽³⁾	2.048	2.049 ⁽³⁾	
			$V_{RS} = 1$	2.498 ⁽³⁾	2.5	2.502 ⁽³⁾	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
			$V_{RS} = 1$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	± 0.05	± 0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	μF
esr	Equivalent Serial Resistor of Cloud	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	$2.8 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	$I_{load} = 500 \mu\text{A}$	-	200	1000	ppm/V
			$I_{load} = 4 \text{ mA}$	-	100	500	
I_{load_reg}	Load regulation	$500 \mu\text{A} \leq I_{load} \leq 4 \text{ mA}$	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	$-40 \text{ }^\circ\text{C} < T_J < +125 \text{ }^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	ppm/ $^\circ\text{C}$
		$0 \text{ }^\circ\text{C} < T_J < +50 \text{ }^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	$CL = 0.5 \mu\text{F}^{(4)}$		-	300	350	μs
		$CL = 1.1 \mu\text{F}^{(4)}$		-	500	650	
		$CL = 1.5 \mu\text{F}^{(4)}$		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase ⁽⁵⁾	-	-	-	8	-	mA

Table 73. VREFBUF characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA}(VREFBUF)$	VREFBUF consumption from V_{DDA}	$I_{load} = 0 \mu A$	-	16	25	μA
		$I_{load} = 500 \mu A$	-	18	30	
		$I_{load} = 4 mA$	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for $V_{RS} = 0$ and $V_{RS} = 1$.

6.3.21 Comparator characteristics

Table 74. COMP characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V _{IN}	Comparator input voltage range	-		0	-	V _{DDA}	
V _{BG} ⁽²⁾	Scaler input voltage	-		V _{REFINT}			
V _{SC}	Scaler offset voltage	-		-	±5	±10	mV
I _{DDA} (SCALER)	Scaler static consumption from V _{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t _{START_SCALER}	Scaler startup time	-		-	100	200	µs
t _{START}	Comparator startup time to reach propagation delay specification	High-speed mode	V _{DDA} ≥ 2.7 V	-	-	5	µs
			V _{DDA} < 2.7 V	-	-	7	
		Medium mode	V _{DDA} ≥ 2.7 V	-	-	15	
			V _{DDA} < 2.7 V	-	-	25	
		Ultra-low-power mode		-	-	40	
t _D ⁽³⁾	Propagation delay with 100 mV overdrive	High-speed mode	V _{DDA} ≥ 2.7 V	-	55	80	ns
			V _{DDA} < 2.7 V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V _{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V _{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 74. COMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA}(COMP)$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ± 100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	μA
			With 50 kHz ± 100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ± 100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	_(4)	nA

1. Guaranteed by design, unless otherwise specified.

2. Refer to [Table 24: Embedded internal voltage reference](#).

3. Guaranteed by characterization results.

4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in [Table 59: I/O static characteristics](#).

6.3.22 Operational amplifiers characteristics

Table 75. OPAMP characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage ⁽²⁾	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
$V_{I\text{OFFSET}}$	Input offset voltage	25 °C, No Load on output.	-	-	± 1.5	mV
		All voltage/Temp.	-	-	± 3	
$\Delta V_{I\text{OFFSET}}$	Input offset voltage drift	Normal mode	-	± 5	-	$\mu V/^{\circ}C$
		Low-power mode	-	± 10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1 \times V_{DDA}$)	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9 \times V_{DDA}$)	-	-	1	1.35	

Table 75. OPAMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I _{LOAD}	Drive current	Normal mode	V _{DDA} ≥ 2 V	-	-	500	μA
		Low-power mode		-	-	100	
I _{LOAD_PGA}	Drive current in PGA mode	Normal mode	V _{DDA} ≥ 2 V	-	-	450	
		Low-power mode		-	-	50	
R _{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	V _{DDA} < 2 V	4	-	-	kΩ
		Low-power mode		20	-	-	
R _{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to VDDA)	Normal mode	V _{DDA} < 2 V	4.5	-	-	
		Low-power mode		40	-	-	
C _{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	C _{LOAD} ≤ 50 pf, R _{LOAD} ≥ 4 kΩ DC	70	85	-	dB
		Low-power mode	C _{LOAD} ≤ 50 pf, R _{LOAD} ≥ 20 kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	V _{DDA} ≥ 2.4 V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	V _{DDA} < 2.4 V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR ⁽³⁾	Slew rate (from 10 and 90% of output voltage)	Normal mode	V _{DDA} ≥ 2.4 V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	V _{DDA} < 2.4 V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V _{OHSAT} ⁽³⁾	High saturation voltage	Normal mode	I _{load} = max or R _{load} = min Input at V _{DDA} .	V _{DDA} - 100	-	-	mV
		Low-power mode		V _{DDA} - 50	-	-	
V _{OLSAT} ⁽³⁾	Low saturation voltage	Normal mode	I _{load} = max or R _{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ _m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Table 75. OPAMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	$C_{\text{LOAD}} \leq 50 \text{ pf}$, $R_{\text{LOAD}} \geq 4 \text{ k}\Omega$ follower configuration	-	5	10	μs
		Low-power mode	$C_{\text{LOAD}} \leq 50 \text{ pf}$, $R_{\text{LOAD}} \geq 20 \text{ k}\Omega$ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input		-	-	-(4)	nA
PGA gain ⁽³⁾	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
R_{network}	R2/R1 internal resistance values in PGA mode ⁽⁵⁾	PGA Gain = 2		-	80/80	-	k Ω /k Ω
		PGA Gain = 4		-	120/40	-	
		PGA Gain = 8		-	140/20	-	
		PGA Gain = 16		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/2	-	MHz
		Gain = 4	-	-	GBW/4	-	
		Gain = 8	-	-	GBW/8	-	
		Gain = 16	-	-	GBW/16	-	

Table 75. OPAMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
e _n	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I _{DDA} (OPAMP) ⁽³⁾	OPAMP consumption from V _{DDA}	Normal mode	no Load, quiescent mode	-	120	260	μA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.
2. The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V
3. Guaranteed by characterization results.
4. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in [Table 59: I/O static characteristics](#).
5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain = 1+R2/R1

6.3.23 Temperature sensor characteristics

Table 76. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T _L ⁽¹⁾	V _{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope ⁽²⁾	Average slope	2.3	2.5	2.7	mV/°C
V ₃₀	Voltage at 30°C (±5 °C) ⁽³⁾	0.742	0.76	0.785	V
t _{START} (TS_BUF) ⁽¹⁾	Sensor Buffer Start-up time in continuous mode ⁽⁴⁾	-	8	15	μs
t _{START} ⁽¹⁾	Start-up time when entering in continuous mode ⁽⁴⁾	-	70	120	μs
t _{S_temp} ⁽¹⁾	ADC sampling time when reading the temperature	5	-	-	μs
I _{DD} (TS) ⁽¹⁾	Temperature sensor consumption from V _{DD} , when selected by ADC	-	4.7	7	μA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V₃₀ ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 7: Temperature sensor calibration values](#).
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} monitoring characteristics

Table 77. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	k Ω
Q	Ratio on V_{BAT} measurement	-	3	-	-
$E_r^{(1)}$	Error on Q	-10	-	10	%
$t_{S_vbat}^{(1)}$	ADC sampling time when reading the VBAT	12	-	-	μ s

1. Guaranteed by design.

Table 78. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	k Ω
		VBRS = 1	-	1.5	-	

6.3.25 LCD controller characteristics

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 79. LCD controller characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	μF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
$I_{LCD}^{(2)}$	Supply current from V_{DD} at $V_{DD} = 2.2 V$	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	μA
	Supply current from V_{DD} at $V_{DD} = 3.0 V$	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} ($V_{LCD} = 3 V$)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	μA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High Resistor value for Low drive resistive network		-	5.5	-	M Ω
R_{LN}	Total Low Resistor value for High drive resistive network		-	240	-	k Ω
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	$3/4 V_{LCD}$	-	
V_{23}	Segment/Common 2/3 level voltage		-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage		-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage		-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage		-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.
2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.

6.3.26 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 80. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	-	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 80 MHz	12.5	-	ns
f _{EXT}	Timer external clock frequency on CH1 to CH4	-	0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 80 MHz	0	40	MHz
Res _{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
t _{COUNTER}	16-bit counter clock period	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 80 MHz	0.0125	819.2	μs
t _{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	t _{TIMxCLK}
		f _{TIMxCLK} = 80 MHz	-	53.68	s

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 81. IWDG min/max timeout period at 32 kHz (LSI)⁽¹⁾

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 82. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	

6.3.27 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0394 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.14: I/O port characteristics](#) for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 83. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by design.
2. Spikes with widths below t_{AF(min)} are filtered.
3. Spikes with widths above t_{AF(max)} are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in [Table 84](#) for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in [Table 21: General operating conditions](#).

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 84. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_c(SCK)$	SPI clock frequency	Master mode receiver/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	-	40	MHz
		Master mode receiver/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			16	
		Master mode transmitter $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode receiver $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1			37 ⁽²⁾	
		Slave mode transmitter/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			20 ⁽²⁾	
		Voltage Range 2			13	
$t_{su}(NSS)$	NSS setup time	Slave mode, SPI prescaler = 2	$4 \times T_{PCLK}$	-	-	ns
$t_h(NSS)$	NSS hold time	Slave mode, SPI prescaler = 2	$2 \times T_{PCLK}$	-	-	ns
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master mode	$T_{PCLK}-2$	T_{PCLK}	$T_{PCLK}+2$	ns
$t_{su}(MI)$	Data input setup time	Master mode	4	-	-	ns
$t_{su}(SI)$		Slave mode	1.5	-	-	
$t_h(MI)$	Data input hold time	Master mode	6.5	-	-	ns
$t_h(SI)$		Slave mode	1.5	-	-	
$t_a(SO)$	Data output access time	Slave mode	9	-	36	ns
$t_{dis}(SO)$	Data output disable time	Slave mode	9	-	16	ns

Table 84. SPI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	13.5	ns
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	24	
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50 %.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

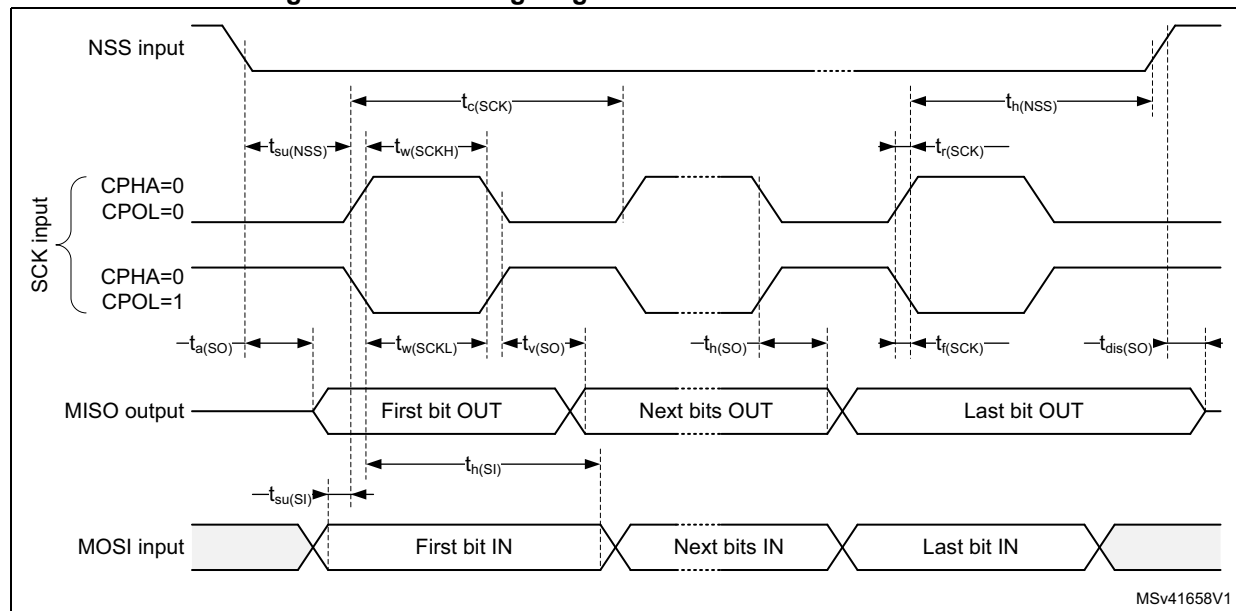
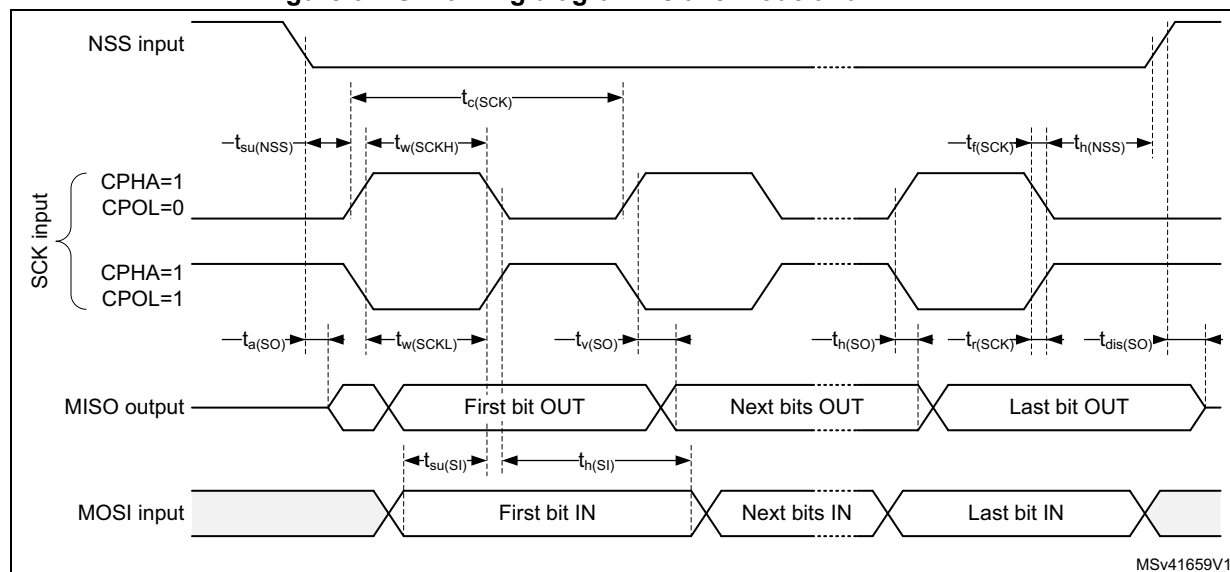
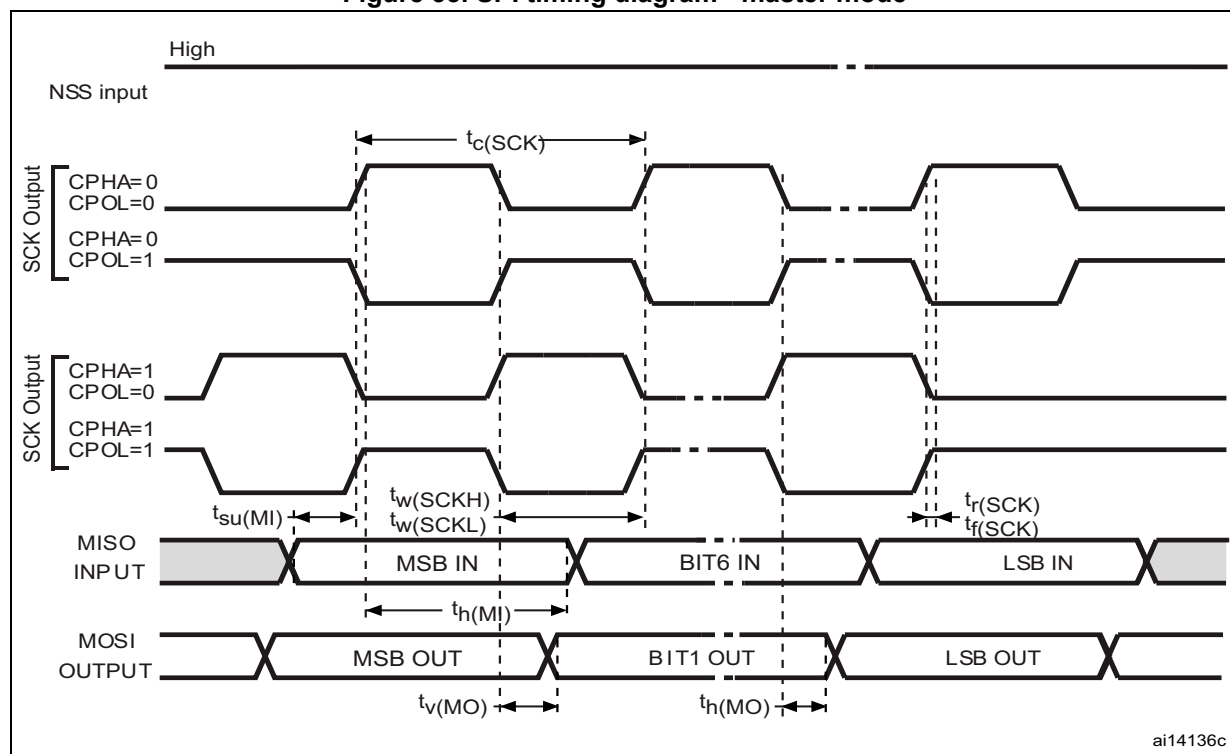


Figure 34. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Figure 35. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Quad SPI characteristics

Unless otherwise specified, the parameters given in [Table 85](#) and [Table 86](#) for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in [Table 21: General operating conditions](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load $C = 15$ or 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{\text{DD}}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

Table 85. Quad SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{\text{CK}}$	Quad SPI clock frequency	$1.71 < V_{\text{DD}} < 3.6 \text{ V}$, $C_{\text{LOAD}} = 20 \text{ pF}$ Voltage Range 1	-	-	40	MHz
		$1.71 < V_{\text{DD}} < 3.6 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$ Voltage Range 1	-	-	48	
		$2.7 < V_{\text{DD}} < 3.6 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$ Voltage Range 1	-	-	60	
		$1.71 < V_{\text{DD}} < 3.6 \text{ V}$, $C_{\text{LOAD}} = 20 \text{ pF}$ Voltage Range 2	-	-	26	
$t_{\text{w(CKH)}}$	Quad SPI clock high and low time	$f_{\text{AHBCLK}} = 48 \text{ MHz}$, $\text{presc} = 0$	$t_{\text{CK}}/2 - 2$	-	$t_{\text{CK}}/2$	ns
$t_{\text{w(CKL)}}$			$t_{\text{CK}}/2$	-	$t_{\text{CK}}/2 + 2$	
$t_{\text{s(IN)}}$	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
$t_{\text{h(IN)}}$	Data input hold time	Voltage Range 1	5	-	-	
		Voltage Range 2	6.5	-	-	
$t_{\text{v(OUT)}}$	Data output valid time	Voltage Range 1	-	1	5	
		Voltage Range 2	-	3	5	
$t_{\text{h(OUT)}}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Table 86. QUADSPI characteristics in DDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	$1.71 < V_{DD} < 3.6 \text{ V}$, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1	-	-	40	MHz
		$2 < V_{DD} < 3.6 \text{ V}$, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 1	-	-	48	
		$1.71 < V_{DD} < 3.6 \text{ V}$, $C_{LOAD} = 15 \text{ pF}$ Voltage Range 1	-	-	48	
		$1.71 < V_{DD} < 3.6 \text{ V}$, $C_{LOAD} = 20 \text{ pF}$ Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	$f_{AHBCLK} = 48 \text{ MHz}$, presc=0	$t_{(CK)}/2-2$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2+2$	
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1	1	-	-	
		Voltage Range 2	3.5	-	-	
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1	1	-	-	
		Voltage Range 2	1.5	-	-	
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1	6	-	-	
		Voltage Range 2	6.5	-	-	
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1	5.5	-	-	
		Voltage Range 2	5.5	-	-	
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	-	5	5.5	
		Voltage Range 2		9.5	14	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	-	5	8.5	
		Voltage Range 2		15	19	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	8	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	13	-	-	

1. Guaranteed by characterization results.

Figure 36. Quad SPI timing diagram - SDR mode

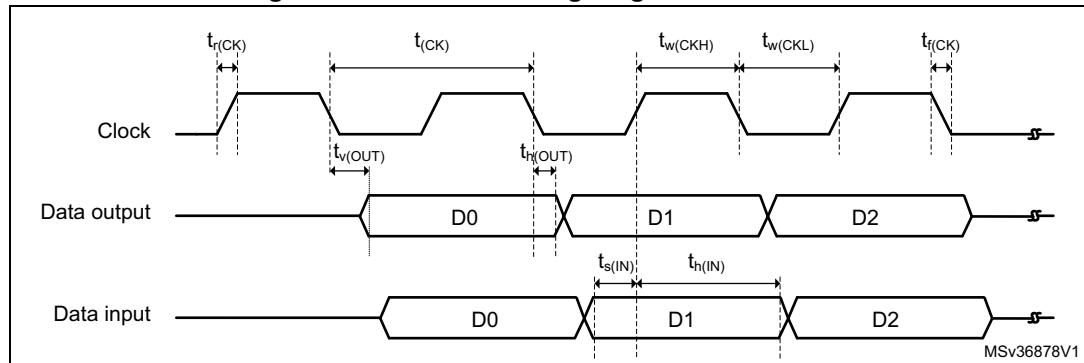
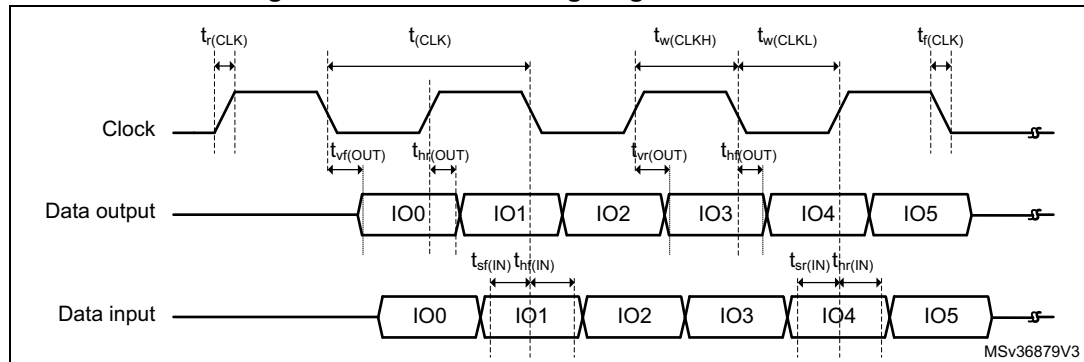


Figure 37. Quad SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in [Table 87](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 21: General operating conditions](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 87. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency ⁽²⁾	Master transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{V(FS)}$	FS valid time	Master mode $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Master mode $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	2	-	ns
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD_B_SR)}$		Slave receiver	2.5	-	

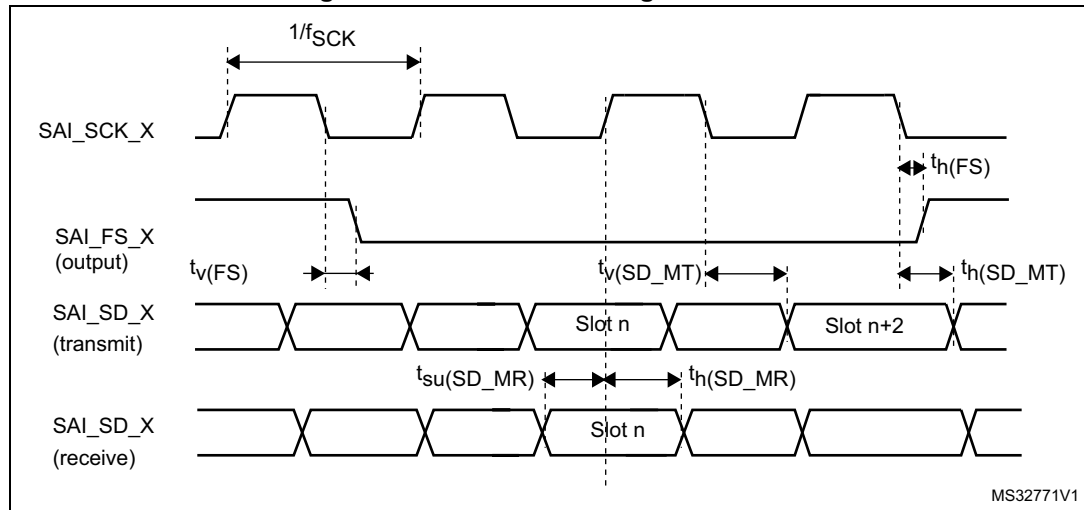
Table 87. SAI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{V(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Slave transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	34	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{V(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	27	ns
		Master transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.

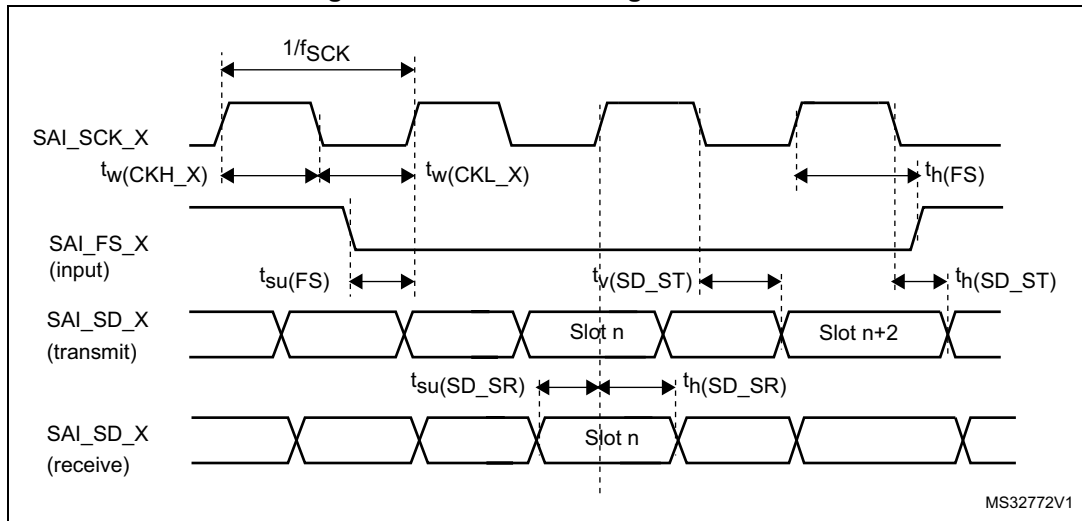
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 38. SAI master timing waveforms



MS32771V1

Figure 39. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in [Table 88](#) for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 21: General operating conditions](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output characteristics.

Table 88. SD / MMC dynamic characteristics, $V_{DD}=2.7$ V to 3.6 V⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	$f_{PP} = 50$ MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	$f_{PP} = 50$ MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	$f_{PP} = 50$ MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	$f_{PP} = 50$ MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	$f_{PP} = 50$ MHz	-	12	13	ns
t_{OH}	Output hold time HS	$f_{PP} = 50$ MHz	10	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	$f_{PP} = 50$ MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	$f_{PP} = 50$ MHz	3	-	-	ns

Table 88. SD / MMC dynamic characteristics, $V_{DD}=2.7\text{ V to }3.6\text{ V}^{(1)}$ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	$f_{PP} = 50\text{ MHz}$	-	2	3	ns
t_{OHD}	Output hold default time SD	$f_{PP} = 50\text{ MHz}$	0	-	-	ns

1. Guaranteed by characterization results.

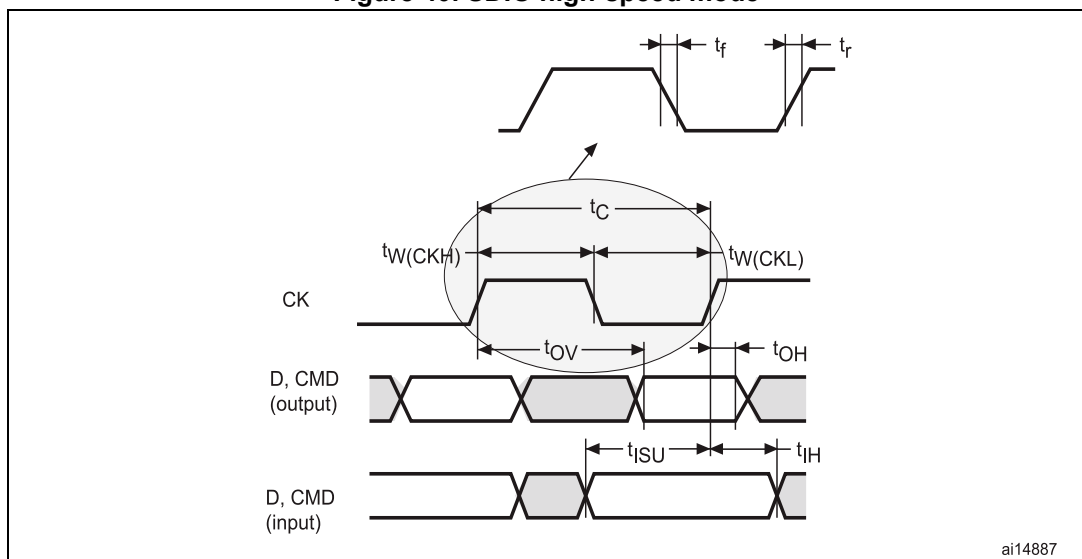
Table 89. eMMC dynamic characteristics, $V_{DD} = 1.71\text{ V to }1.9\text{ V}^{(1)(2)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/ f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	$f_{PP} = 50\text{ MHz}$	8	10	-	ns
$t_{W(CKH)}$	Clock high time	$f_{PP} = 50\text{ MHz}$	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	$f_{PP} = 50\text{ MHz}$	0	-	-	ns
t_{IH}	Input hold time HS	$f_{PP} = 50\text{ MHz}$	1.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	$f_{PP} = 50\text{ MHz}$	-	13.5	15	ns
t_{OH}	Output hold time HS	$f_{PP} = 50\text{ MHz}$	9	-	-	ns

1. Guaranteed by characterization results.

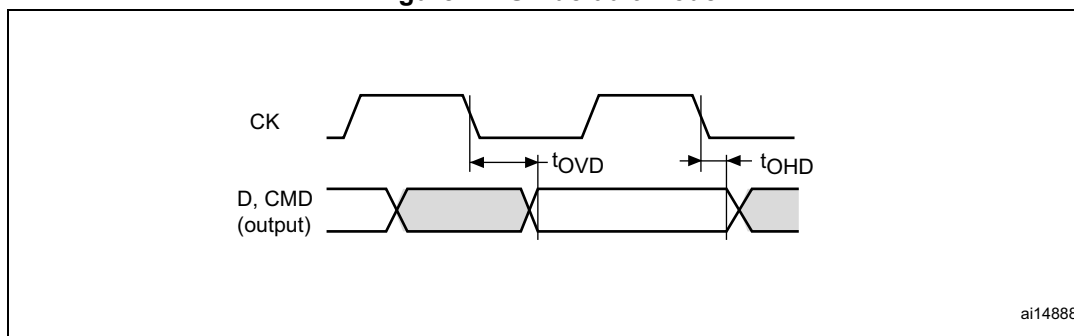
2. $C_{LOAD} = 20\text{ pF}$.

Figure 40. SDIO high-speed mode



ai14887

Figure 41. SD default mode



USB characteristics

The STM32L443xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 90. USB electrical characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage		3.0 ⁽²⁾	-	3.6	V
$T_{crystal_less}$	USB crystal less operation temperature		-15	-	85	°C
$t_{STARTUP}$ ⁽³⁾	USB transceiver startup time		-	-	1.0	μs
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception		1400	2300	3200	
Z_{DRV} ⁽³⁾	Output driver impedance ⁽⁴⁾	Driving high and low	28	36	44	Ω

1. T_A = -40 to 125 °C unless otherwise specified.

2. The STM32L443xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.

3. Guaranteed by design.

4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

SWPMI characteristics

The Single Wire Protocol Master Interface (SWPMI) and the associated SWPMI_IO transceiver are compliant with the ETSI TS 102 613 technical specification.

Table 91. SWPMI electrical characteristics

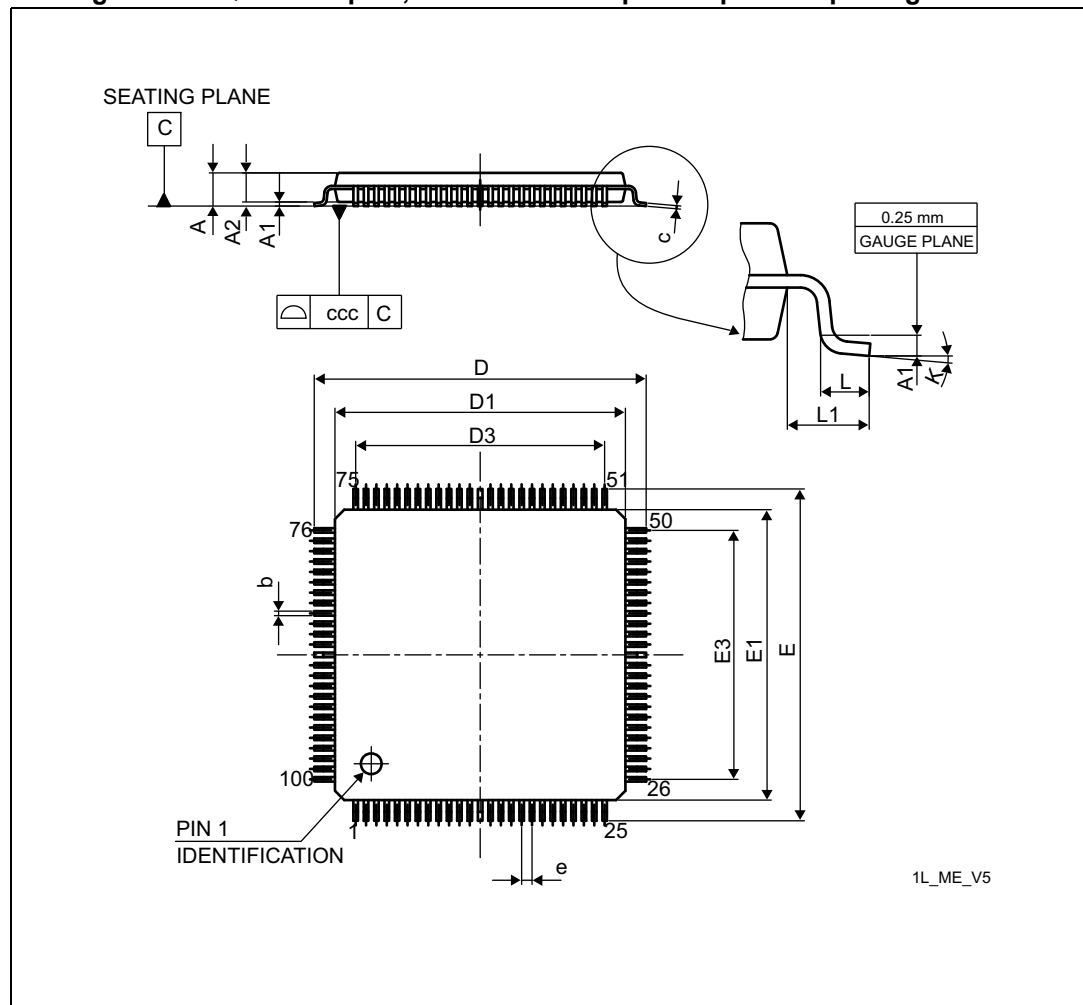
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SWPSTART}	SWPMI regulator startup time	SWP Class B $2.7\text{ V} \leq V_{\text{DD}} \leq 3.3\text{ V}$	-	-	300	μs
t_{SWPBIT}	SWP bit duration	V_{CORE} voltage range 1	500	-	-	ns
		V_{CORE} voltage range 2	620	-	-	

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 LQFP100 package information

Figure 42. LQFP - 100 pins, 14 x 14 mm low-profile quad flat package outline



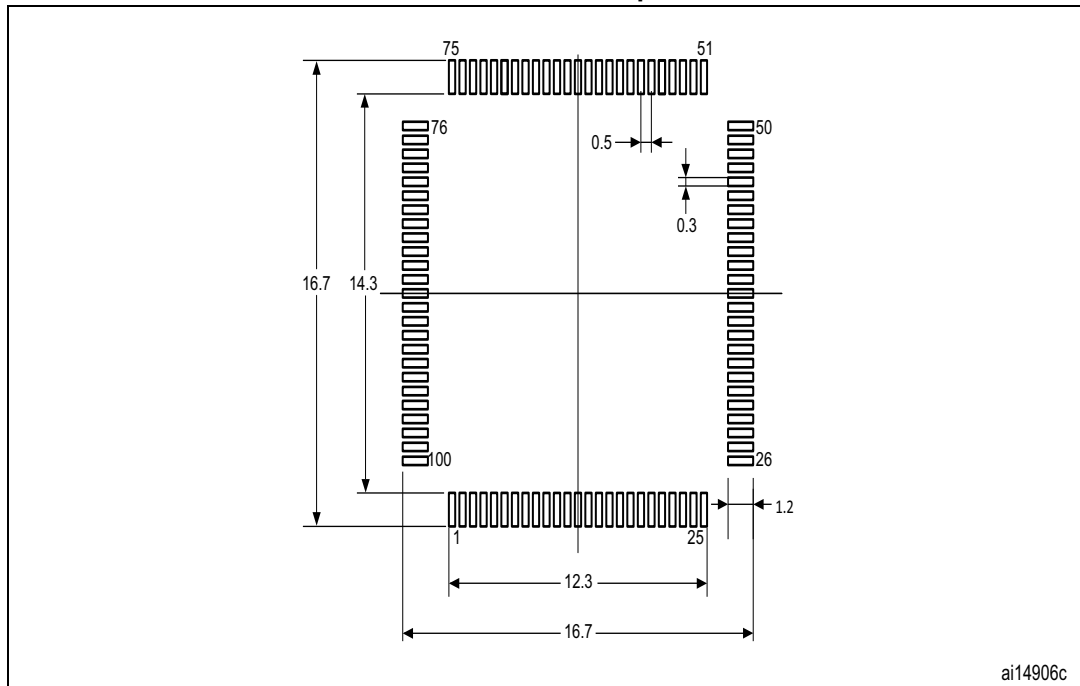
1. Drawing is not to scale.

**Table 92. LQFP - 100 pins, 14 x 14 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. LQFP - 100 pins, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

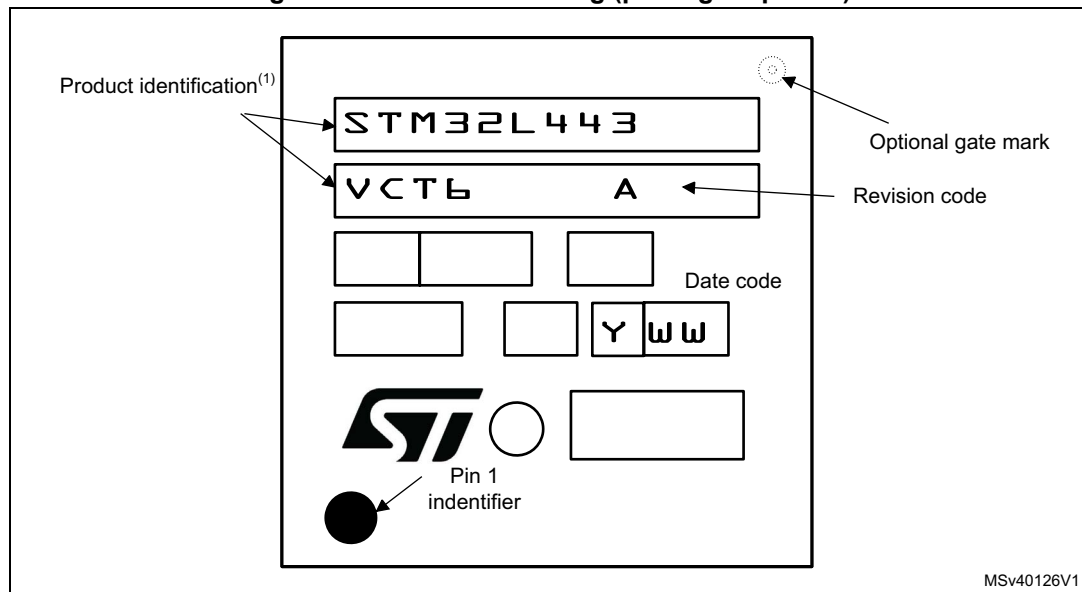
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

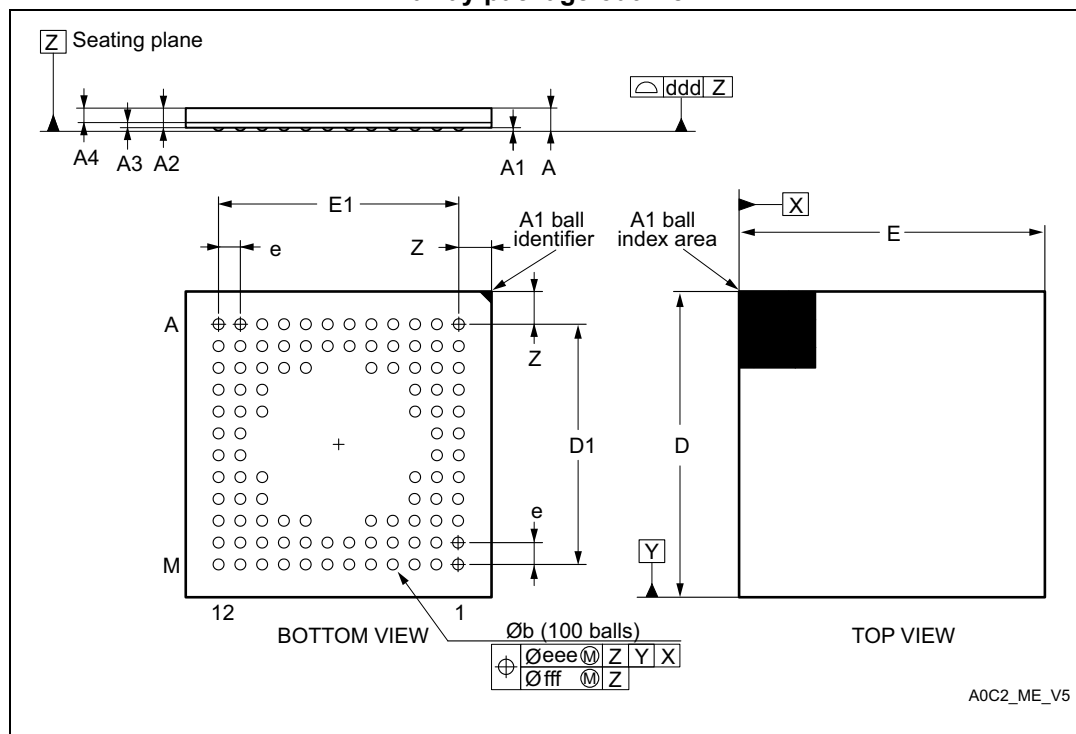
Figure 44. LQFP100 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 UFBGA100 package information

Figure 45. UFBGA - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 93. UFBGA - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

Table 93. UFBGA - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

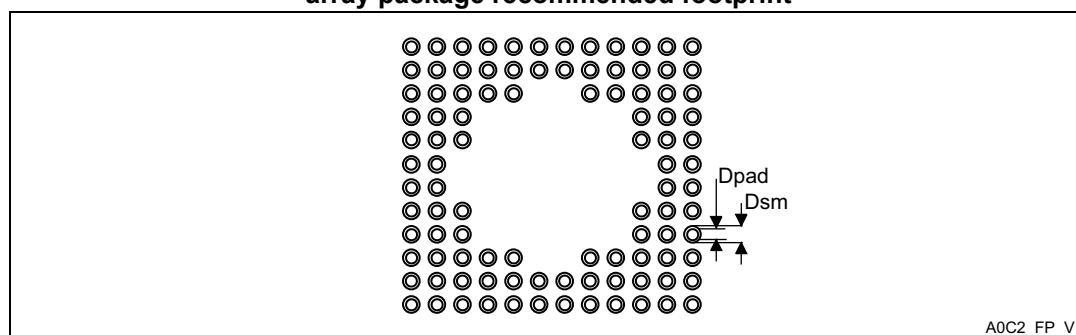


Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

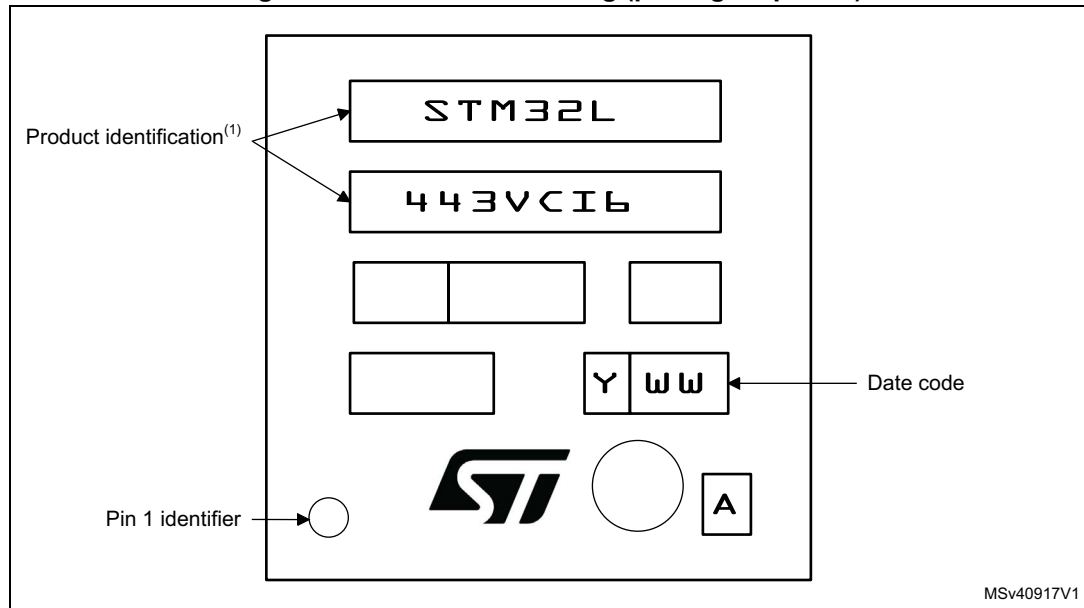
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

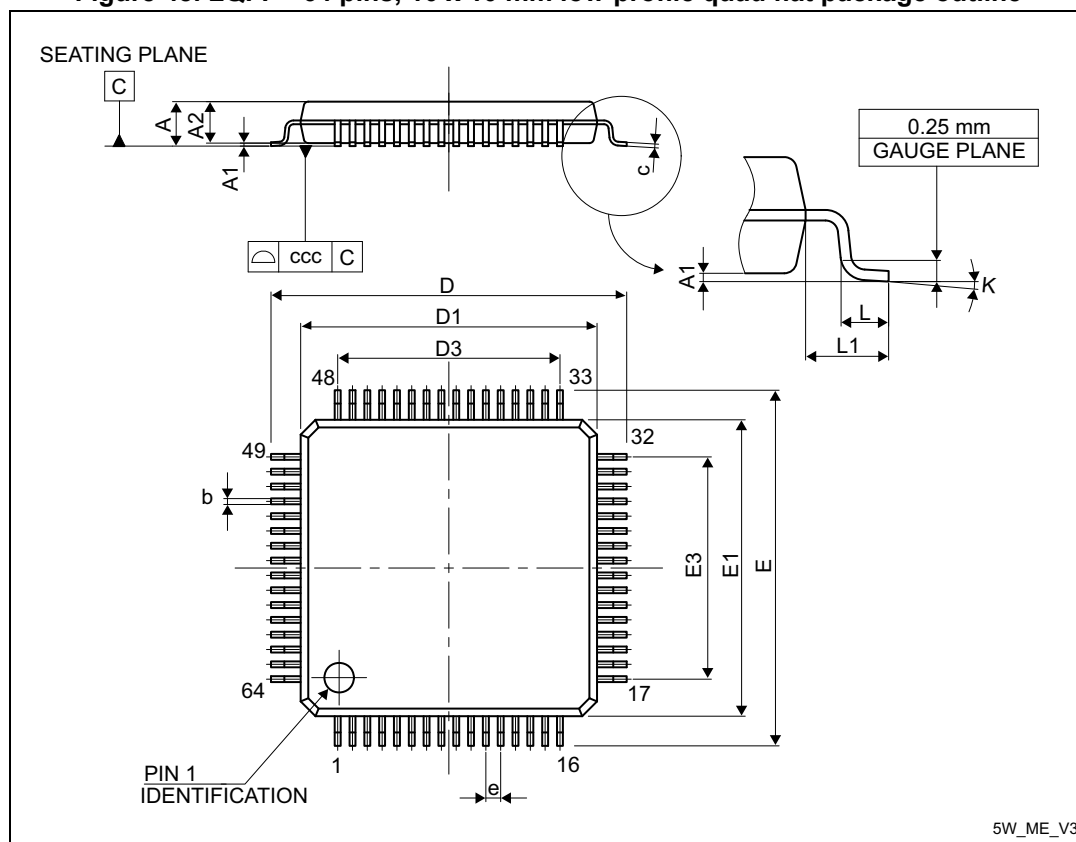
Figure 47. UFBGA100 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP64 package information

Figure 48. LQFP - 64 pins, 10 x 10 mm low-profile quad flat package outline



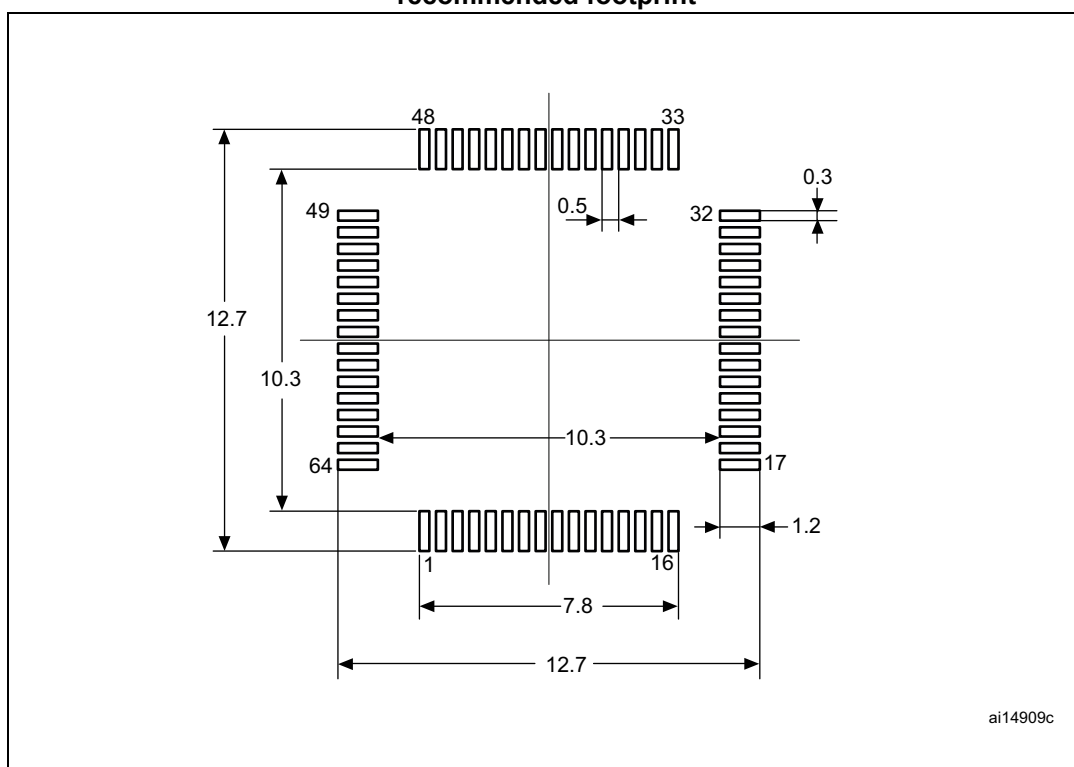
1. Drawing is not to scale.

Table 95. LQFP - 64 pins, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

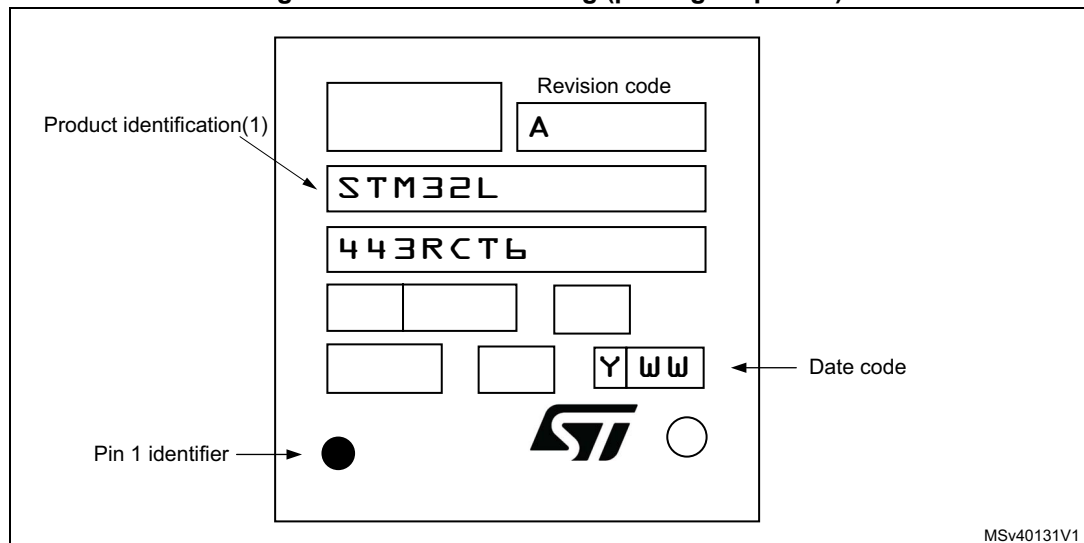
Figure 49. LQFP - 64 pins, 10 x 10 mm low-profile quad flat package recommended footprint



Device marking

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

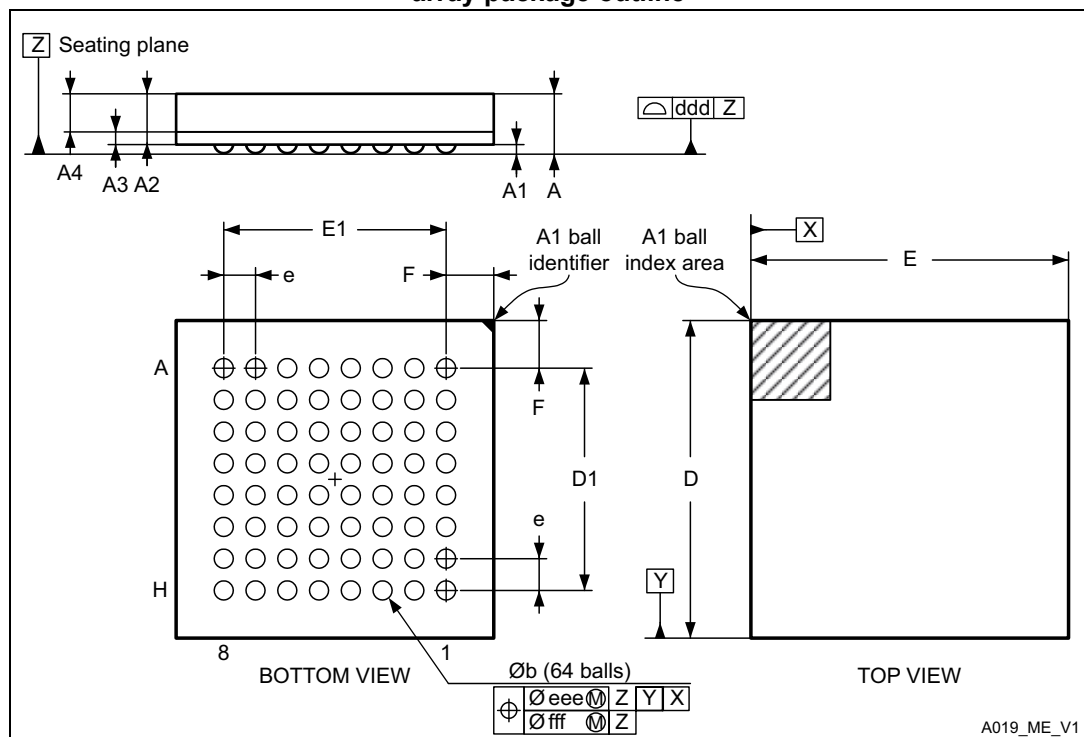
Figure 50. LQFP64 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 UFBGA64 package information

Figure 51. UFBGA – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 96. UFBGA – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

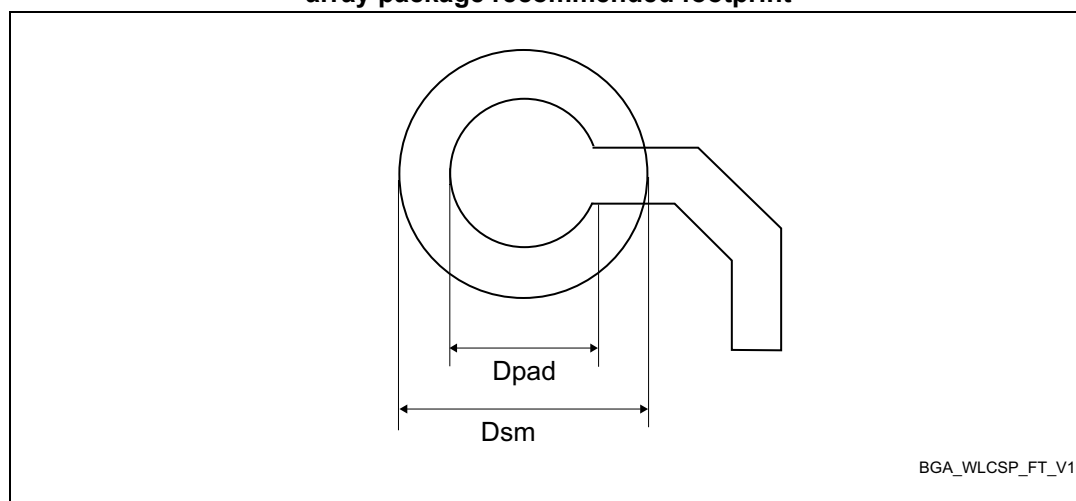
Figure 52. UFBGA64 – 64 balls, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

Table 97. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

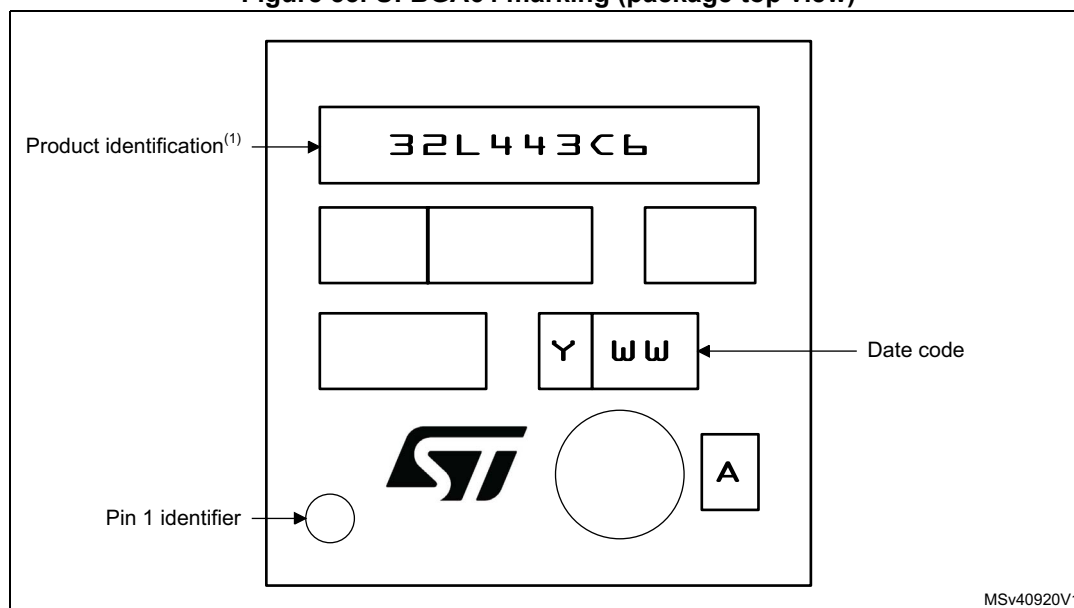
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

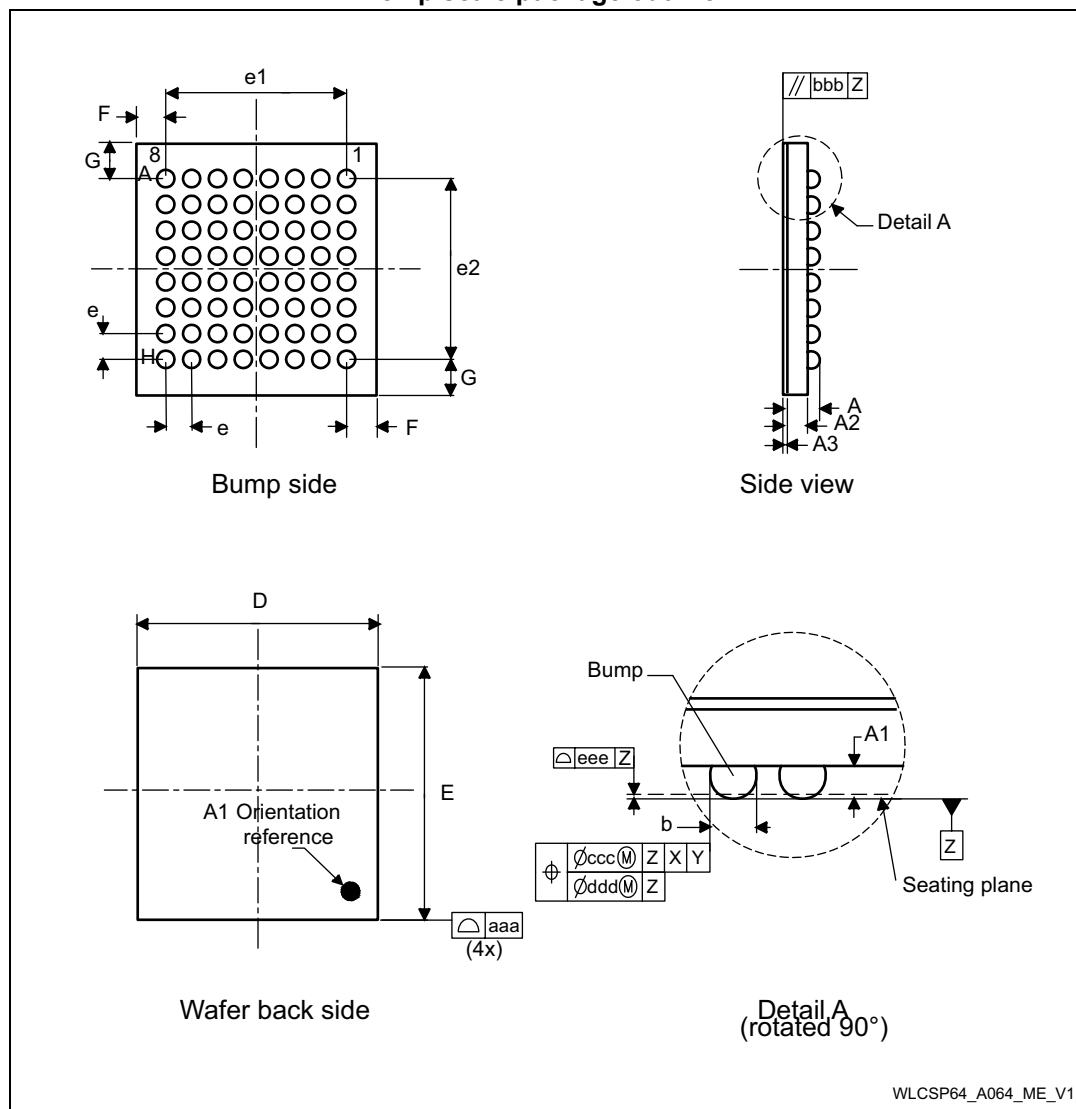
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 53. UFBGA64 marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 STANDARD WLCSP64 package information

Figure 54. STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

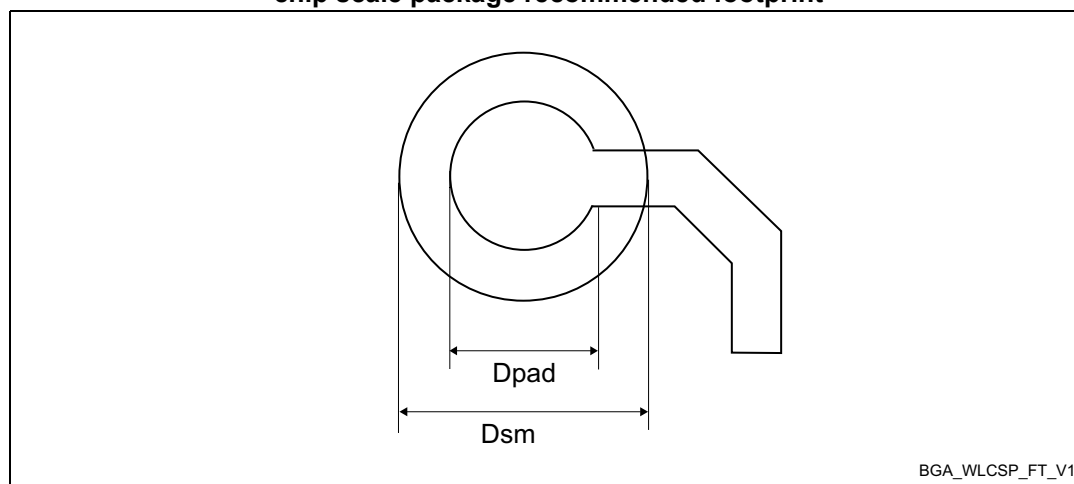
Table 98. STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.516	0.546	0.576	0.0203	0.0215	0.0227
A1	-	0.166	-	-	0.0065	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-

Table 98. STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
b ⁽³⁾	0.190	0.220	0.250	0.0075	0.0087	0.0098
D	3.106	3.141	3.176	0.1223	0.1237	0.1250
E	3.092	3.127	3.162	0.1217	0.1231	0.1245
e	-	0.350	-	-	0.0138	-
e1	-	2.450	-	-	0.0965	-
e2	-	2.450	-	-	0.0965	-
F	-	0.3455	-	-	0.0136	-
G	-	0.3385	-	-	0.0133	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 55. STANDARD WLCSP - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package recommended footprint

**Table 99. STANDARD WLCSP64 recommended PCB design rules
(0.35 mm pitch)**

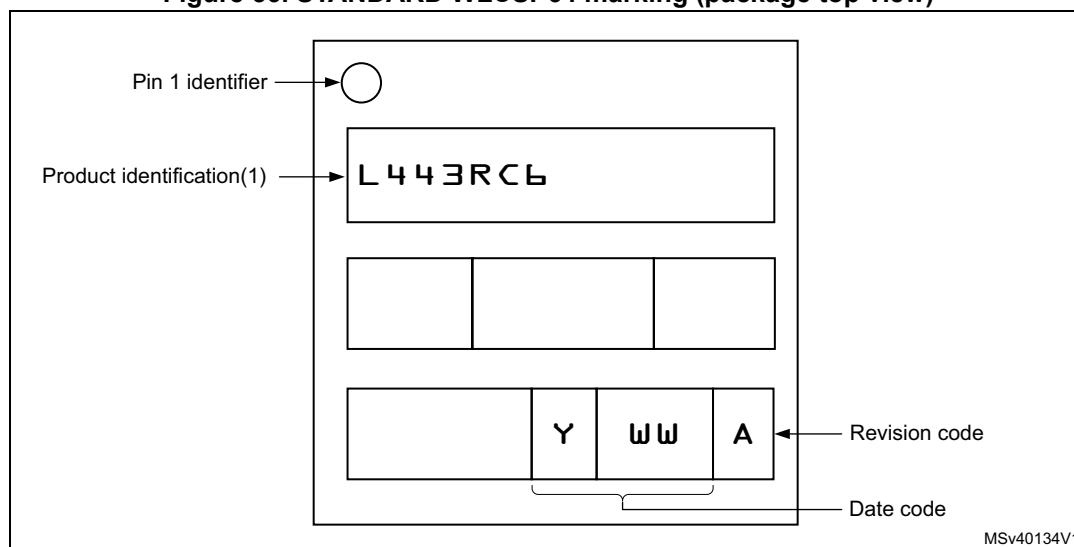
Dimension	Recommended values
Pitch	0.35 mm
Dpad	0.210 mm
Dsm	0.275 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.235 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

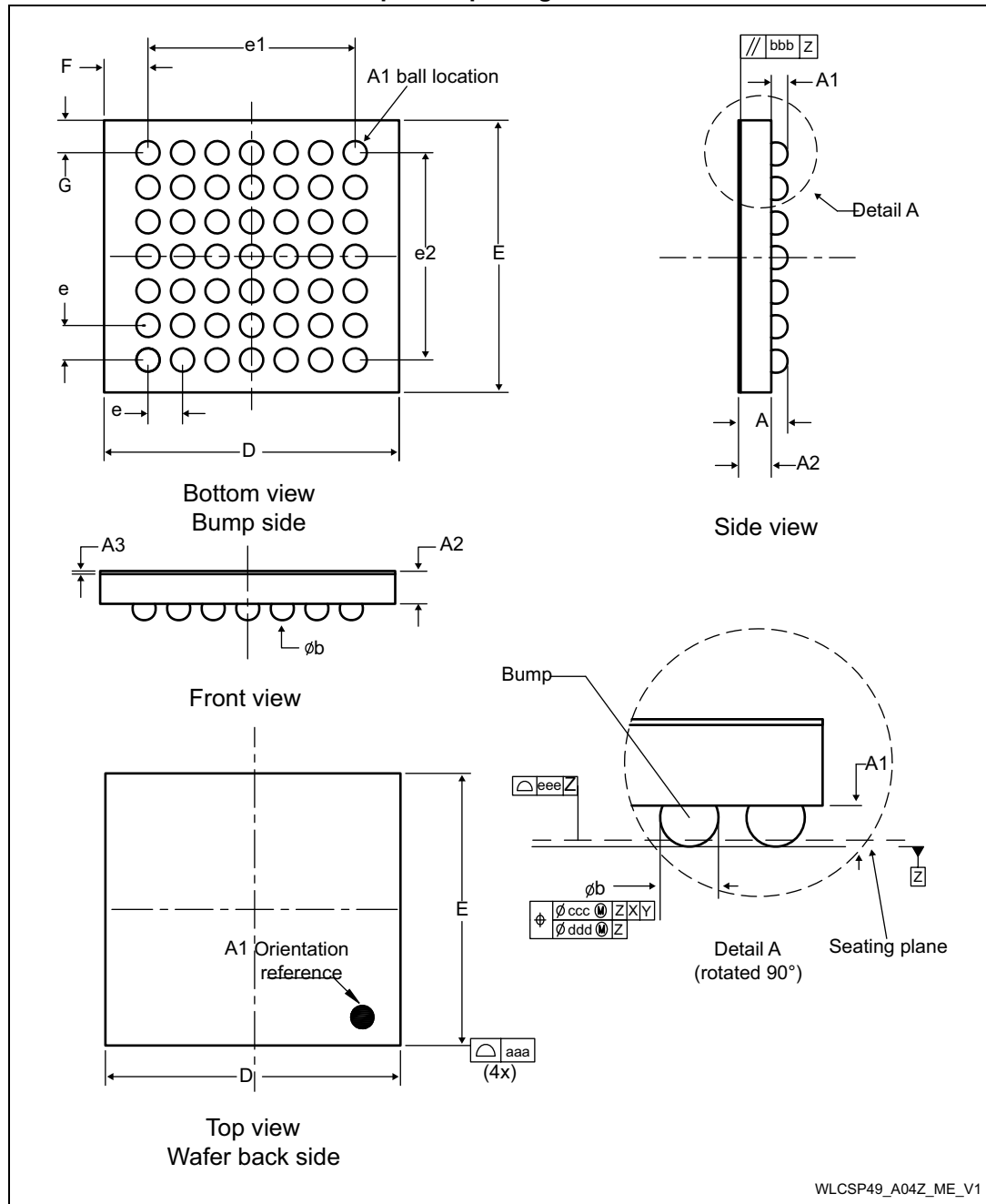
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. STANDARD WLCSP64 marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 STANDARD WLCSP49 package information

Figure 57. STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 100. STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.106	3.141	3.176	0.1223	0.1237	0.1250
E	3.092	3.127	3.162	0.1217	0.1231	0.1245
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.3705	-	-	0.0146	-
G	-	0.3635	-	-	0.0143	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

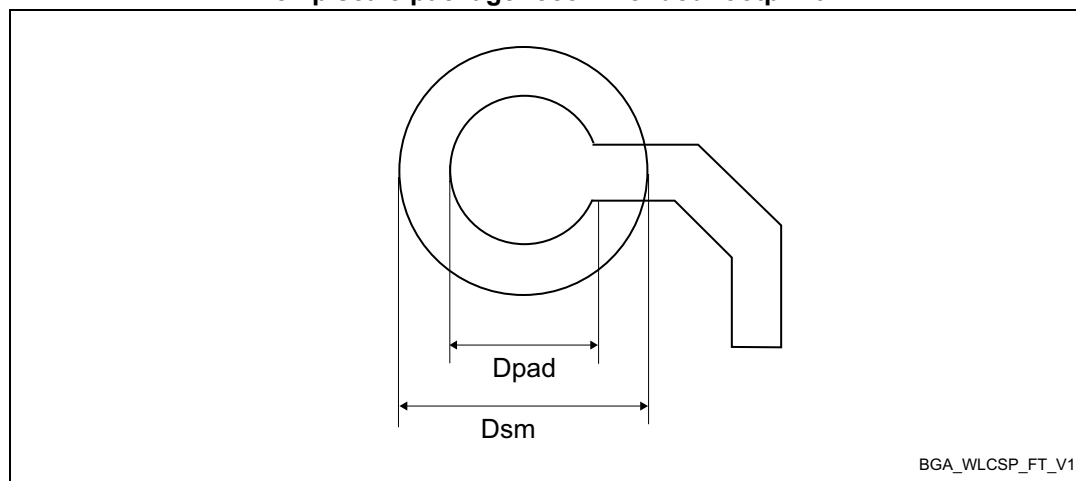
Figure 58. STANDARD WLCSP - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

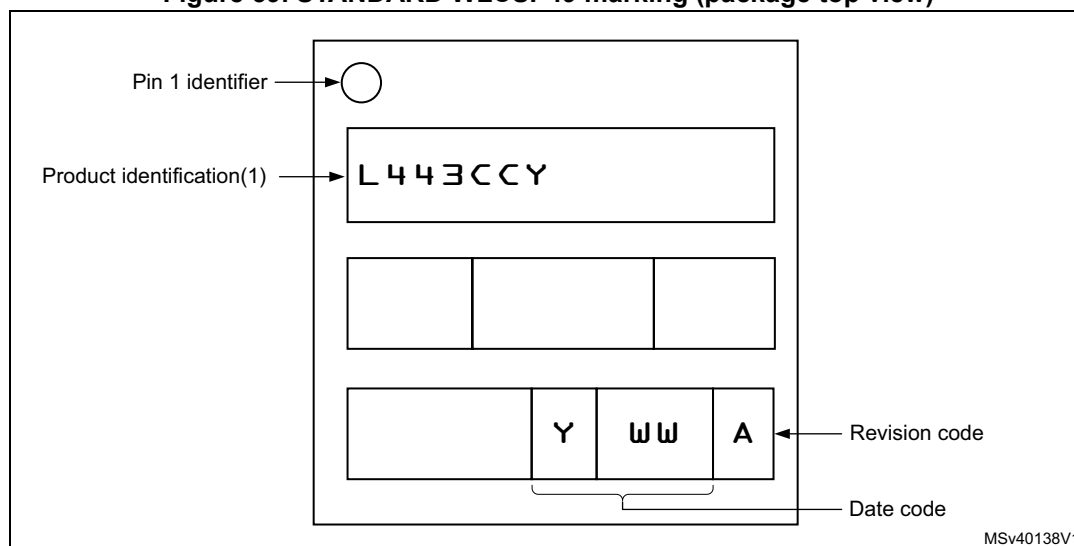
Table 101. STANDARD WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

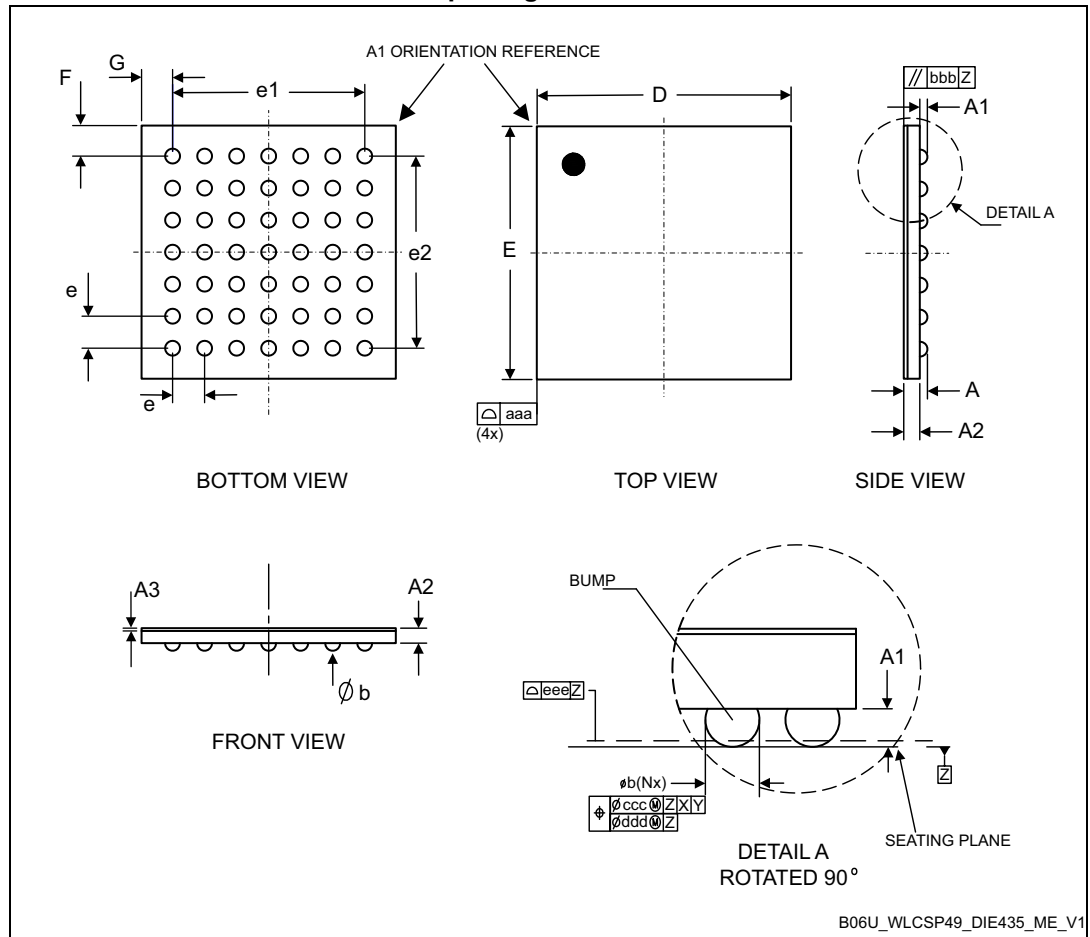
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. STANDARD WLCSP49 marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7

Figure 60. WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale package outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

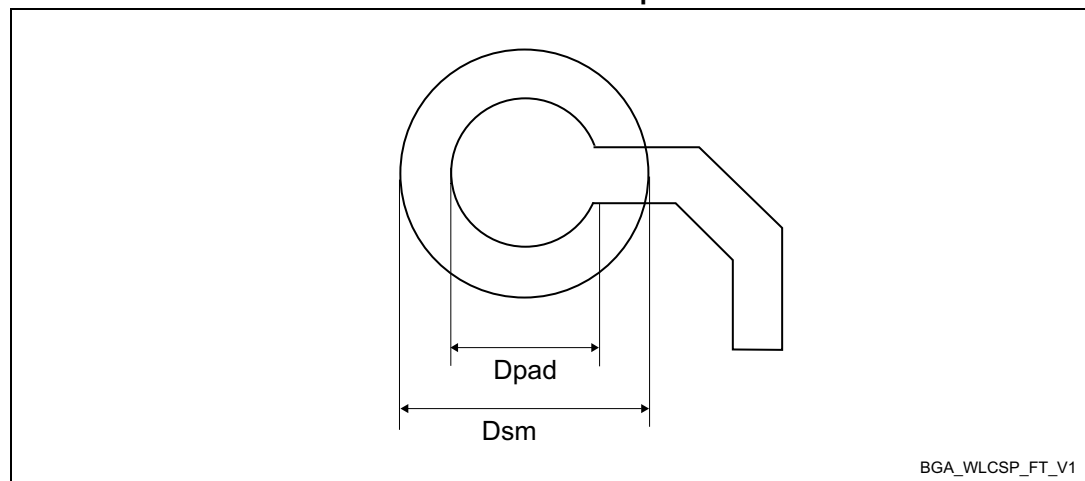
Table 102. THIN WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A ⁽²⁾	-	-	0.33	-	-	0.013
A1	-	0.09	-	-	0.004	-
A2	-	0.20	-	-	0.008	-
A3 ⁽³⁾	-	0.025	-	-	0.001	-
b ⁽⁴⁾	0.16	0.19	0.22	0.006	0.007	0.009
D	3.13	3.15	3.17	0.123	0.124	0.125

Table 102. THIN WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E	3.12	3.14	3.16	0.123	0.124	0.124
e	-	0.40	-	-	0.016	-
e1	-	2.40	-	-	0.094	-
e2	-	2.40	-	-	0.094	-
F ⁽⁵⁾	-	0.375	-	-	0.015	-
G ⁽⁵⁾	-	0.370	-	-	0.015	-
aaa	-	0.10	-	-	0.004	-
bbb	-	0.10	-	-	0.004	-
ccc	-	0.10	-	-	0.004	-
ddd	-	0.05	-	-	0.002	-
eee	-	0.05	-	-	0.002	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Calculated dimensions are rounded to the 3rd decimal place

Figure 61. THIN WLCSP - 49 balls, 3.14x 3.15 mm, 0.4 mm pitch, wafer level chip scale recommended footprint

1. Dimensions are expressed in millimeters.

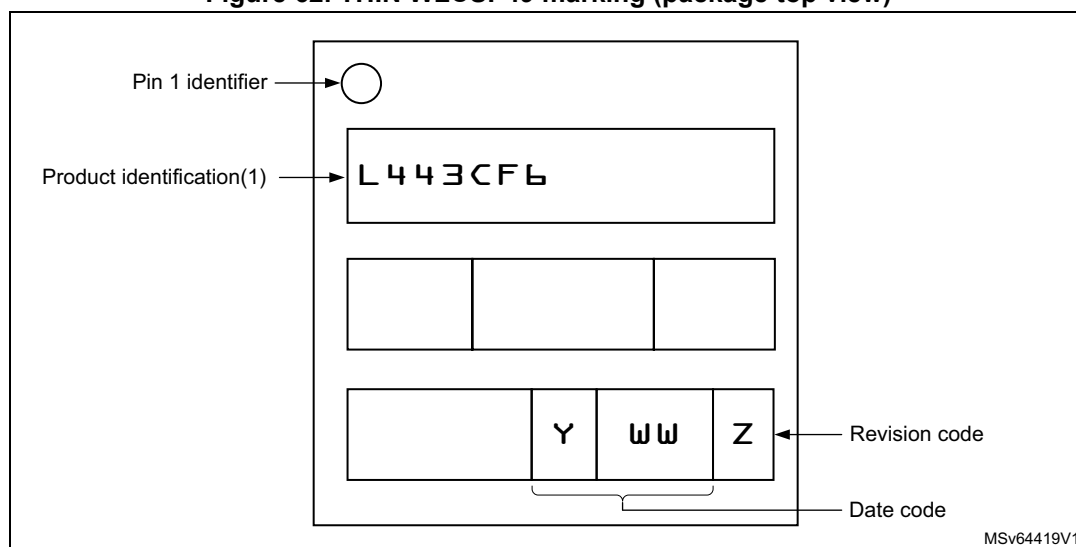
Table 103. THIN WLCSP49 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

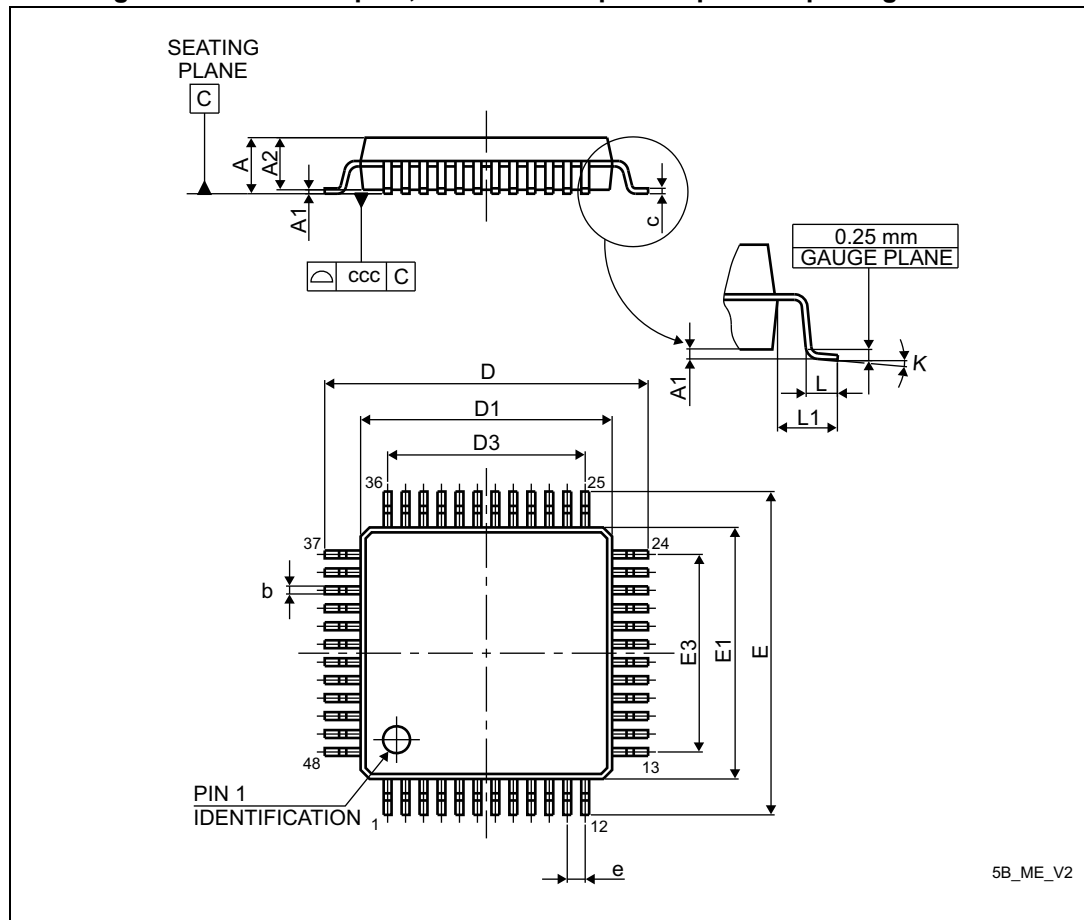
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 62. THIN WLCSP49 marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.8 LQFP48 package information

Figure 63. LQFP - 48 pins, 7 x 7 mm low-profile quad flat package outline



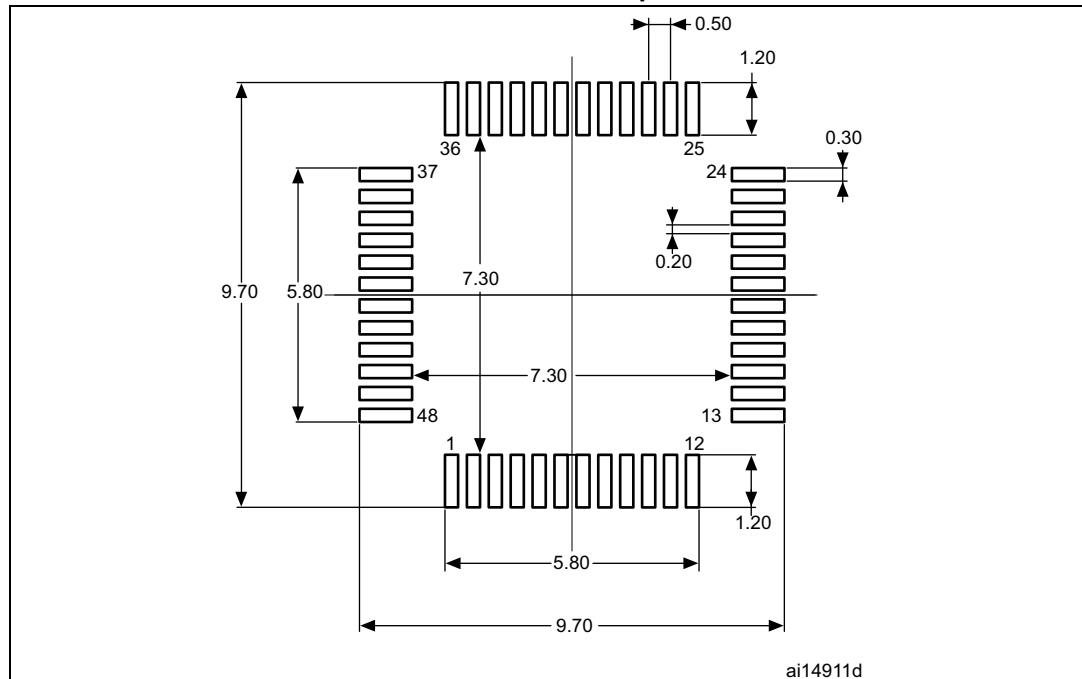
1. Drawing is not to scale.

Table 104. LQFP - 48 pins, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 64. LQFP - 48 pins, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

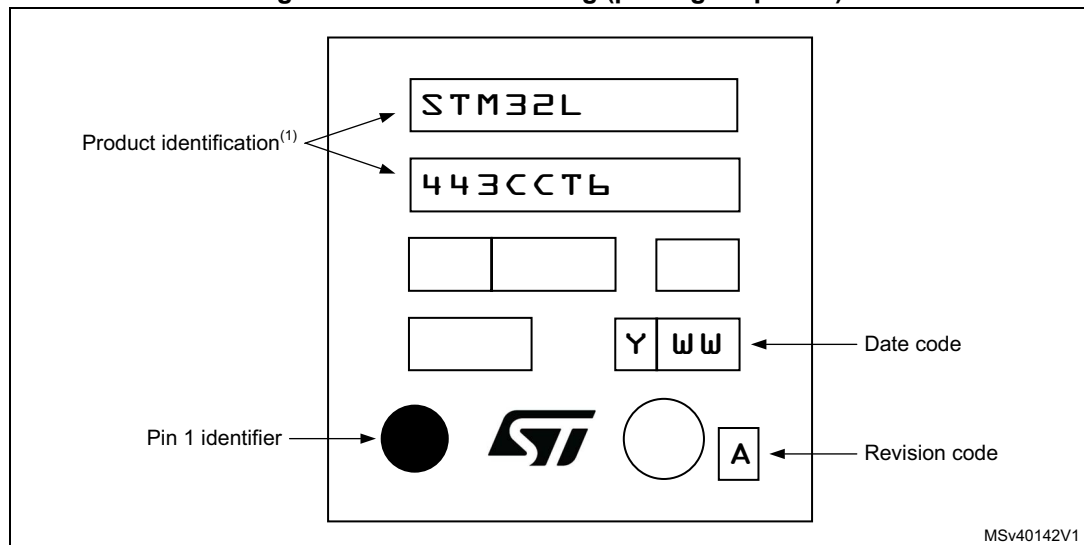
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

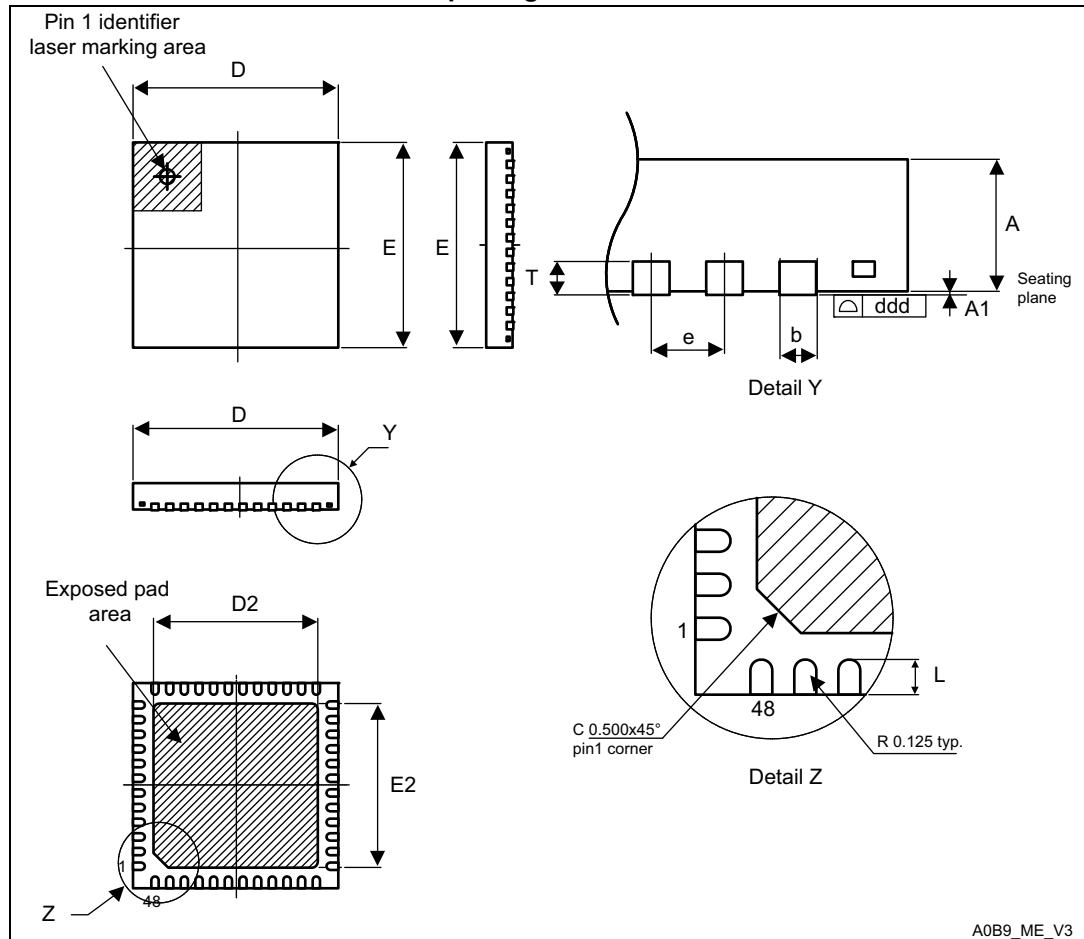
Figure 65. LQFP48 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.9 UFQFPN48 package information

Figure 66. UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

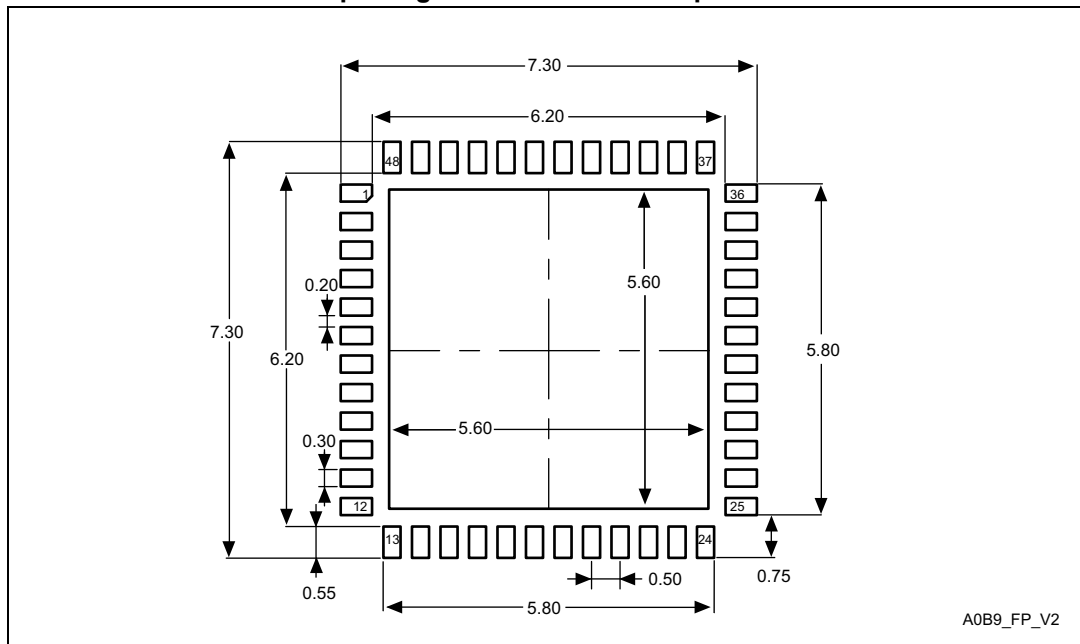


1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 105. UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. UFQFPN - 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

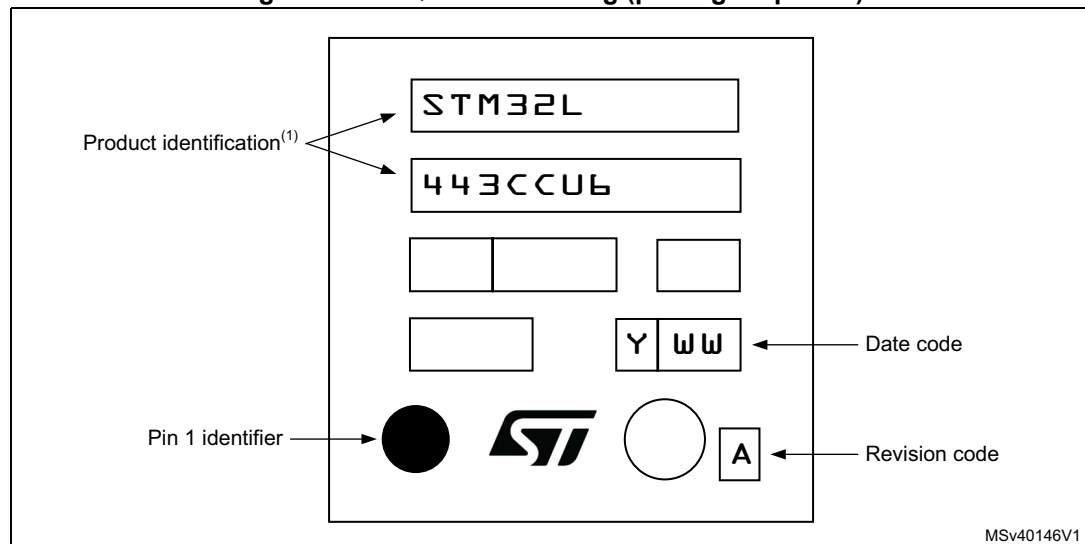
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 68. UFQFPN48 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.10 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 21: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and P_{IO} max ($P_D \text{ max} = P_{INT} \text{ max} + P_{IO} \text{ max}$),
- P_{INT} max is the product of all I_{DDXXX} and V_{DDXXX} , expressed in Watts. This is the maximum chip internal power.

P_{IO} max represents the maximum power dissipation on output pins where:

$$P_{IO} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 106. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm / 0.5 mm pitch	33	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm / 0.5 mm pitch	57	
	Thermal resistance junction-ambient WLCSP49 3.141 x 3.127 / 0.4 mm pitch	48	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient WLCSP64 3.141 x 3.127 / 0.35 mm pitch	46	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	42	
	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm / 0.5 mm pitch	57	

7.10.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.10.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L443xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 106](#) T_{Jmax} is calculated as follows:

– For LQFP64, $46\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (46\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.562\text{ }^{\circ}\text{C} = 102.562\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$) see [Section 8: Ordering information](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: *With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).*

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (46\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 105 - 20.562 = 84.438\text{ }^{\circ}\text{C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (46\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 125 - 20.562 = 104.438\text{ }^{\circ}\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 100\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 106](#) T_{Jmax} is calculated as follows:

– For LQFP64, $46\text{ }^{\circ}\text{C/W}$

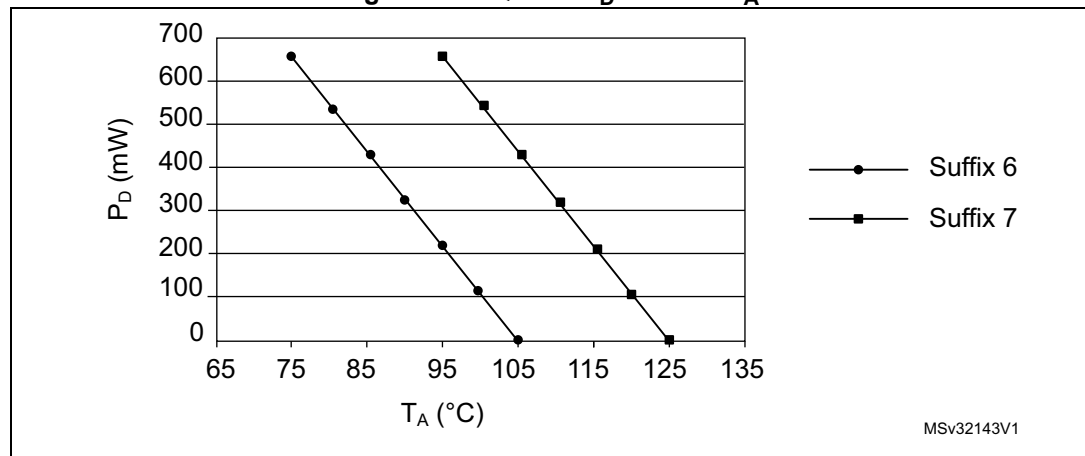
$$T_{Jmax} = 100\text{ }^{\circ}\text{C} + (46\text{ }^{\circ}\text{C/W} \times 134\text{ mW}) = 100\text{ }^{\circ}\text{C} + 6.164\text{ }^{\circ}\text{C} = 106.164\text{ }^{\circ}\text{C}$$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Ordering information](#)) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to [Figure 69](#) to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 69. LQFP64 P_D max vs. T_A



8 Ordering information

Table 107. STM32L443xx ordering information scheme

Example:	STM32	L	443	C	C	T	6	TR								
Device family																
STM32 = Arm® based 32-bit microcontroller																
Product type																
L = ultra-low-power																
Device subfamily																
443: STM32L443xx																
Pin count																
C = 48 pins																
R = 64 pins																
V = 100 pins																
Flash memory size																
C = 256 KB of Flash memory																
Package																
T = LQFP ECOPACK®2																
U = QFN ECOPACK®2																
I = UFBGA ECOPACK®2																
Y = STANDARD WLCSP ECOPACK®2																
F = THIN WLCSP ECOPACK®2																
Temperature range																
6 = Industrial temperature range, -40 to 85 °C (105 °C junction)																
7 = Industrial temperature range, -40 to 105 °C (125 °C junction)																
3 = Industrial temperature range, -40 to 125 °C (130 °C junction)																
Packing																
TR = tape and reel																
xxx = programmed parts																

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 108. Document revision history

Date	Revision	Changes
08-Feb-2016	1	Initial release.
23-May-2016	2	Updated document title. Updated Table 1: STM32L443xx family device features and peripheral counts. Updated Section 3.15.3: VBAT battery voltage monitoring. Updated Section 3.27: Universal synchronous/asynchronous receiver transmitter (USART). Updated Table 14: STM32L443xx pin definitions. Updated Table 16: Alternate function AF8 to AF15. Updated Table 18: Voltage characteristics. Updated Table 21: General operating conditions. Added Figure 19: VREFINT versus temperature. Updated Table 23: Embedded reset and power control block characteristics. Updated Table 25 to Table 27 and Table 31 to Table 40. Updated Table 40: Low-power mode wakeup timings. Added Table 42: Wakeup time using USART/LPUART. Updated Table 48: MSI oscillator characteristics. Added Table 49: HSI48 oscillator characteristics. Added Figure 26: HSI48 frequency versus temperature. Updated Table 51: PLL, PLLSAI1 characteristics. Updated introduction of Section 6.3.14: I/O port characteristics. Added note to Figure 29: Recommended NRST pin protection. Updated Table 64: Analog switches booster characteristics. Updated Table 65: ADC characteristics. Updated Table 73: VREFBUF characteristics. Updated Table 74: COMP characteristics. Updated Table 90: USB electrical characteristics. Added Section : SWPMI characteristics. Updated Table 106: Package thermal characteristics.
12-Jun-2017	3	Added 1x LPUART on cover page. Updated Reference Manual title when referring to RM0394. Added Table 3: STM32L443xx modes overview. Updated Table 5: STM32L443xx peripherals interconnect matrix. Added Section 3.24.5: Infrared interface (IRTIM).

Table 108. Document revision history (continued)

Date	Revision	Changes
12-Jun-2017	3 (continued)	Updated baudrate in Section 3.27: Universal synchronous/asynchronous receiver transmitter (USART). Updated Section 6.1.7: Current consumption measurement. Added footnote to Table 58: I/O current injection susceptibility. Updated Table 59: I/O static characteristics. Updated Section 6.3.18: Analog-to-Digital converter characteristics. Added F_{ADC} min in Table 65: ADC characteristics. Updated Table 71: DAC characteristics. Added I_{bias} parameter in Table 74: COMP characteristics. Updated Section 7: Package information.
22-May-2018	4	Updated DAC terminology in all the document for clarification: single DAC instance (= DAC1) with 2 output channels. Added ECOPACK2® information in Features. Updated Section 3.9.1: Power supply schemes. Added Figure 3: Power-up/down sequence. Updated Clock-out capability in Section 3.11: Clocks and startup. Updated Figure 4: Clock tree. Updated Section 3.14.1: Nested vectored interrupt controller (NVIC). Updated Section 6.3.2: Operating conditions at power-up / power-down. Updated A_{Coeff} in Table 24: Embedded internal voltage reference. Updated Table 59: I/O static characteristics. Added Section 6.3.16: Extended interrupt and event controller input (EXTI) characteristics. Updated Table 71: DAC characteristics.
29-Oct-2019	5	Added THIN WLCSP in Features. Updated Table 90: USB electrical characteristics Updated Section 7.5: STANDARD WLCSP64 package information. Updated Section 7.6: STANDARD WLCSP49 package information. Added Section 7.7: THIN WLCSP49 package information. updated Section 8: Ordering information.

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