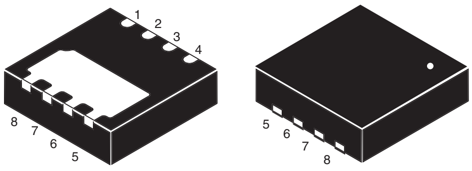
STL3NM60N

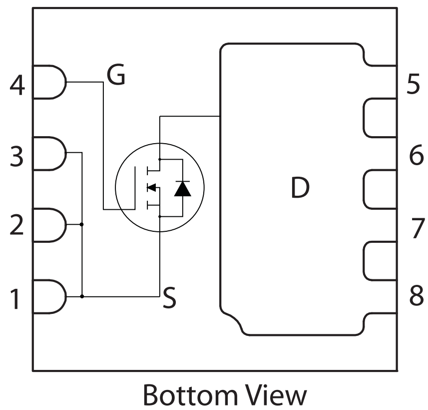
N-channel 600 V, 1.5 Ω, 2.2 A MDmesh™ II Power MOSFET in a PowerFLAT™ 3.3 x 3.3 HV package

Datasheet - production data



PowerFLAT™ 3.3x3.3 HV

Figure 1. Internal schematic diagram



Features

Order code	$R_{DS(on)}$ max.	I_D
STL3NM60N	1.8 Ω	2.2 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL3NM60N	3NM60N	PowerFLAT™ 3.3 x 3.3 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	2.2	A
I_D (1)	Drain current (continuous) at T_C=100 °C	1.7	A
I_D (2)	Drain current (continuous) at T_{amb} = 25 °C	0.65	A
I_D (2)	Drain current (continuous) at T_{amb} =100 °C	0.5	A
I_{DM} (2)(3)	Drain current (pulsed)	2.6	A
P_{TOT} (2)	Total dissipation at T_{amb} = 25 °C	2	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C	22	W
I_{AS}	Avalanche current, repetitive or not-repetitive (3)	1	A
E_{AS}	Single pulse avalanche energy (4)	119	mJ
	Derating factor (2)	0.016	W/°C
dv/dt (5)	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj-case}$.
2. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec
3. Pulse width limited by Tjmax
4. Starting Tj = 25 °C, I_D= I_{AS}, V_{DD}= 50V
5. I_{SD} ≤ 2.2 A, dv/dt ≤ 400 A/µs, V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD}= 80% $V_{(BR)DSS}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	5.6	°C/W
$R_{thj-amb}$ (1)	Thermal resistance junction-amb max.	62.5	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V,			1	µA
		V_{DS} = 600 V, T_c = 125 °C			100	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 1 A		1.5	1.8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50V, f=1 MHz, V_{GS}=0	-	188	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{GS} =0, V_{DS} =0 to 480 V	-	100	-	pF
R_g	Gate input resistance	f =1 MHz gate DC bias=0 test signal level = 20 mV open drain	-	6	-	Ω
Q_g	Total gate charge	V_{DD}= 480 V, I_D = 2.2 A V_{GS} =10 V *(see Figure 15)*	-	9.5	-	nC
Q_{gs}	Gate-source charge		-	1.6	-	nC
Q_{gd}	Gate-drain charge		-	5.3	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 1.1 A, R_G= 4.7 Ω, V_{GS} = 10 V (see *Figure 14*)	-	8.6	-	ns
t_r	Rise time		-	6.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	20.8	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		2.2	A
I_{SDM} (1)	Source-drain current (pulsed)		-		8.8	A
V_{SD}(2)	Forward on voltage	I_{SD}= 2.2 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 2.2 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16*)	-	168		ns
Q_{rr}	Reverse recovery charge		-	672		nC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	I_{SD}= 2.2 A, di/dt = 100 A/µs, V_{DD} = 60 V, Tj= 150 °C (see *Figure 16*)	-	2.3		ns
Q_{rr}	Reverse recovery charge		-	913		nC
I_{RRM}	Reverse recovery current		-	9		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

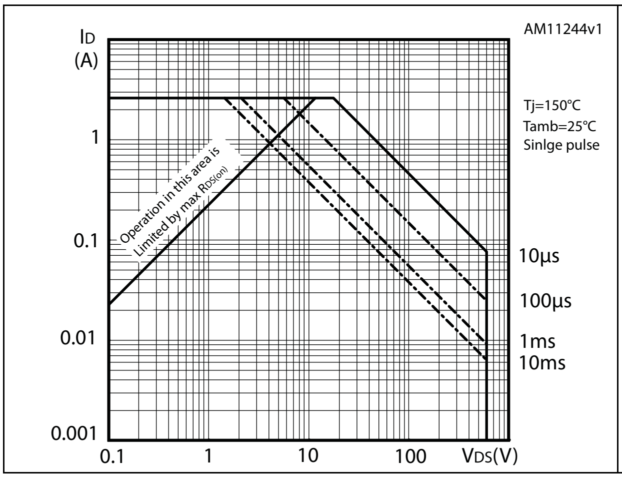


Figure 3. Thermal impedance

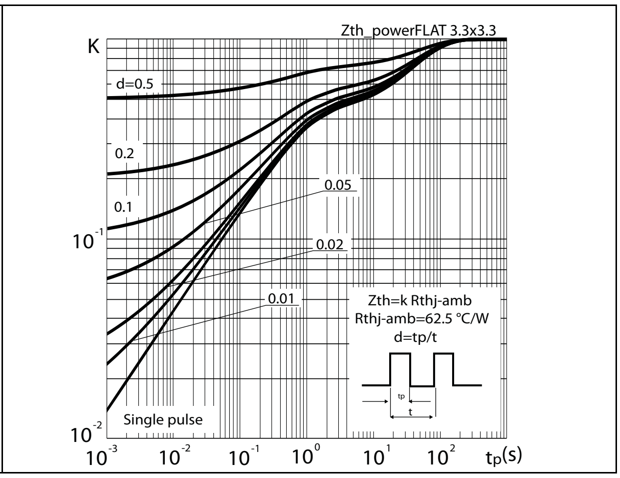


Figure 4. Output characteristics

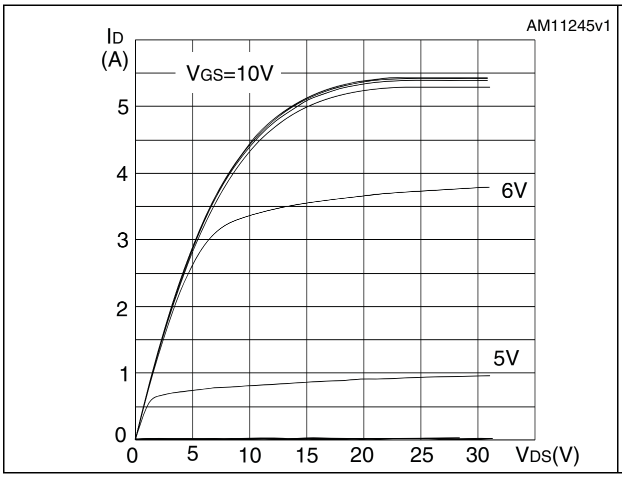


Figure 5. Transfer characteristics

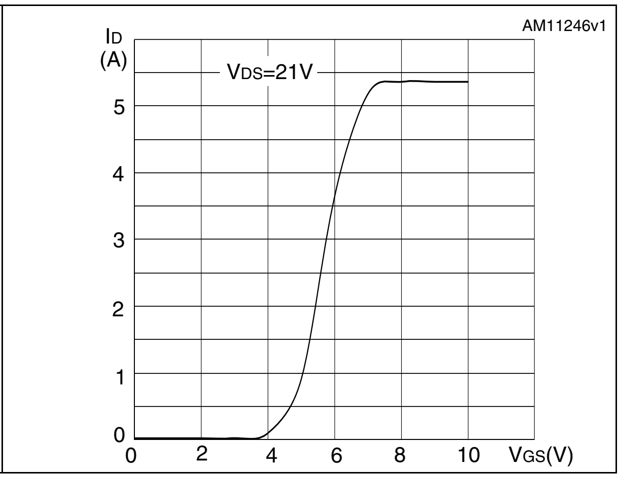


Figure 6. Gate charge vs gate-source voltage

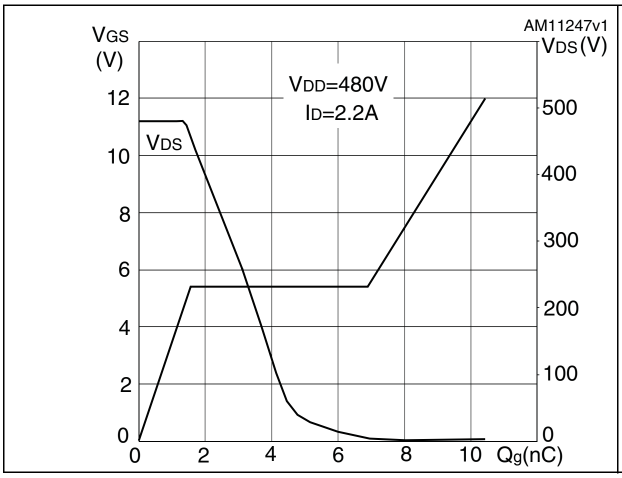


Figure 7. Static drain-source on resistance

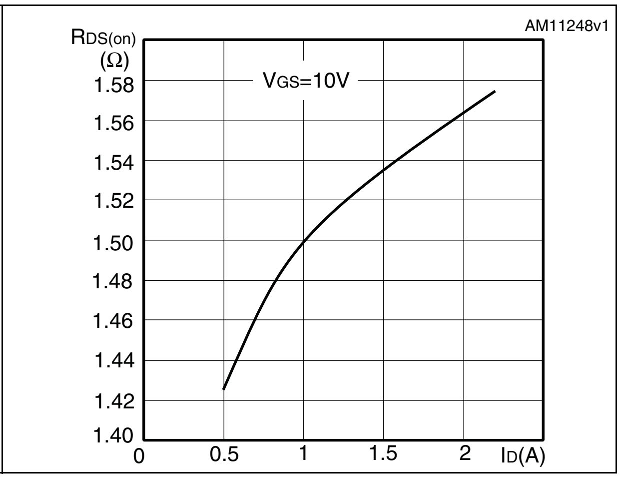


Figure 8. Capacitance variations

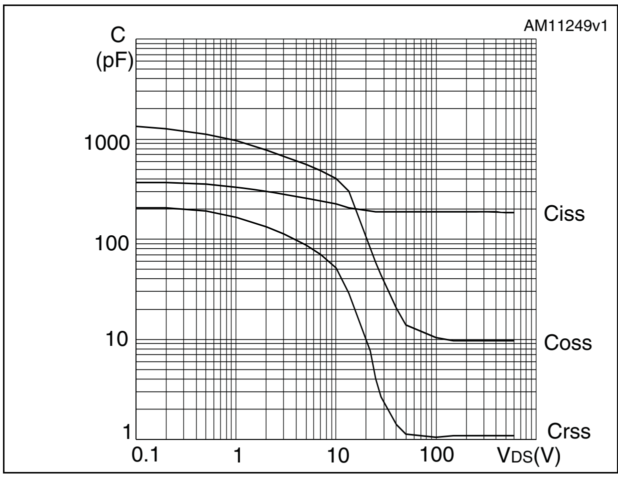


Figure 9. Output capacitance stored energy

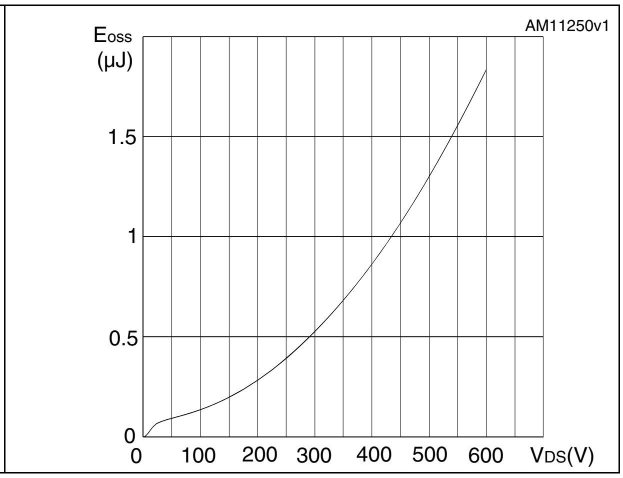


Figure 10. Normalized gate threshold voltage vs temperature

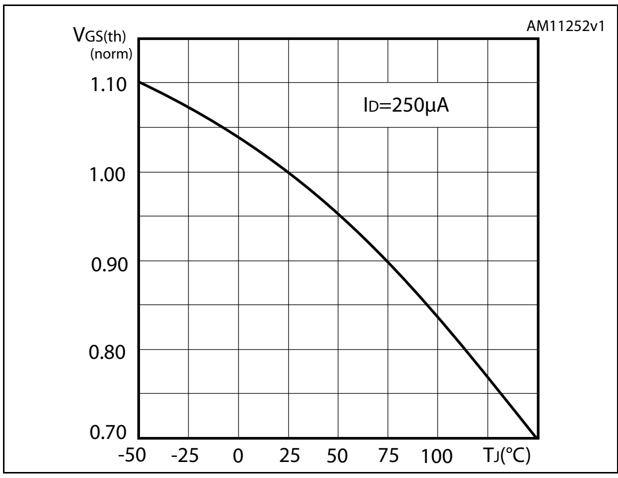


Figure 11. Normalized on resistance vs temperature

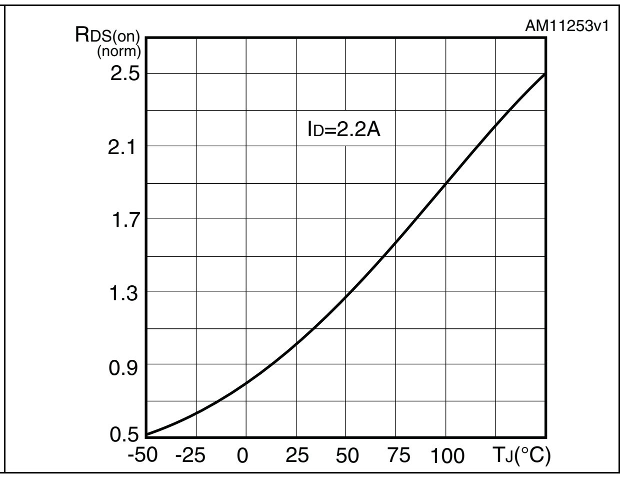


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

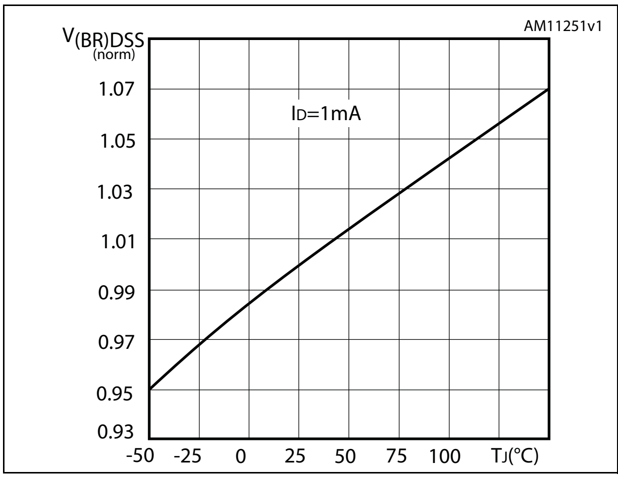
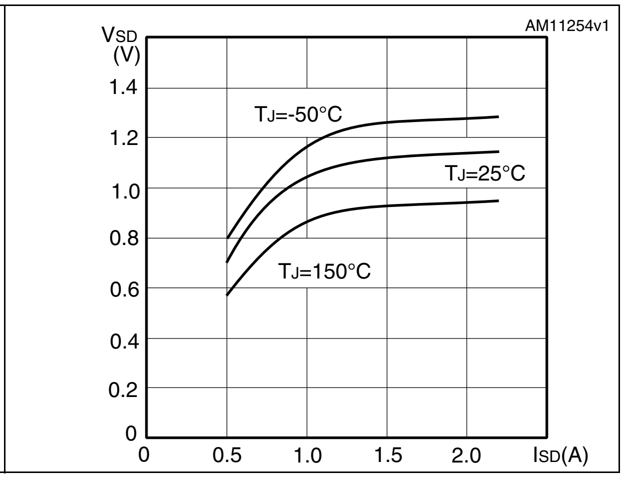


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

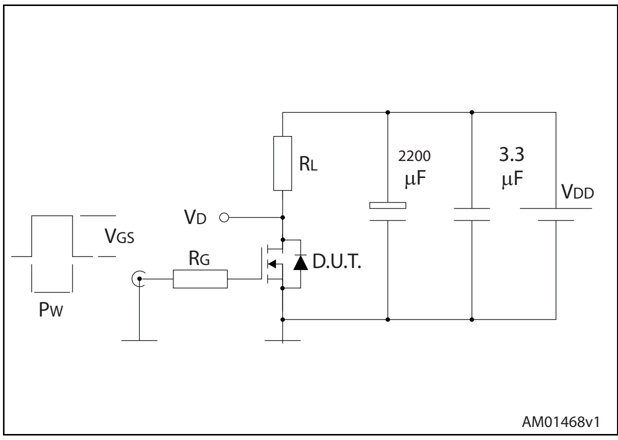


Figure 15. Gate charge test circuit

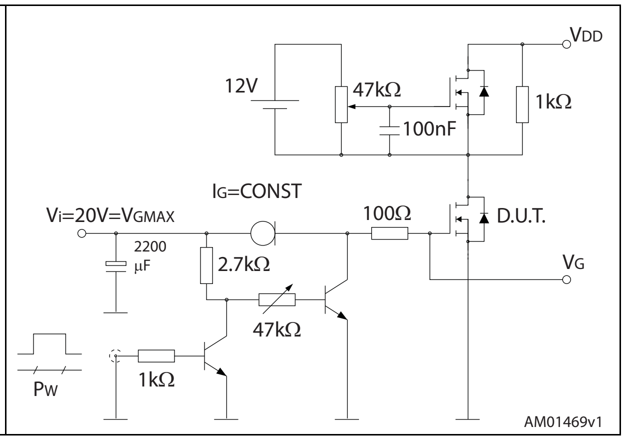


Figure 16. Test circuit for inductive load switching and diode recovery times

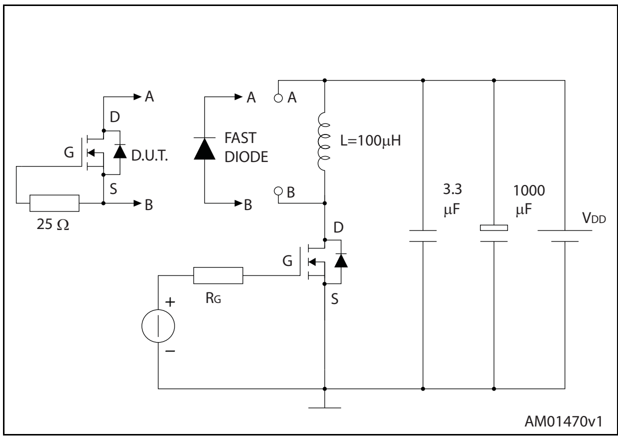


Figure 17. Unclamped inductive load test circuit

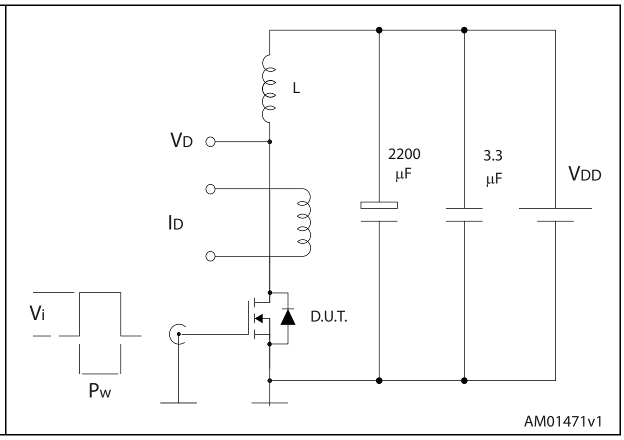


Figure 18. Unclamped inductive waveform

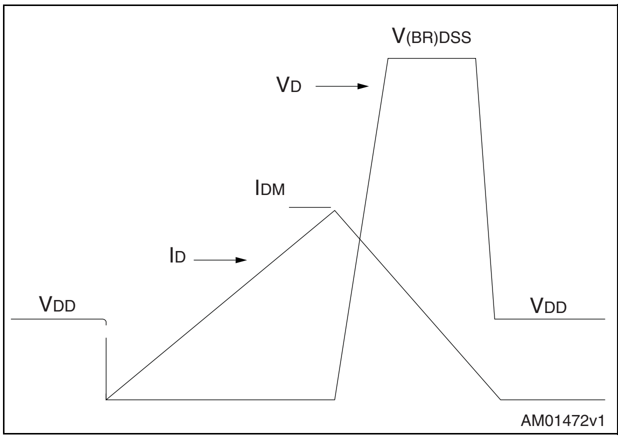
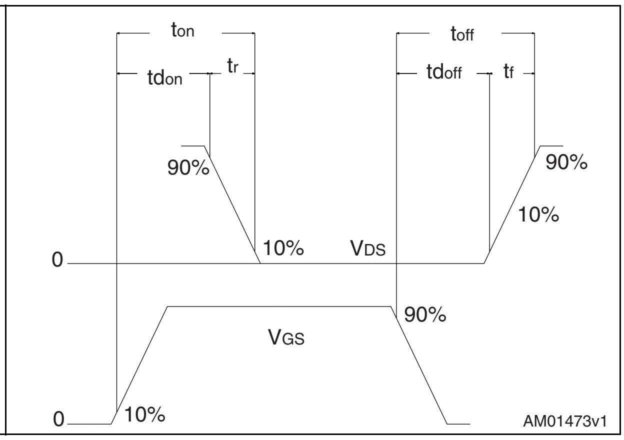


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. PowerFLAT™ 3.3 x 3.3 HV drawing

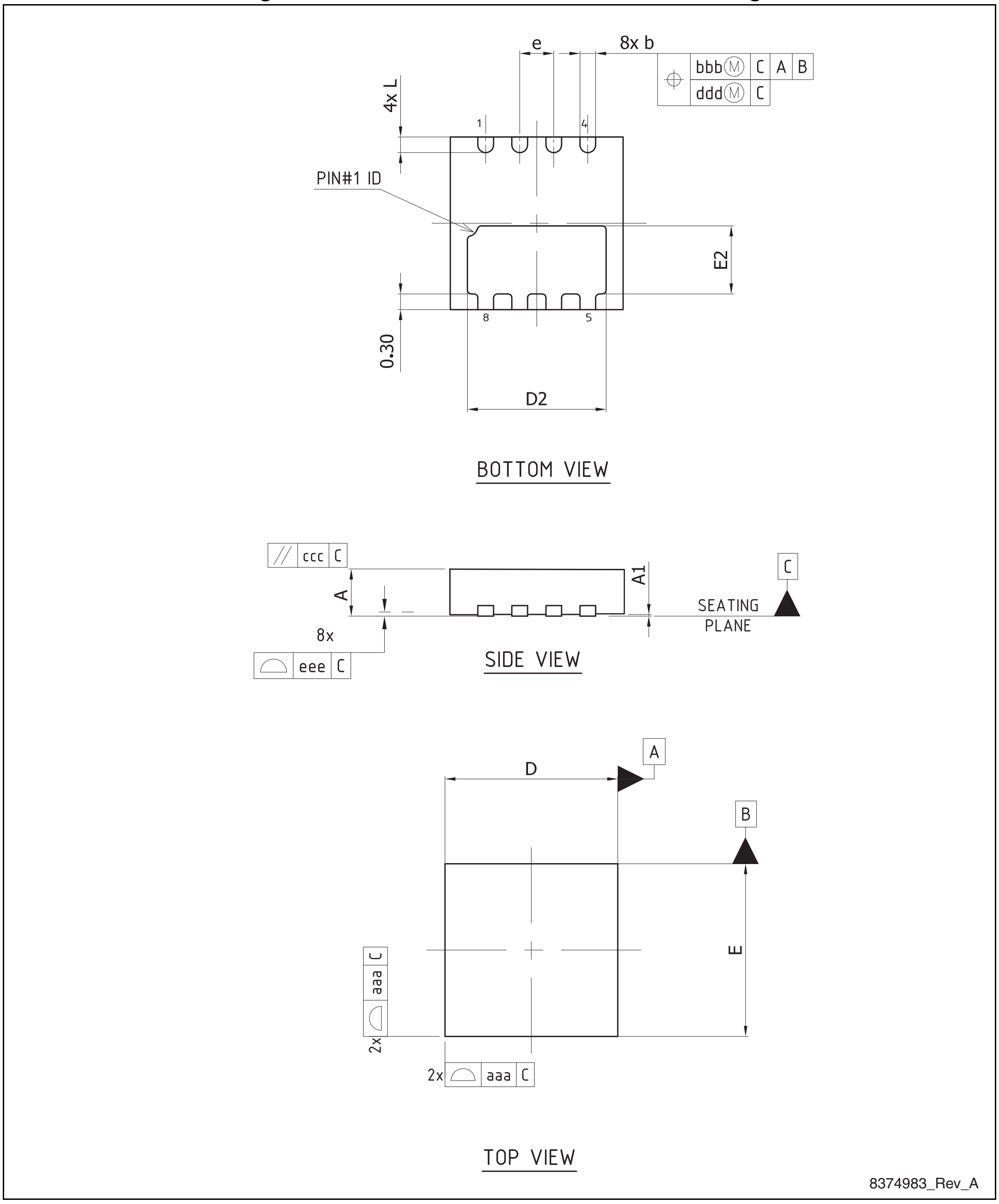
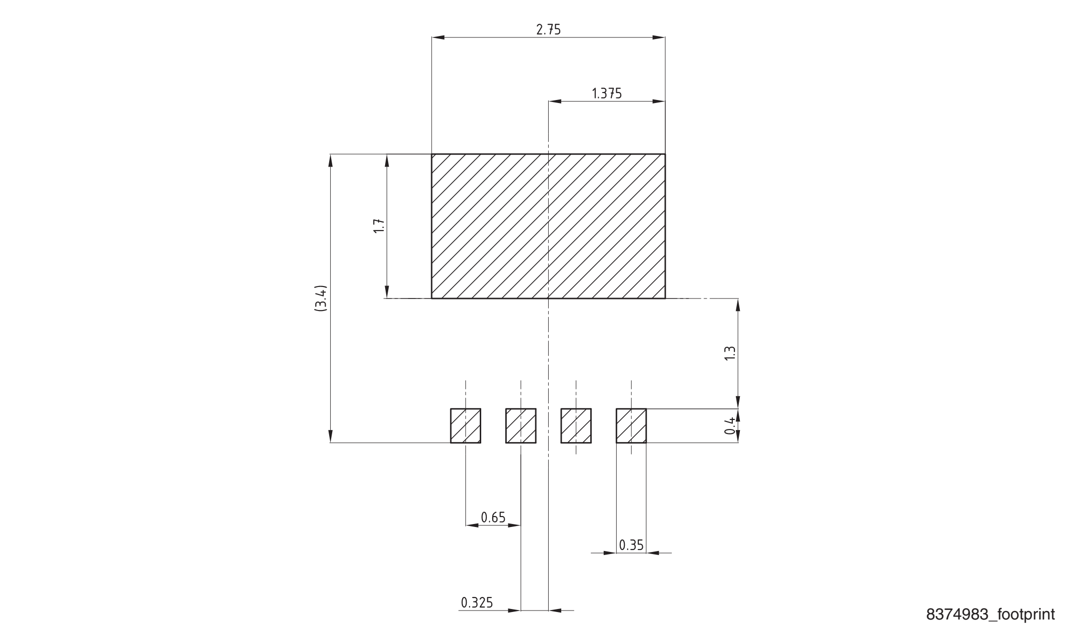


Table 8. PowerFLAT™ 3.3 x 3.3 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.25	0.30	0.40
D		3.30	
D2	2.50	2.65	2.75
E		3.30	
E2	1.15	1.30	1.40
e		0.65	
L	0.20	0.30	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 21. PowerFLAT™ 3.3 x 3.3 HV recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Mar-2012	1	First release.
19-Nov-2014	2	Document status changed from preliminary to production data. Updated *Figure 1.: Internal schematic diagram*,*Figure 2.: Safe operating area*, *Figure 3.: Thermal impedance* and *Figure 12.: Normalized $V_{(BR)DSS}$ vs temperature*. Updated *Table 5.: Dynamic* and *Table 7.: Source drain diode*. Minor text changes.