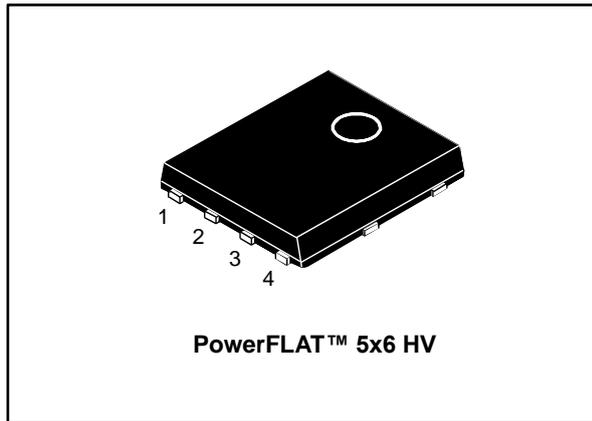
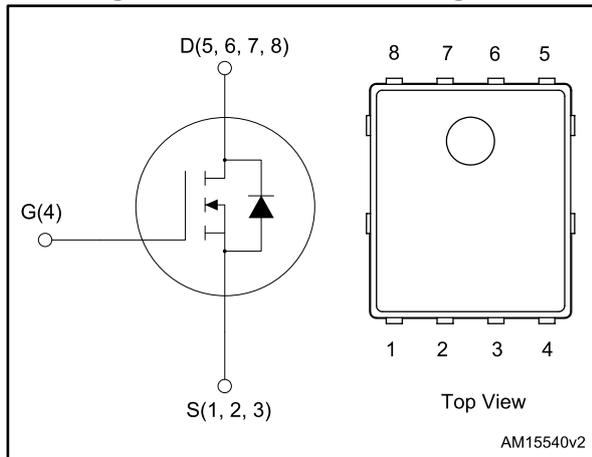


## N-channel 650 V, 0.335 $\Omega$ typ., 10 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



**Figure 1: Internal schematic diagram**



### Features

Order code	V <sub>DS</sub> @ T <sub>J</sub> max.	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL15N65M5	710 V	0.375 $\Omega$	10 A

- Extremely low R<sub>DS(on)</sub>
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

**Table 1: Device summary**

Order code	Marking	Package	Packing
STL15N65M5	15N65M5	PowerFLAT™ 5x6 HV	Tape and reel

---

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	650	V
V <sub>GS</sub>	Gate-source voltage	± 25	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	10	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	40	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	52	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	2.5	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	160	mJ
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage temperature range	- 55 to 150	°C
T <sub>j</sub>	Operating junction temperature range		°C

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup>I<sub>SD</sub> ≤ 10 A, di/dt ≤ 400 A/μs, V<sub>DS(peak)</sub> ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 400 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	2.4	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb	59	°C/W

**Notes:**

<sup>(1)</sup>When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup> , $V_{GS} = 0\text{ V}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		0.335	0.375	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	816	-	pF
$C_{oss}$	Output capacitance		-	23	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2.6	-	pF
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	70	-	pF
$C_{o(er)}$ <sup>(2)</sup>	Equivalent capacitance energy related		-	21	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16: "Test circuit for gate charge behavior"</a> )	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	5.5	-	nC
$Q_{gd}$	Gate-drain charge		-	11	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss}$  eq. time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80 %  $V_{DSS}$ .

<sup>(2)</sup> $C_{oss}$  eq. energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80 %  $V_{DSS}$ .

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 7\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> and <a href="#">Figure 20: "Switching time waveform"</a> )	-	30	-	ns
$t_{r(V)}$	Voltage rise time		-	8	-	ns
$t_{f(I)}$	Current fall time		-	11	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns

Table 7: Source drain diode

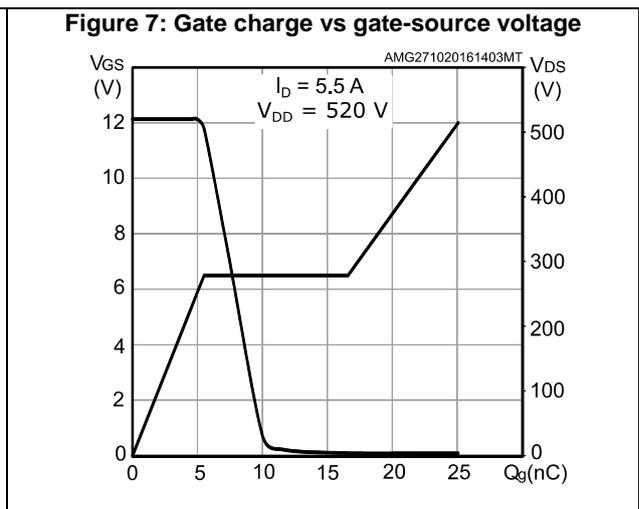
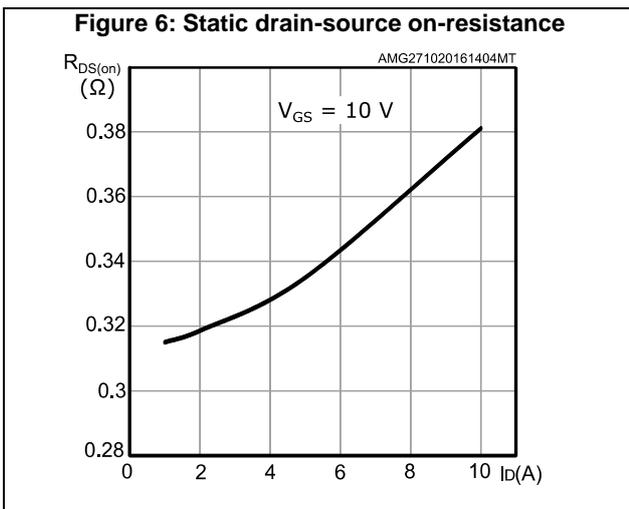
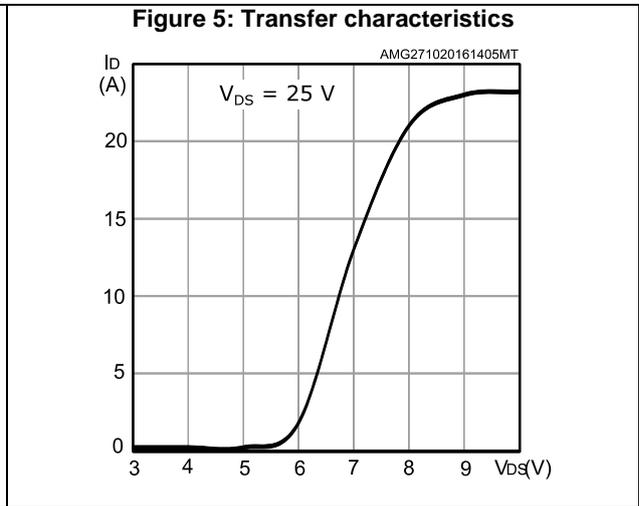
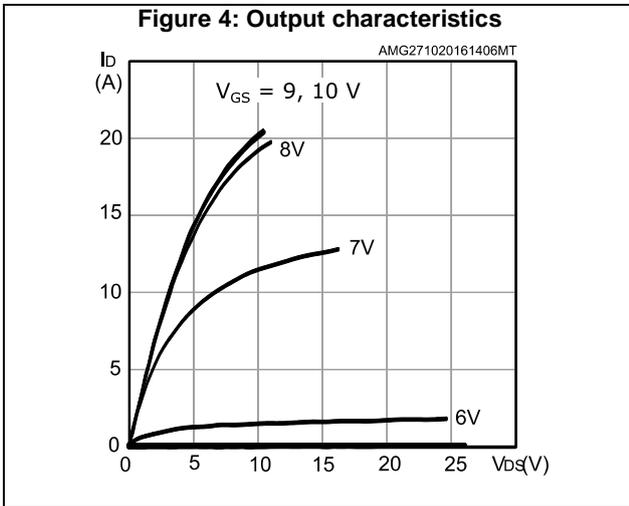
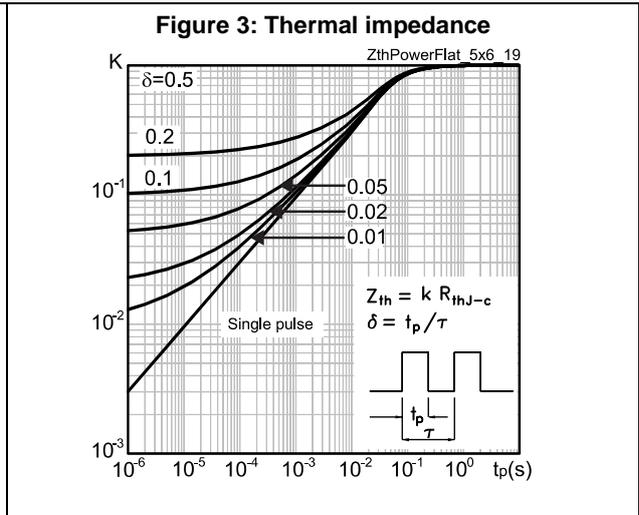
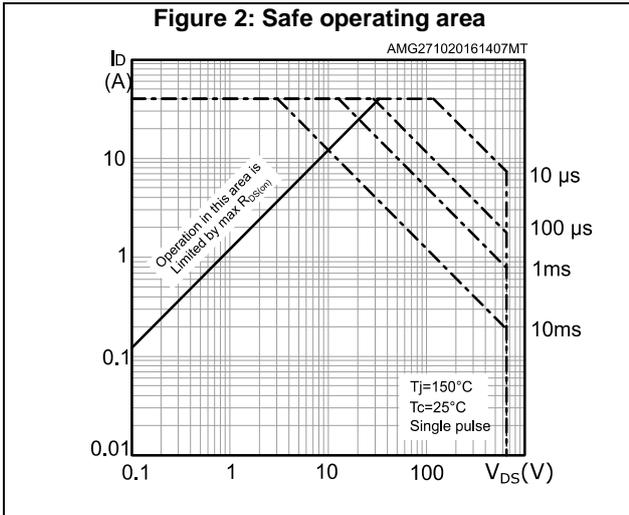
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	244		ns
$Q_{rr}$	Reverse recovery charge		-	2.35		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	308		ns
$Q_{rr}$	Reverse recovery charge		-	2.93		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19		A

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)



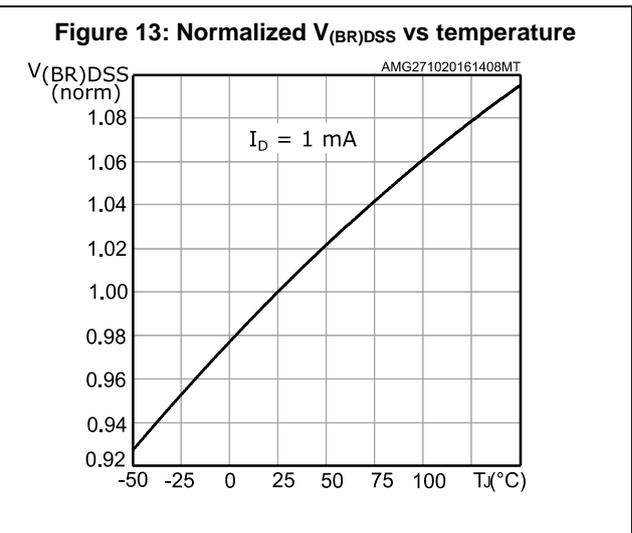
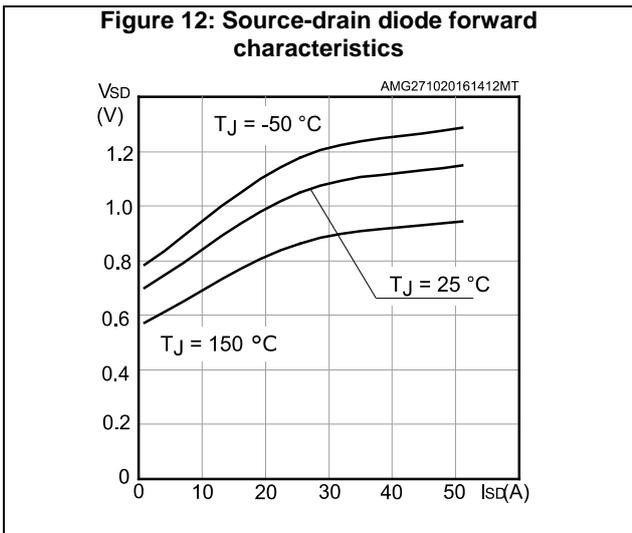
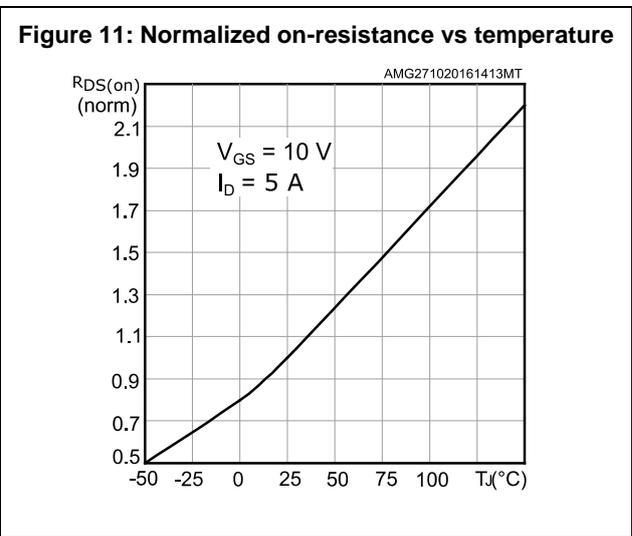
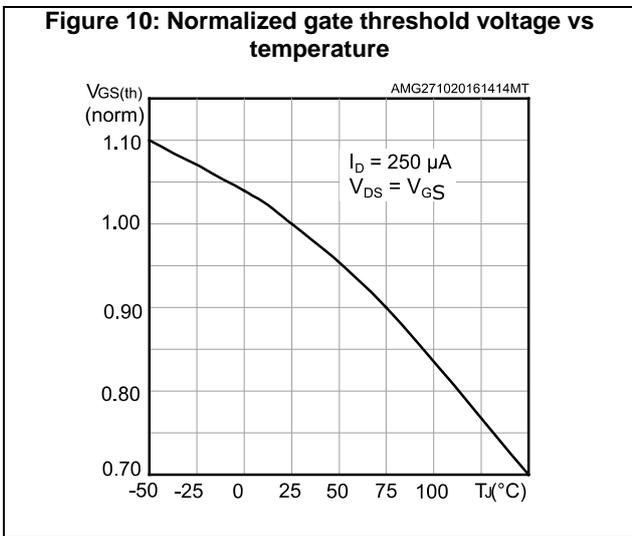
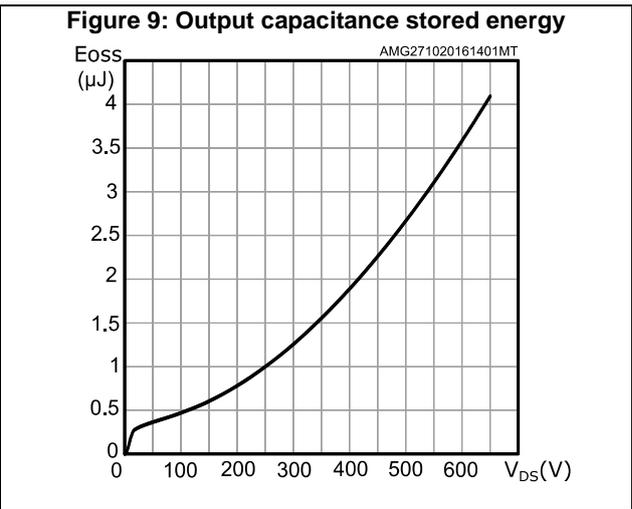
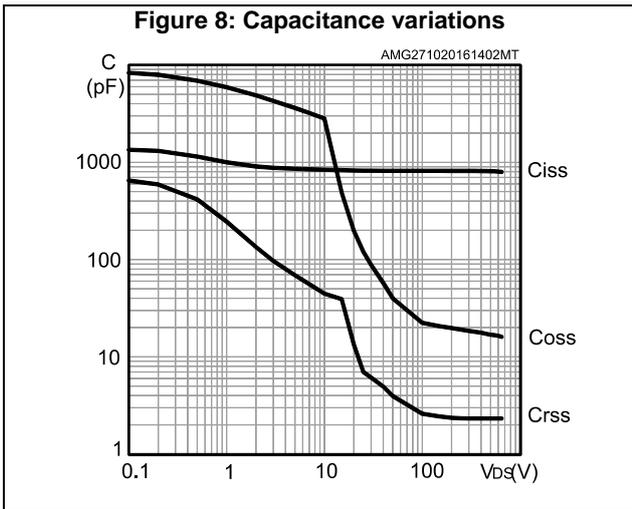
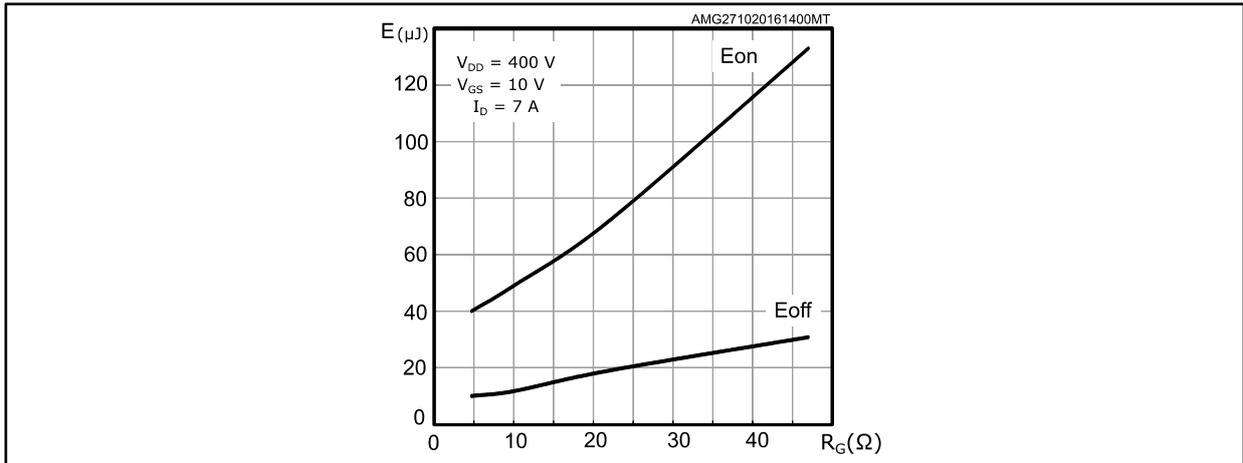


Figure 14: Switching energy vs gate resistance<sup>(1)</sup>

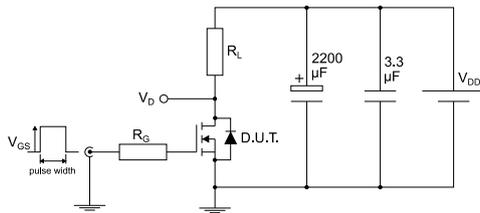


**Notes:**

<sup>(1)</sup> $E_{on}$  including reverse recovery of a SiC diode.

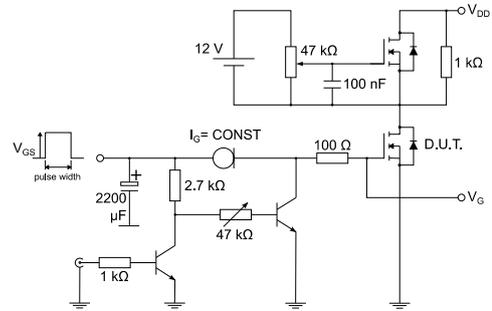
### 3 Test circuits

**Figure 15: Test circuit for resistive load switching times**



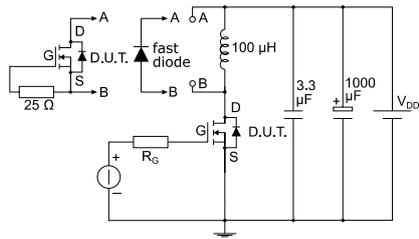
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**Figure 16: Test circuit for gate charge behavior**



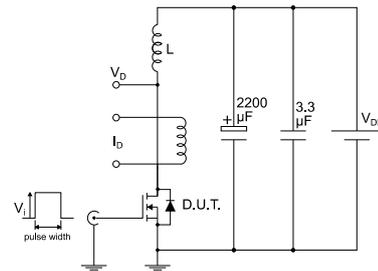
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**Figure 17: Test circuit for inductive load switching and diode recovery times**



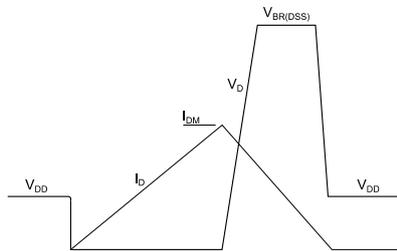
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**Figure 18: Unclamped inductive load test circuit**



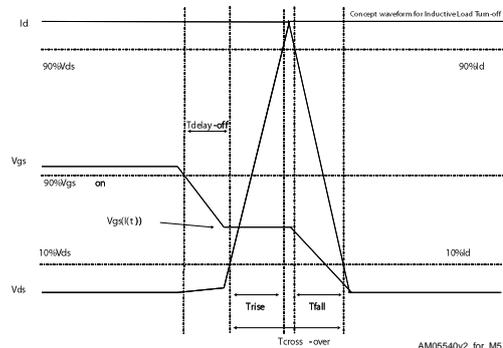
AM01471v1

**Figure 19: Unclamped inductive waveform**



AM01472v1

**Figure 20: Switching time waveform**



AM05540v2\_for\_M5

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 Power Flat™ 5x6 HV package information

Figure 21: PowerFLAT™ 5x6 HV package outline

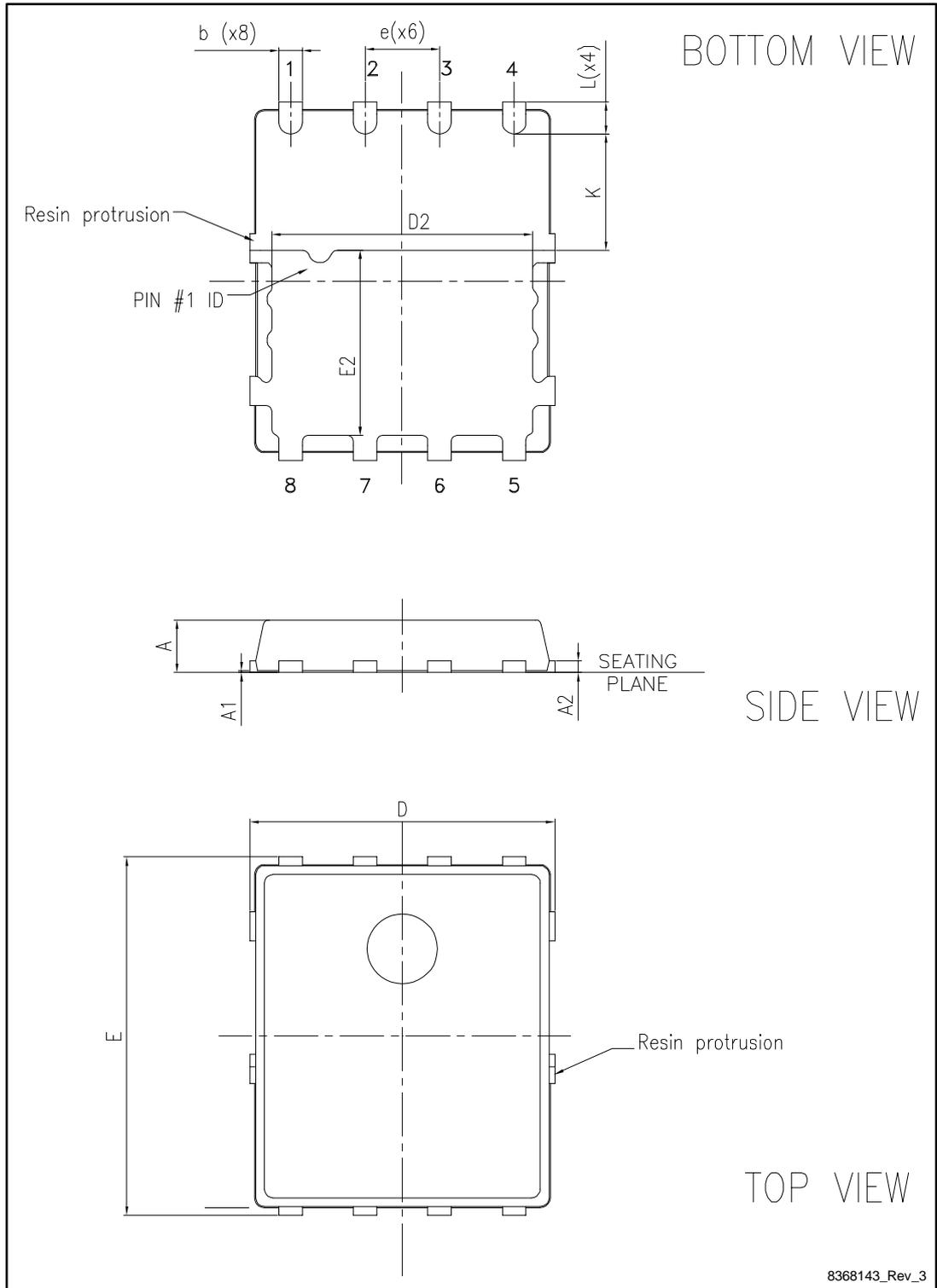
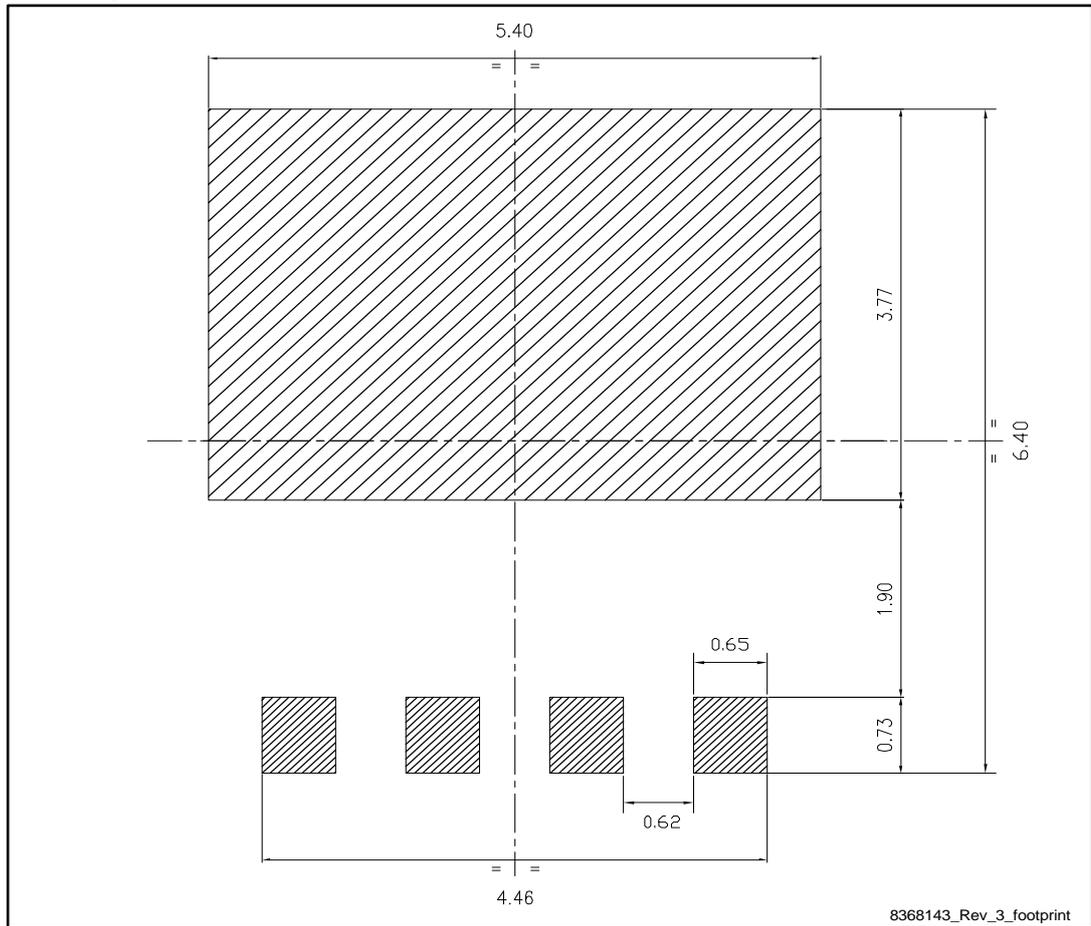


Table 8: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 22: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



### 4.2 Power Flat™ 5x6 HV packing information

Figure 23: PowerFLAT™ 5x6 tape (dimensions are in mm)

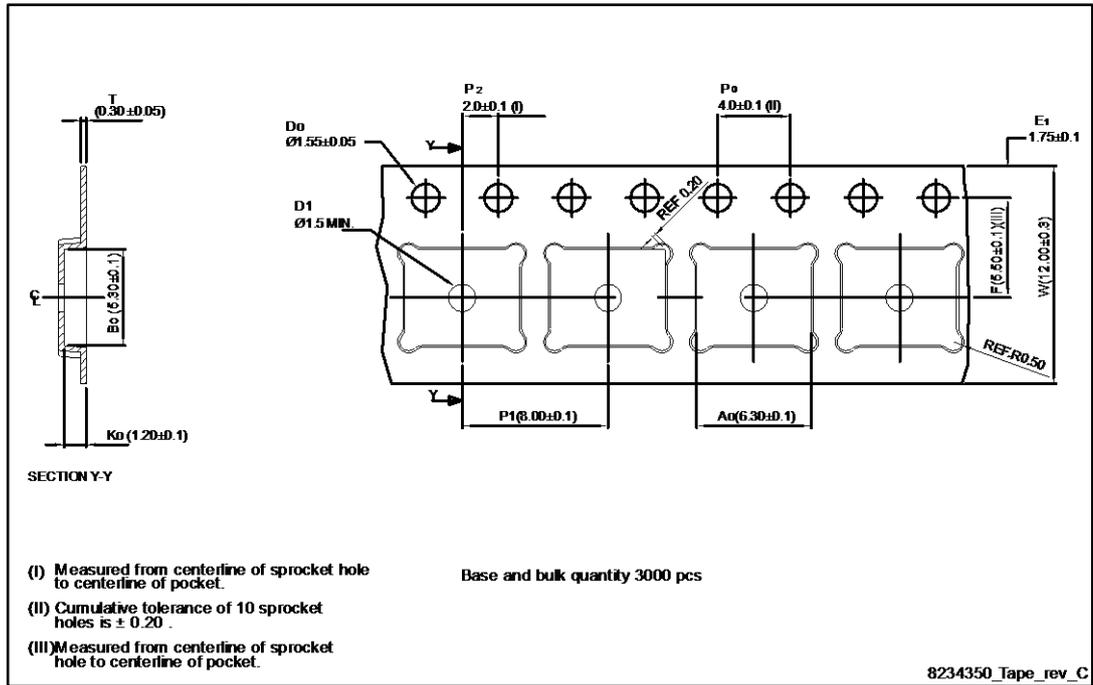


Figure 24: PowerFLAT™ 5x6 package orientation in carrier tape

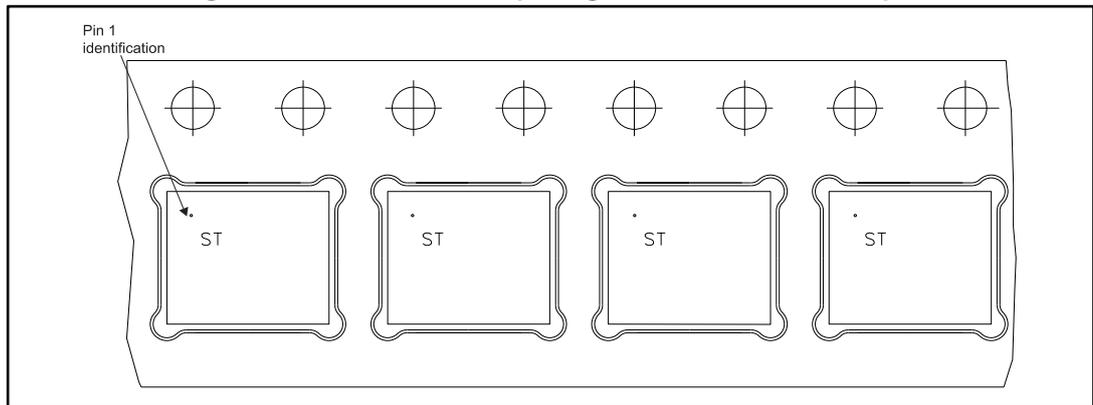
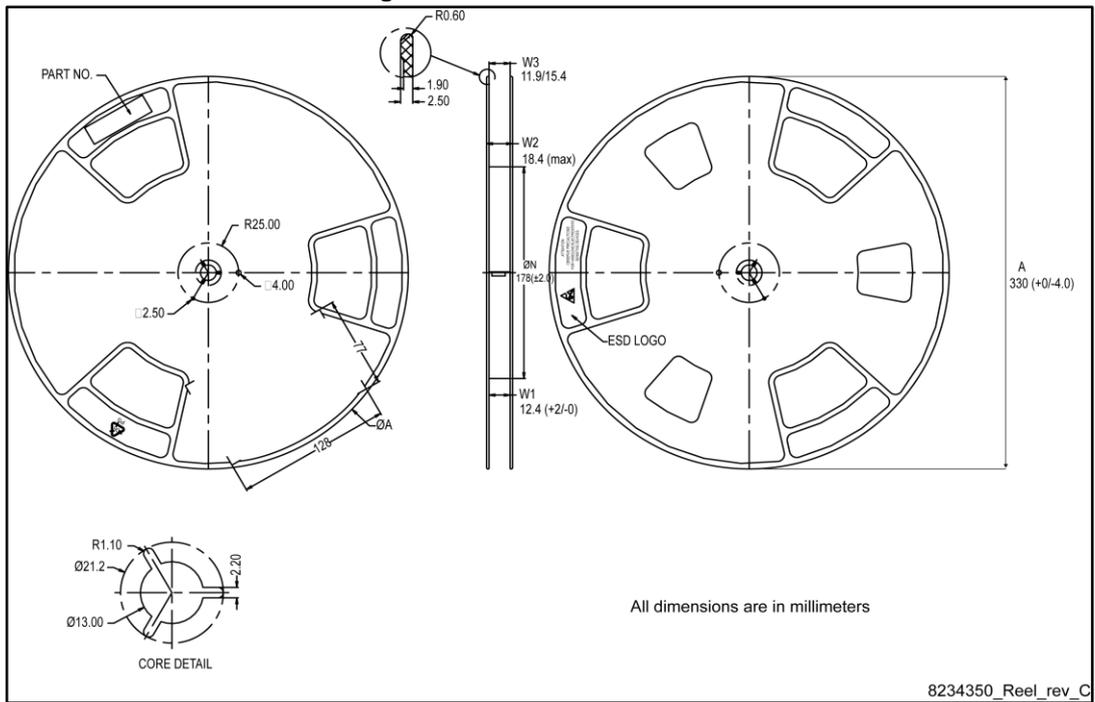


Figure 25: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release
05-Dec-2016	2	Updated title, features and description in cover page. Updated <i>Figure 1: "Internal schematic diagram"</i> , <i>Table 2: "Absolute maximum ratings"</i> and <i>Section 4: "Package information"</i> . Minor text changes.

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