

N-channel 100 V, 3.9 mΩ typ., 180 A, STripFET™ F3 Power MOSFET in H²PAK-2 package

Datasheet - production data

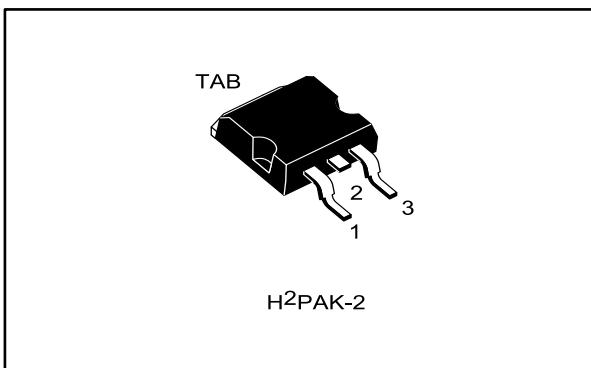
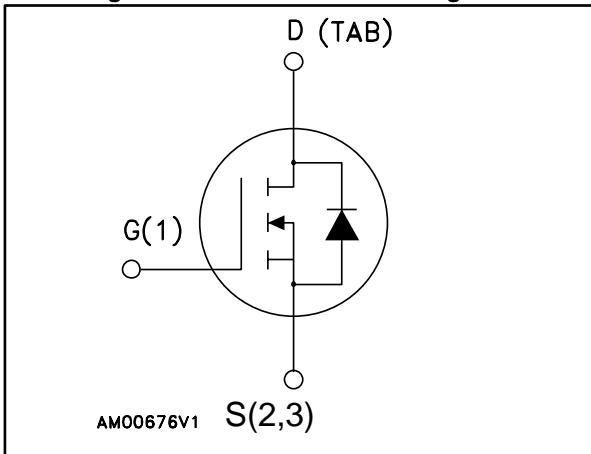


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH180N10F3-2	100 V	4.5 mΩ	180 A

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STH180N10F3-2	180N10F3	H ² PAK-2	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
dv/dt	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	350	mJ
T_J	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

Notes:

(1) Current limited by package

(2) Pulse width limited by safe operating area

(3) Starting $T_J = 25^\circ\text{C}$, $I_D = 80$, $V_{DD} = 50$ V**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C}/\text{W}$

Notes:(1) When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25^\circ C$ unless otherwise specified)

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250 \mu A$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 100 V$			10	μA
		$V_{DS} = 100 V; T_C = 125^\circ C$			100	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 60 A$		3.9	4.5	$m\Omega$

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			6665		pF
C_{oss}	Output capacitance			786		pF
C_{rss}	Reverse transfer capacitance			49		pF
Q_g	Total gate charge			114.6		nC
Q_{gs}	Gate-source charge			38.8		nC
Q_{gd}	Gate-drain charge	See <i>Figure 14: "Gate charge test circuit"</i>		31.9		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50 V, I_D = 60 A,$		25.6		ns
t_r	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$		97.1		ns
$t_{d(off)}$	Turn-off delay time	See <i>Figure 13: "Switching times test circuit for resistive load"</i>		99.9		ns
t_f	Fall time			6.9		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$I_{SD} = 120 \text{ A}, V_{GS} = 0$	-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				720	A
$V_{SD}^{(2)}$	Forward on voltage				1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 120 \text{ A},$ $dI/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 80 \text{ V},$ $T_j = 150^\circ\text{C}$	-	83.4		ns
Q_{rr}	Reverse recovery charge			295.7		nC
I_{RRM}	Reverse recovery current			7.1		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1

Electrical characteristics (curves)

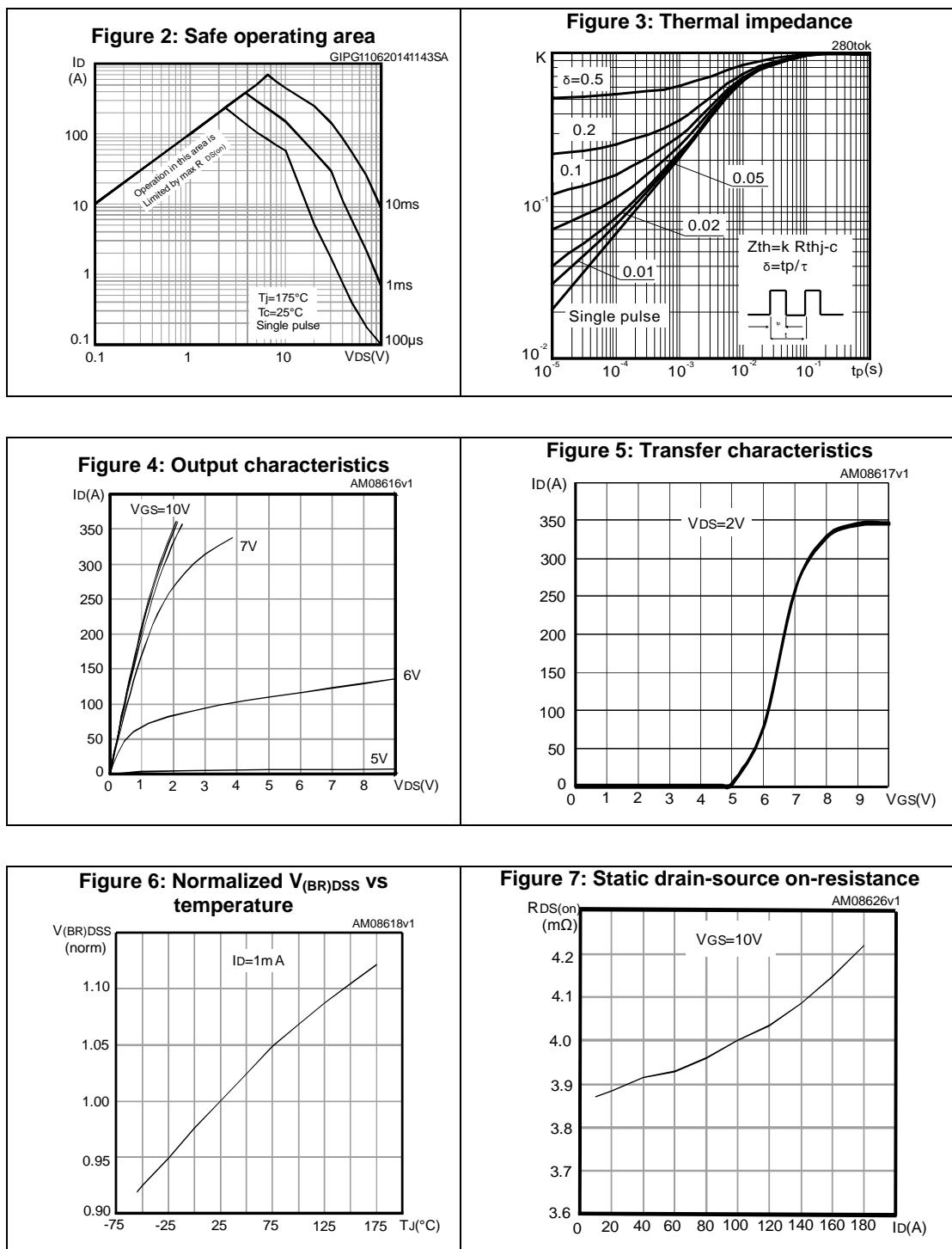
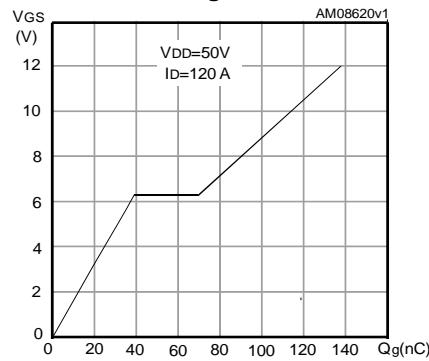
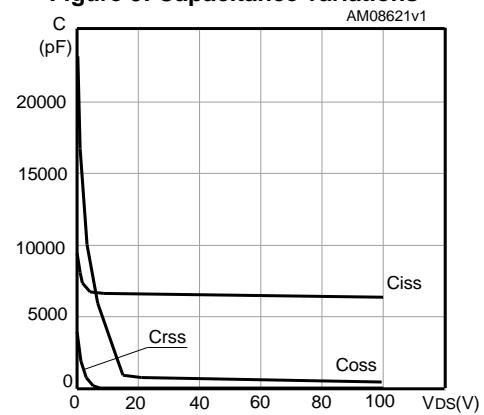
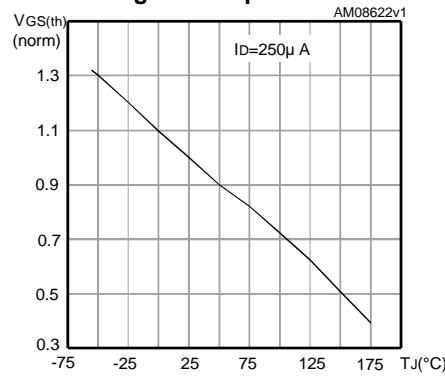
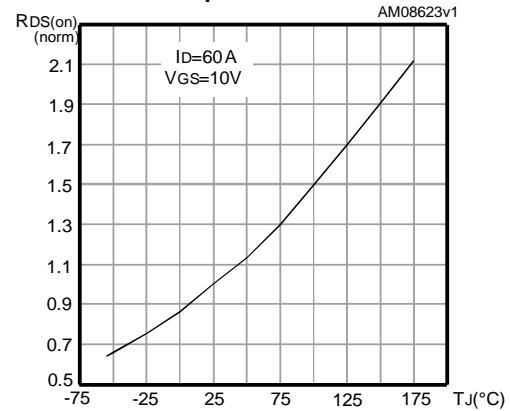
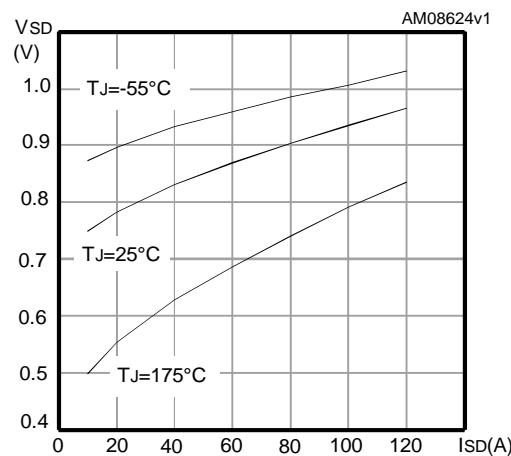
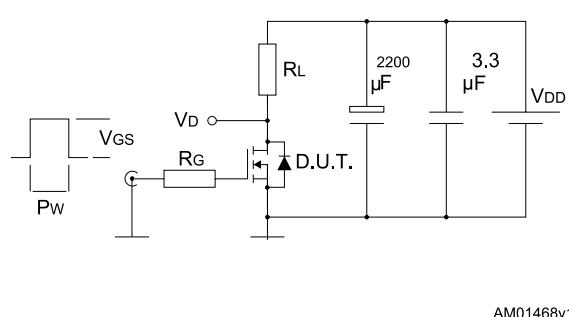


Figure 8: Gate charge vs gate-source voltage**Figure 9: Capacitance variations****Figure 10: Normalized gate threshold voltage vs temperature****Figure 11: Normalized on-resistance vs temperature****Figure 12: Source-drain diode forward characteristics**

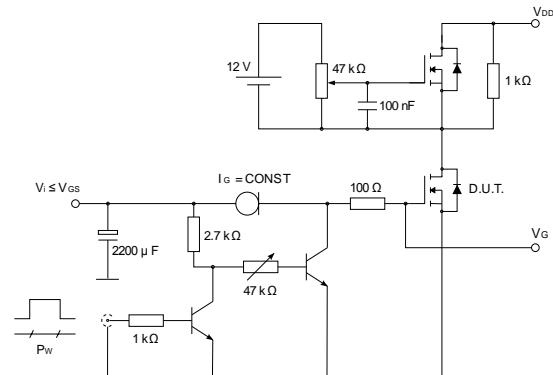
3 Test circuits

Figure 13: Switching times test circuit for resistive load



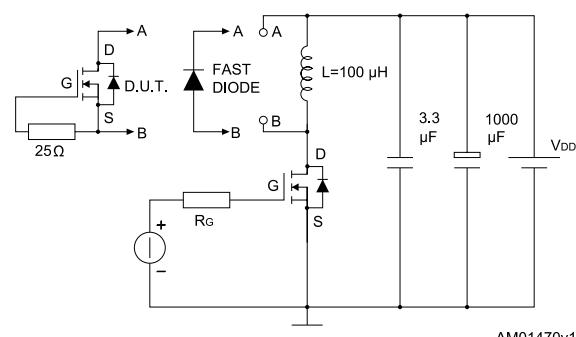
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Figure 14: Gate charge test circuit



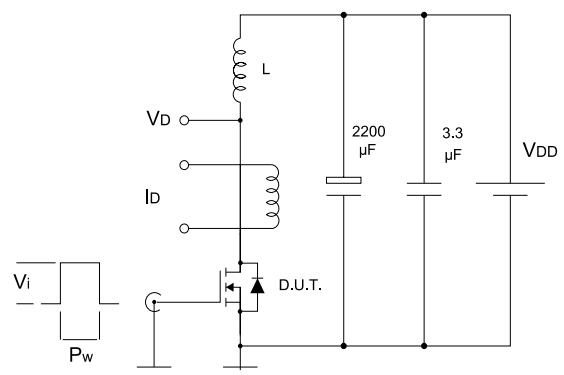
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Figure 15: Test circuit for inductive load switching and diode recovery times



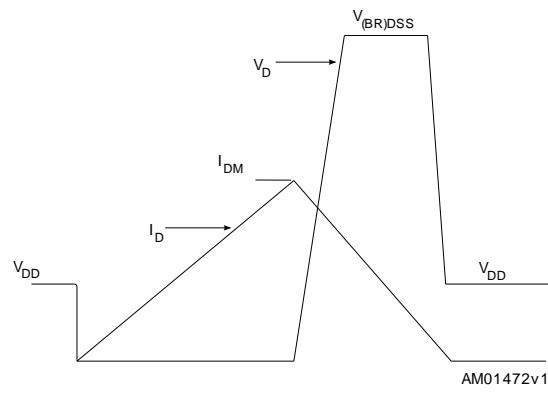
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Figure 16: Unclamped inductive load test circuit



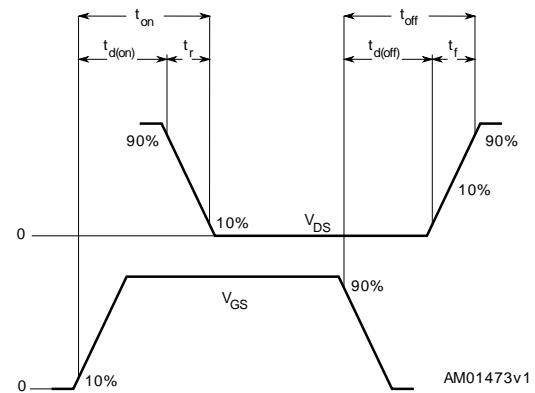
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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4.1 H²PAK-2 package information

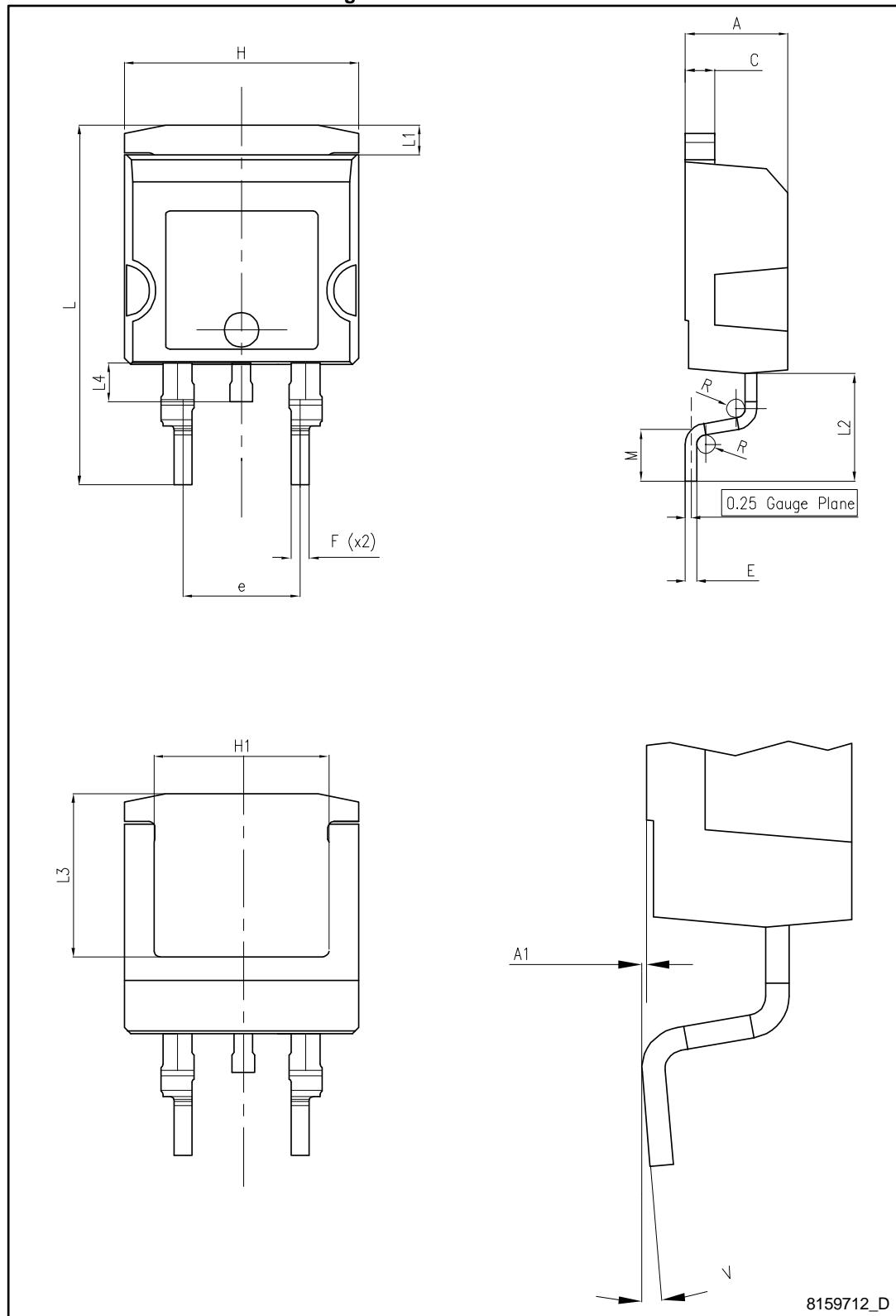
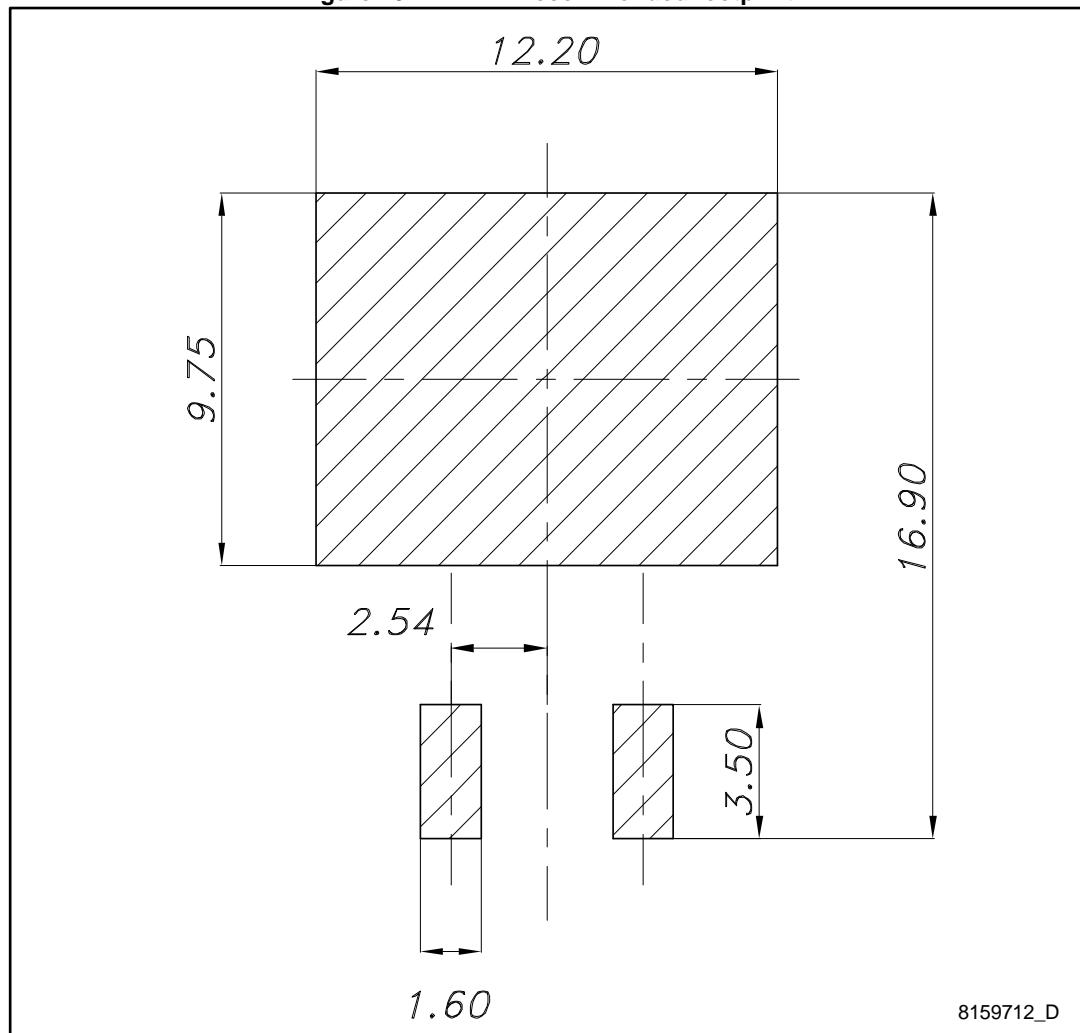
Figure 19: H²PAK-2 outline

Table 8: H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint

4.2 Packing information

Figure 21: Tape outline

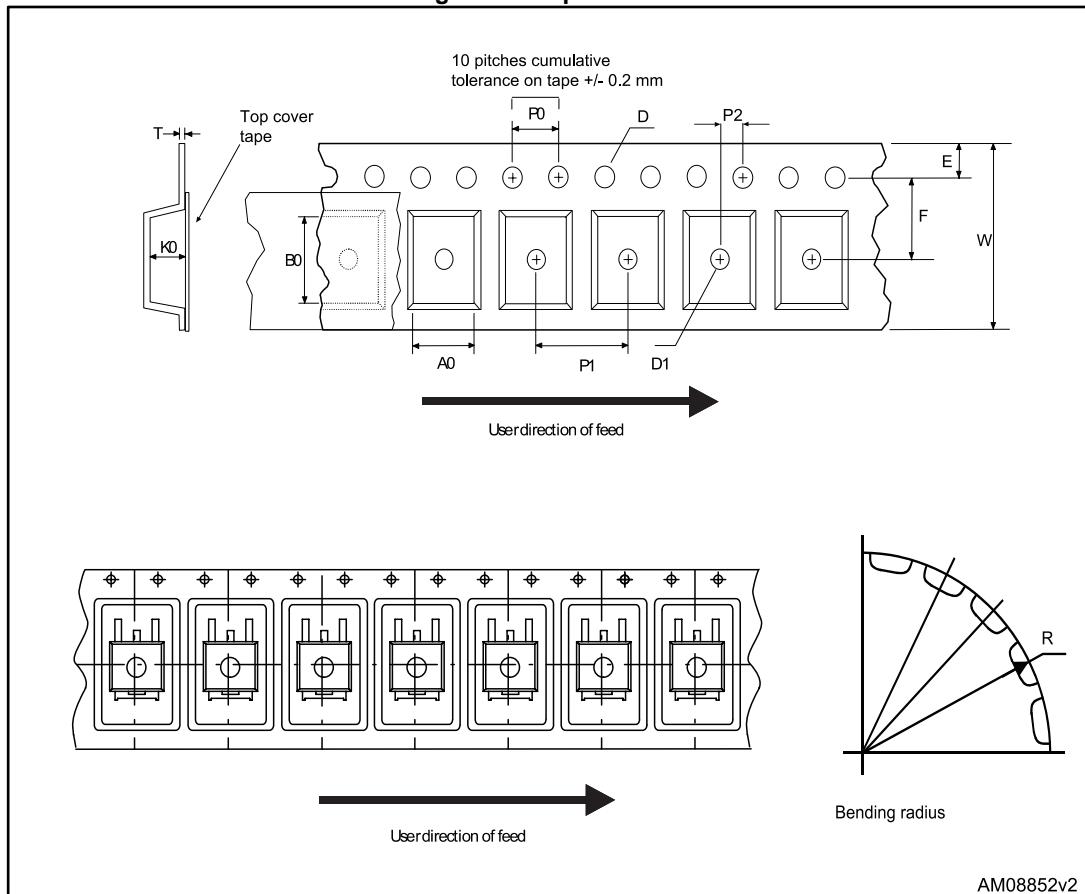


Figure 22: Reel outline

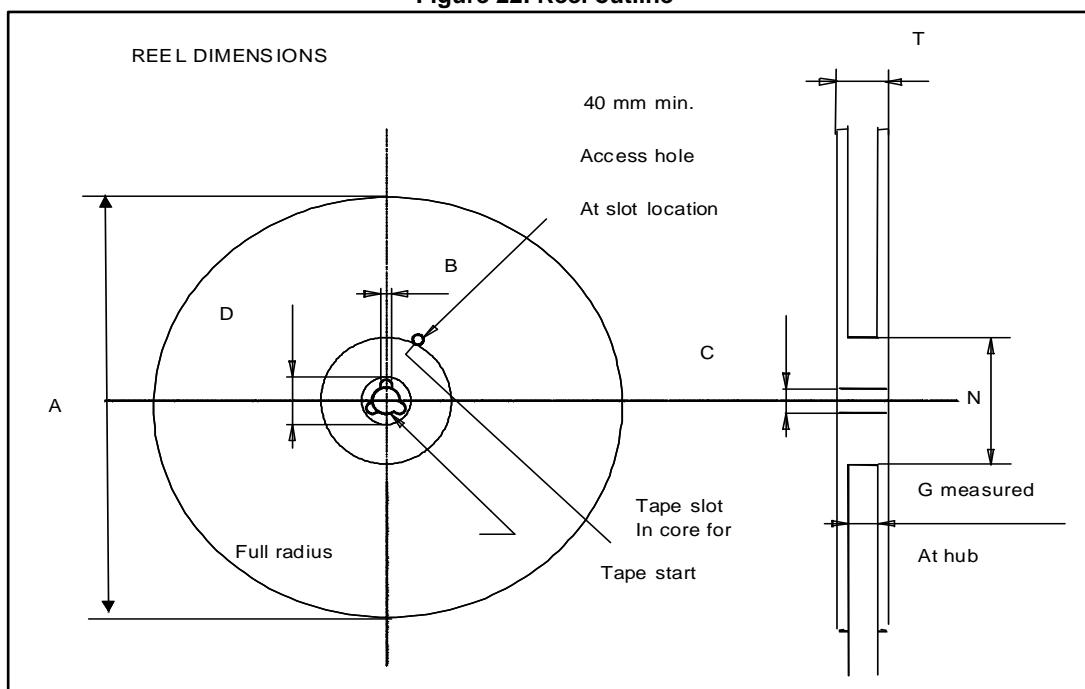


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
18-Jul-2011	1	First version
26-Nov-2014	2	<ul style="list-style-type: none">• Modified fig 2.• Updated package mechanical data.• Updated the title, features and description.

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