



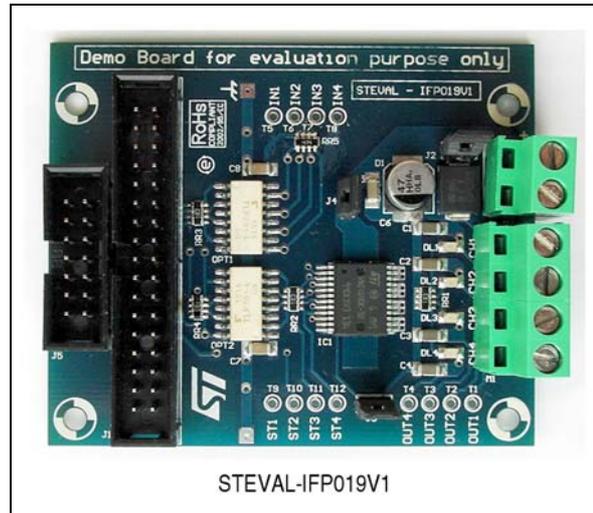
STEVAL-IFP019V1

Quad high-side smart-power solid-state relay demonstration board based on the VNI4140K-32

Data brief

Features

- Output current: 1 A per channel
- Shorted load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown non-simultaneous restart for the various channels
- Protection against loss of ground
- Current limitation
- Undervoltage shutdown
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2
- RoHS compliant



STEVAL-IFP019V1

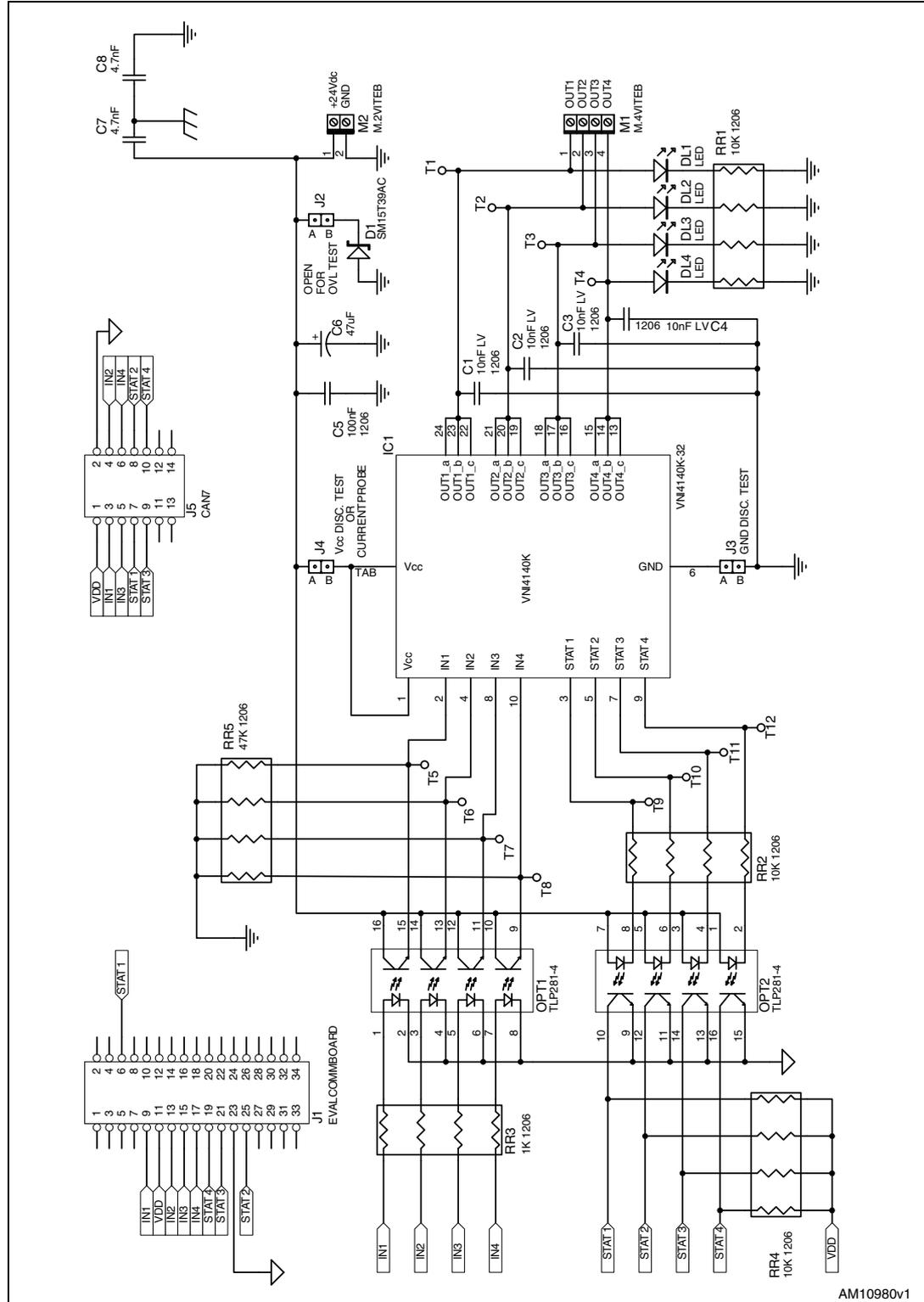
Description

The STEVAL-IFP019V1 demonstration board shows the features of the VNI4140K-32 quad high-side smart-power solid-state relay.

The application offers robustness and complies with EMC industrial standards. It implements short-circuit/overload protection and also thermal management, achieving best-in-class MTBF values. The reference design is suitable for use in programmable logic controllers (PLCs) as well as to drive generic loads which require up to 1 A of nominal current (the typical current limitation is 1.1 - 2.6 A). Thanks to the very low $R_{DS(on)}$ (only 80 m Ω typical @ 25 °C per channel) the device allows very low power consumption during operation and for this reason it offers an ideal solution for IP65 / IP67 requirements. The VNI4140K-32 is compliant with IEC 61131-2 (international standard for programmable controllers).

1 Schematic circuit

Figure 1. Schematic circuit



AM10980v1

2 Connectors

The STEVAL-IFP019V1 demonstration board uses input header connectors; one screw drives the four-channel output connector and one screw drives the two-channel supply connector.

Both input connectors, J5 and J1, provide the same bi-directional demonstration board signalization guaranteeing maximum compatibility with existing ST tools.

Figure 2. J1 connector pinout

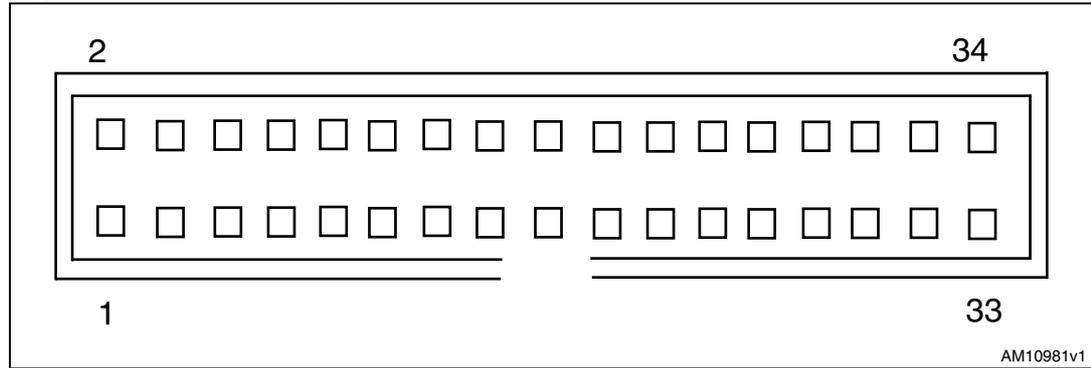


Figure 3. J5 connector pinout

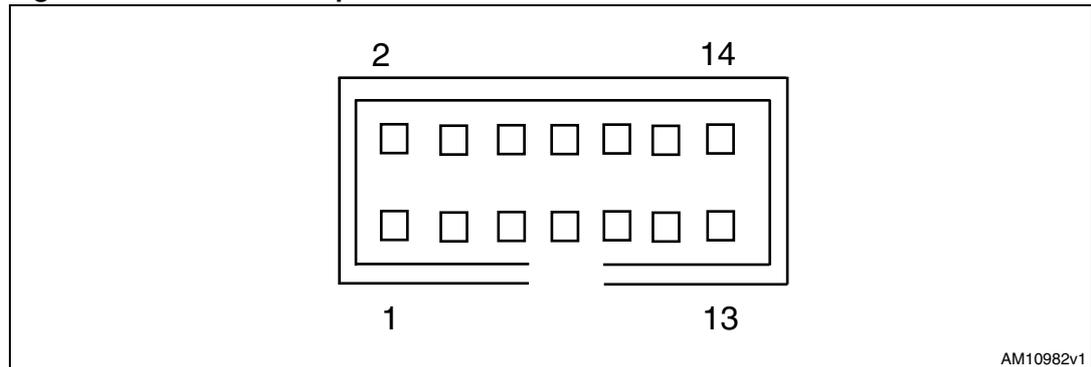


Table 1. Connector J1 and J5 pinout mapping

| J1 pin number | J5 pin number | Signal | Type |
|---------------|---------------|-----------------|--------------------------|
| 11 | 1 | V _{dd} | 5 / 3.3 V supply voltage |
| 23 | 2 | GND | Signal ground |
| 9 | 3 | IN1 | Input channel 1 |
| 13 | 4 | IN2 | Input channel 2 |
| 15 | 5 | IN3 | Input channel 3 |
| 17 | 6 | IN4 | Input channel 4 |
| 6 | 7 | STAT1 | Status channel 1 |
| 25 | 8 | STAT2 | Status channel 2 |
| 21 | 9 | STAT3 | Status channel 3 |
| 19 | 10 | STAT4 | Status channel 4 |

3 Revision history

Table 2. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 19-Dec-2011 | 1 | Initial release. |

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