

## Medium current, high performance, low voltage PNP transistor

### Features

- Very low collector to emitter saturation voltage
- DC current gain,  $h_{FE} > 100$
- 3 A continuous collector current
- 40 V breakdown voltage  $V_{(BR)CER}$
- Surface mounting DPAK (TO-252) power package in tape and reel packing

### Applications

- Power management in portable equipment
- Voltage regulation in bias supply circuits
- Switching regulator in battery charger applications
- Heavy load driver

### Description

The device is manufactured in low voltage PNP planar technology by using a "Base Island" layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

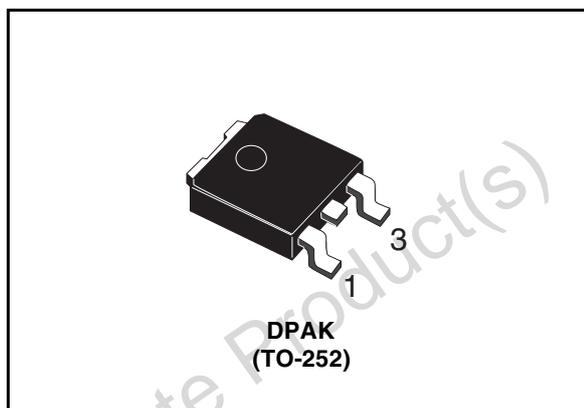


Figure 1. Internal schematic diagram

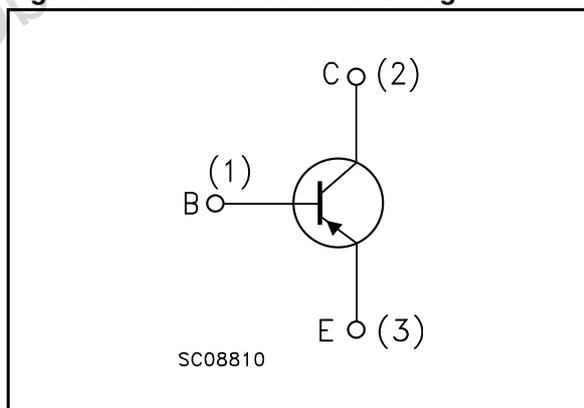


Table 1. Device summary

Order code	Marking	Package	Packaging
STD790AT4	D790A	DPAK	Tape and reel

# 1 Electrical ratings

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-base voltage ( $I_E = 0$ )	-40	V
$V_{CER}$	Collector-emitter voltage ( $R_{BE} = 47 \Omega$ )	-40	V
$V_{CEO}$	Collector-emitter voltage ( $I_B = 0$ )	-30	V
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ )	-5	V
$I_C$	Collector current	-3	A
$I_{CM}$	Collector peak current ( $t_p < 5$ ms)	-6	A
$P_{tot}$	Total dissipation at $T_C = 25$ °C	15	W
$T_{stg}$	Storage temperature	-65 to 150	°C
$T_J$	Max. operating junction temperature	150	°C

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	8.33	°C/W

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>CBO</sub>	Collector cut-off current (I <sub>E</sub> = 0)	V <sub>CB</sub> = -30 V			-10	μA
		V <sub>CB</sub> = -30 V; T <sub>C</sub> = 100 °C			-100	μA
I <sub>EBO</sub>	Emitter cut-off current (I <sub>C</sub> = 0)	V <sub>EB</sub> = -4 V			-10	μA
V <sub>(BR)CEO</sub> <sup>(1)</sup>	Collector-emitter breakdown voltage (I <sub>B</sub> = 0)	I <sub>C</sub> = -10 mA	-30			V
V <sub>(BR)CER</sub> <sup>(1)</sup>	Collector-emitter breakdown voltage (R <sub>BE</sub> = 47 Ω)	I <sub>C</sub> = -10 mA	-40			V
V <sub>(BR)CBO</sub>	Collector-base breakdown voltage (I <sub>E</sub> = 0)	I <sub>C</sub> = -100 μA	-40			V
V <sub>(BR)EBO</sub>	Emitter-base breakdown voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = -100 μA	-5			V
V <sub>CE(sat)</sub> <sup>(1)</sup>	Collector-emitter saturation voltage	I <sub>C</sub> = -0.5 A I <sub>B</sub> = -5 mA			-0.15	V
		I <sub>C</sub> = -1.2 A I <sub>B</sub> = -20 mA			-0.25	V
		I <sub>C</sub> = -2 A I <sub>B</sub> = -20 mA			-0.5	V
		I <sub>C</sub> = -3 A I <sub>B</sub> = -100 mA			-0.7	V
		I <sub>C</sub> = -3 A I <sub>B</sub> = -100 mA T <sub>J</sub> = 100 °C			-0.9	V
V <sub>BE(sat)</sub> <sup>(1)</sup>	Base-emitter saturation voltage	I <sub>C</sub> = -1 A I <sub>B</sub> = -10 mA		-0.8	-1	V
V <sub>BE(on)</sub> <sup>(1)</sup>	Base-emitter on voltage	I <sub>C</sub> = -1 A V <sub>CE</sub> = -2 V		-0.8	-1	V
h <sub>FE</sub> <sup>(1)</sup>	DC current gain	I <sub>C</sub> = -10 mA V <sub>CE</sub> = -2 V	100	200	400	
		I <sub>C</sub> = -500 mA V <sub>CE</sub> = -2 V	100	200	400	
		I <sub>C</sub> = -1 A V <sub>CE</sub> = -2 V	100			
		I <sub>C</sub> = -2 A V <sub>CE</sub> = -1 V	100	160		
		I <sub>C</sub> = -3 A V <sub>CE</sub> = -1 V	90	130		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$f_t$	Transition frequency	$I_C = -50 \text{ mA}$ $V_{CE} = -5 \text{ V}$ $f = 50 \text{ MHz}$		100		MHz
$t_d$	Resistive load Delay time	$I_C = -3 \text{ A}$ $V_{CC} = -20 \text{ V}$		180	220	ns
$t_r$	Rise time	$I_{B1} = -I_{B2} = -60 \text{ mA}$		160	210	ns
$t_s$	Storage time	see <a href="#">Figure 8</a>		250	300	ns
$t_f$	Fall time			80	100	ns

1. Pulse duration = 300  $\mu\text{s}$ , duty cycle  $\leq 1.5\%$

## 2.1 Electrical characteristics (curves)

Figure 2. DC current gain

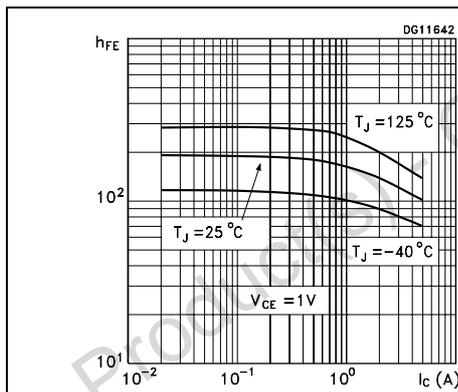


Figure 3. DC current gain

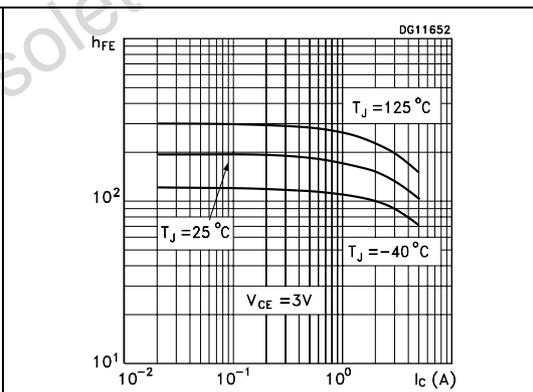


Figure 4. Collector-emitter saturation voltage

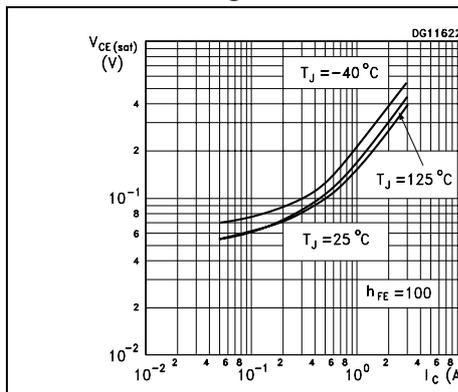


Figure 5. Base-emitter saturation voltage

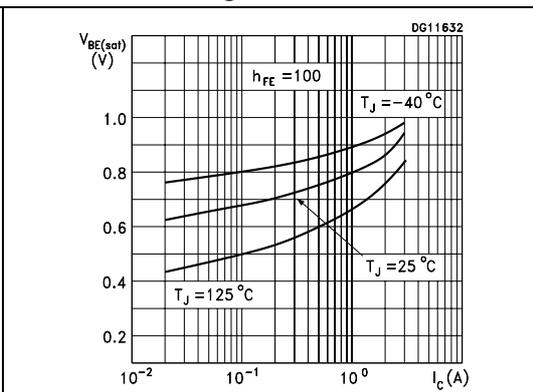
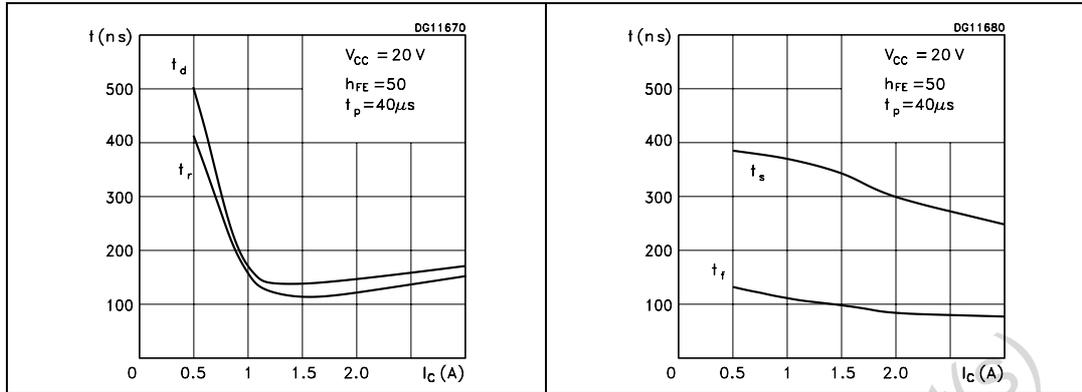
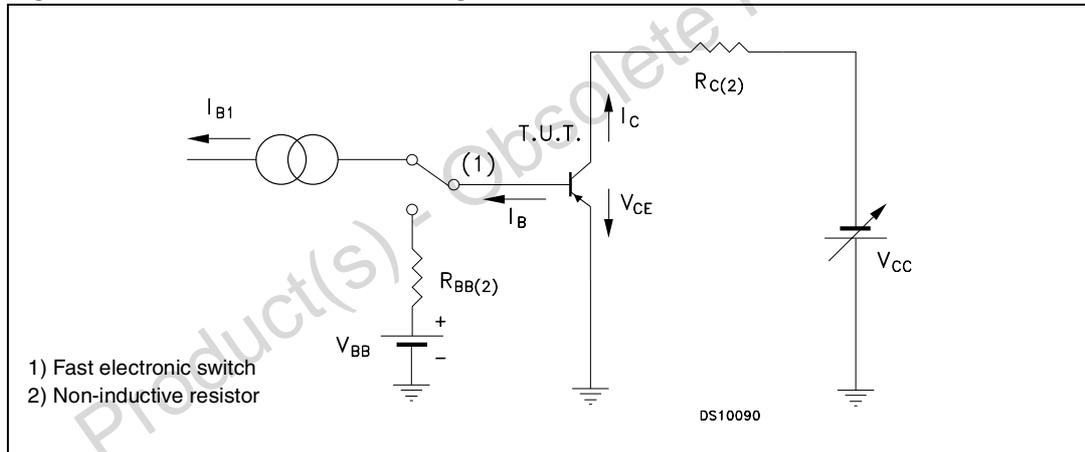


Figure 6. Switching time resistive load Figure 7. Switching time resistive load



## 2.2 Test circuit

Figure 8. Resistive load switching test circuit



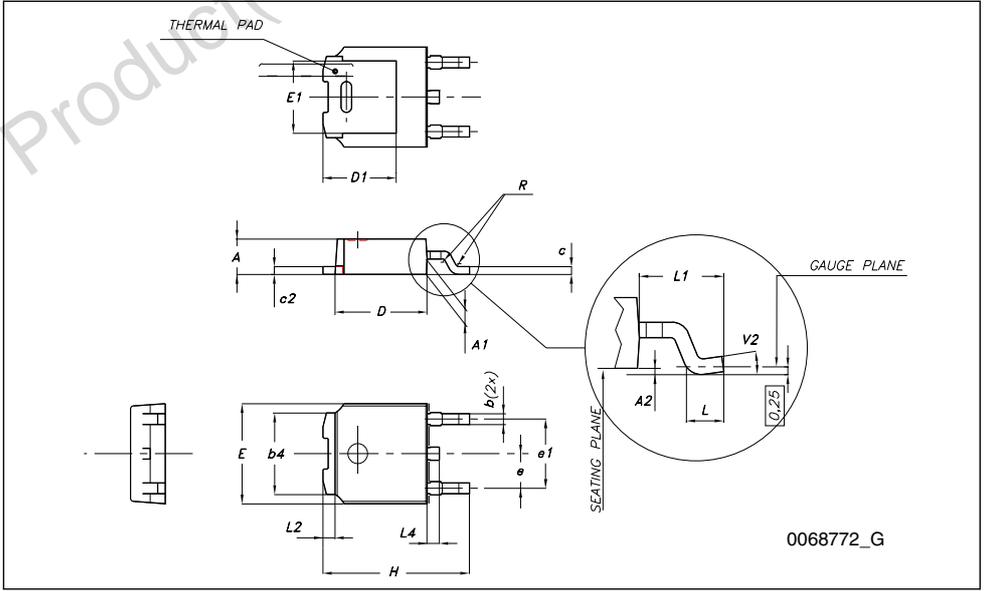
### 3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



## 4 Revision history

**Table 5. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
24-Mar-2004	1	Initial release.
27-Mar-2006	2	New template, new graphics
25-Jun-2008	3	Updated TO-252 mechanical data

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