STD2N80K5, STF2N80K5, STP2N80K5, STU2N80K5

N-channel 800 V, 3.5 Ω typ., 2 A MDmesh™ K5 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK packages

Datasheet − production data

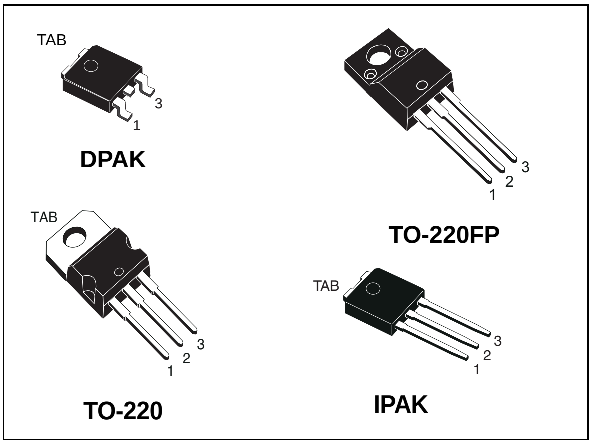
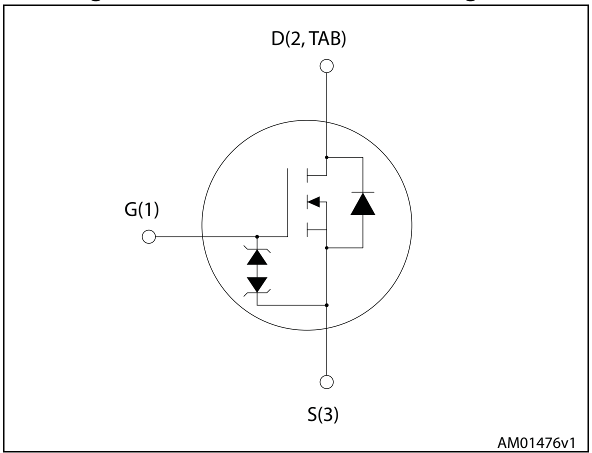


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$max	I_D	P_{TOT}
STD2N80K5	800 V	4.5 Ω	2 A	45 W
STF2N80K5				20 W
STP2N80K5				45 W
STU2N80K5				

- Industry's lowest $R_{DS(on)}$ * area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD2N80K5	2N80K5	DPAK	Tape and reel
STF2N80K5		TO-220FP	Tube
STP2N80K5		TO-220	
STU2N80K5		IPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V_{GS}	Gate- source voltage	30		V
I_D	Drain current (continuous) at T_C = 25 °C	2(1)		A
I_D	Drain current (continuous) at T_C = 100 °C	1.3		A
I_{DM} (2)	Drain current (pulsed)	8		A
P_{TOT}	Total dissipation at T_C = 25 °C	45	20	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	0.5		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	60.5		mJ
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		V/ns
T_j	Operating junction temperature	-55 to 150		°C
T_{stg}	Storage temperature			°C

1. For TO-220FP limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 2$ A, di/dt $\leq$ 100 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$
4. $V_{DS} \leq 640$ V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78	6.25	2.78	2.78	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb	50(1)				
$R_{thj-amb}$	Thermal resistance junction-amb		62.5		100	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V			1	µA
		V_{DS} = 800 V T_C=125 °C			50	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 1 A		3.5	4.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	105	-	pF
C_{oss}	Output capacitance		-	8	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 640 V	-	16	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	7	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0	-	18	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 2 A V_{GS} =10 V	-	5	-	nC
Q_{gs}	Gate-source charge		-	1	-	nC
Q_{gd}	Gate-drain charge		-	3.7	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 1 A, R_G=4.7 Ω, V_{GS}=10 V	-	8	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
t_f	Fall time		-	32	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
I_{SDM}(1)	Source-drain current (pulsed)		-		8	A
V_{SD}(2)	Forward on voltage	I_{SD}= 2 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 2 A, V_{DD}= 60 V di/dt = 100 A/µs,	-	255		ns
Q_{rr}	Reverse recovery charge		-	1		µC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	I_{SD}= 2 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C	-	285		ns
Q_{rr}	Reverse recovery charge		-	1.45		µC
I_{RRM}	Reverse recovery current		-	7.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA, I_D= 0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

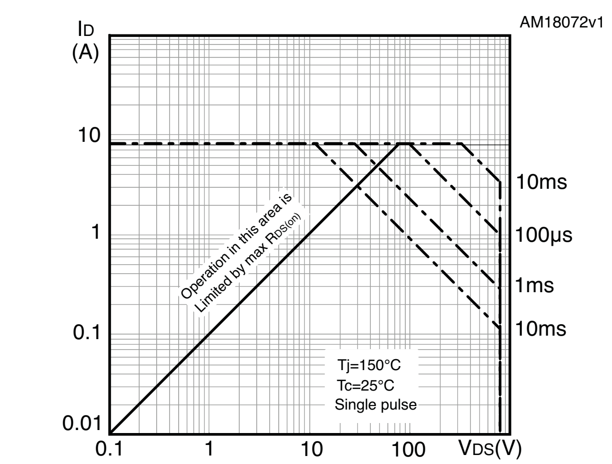


Figure 3. Thermal impedance for DPAK and IPAK

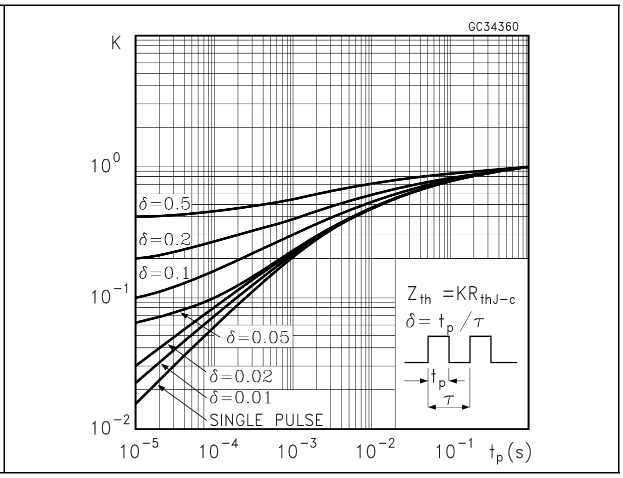


Figure 4. Safe operating area for TO-220FP

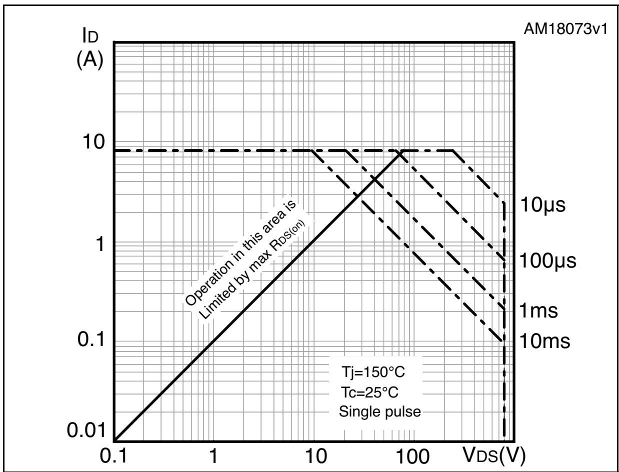


Figure 5. Thermal impedance for TO-220FP

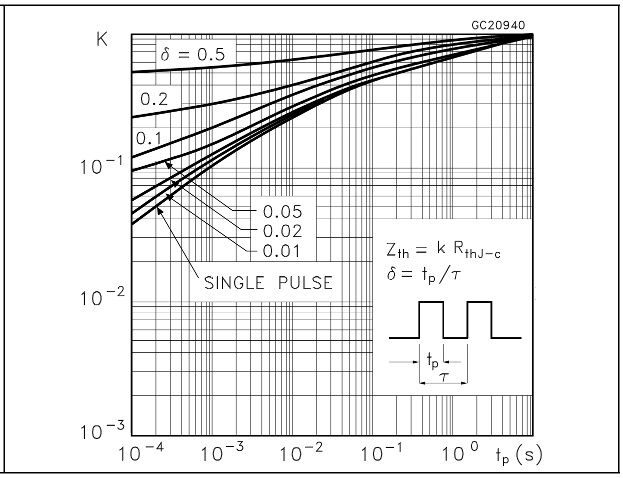


Figure 6. Safe operating area for TO-220

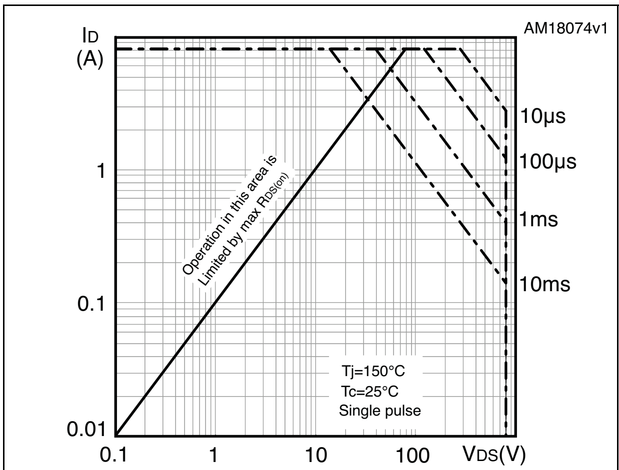


Figure 7. Thermal impedance for TO-220

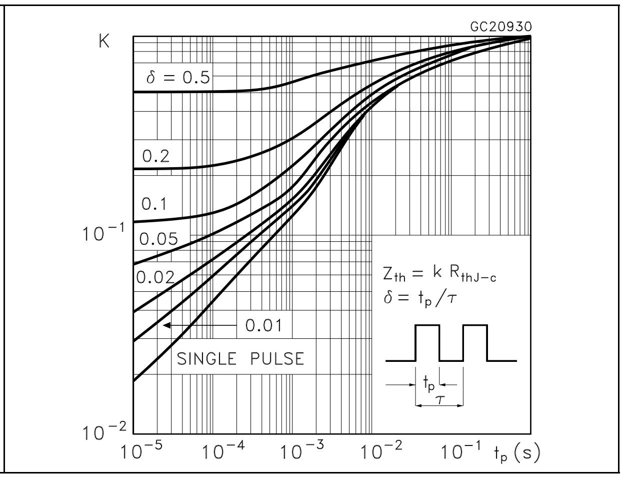


Figure 8. Output characteristics

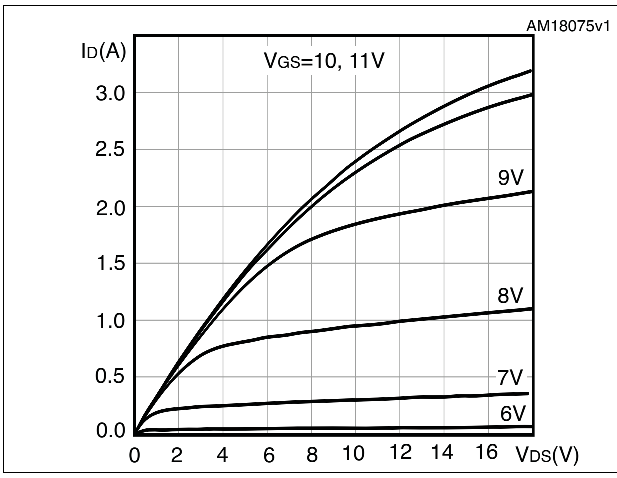


Figure 9. Transfer characteristics

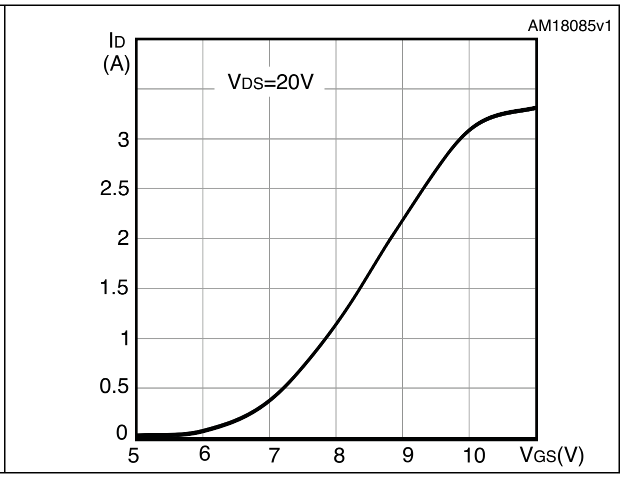


Figure 10. Gate charge vs gate-source voltage

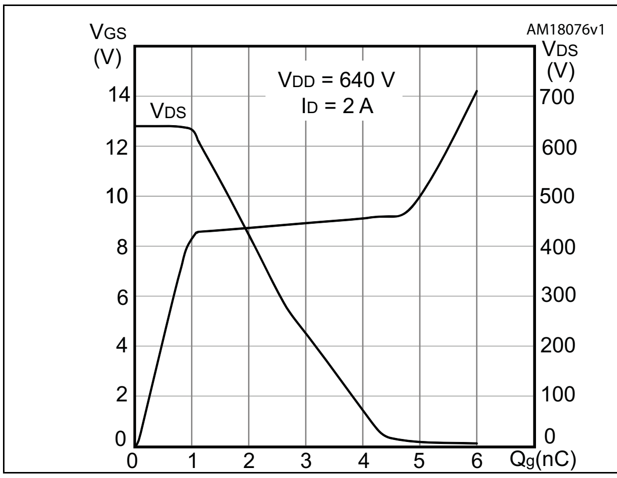


Figure 11. Static drain-source on-resistance

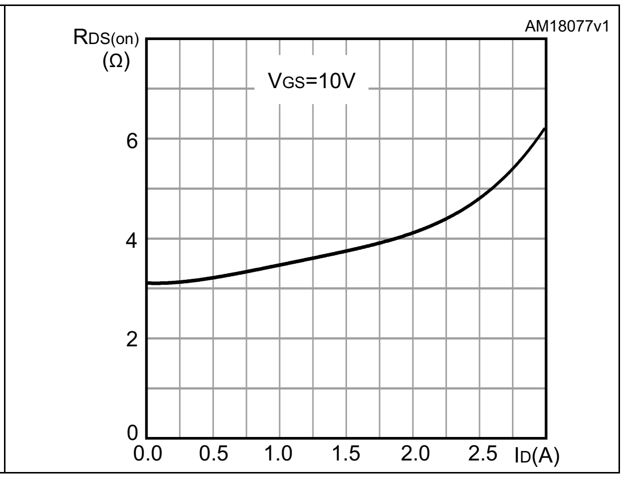


Figure 12. Capacitance variations

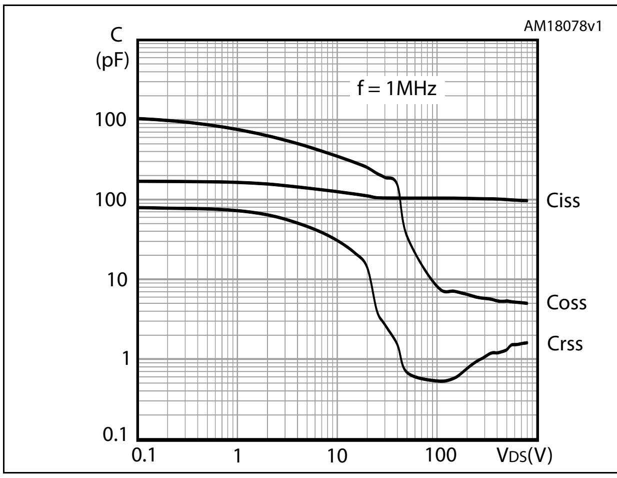


Figure 13. Output capacitance stored energy

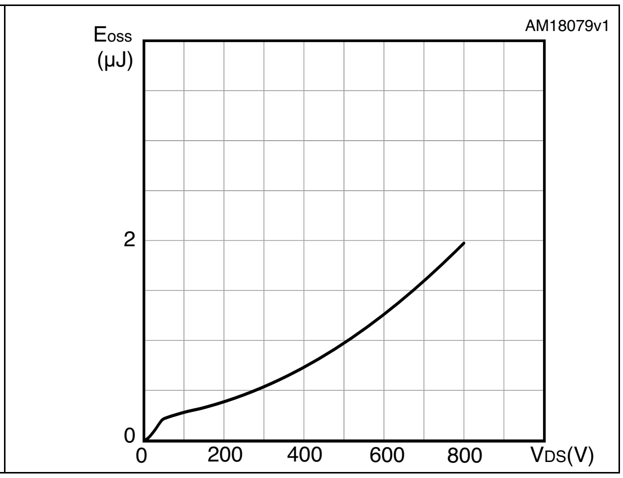


Figure 14. Normalized gate threshold voltage vs temperature

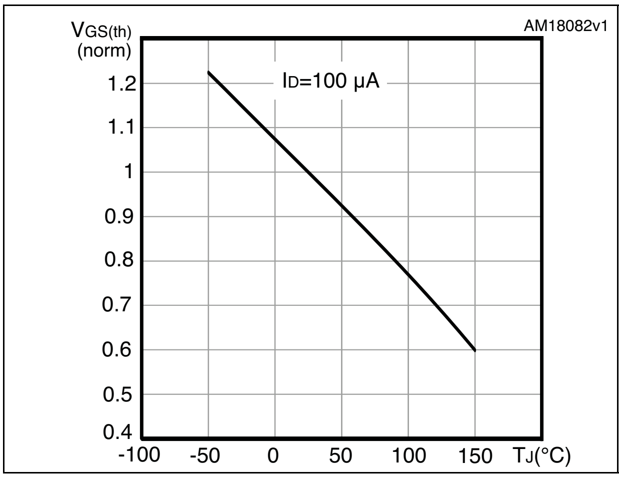


Figure 15. Normalized on-resistance vs temperature

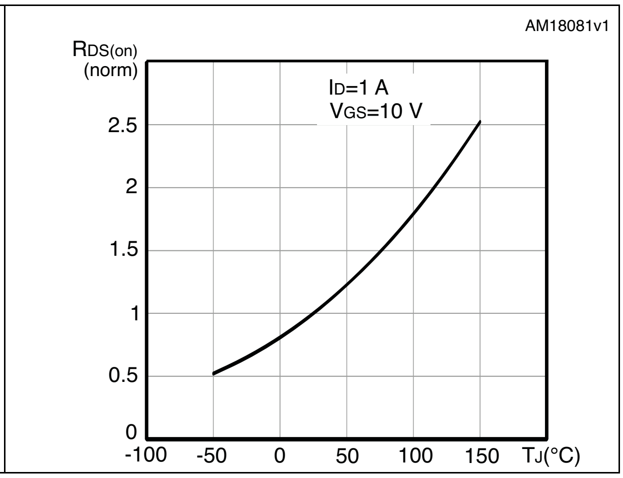


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

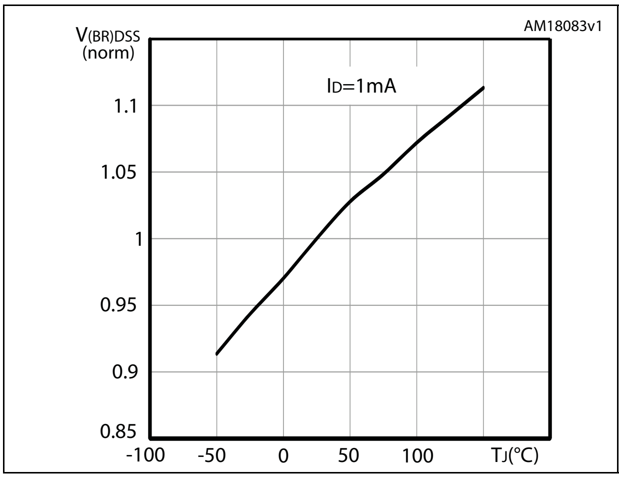


Figure 17. Source-drain diode forward characteristics

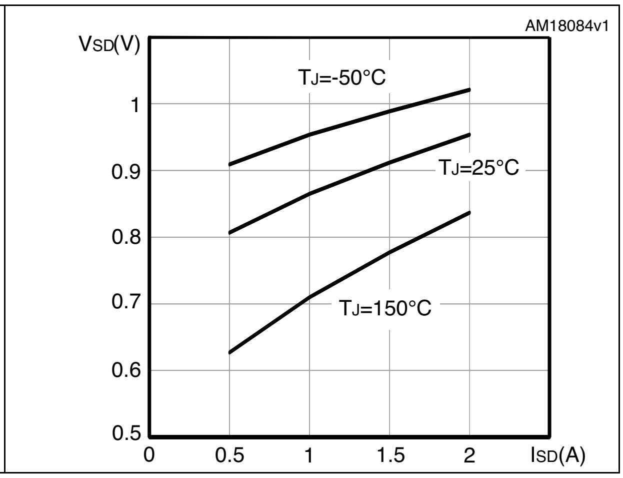
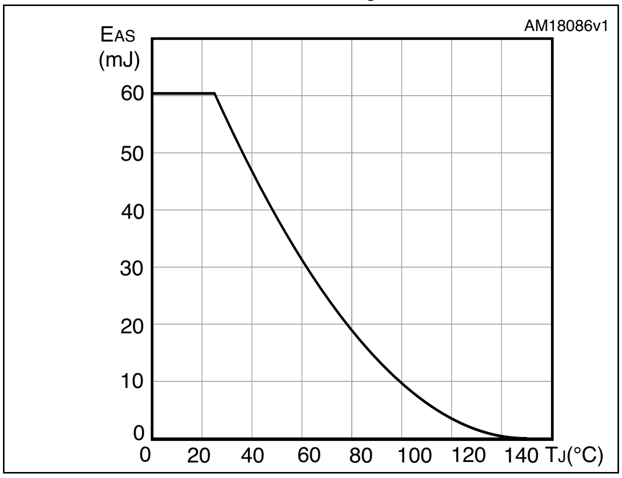


Figure 18. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 19. Switching times test circuit for resistive load

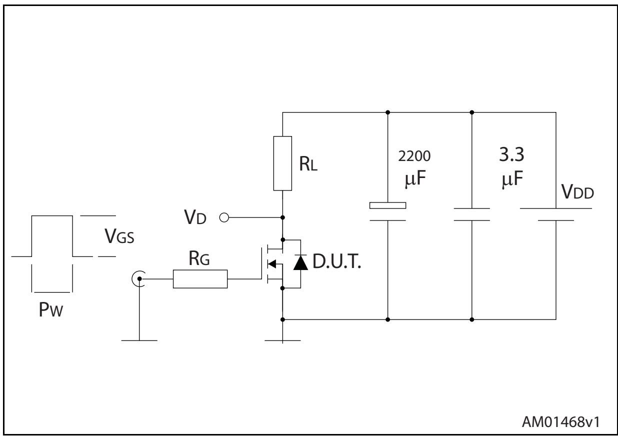


Figure 20. Gate charge test circuit

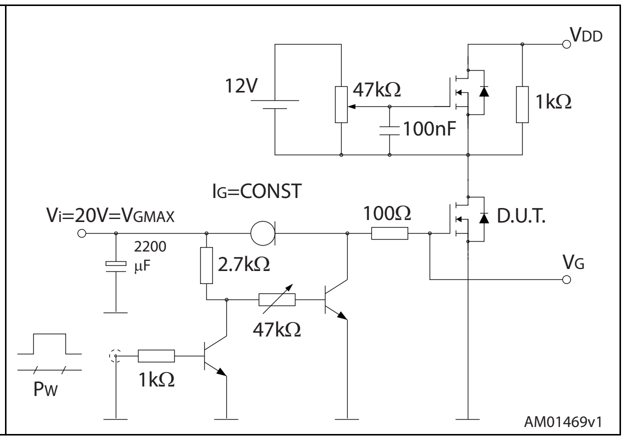


Figure 21. Test circuit for inductive load switching and diode recovery times

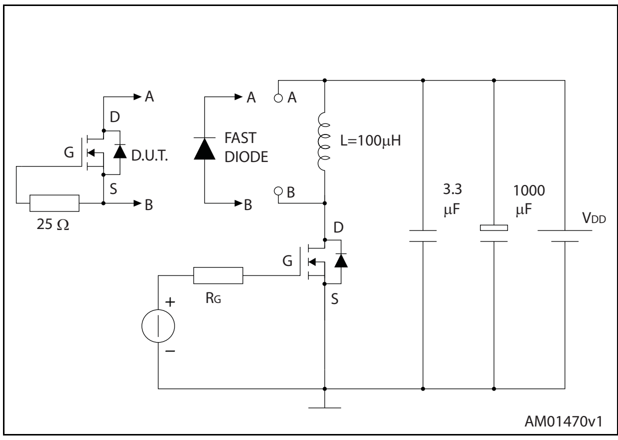


Figure 22. Unclamped inductive load test circuit

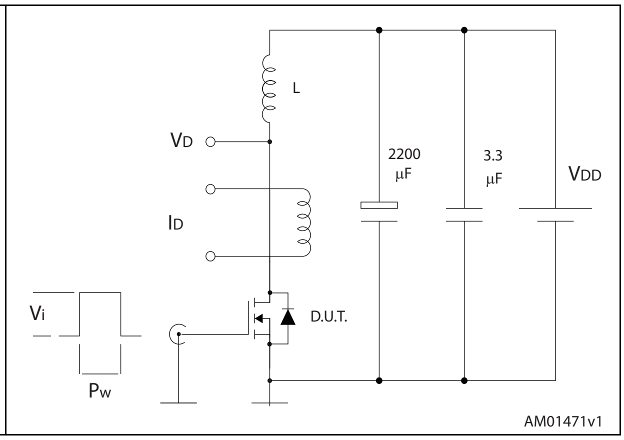


Figure 23. Unclamped inductive waveform

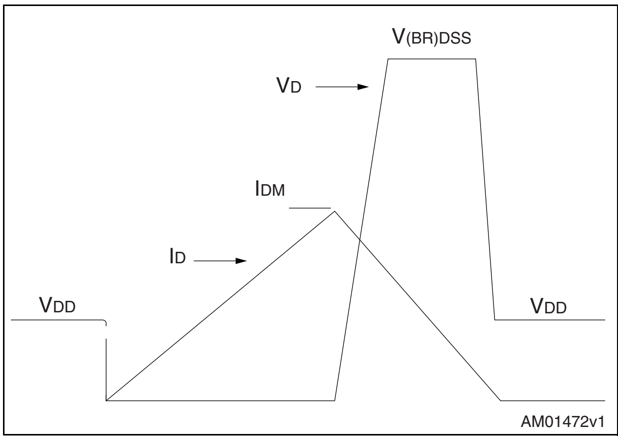
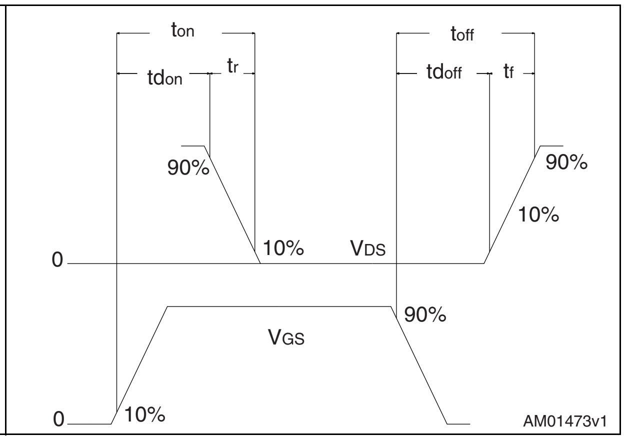


Figure 24. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 25. DPAK (TO-252) type A outline

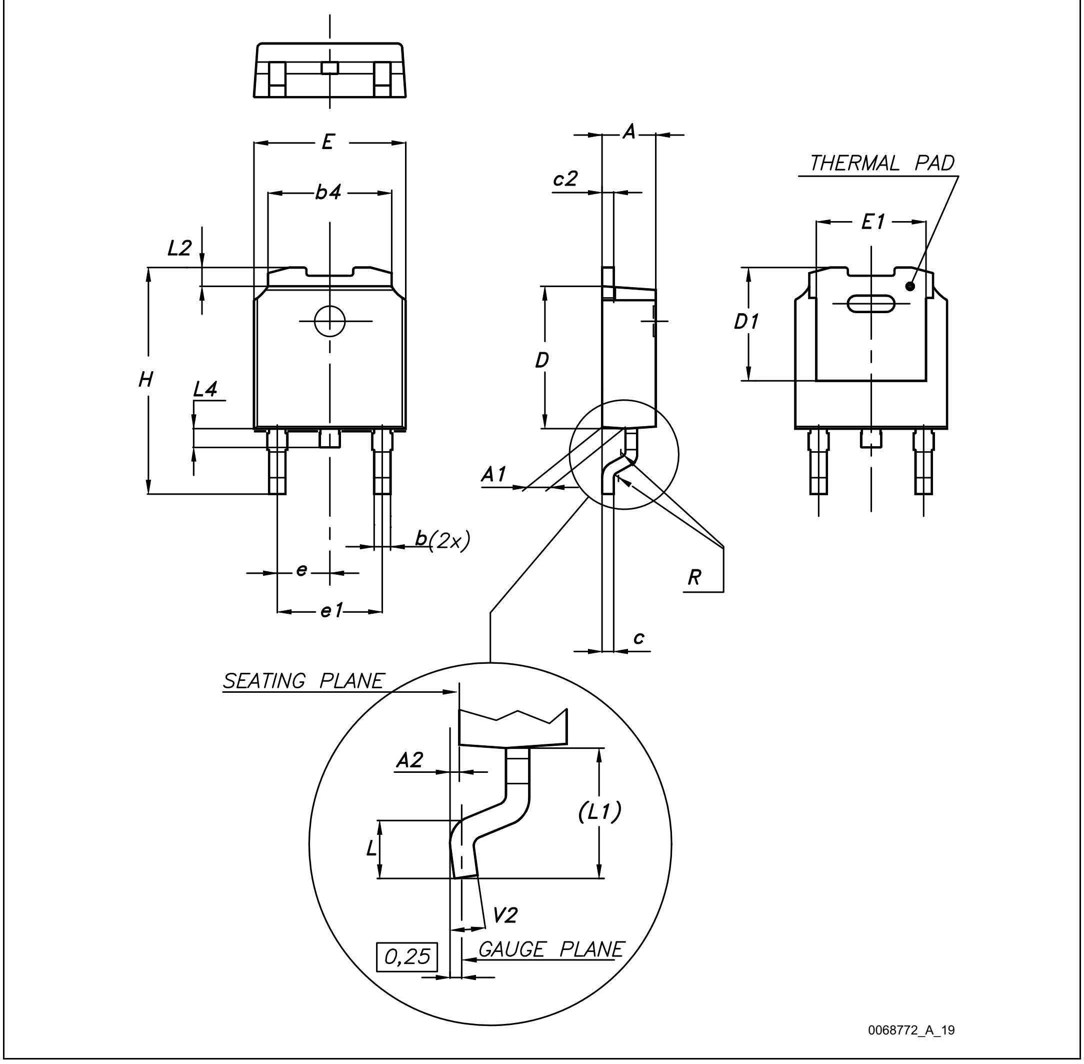
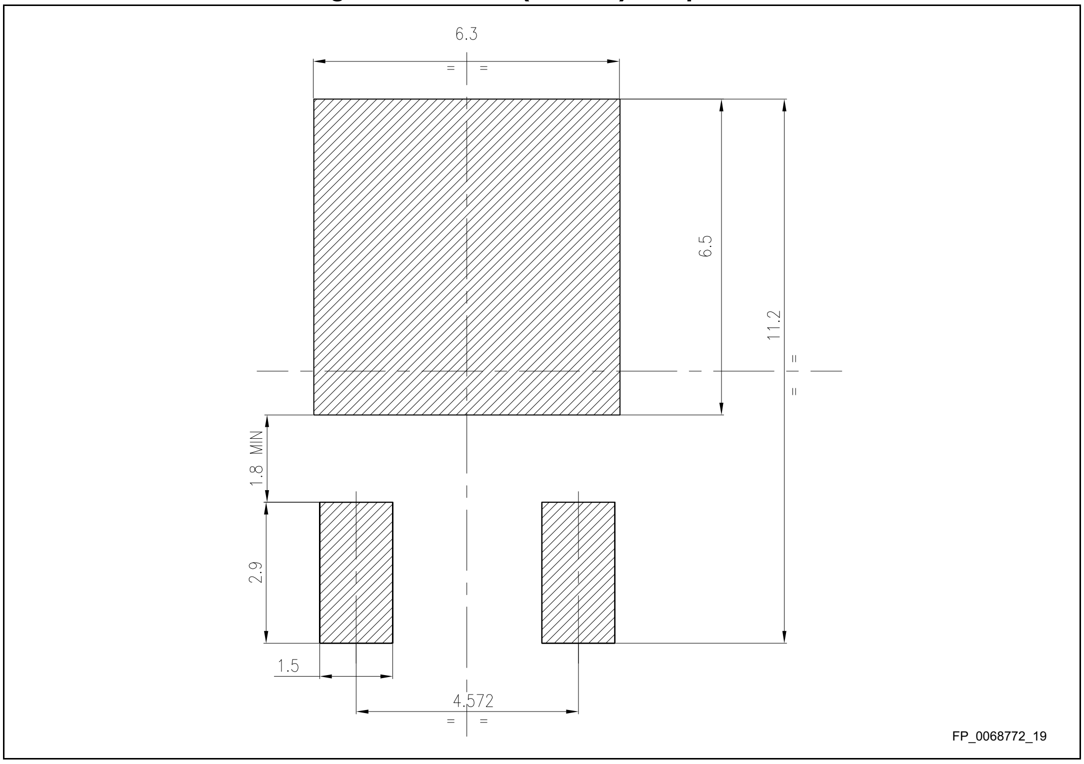


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 26. DPAK (TO-252) footprint [(a)]



a. All dimensions are in millimeters

4.2 TO-220FP package information

Figure 27. TO-220FP package outline

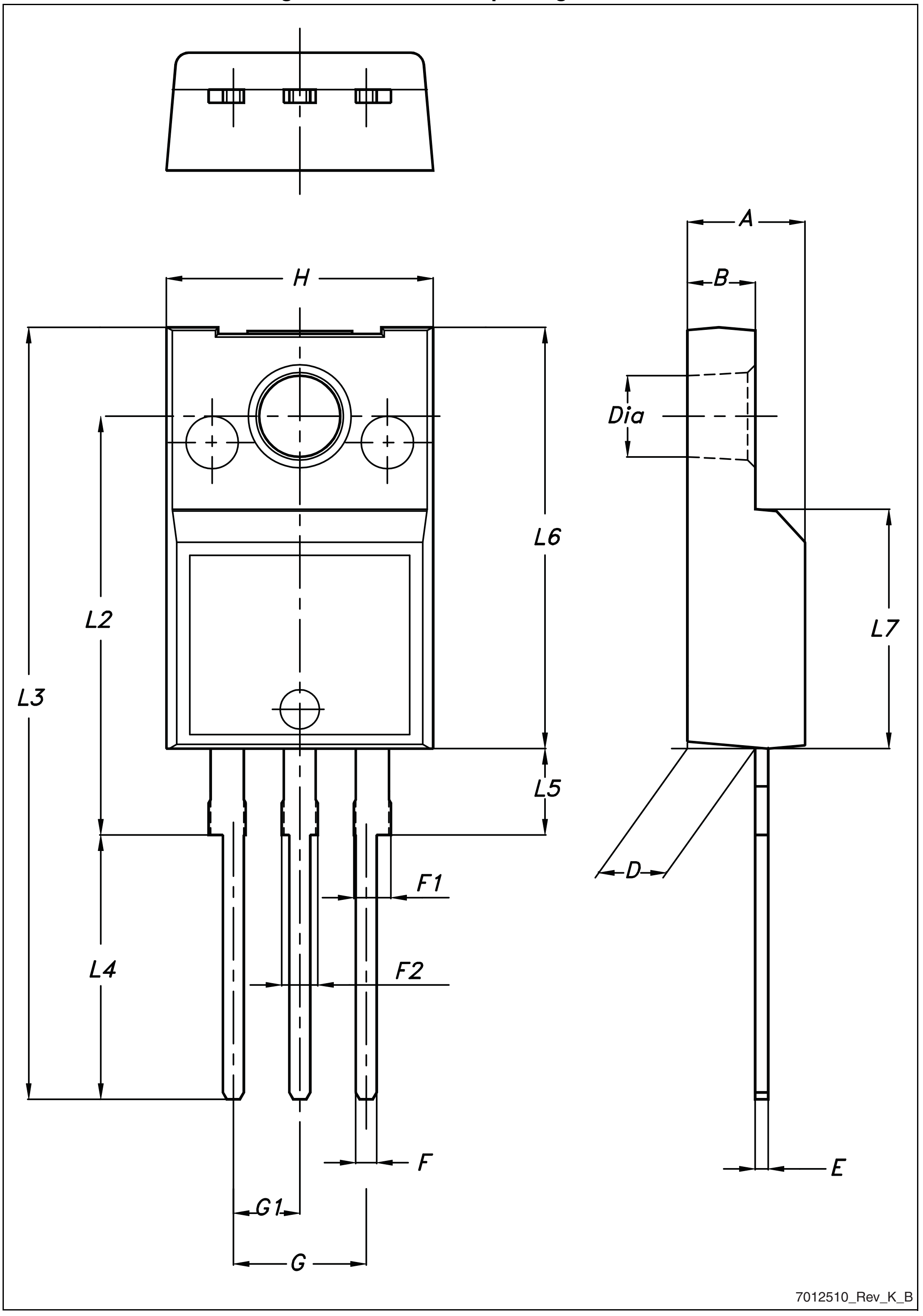


Table 10. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 TO-220 package information

Figure 28. TO-220 package outline

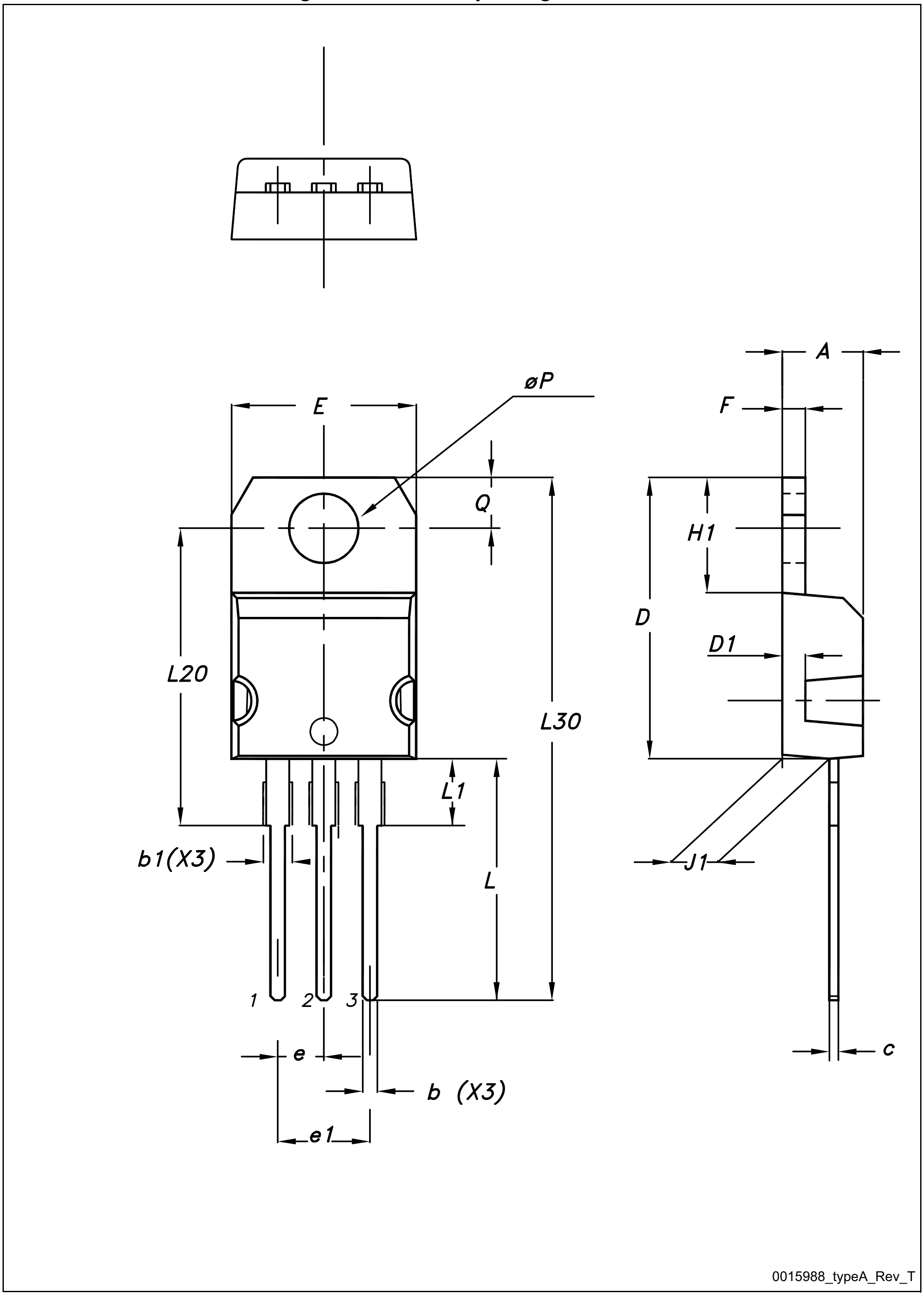


Table 11. TO-220 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

4.4 IPAK (TO-251) type A package information

Figure 29. IPAK (TO-251) type A package outline

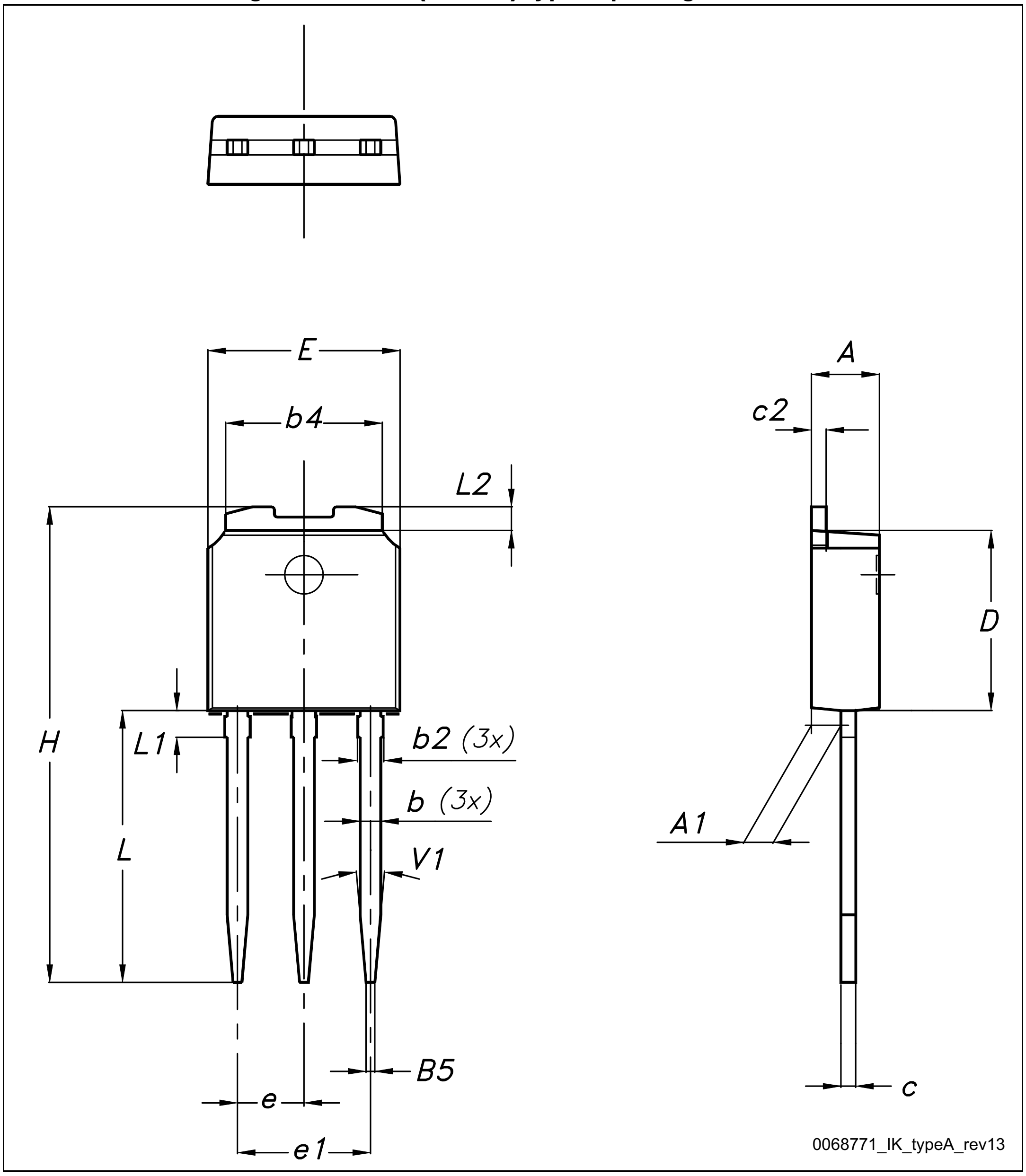


Table 12. IPAK (TO-251) type A package mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Packaging information

Figure 30. Tape for DPAK

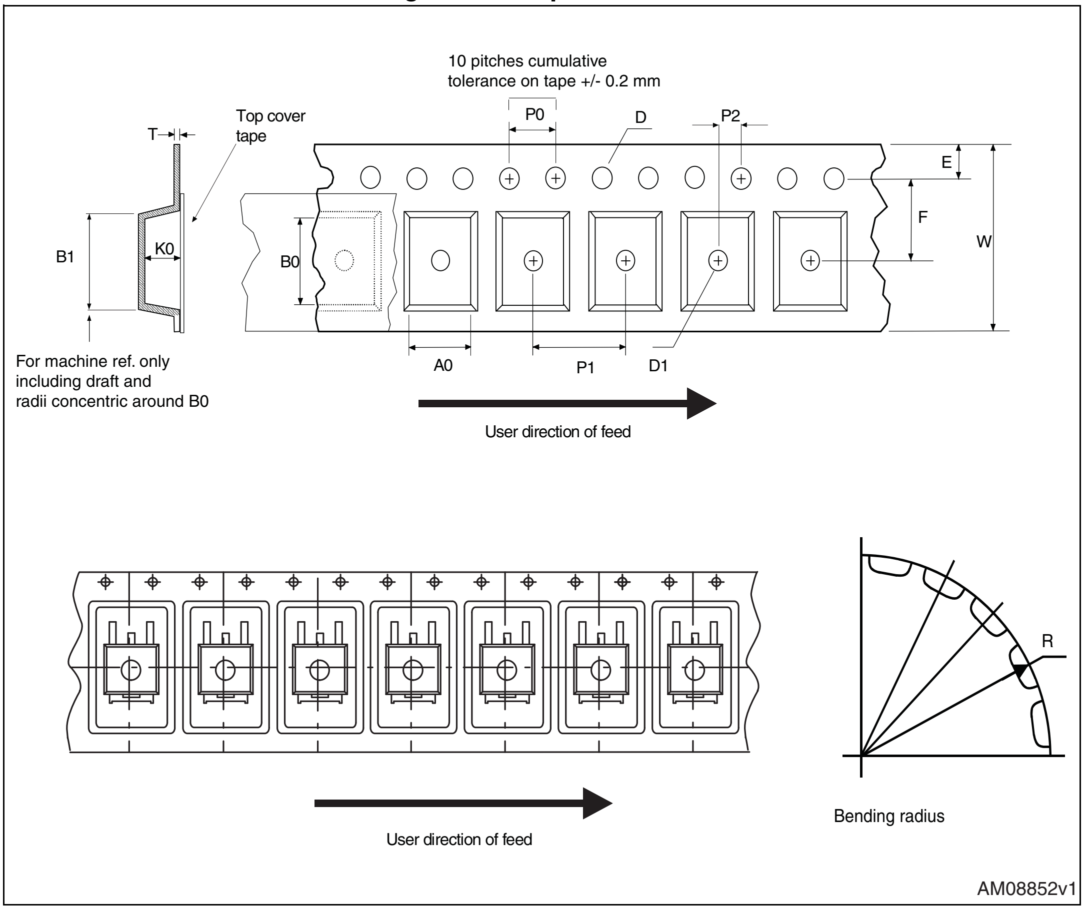


Figure 31. Reel for DPAK

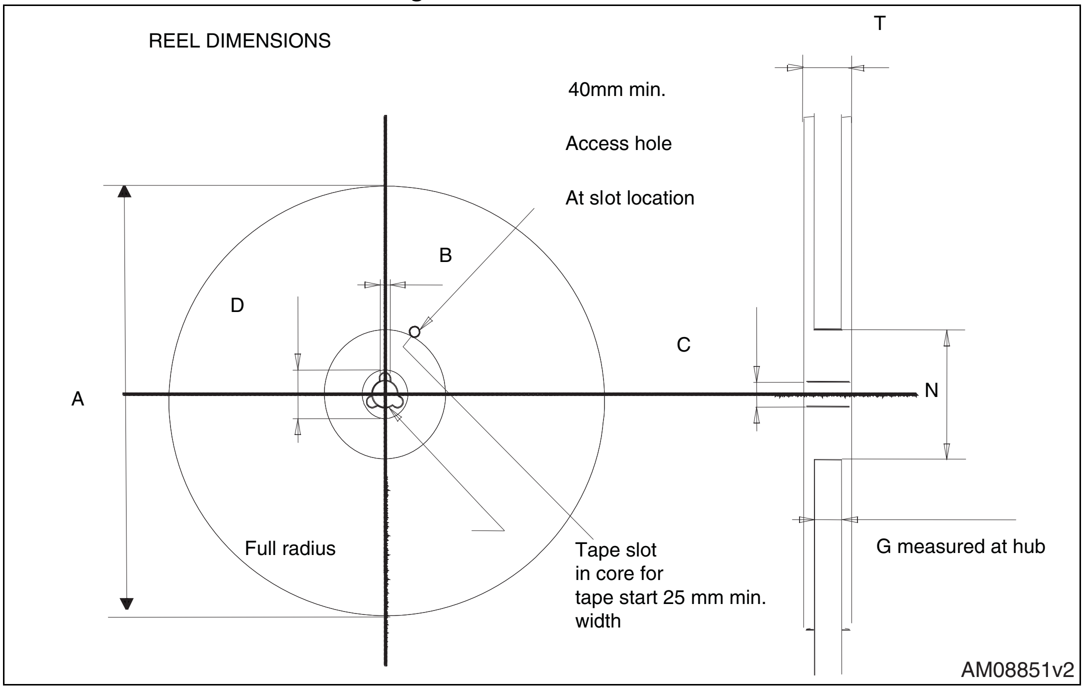


Table 13. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
11-Jul-2013	1	First release.
18-Feb-2014	2	– Added: IPAK package – Modified: E_{AS} value in *Table 2* – Modified: $R_{thj-case}$ in *Table 3* – Modified: typical values in *Table 5*, *6* and *7* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Figure 25*, *26* and *Table 9* – Added: *Table 12* and *Figure 29* – Minor text changes
25-Sep-2015	3	– Updated title, features and description in cover page. – Updated *Figure 10*, *Figure 11* and *Section 4: Package information*. – Minor text changes.