STD2N105K5, STP2N105K5, STU2N105K5

N-channel 1050 V, 6 Ω typ., 1.5 A MDmesh™ K5 Power MOSFETs in DPAK, TO-220 and IPAK packages

Datasheet - production data

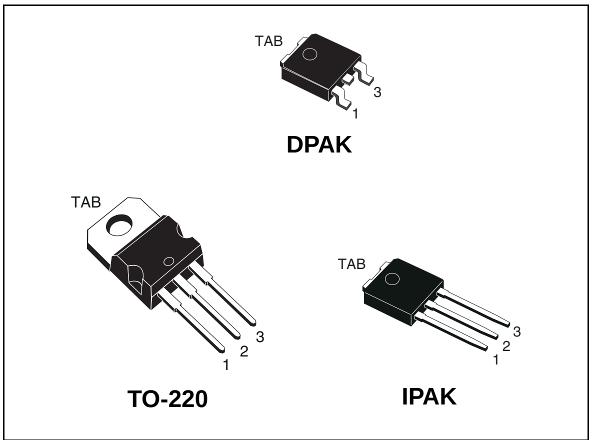
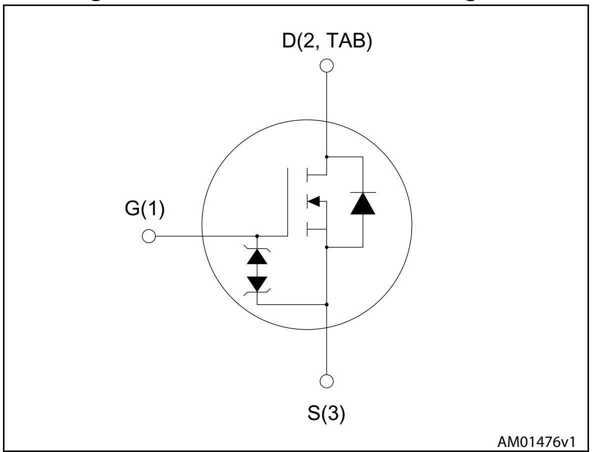


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STD2N105K5				
STP2N105K5	1050 V	8 Ω	1.5 A	60 W
STU2N105K5				

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD2N105K5		DPAK	Tape and reel
STP2N105K5	2N105K5	TO-220	Tube
STU2N105K5		IPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	1.5	A
I_D	Drain current (continuous) at T_C = 100 °C	0.95	A
I_{DM} (1)	Drain current (pulsed)	6	A
P_{TOT}	Total dissipation at T_C = 25 °C	60	W
I_{AR}	Max current during repetitive or single pulse avalanche	0.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=0.5 A, V_{DD}= 50 V)	90	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 1.5 A, di/dt ≤ 100 A/µs, $V_{DS(peak)} \leq V_{(BR)DSS}$.
3. $V_{DS} \leq$ 840 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.08	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50	°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	1050			V
I_{DSS}	Zero gate voltage, drain current (V_{GS} = 0)	V_{DS} = 1050 V			1	µA
		V_{DS} = 1050 V, T_C=125 °C			50	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V; V_{DS}=0			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.75 A		6	8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	115	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 840 V	-	17	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	6	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	20	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 1.5 A V_{GS} =10 V *(see Figure 18)*	-	10	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525 V, I_D = 0.75 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 17)*	-	14.5	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	35	-	ns
t_f	Fall time		-	38.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		1.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		6	A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 19)*	-	326		ns
Q_{rr}	Reverse recovery charge		-	1.19		µC
I_{RRM}	Reverse recovery current		-	7.3		A
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 19)*	-	525		ns
Q_{rr}	Reverse recovery charge		-	1.83		µC
I_{RRM}	Reverse recovery current		-	7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

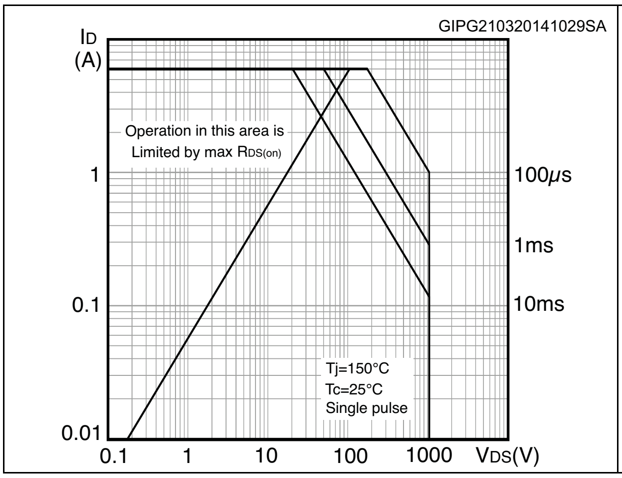


Figure 3. Thermal impedance for DPAK and IPAK

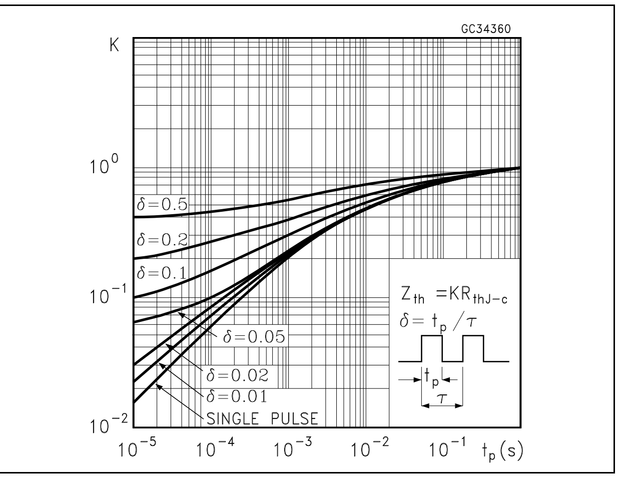


Figure 4. Safe operating area for TO-220

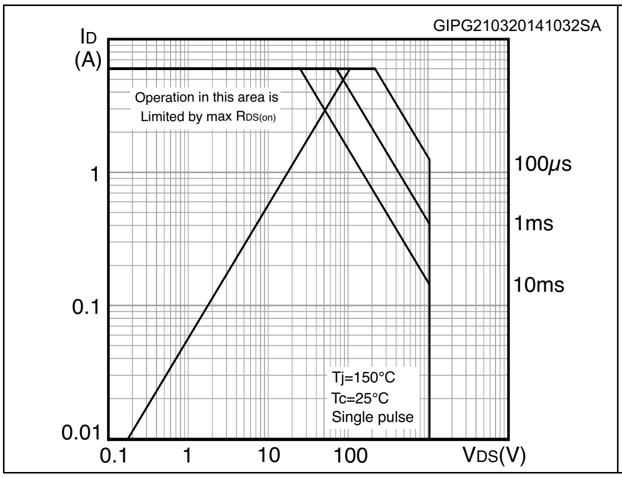


Figure 5. Thermal impedance for TO-220

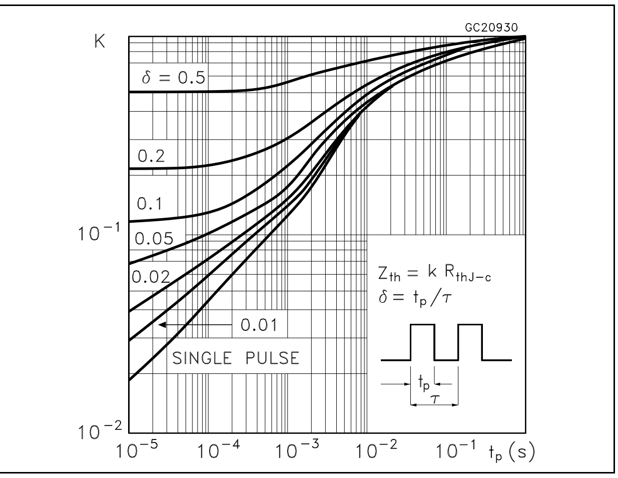


Figure 6. Output characteristics

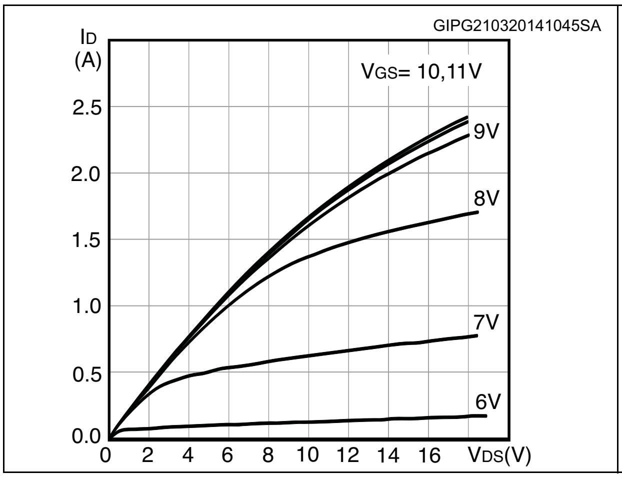


Figure 7. Transfer characteristics

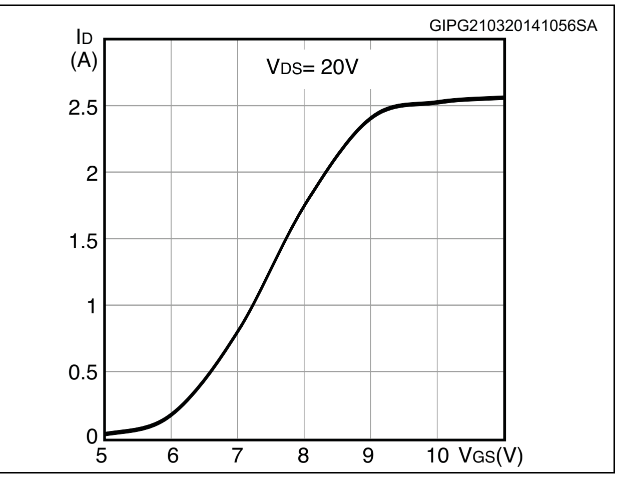


Figure 8. Gate charge vs gate-source voltage

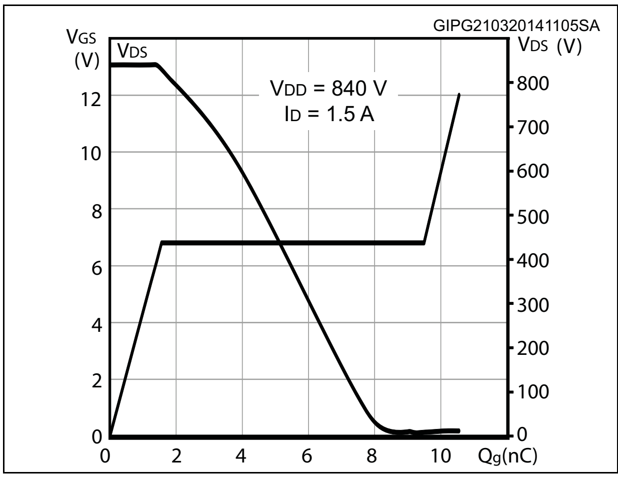


Figure 9. Static drain-source on-resistance

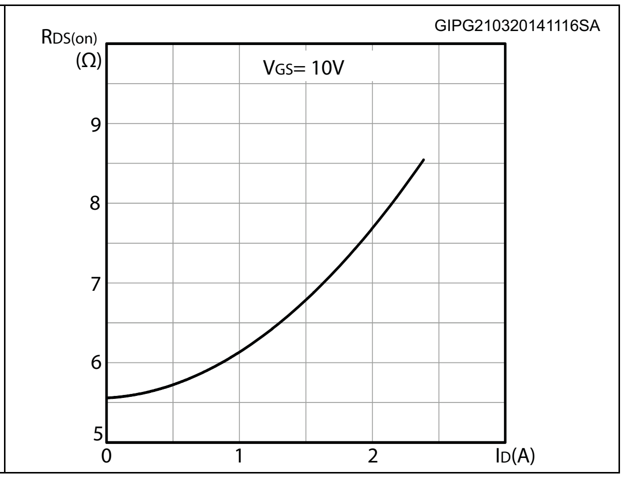


Figure 10. Capacitance variations

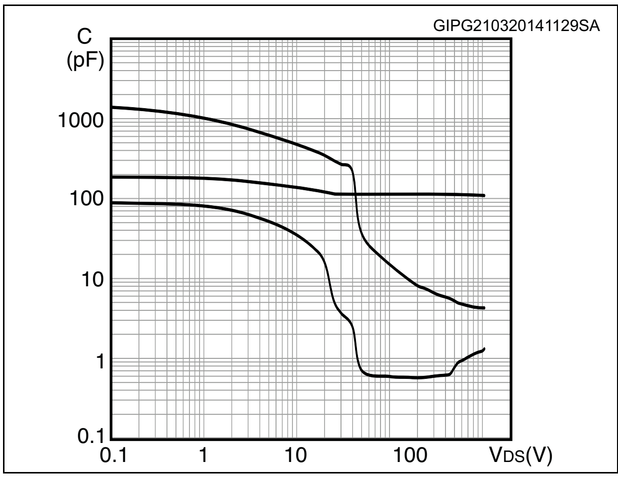


Figure 11. Output capacitance stored energy

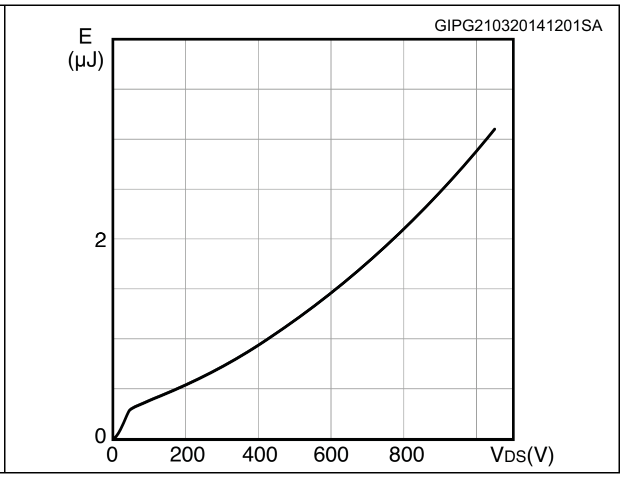


Figure 12. Normalized gate threshold voltage vs temperature

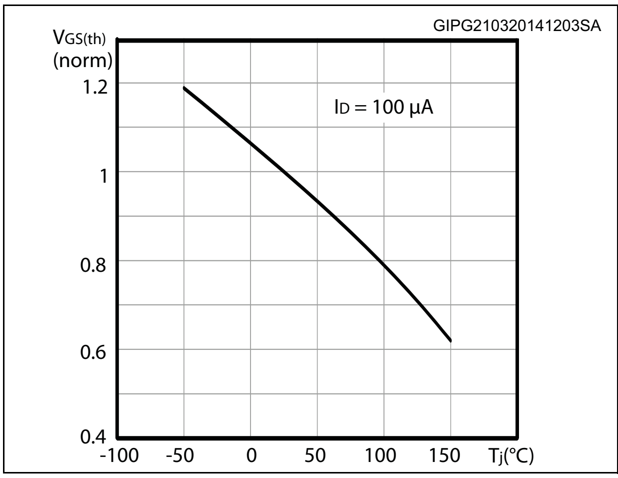


Figure 13. Normalized on-resistance vs temperature

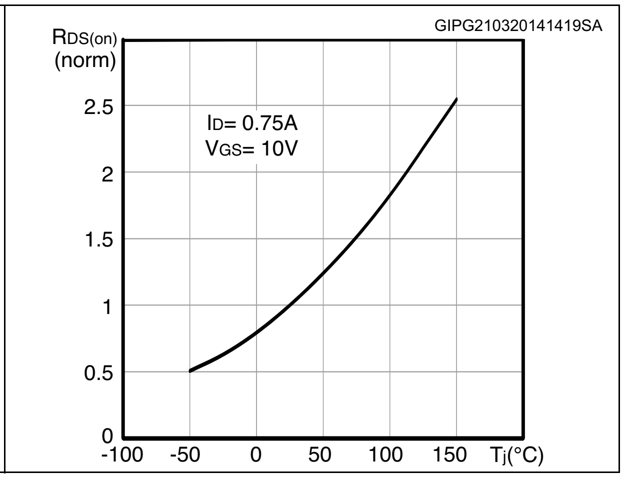


Figure 14. Source-drain diode forward characteristics

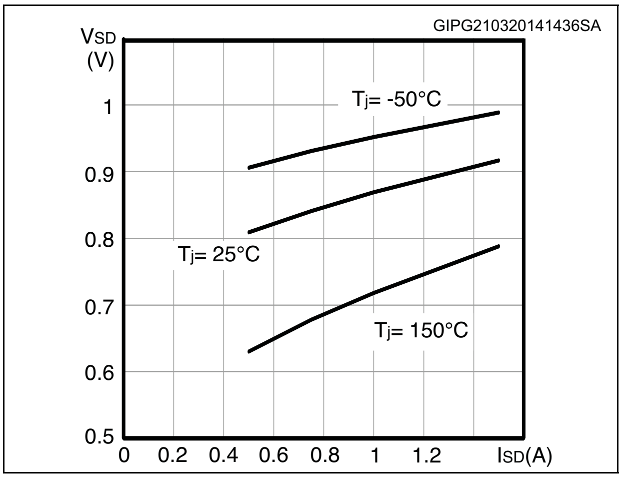


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

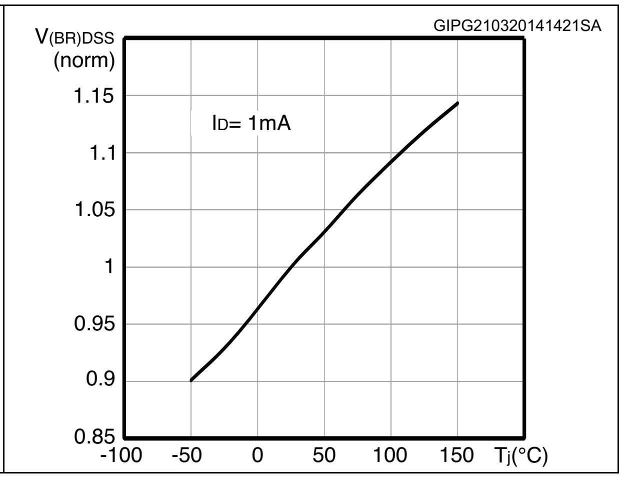
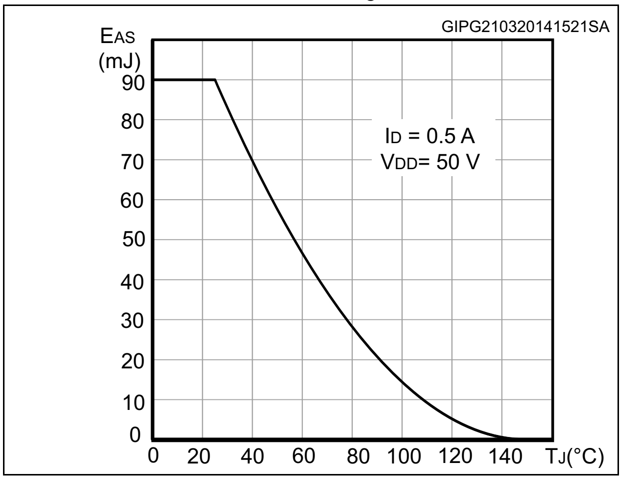


Figure 16.Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 17. Switching times test circuit for resistive load

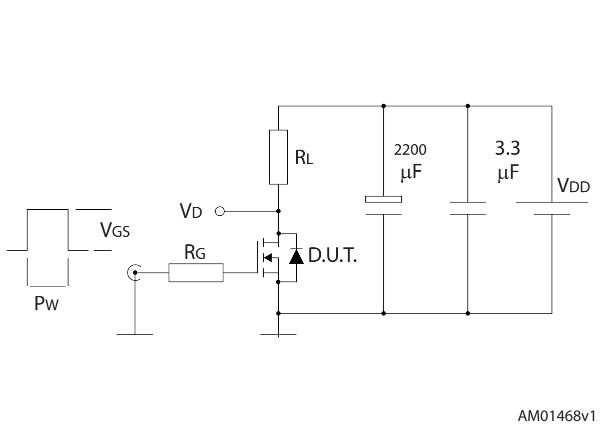


Figure 18. Gate charge test circuit

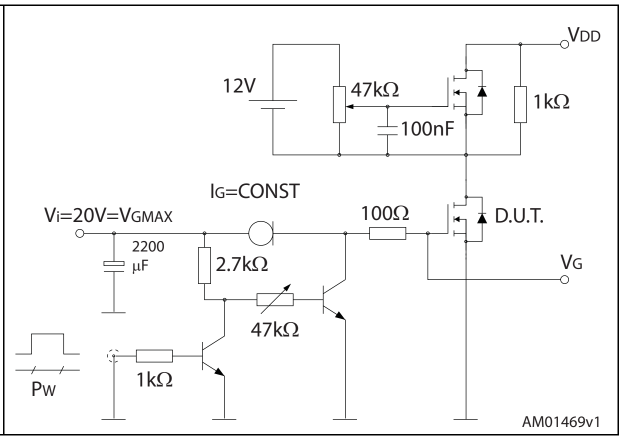


Figure 19. Test circuit for inductive load switching and diode recovery times

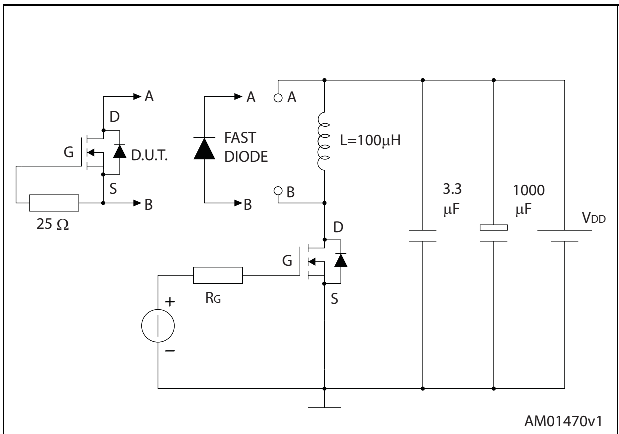


Figure 20. Unclamped inductive load test circuit

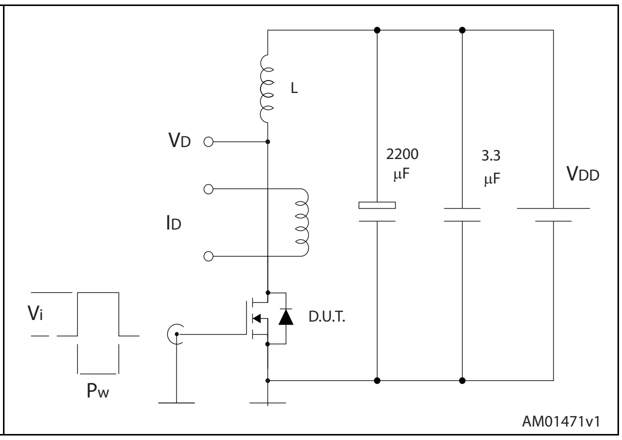


Figure 21. Unclamped inductive waveform

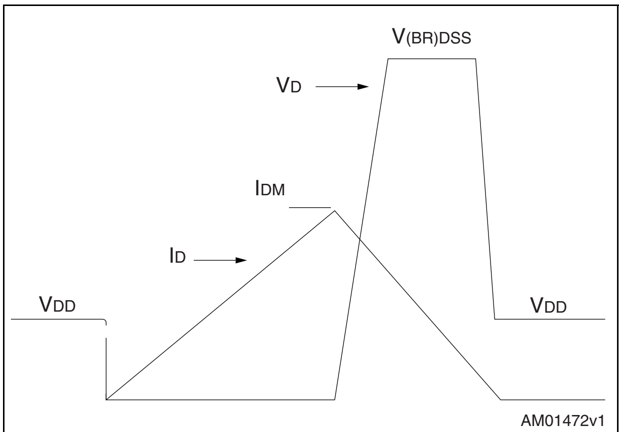
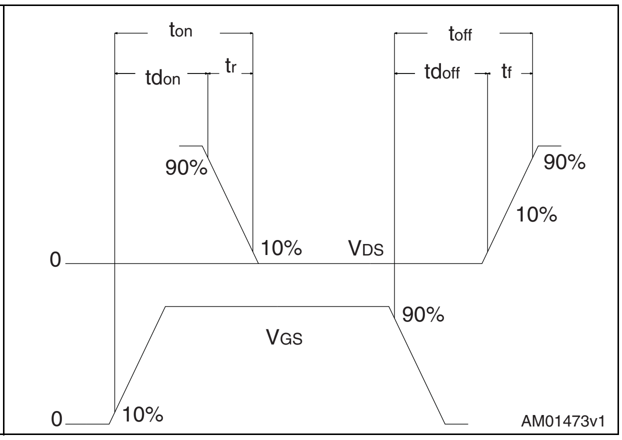


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 DPAK, STD2N105K5

Figure 23. DPAK (TO-252) type A drawing

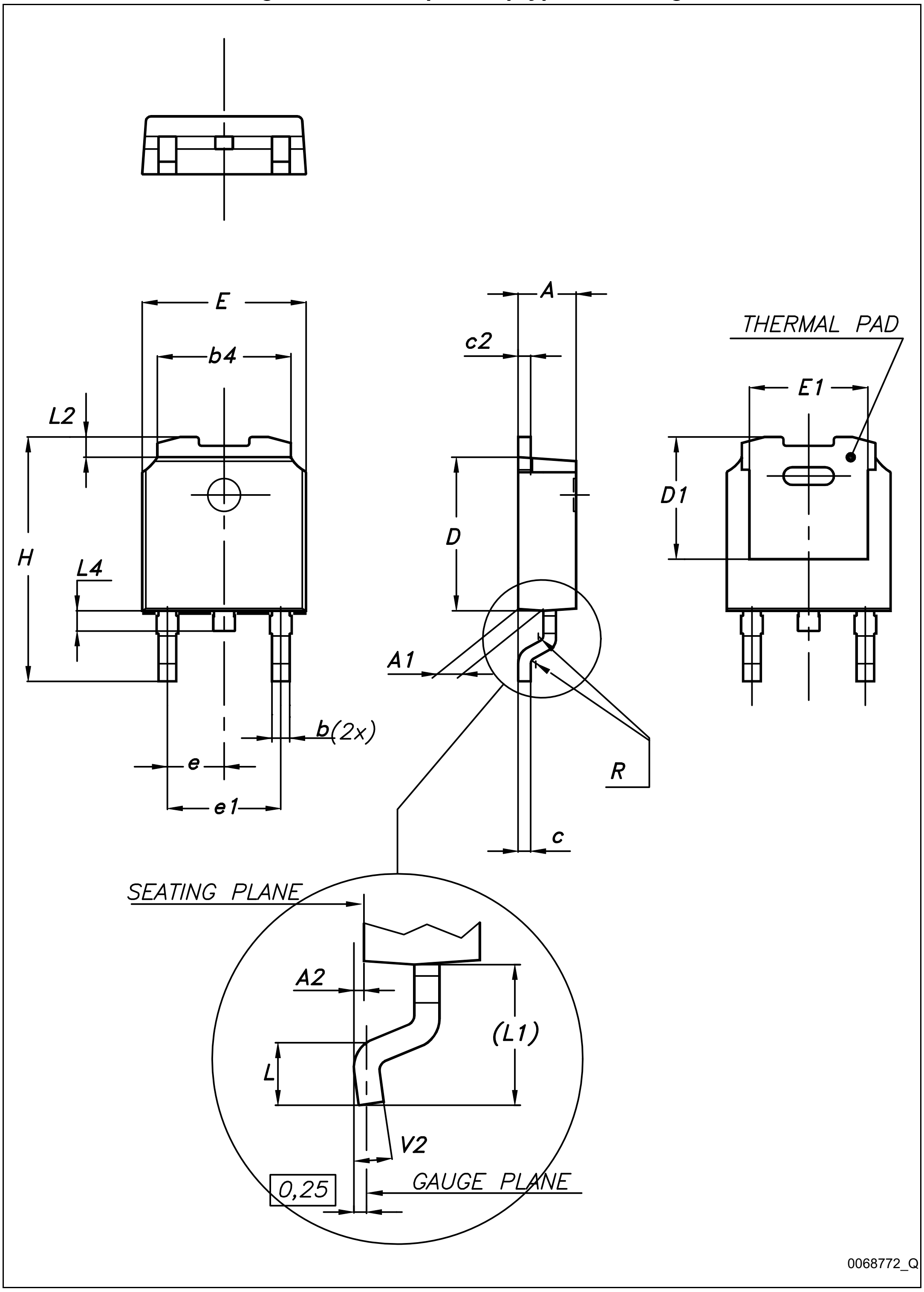
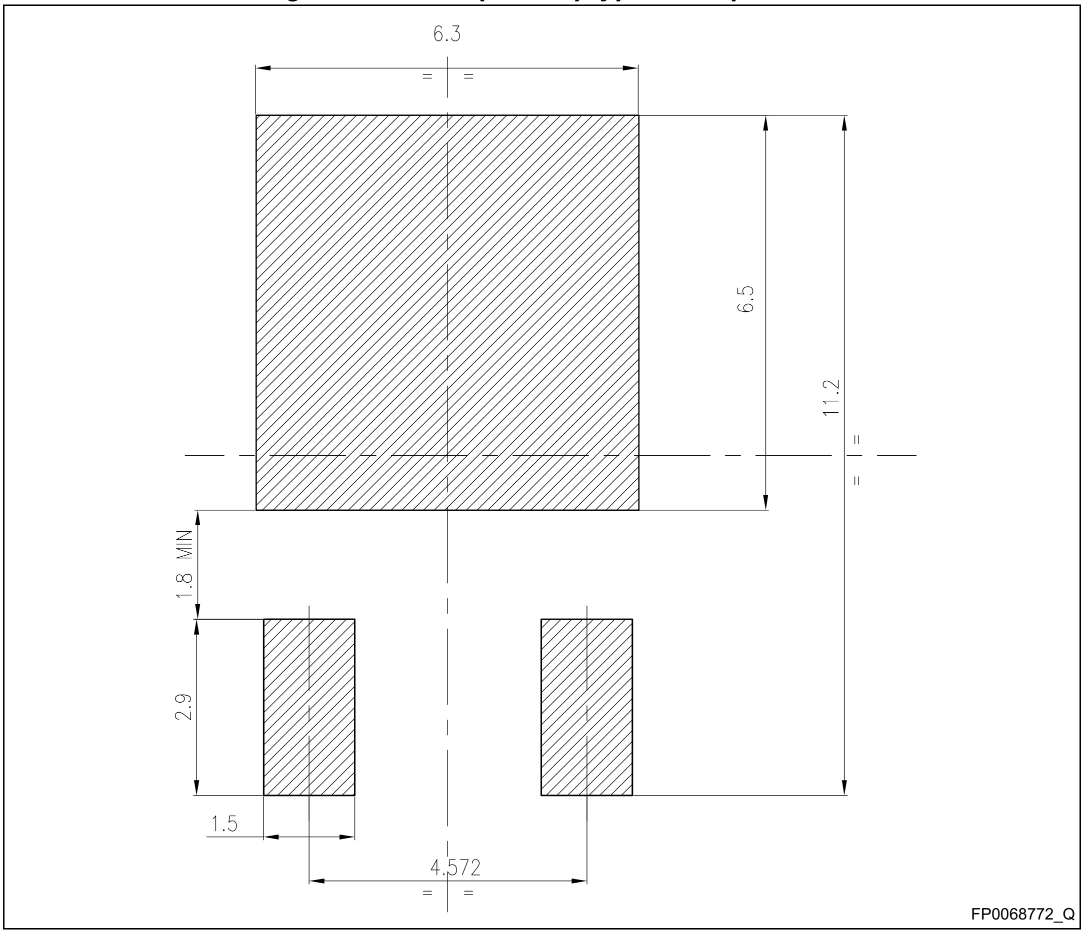


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) type A footprint [(a)]



a. All dimensions are in millimeters

4.2 TO-220, STP2N105K5

Figure 25. TO-220 type A drawing

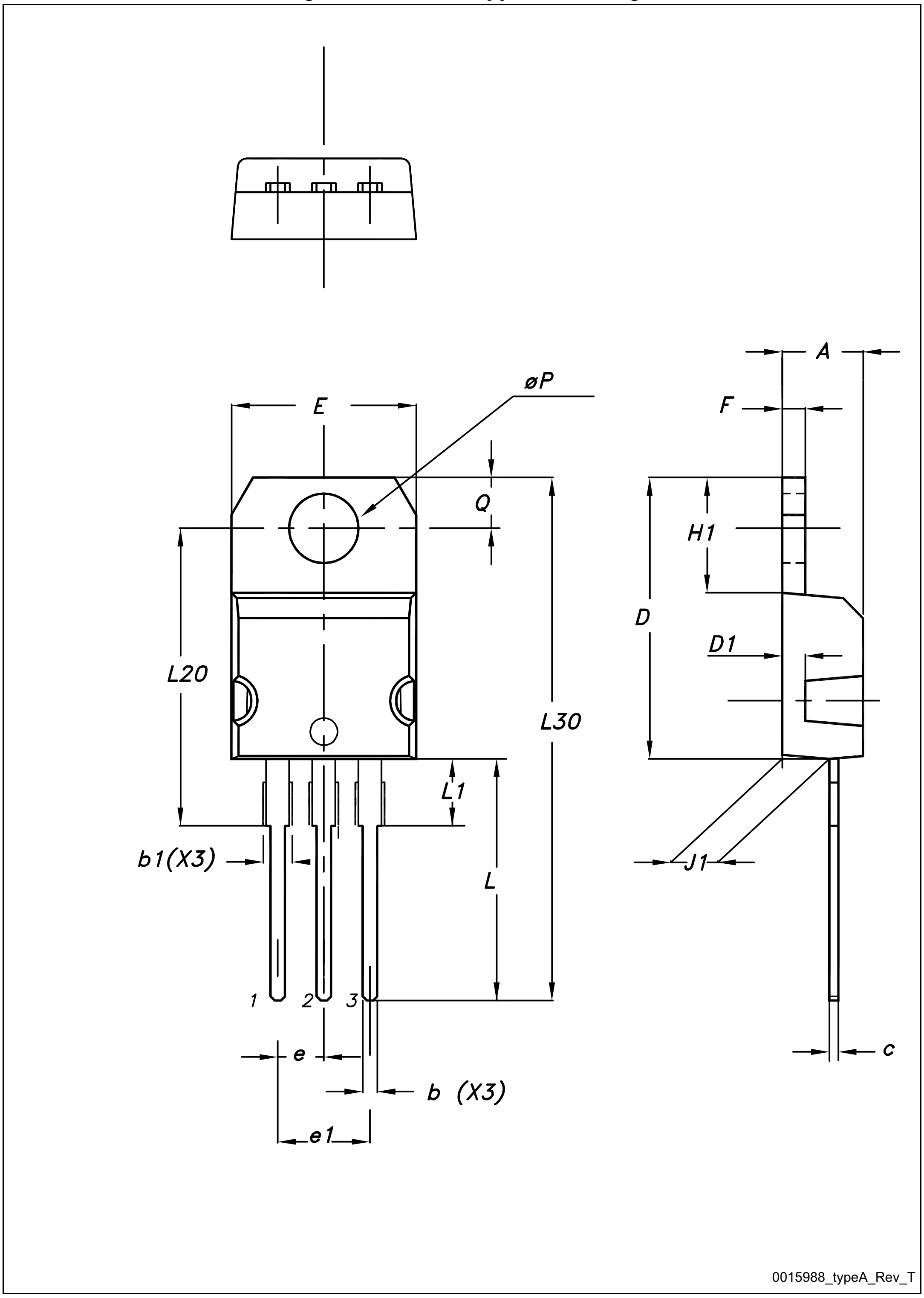


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

4.3 IPAK, STU2N105K5

Figure 26. IPAK (TO-251) drawing

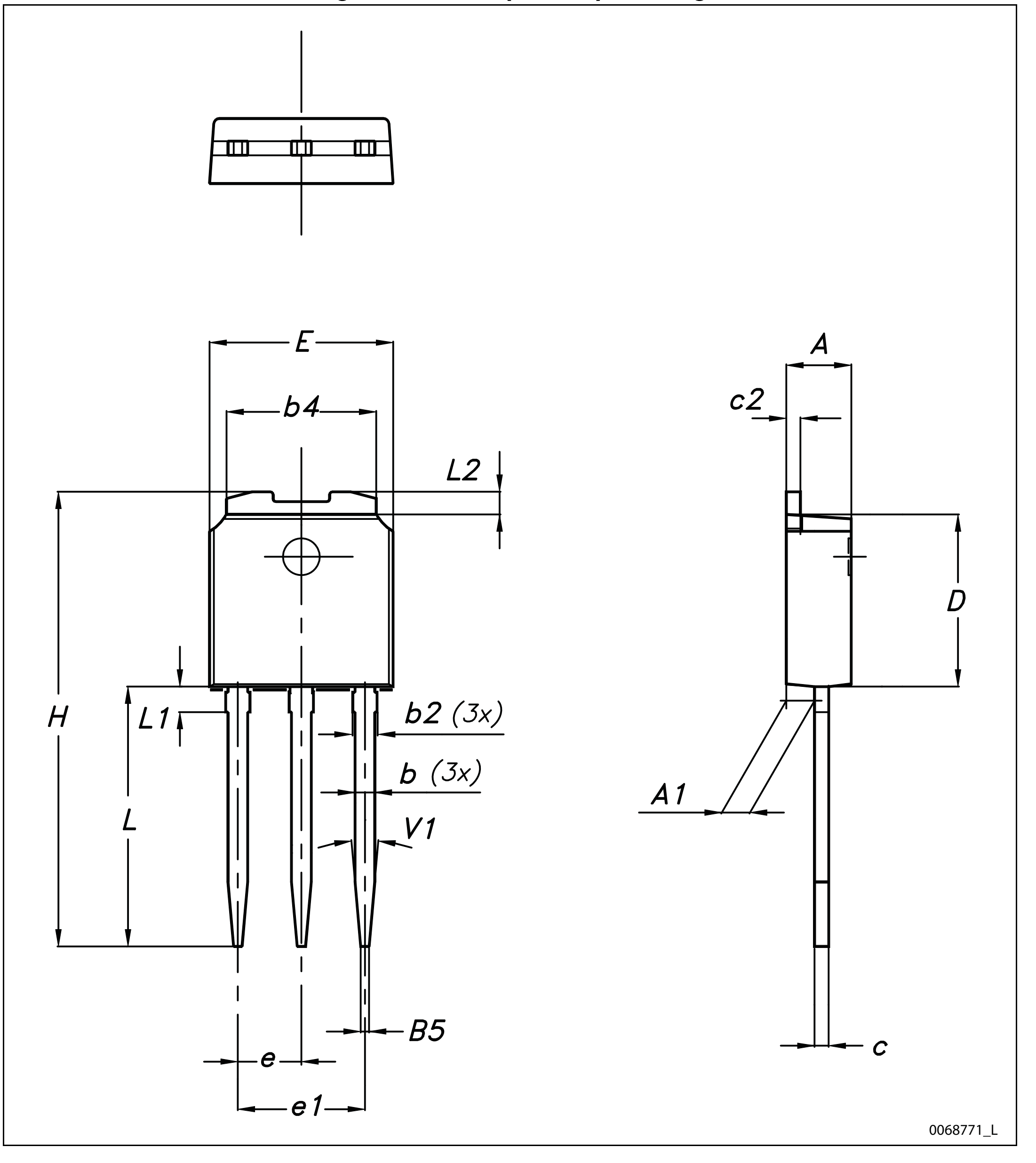


Table 11. IPAK (TO-251) type A mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Packaging mechanical data

Figure 27. Tape

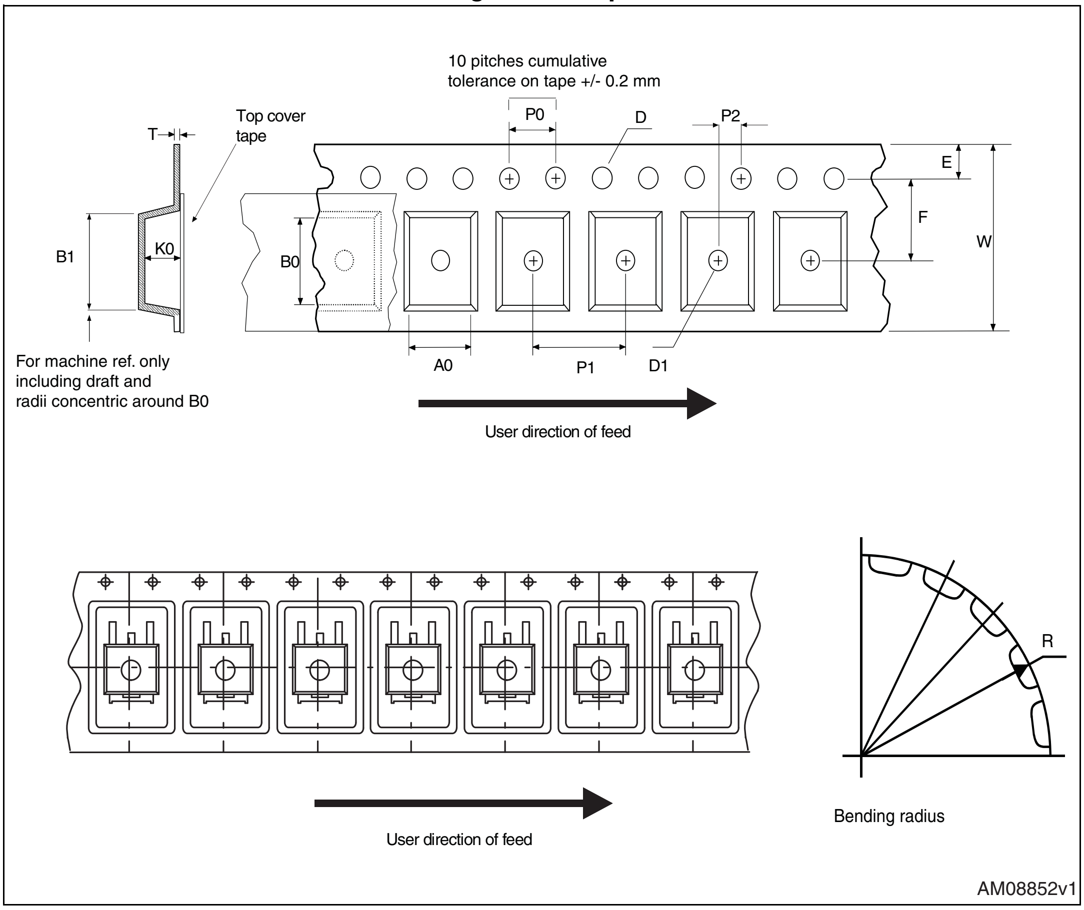


Figure 28. Reel

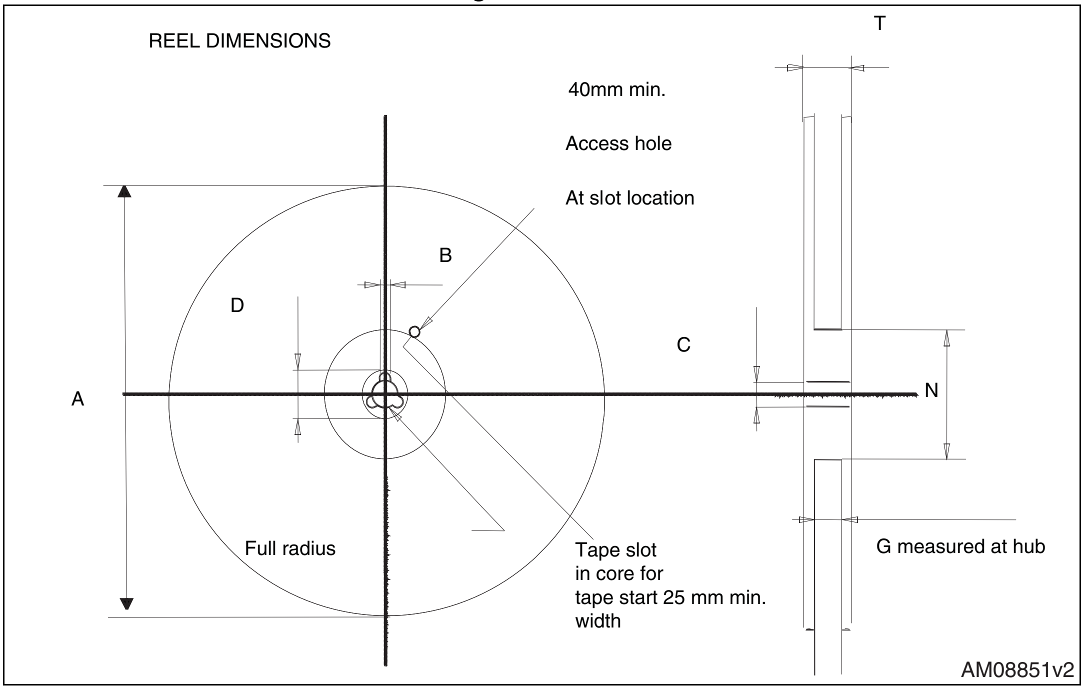


Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
08-May-2014	1	First release.
14-Nov-2014	2	Document status promoted from preliminary to production data. Updated title, features and description in cover page. Updated *Figure 9: Static drain-source on-resistance*, *Section 4.1: DPAK, STD2N105K5* and *Section 4.3: IPAK, STU2N105K5*. Minor text changes.
19-Nov-2004	3	Updated V_{GS} in *Table 2: Absolute maximum ratings* and I_{GSS} in *Table 4: On /off states*.