STD1HN60K3, STU1HN60K3

N-channel 600 V, 6.7 Ω typ., 1.2 A SuperMESH3™ Power MOSFET in DPAK and IPAK packages

Datasheet — production data

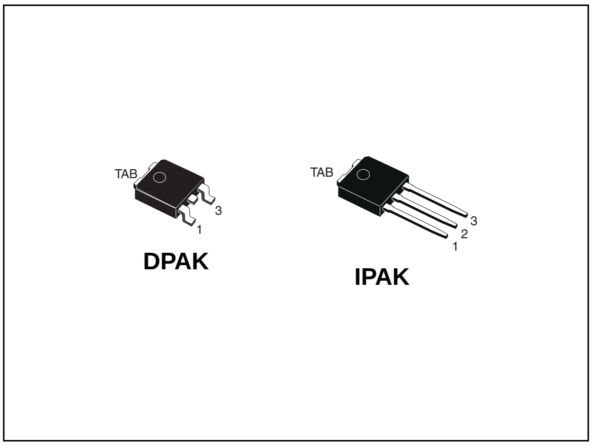
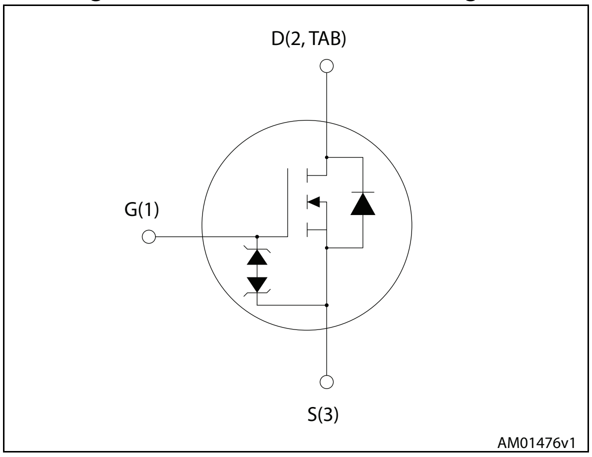


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STD1HN60K3	600 V	8 Ω	1.2 A	27 W
STU1HN60K3				

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD1HN60K3	1HN60K3	DPAK	Tape and reel
STU1HN60K3		IPAK	Tube

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 9

4 Package mechanical data 10

5 Packaging mechanical data 16

6 Revision history 18

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain- source voltage	600	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	1.2(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	0.76	A
I_{DM}(1)	Drain current (pulsed)	4.8	A
P_{TOT}	Total dissipation at T_C = 25 °C	27	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	1.2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	60	mJ
dv/dt(2)	Peak diode recovery voltage slope	5	V/ns
T_J	Operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 1.2 A, di/dt ≤ 400 A/µs,V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	4.63		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		100	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max.	50		°C/W

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	2	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.6 A		6.7	8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	140	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 480 V, V_{GS} = 0	-	9	-	pF
$C_{o(tr)}$ (2)	Equivalent capacitance energy related		-	6	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	10	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 1.2 A, V_{GS} = 10 V *(see Figure 16)*	-	9.5	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	6.5	-	nC

1. $C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}
2. $C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 0.6 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 10)*	-	7	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	23	-	ns
t_f	Fall time		-	31	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		1.2	A
I_{SDM} (1)	Source-drain current (pulsed)		-		4.8	A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.2 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 1.2 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 11)*	-	180		ns
Q_{rr}	Reverse recovery charge		-	500		nC
I_{RRM}	Reverse recovery current		-	5.6		A
t_{rr}	Reverse recovery time	I_{SD} = 1.2 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 11)*	-	200		ns
Q_{rr}	Reverse recovery charge		-	570		nC
I_{RRM}	Reverse recovery current		-	6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

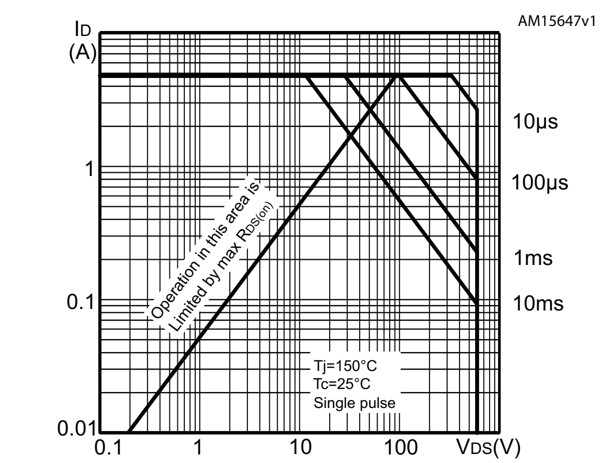


Figure 3. Thermal impedance

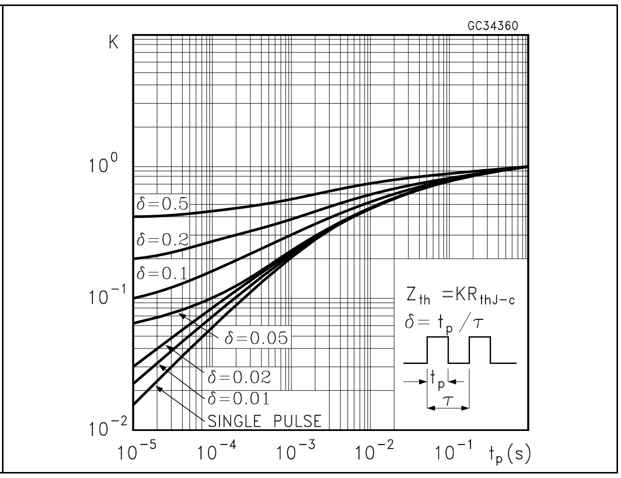


Figure 4. Output characteristics

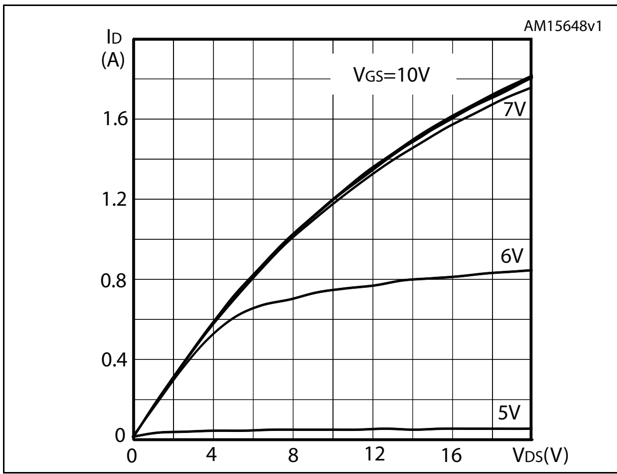


Figure 5. Transfer characteristics

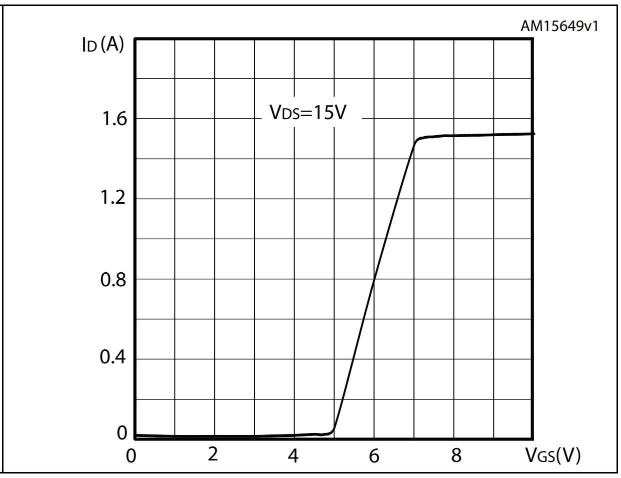


Figure 6. Normalized B_{VDSS} vs temperature

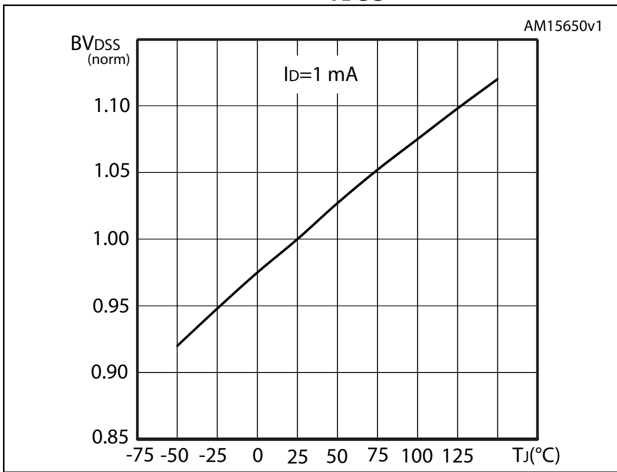


Figure 7. Static drain-source on-resistance

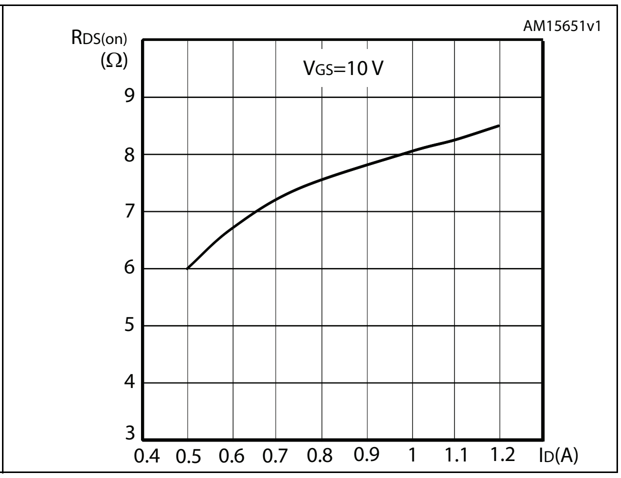


Figure 8. Gate charge vs gate-source voltage

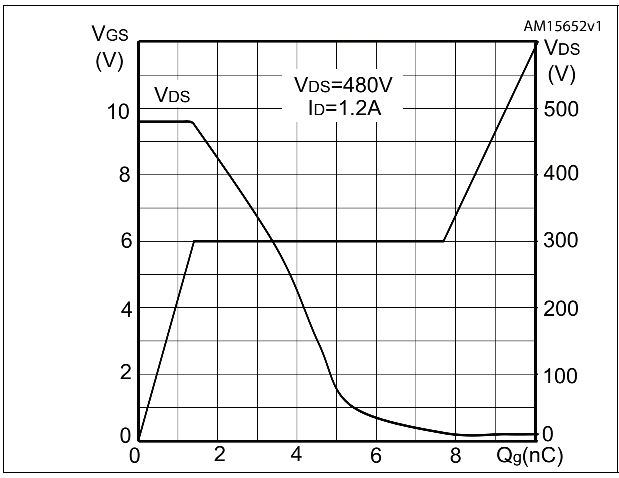


Figure 9. Capacitance variations

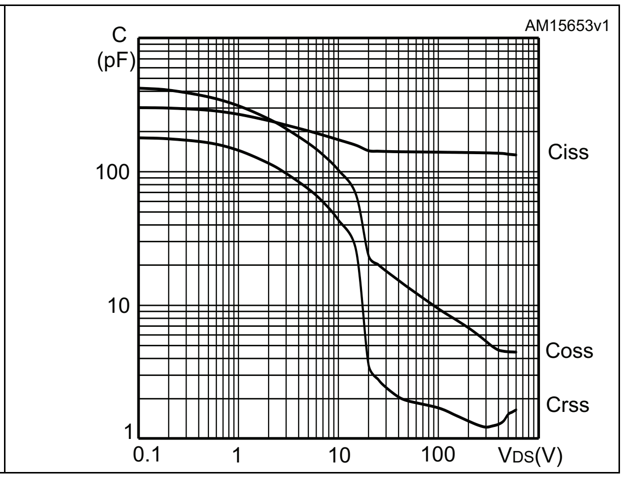


Figure 10. Normalized gate threshold voltage vs temperature

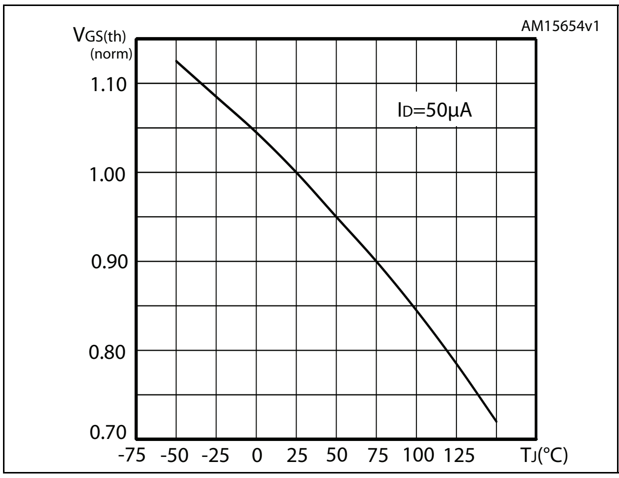


Figure 11. Normalized on-resistance vs temperature

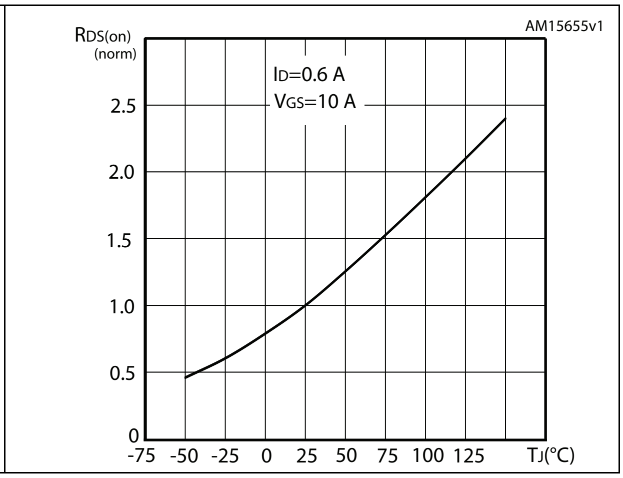


Figure 12. Source-drain diode forward characteristics

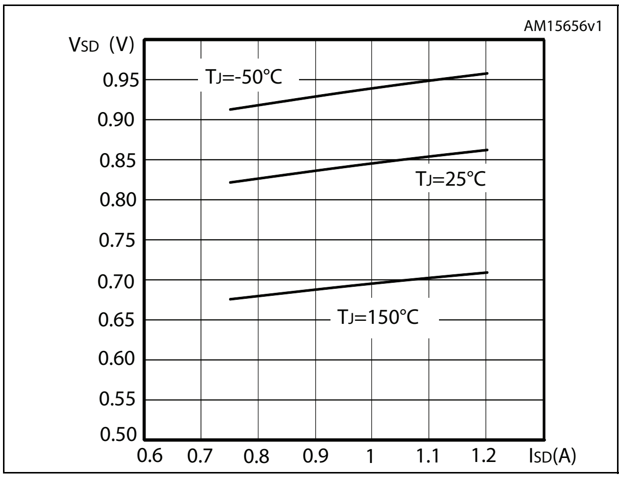


Figure 13. Output capacitance stored energy

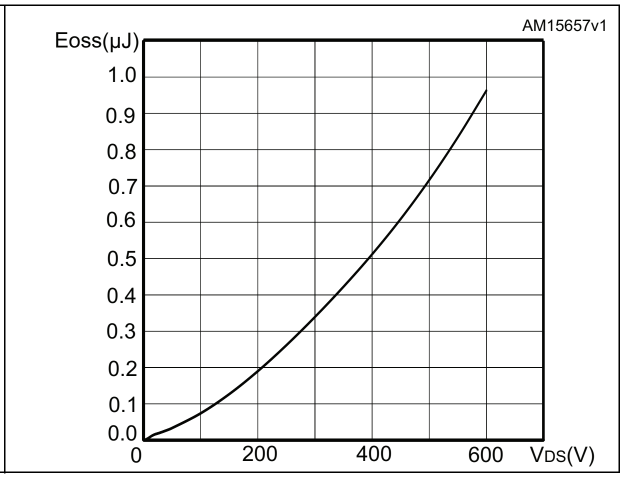
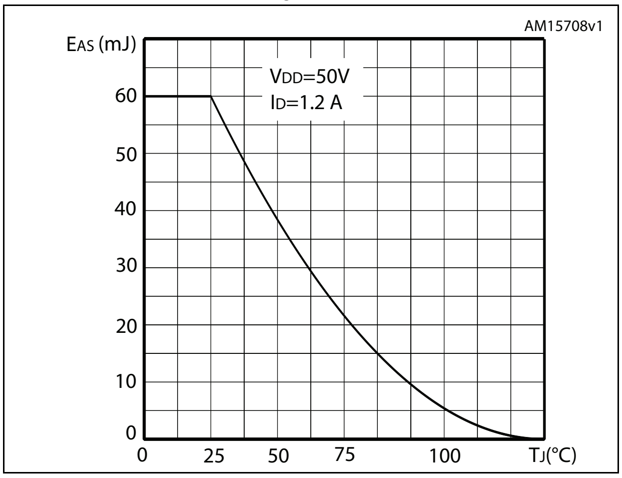


Figure 14. Maximum avalanche energy vs. starting T_J



3 Test circuits

Figure 15. Switching times test circuit for resistive load

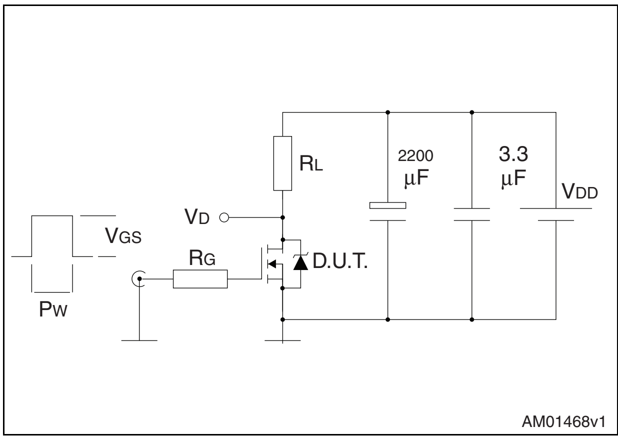


Figure 16. Gate charge test circuit

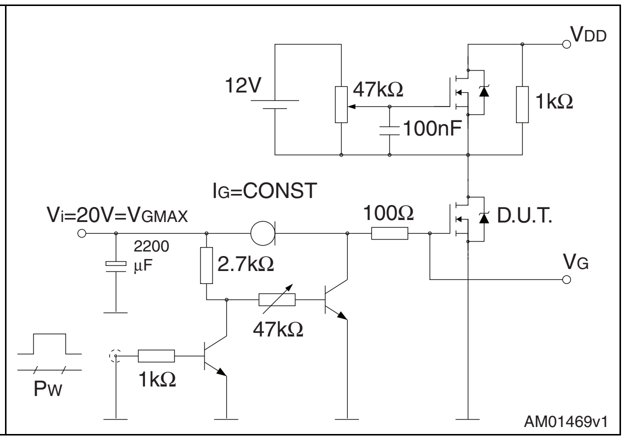


Figure 17. Test circuit for inductive load switching and diode recovery times

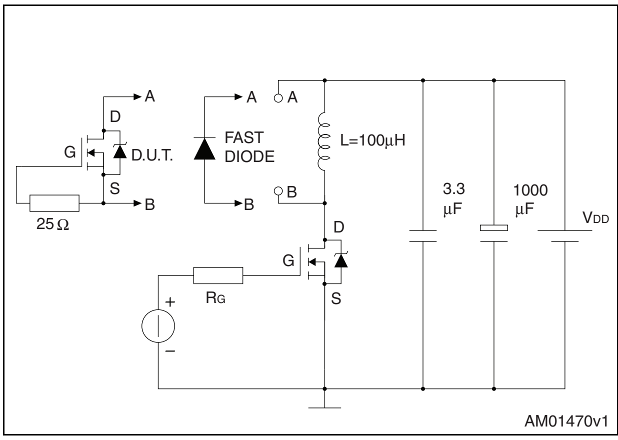


Figure 18. Unclamped inductive load test circuit

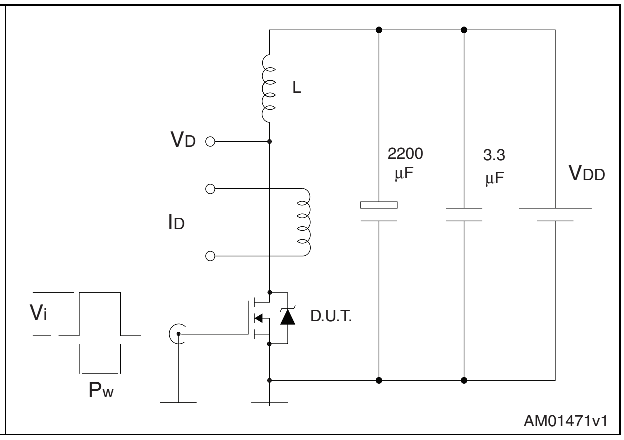


Figure 19. Unclamped inductive waveform

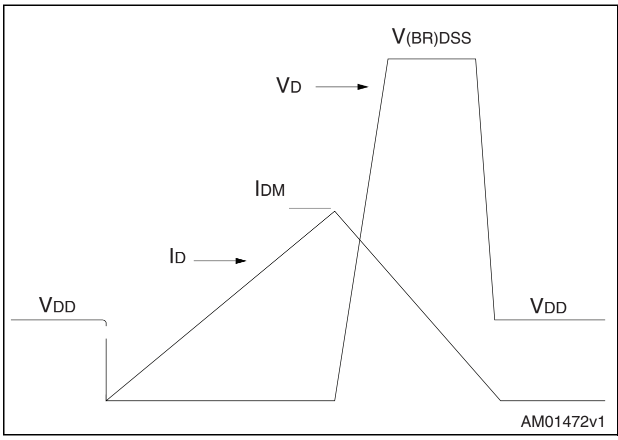
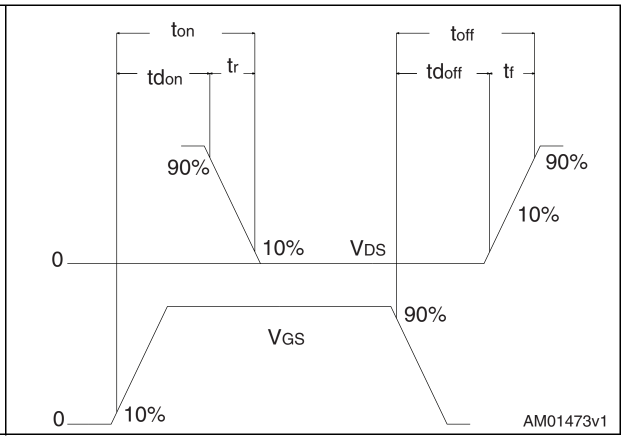


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) drawing

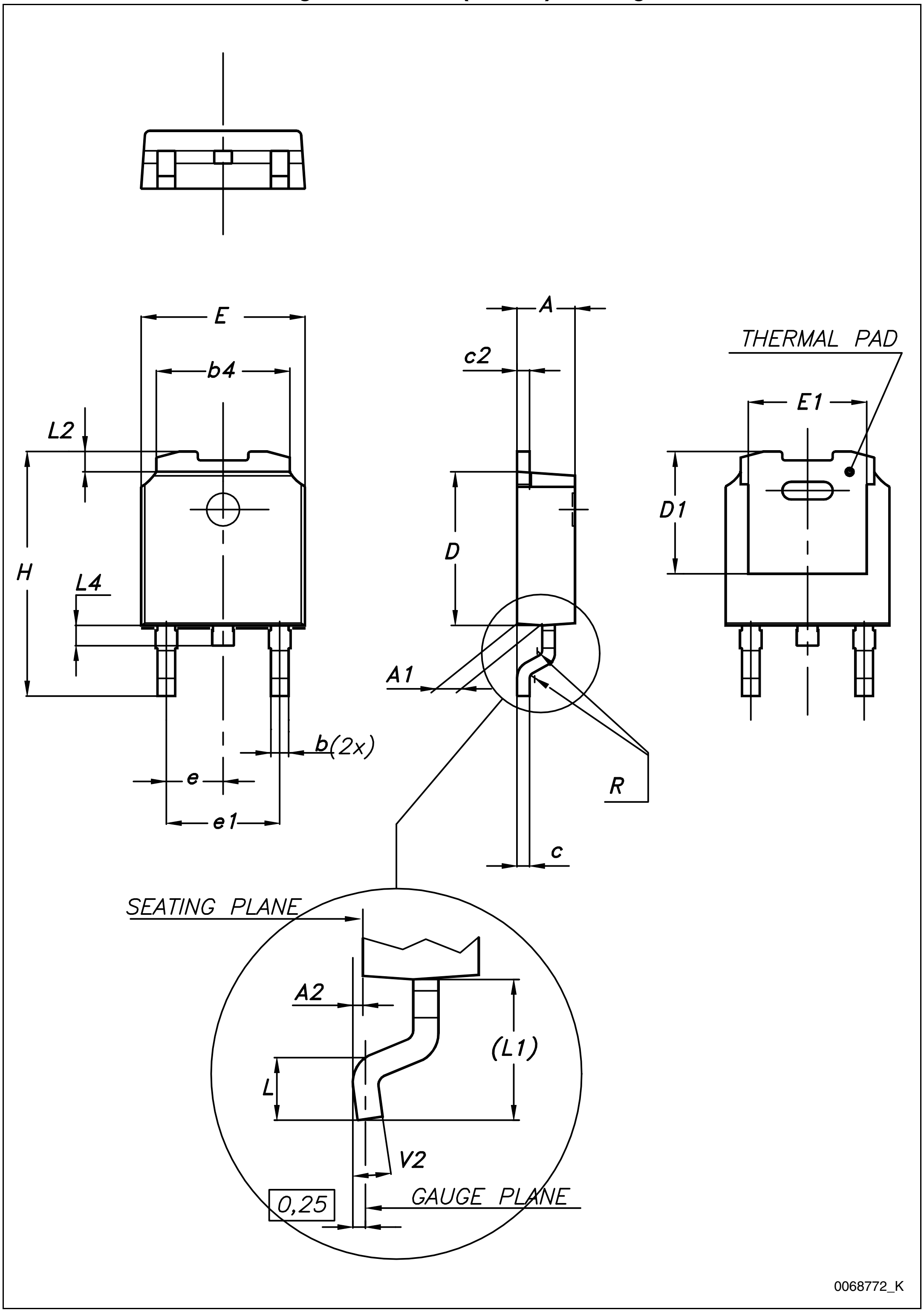
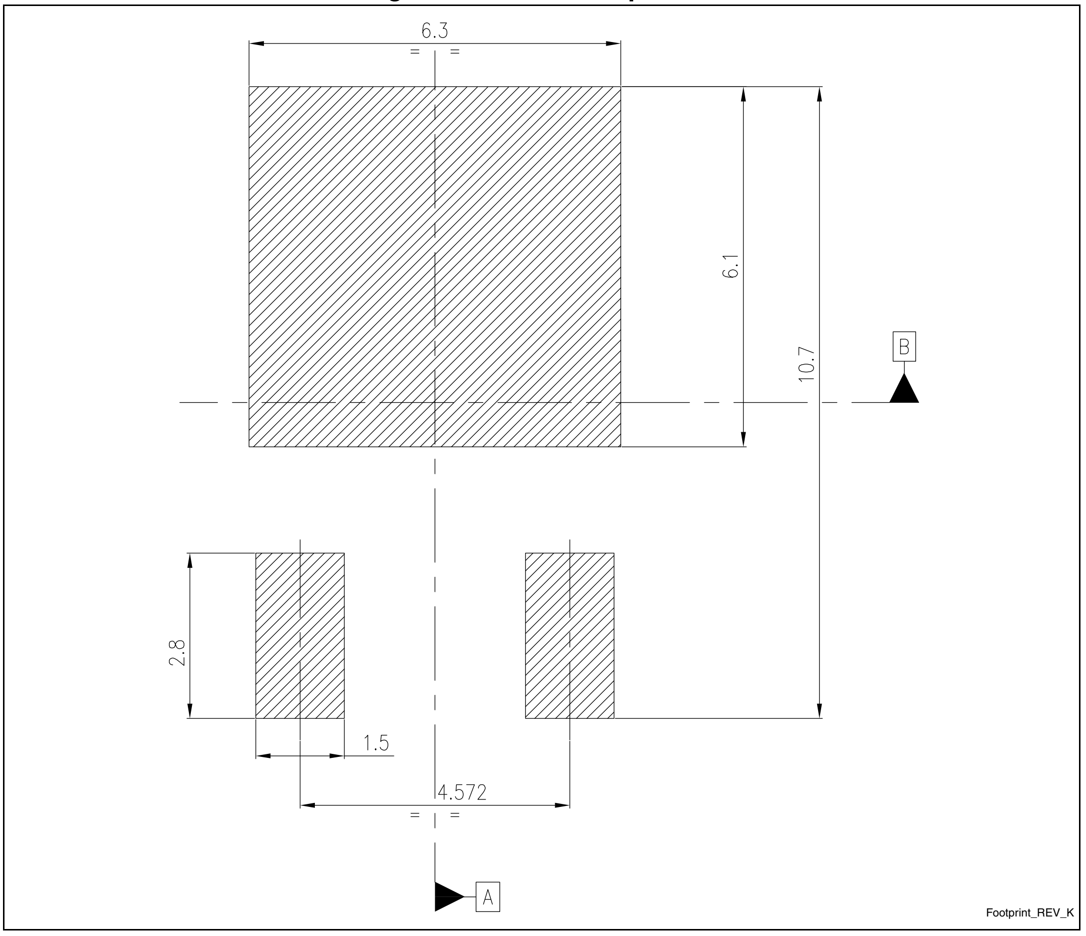


Figure 22. DPAK footprint [(a)]

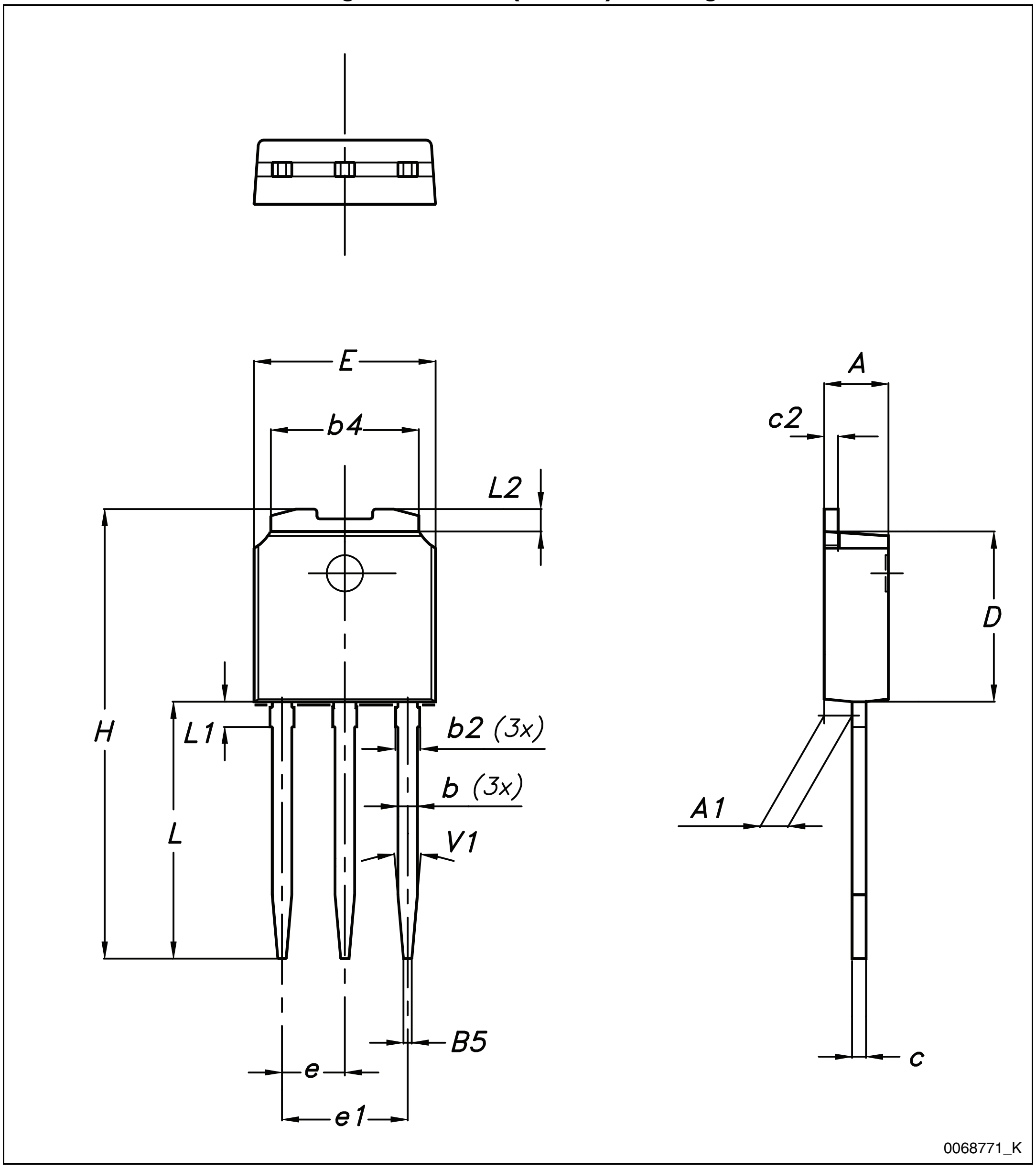


a. All dimensions are in millimeters

Table 10. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 23. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 24. Tape for DPAK (TO-252)

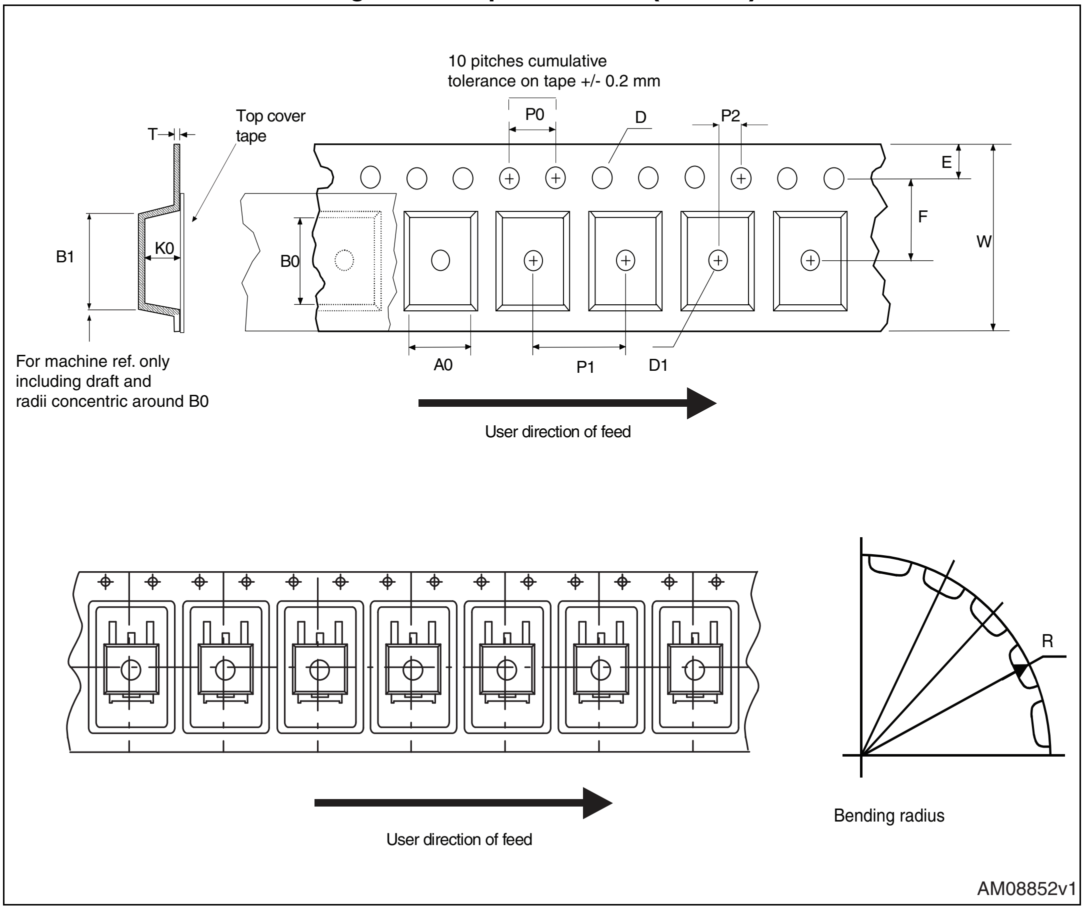
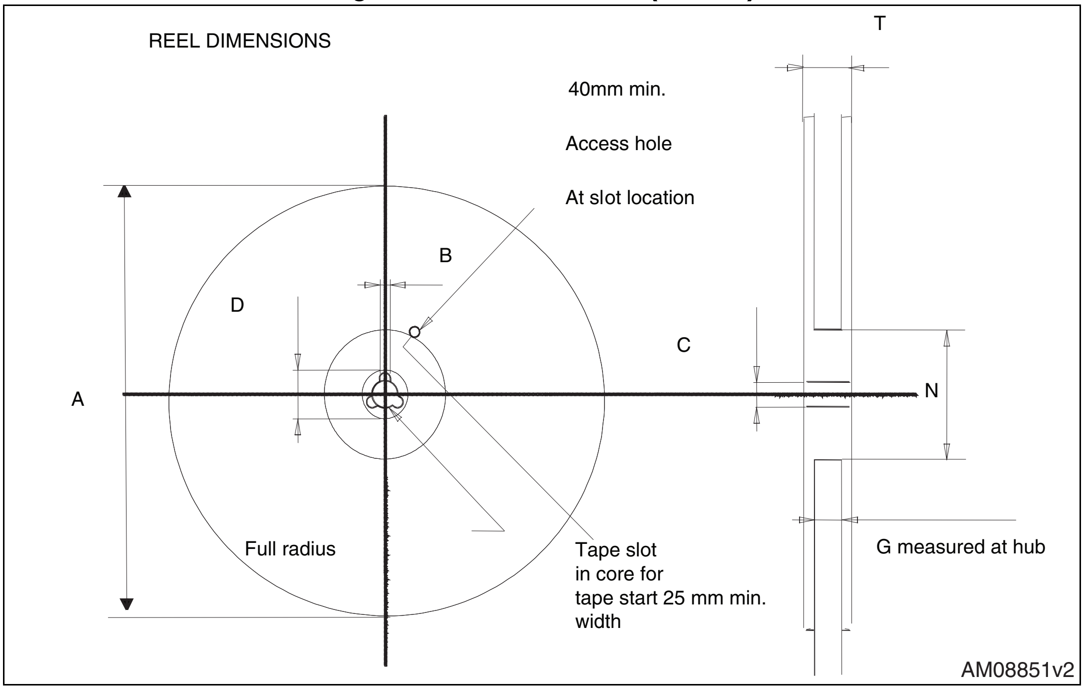


Figure 25. Reel for DPAK (TO-252)



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Apr-2013	1	First release.