

Demonstration board for STGAP2SiCSC isolated 4 A single gate driver



Features

- Board
 - High voltage rail up to 1200 V
 - Negative gate driving
 - Onboard isolated DC-DC converters to supply high-side and low-side gate drivers, fed by VAUX = 5 V, with 5.2 kV maximum isolation
 - 3.3 V VDD logic supply generated onboard or 5 V (externally applied)
 - Easy jumper selection of driving voltage configuration: +17/0 V; +17/-3 V; +19/0 V; +19/-3 V
- Device
 - Driver current capability: 4 A source/sink @ 25 °C
 - 6000 V Galvanic isolation
 - Short propagation delay: 75 ns
 - UVLO function
 - Gate driving voltage up to 26 V
 - 3.3 V, 5 V TTL/CMOS inputs with hysteresis
 - Temperature shut down protection
 - Stand-by function
 - 4 A Miller CLAMP

Description

The STGAP2SiCSC is an isolated single gate driver.

The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications equipped with SiC MOSFET power switches.

The configuration featuring single output pin and Miller CLAMP function allow avoiding gate spikes during fast commutations in half-bridge topologies.

The device integrates protection functions: UVLO and thermal shut down are included to easily design highly reliable systems. Dual input pins allow choosing the control signal polarity and also implementing HW interlocking protection in order to avoid cross-conduction in case of controller malfunction.

The device allows implementing negative gate driving, and the on board isolated DC-DC converters allows working with optimized driving voltage for SiC MOSFET.

The EVALSTGAP2SiCSC board allows evaluation of all the STGAP2SiCSC features while driving a half-bridge power stage with voltage rating up to 1200 V in TO-220 or TO-247 packages.

The board components are easy to access and modify in order to make driver performance evaluation easier under different application conditions and fine adjustment of final application components.

Product status link

[EVALSTGAP2SiCSC](#)

1 Schematic diagrams

Figure 1. EVALSTGAP2SiCSC circuit schematic – gate drivers

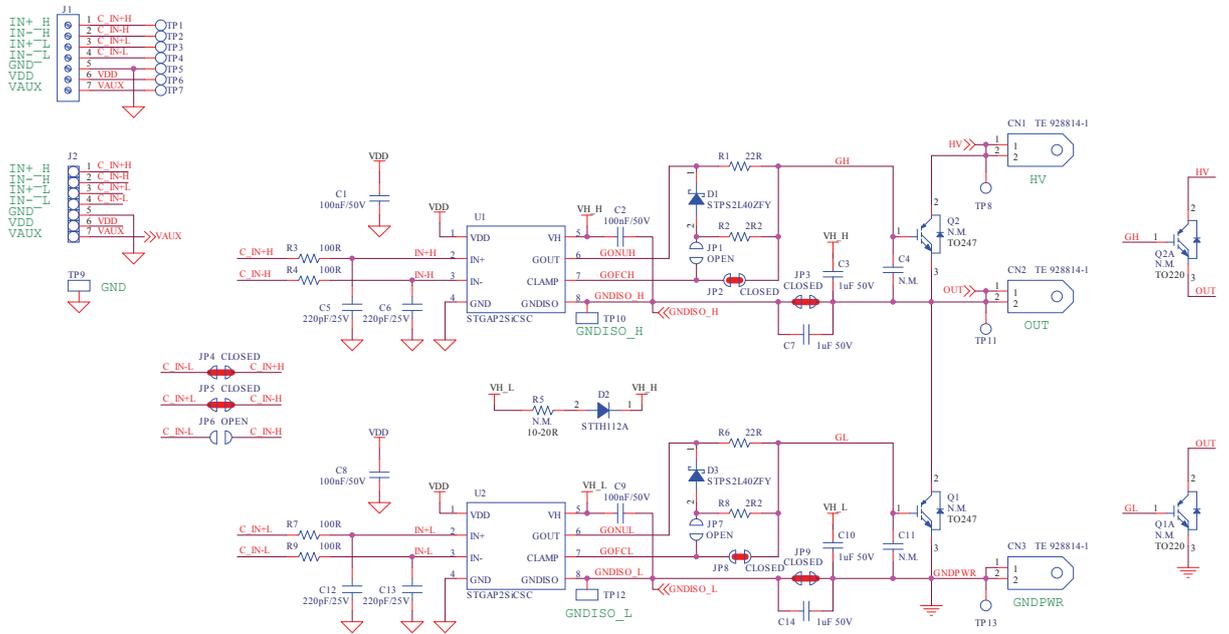
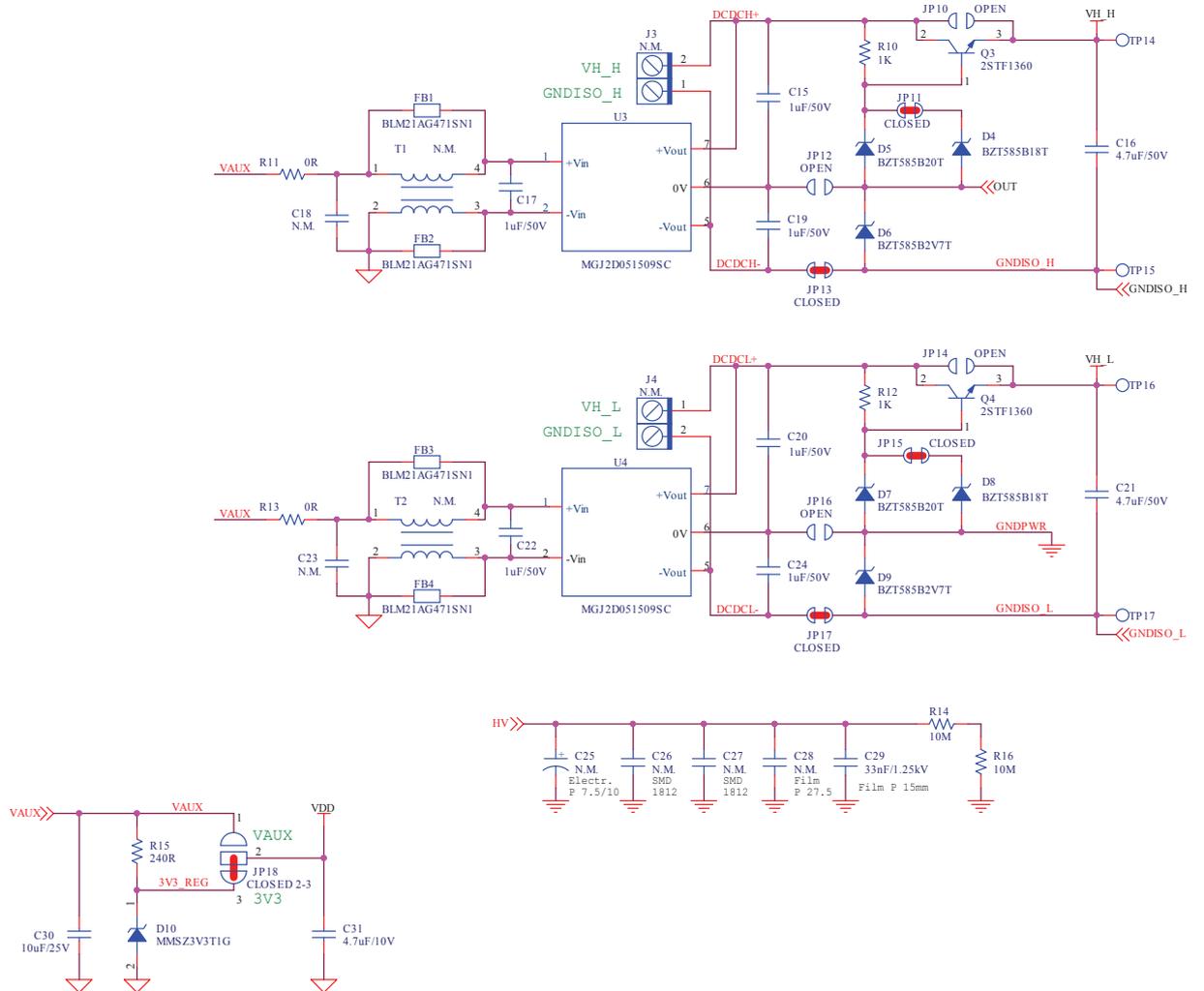


Figure 2. EVALSTGAP2SiCSC circuit schematic – supply, connectors and decoupling



2 Bill of material

Table 1. Bill of Material – components common to all device variants

| Reference | Description | Value / Generic Part Number |
|--|--------------------|--|
| CN1, CN2, CN3 | TE 928814-1 | Tab FASTON 250 Horizontal |
| C1, C2, C8, C9 | 100nF/50V | SMT Ceramic capacitor |
| C3, C7, C10, C14 | 1uF/50V | SMT Ceramic capacitor |
| C4, C11 | N.M. | SMT Ceramic capacitor |
| C5, C6, C12, C13 | 220pF/25V | SMT Ceramic capacitor |
| C15, C17, C19, C20, C22, C24 | 1uF/50V | SMT Ceramic capacitor |
| C16, C21 | 4.7uF/50V | SMT Ceramic capacitor |
| C18, C23 | N.M. | SMT Ceramic capacitor |
| C25 | N.M. | THT Electrolytic capacitor |
| C26, C27 | N.M. | SMT Ceramic capacitor |
| C28 | N.M. | Film capacitor |
| C29 | 33nF/1.25kV | Film capacitor |
| C30 | 10uF/25V | SMT Ceramic capacitor |
| C31 | 4.7uF/10V | SMT Ceramic capacitor |
| D1, D3 | STPS2L40ZFY | Automotive low drop power Schottky rectifier |
| D2 | STTH112A | High voltage ultrafast rectifier |
| D4, D8 | BZT585B18T | SURFACE MOUNT PRECISION ZENER DIODE |
| D5, D7 | BZT585B20T | SURFACE MOUNT PRECISION ZENER DIODE |
| D6, D9 | BZT585B2V7T | SURFACE MOUNT PRECISION ZENER DIODE |
| D10 | MMSZ3V3T1G | Zener Voltage Regulator 500mW |
| FB1, FB2, FB3, FB4 | BLM21AG471SN1 | Ferrite Beads |
| JP1, JP3, JP4, JP5, JP7, JP9, JP11, JP13, JP15, JP17 | CLOSED | SMT jumper |
| JP2, JP6, JP8, JP10, JP12, JP14, JP16 | OPEN | SMT jumper |
| JP18 | CLOSED 2-3 | SMT jumper |
| J1 | MORSV-350-7P_screw | Connector terminal block T.H. 7 POS 3.5 mm |
| J2 | STRIP 1x7 | Strip connector 7 pos, 2.54 mm |
| J3, J4 | N.M. | Connector terminal block T.H. 2 POS 5.08 mm |
| Q1, Q2 | N.M. | N-channel MOSFET up to 1700 V |
| Q1A, Q2A | N.M. | N-channel MOSFET up to 1700 V |
| Q3, Q4 | 2STF1360 | Low voltage fast-switching NPN power transistors |
| R1, R6 | 22R | SMT Resistor |
| R2, R8 | 2R2 | SMT Resistor |
| R3, R4, R7, R9 | 100R | SMT Resistor |
| R5 | N.M. | SMT Resistor |
| R10, R12 | 1K | SMT Resistor |

| Reference | Description | Value / Generic Part Number |
|--|-----------------|--|
| R11, R13 | 0R | SMT Resistor |
| R14, R16 | 10M | SMT Resistor |
| R15 | 240R | SMT Resistor |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP11, TP13, TP14, TP15, TP16, TP17 | T POINT R | Test point - PCB 1.5 mm diameter |
| TP9, TP10, TP12 | TPTH-ANELLO-1MM | THT Ring Test Point |
| T1, T2 | N.M. | Common mode choke, SMD 4.7x4.5 mm |
| U1, U2 | STGAP2SiCSC | Galvanically isolated 4 A single gate driver for SiC MOSFETs |
| U3, U4 | MGJ2D051509SC | 5.2KVDC Isolated 2W Gate Drive DC/DC Converters |
| | | P.C.B. EVALSTGAP2SiC Rev.1 |

3 Layout and component placements

Figure 3. EVALSTGAP2SiCSC – Layout (component placement top view)

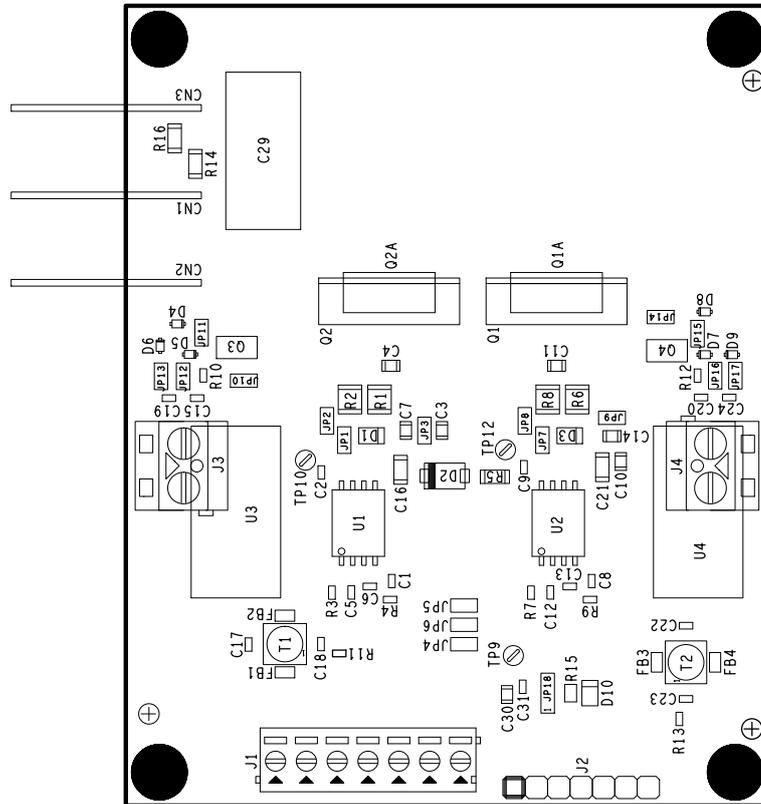


Figure 4. EVALSTGAP2SiCSC – Layout (component placement bottom view)

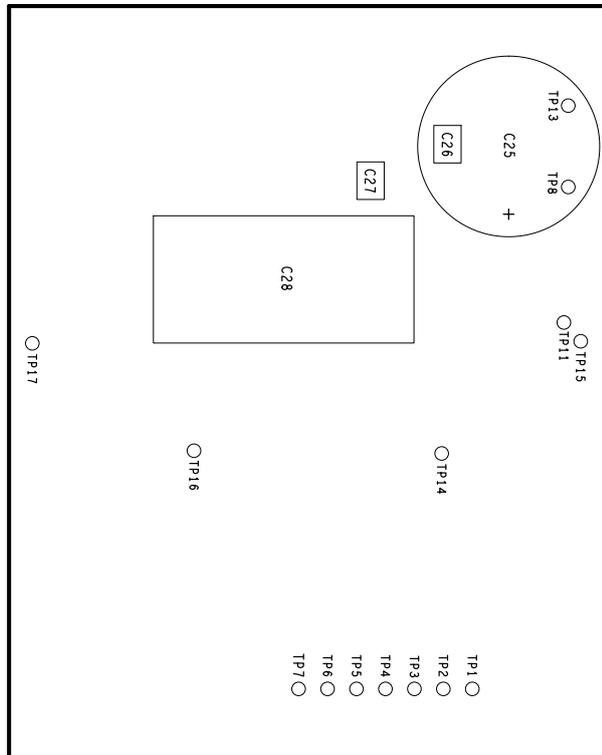


Figure 5. EVALSTGAP2SiCSC – Layout (top layer)

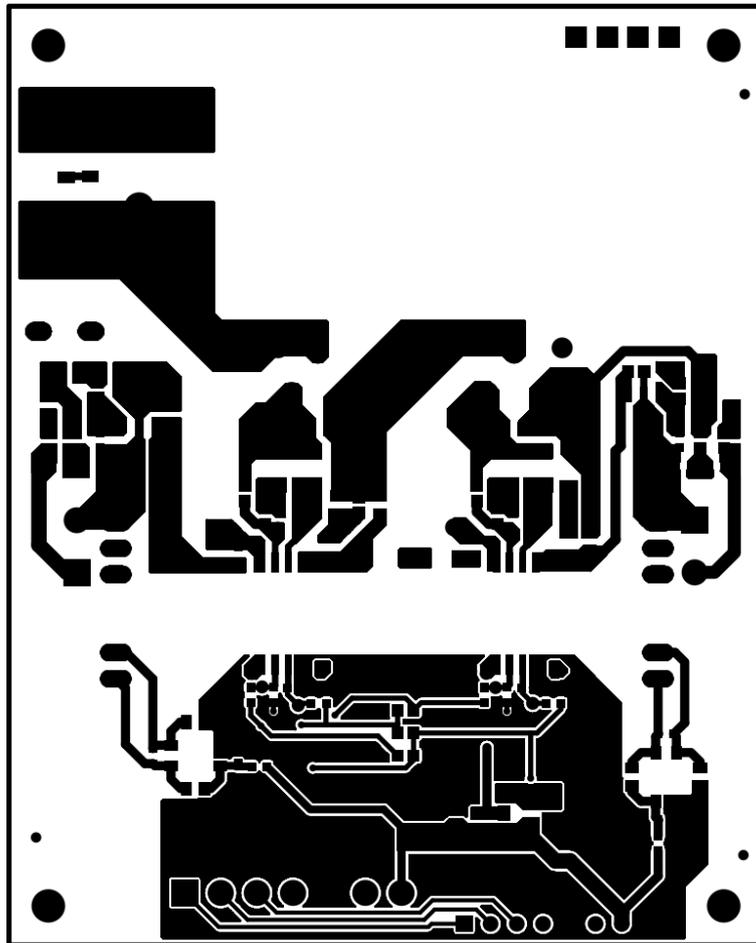
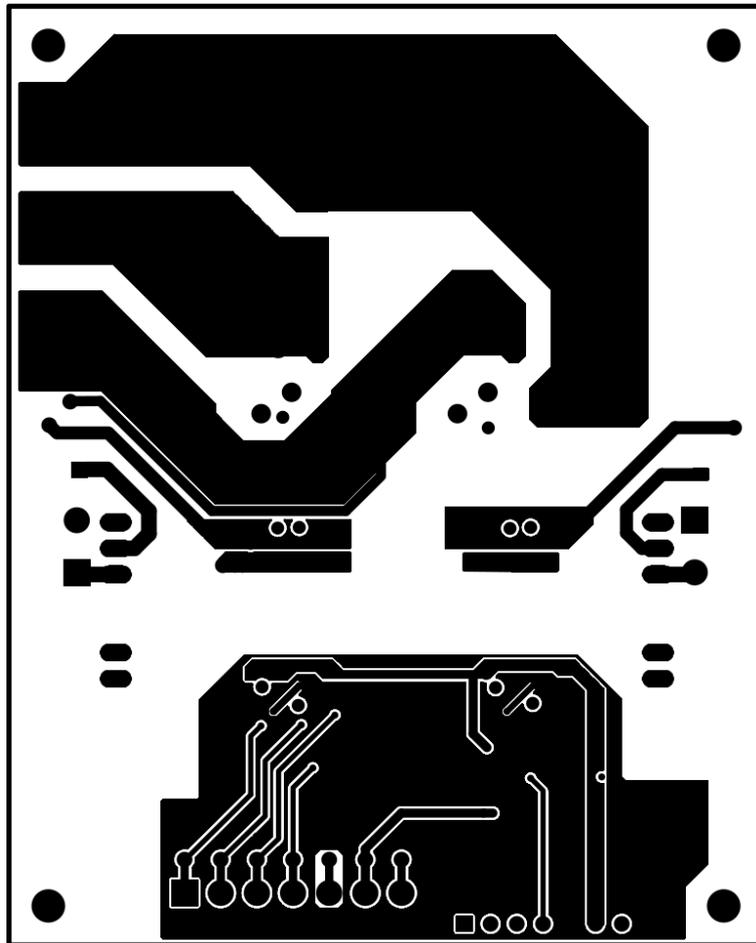


Figure 6. EVALSTGAP2SiCSC – Layout (bottom layer)



Revision history

Table 2. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 01-Oct-2020 | 1 | Initial release. |

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