

Silicon Carbide Power MOSFET N-Channel Enhancement Mode

Features

- ★ 3rd Generation SIC MOSFET technology
- ★ High blocking voltage with low on-resistance
- ★ High speed switching with low capacitances
- ★ Fast intrinsic diode with low reverse recovery (Qrr)
- ★ Halogen free, Rohs compliant

Benefits

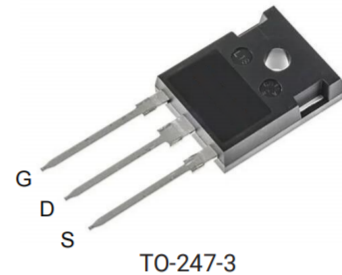
- ★ Higher system efficiency
- ★ Reduced Cooling requirements
- ★ Increased power density
- ★ Increased system switching frequency
- ★ Easy to parallel and simple to drive
- ★ Enable new hard switching PFC topologies(Totem-Pole)

Applications

- ★ EV charging
- ★ Server power supplies
- ★ Solar PV inverters
- ★ UPS
- ★ DC/DC converters

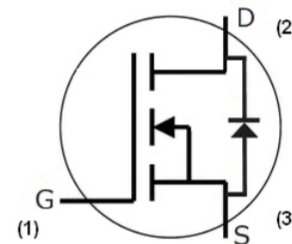
Product Summary

V_{DS}	$R_{DS(on)}$	$I_D @25^\circ$
650V	60m Ω	29 A



TO-247-3

Package



Maximum Ratings

Symbol	Parameter	Value	Unit	Note
V_{DSS}	Drain - Source Voltage, $T_c = 25^\circ\text{C}$	650	V	
V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 29
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 25^\circ\text{C}$	29	A	Fig. 19 Note 1
	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 100^\circ\text{C}$	20		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_p limited by T_{jmax}	99	A	
P_D	Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 175^\circ\text{C}$	150	W	Fig. 20
T_j, T_{stg}	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$	
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$	
M_d	Mounting Torque, (M3 or 6-32 screw)	1	Nm lbf-in	
		8.8		

Note (1): Die limits are 37A (25°C) and 27A (100°C)

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
V_{GSon}	Gate-Source Recommended Turn-On Voltage		15		V	Static	Fig. 29
V_{GSoff}	Gate-Source Recommended Turn-Off Voltage		-4		V		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 5\ \text{mA}$	Fig. 11
			1.9		V	$V_{DS} = V_{GS}, I_D = 5\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance	42	60	79	m Ω	$V_{GS} = 15\ \text{V}, I_D = 13.2\ \text{A}$	Fig. 4, 5,6
			80			$V_{GS} = 15\ \text{V}, I_D = 13.2\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		10		S	$V_{DS} = 20\ \text{V}, I_{DS} = 13.2\ \text{A}$	Fig. 7
			9			$V_{DS} = 20\ \text{V}, I_{DS} = 13.2\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		1020		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 600\ \text{V}$ $f = 1\ \text{MHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		80				
C_{rss}	Reverse Transfer Capacitance		9				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		95		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$	Note 1
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		132				
E_{oss}	C_{oss} Stored Energy		15		μJ	$V_{DS} = 600\ \text{V}, 1\ \text{MHz}$	Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		110		μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 13.2\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		22				
E_{ON}	Turn-On Switching Energy (External SiC Diode)		63		μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 13.2\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC Diode	Fig. 25
E_{OFF}	Turn Off Switching Energy (External SiC Diode)		28				
$t_{d(on)}$	Turn-On Delay Time		9		ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 13.2\ \text{A}, R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		20				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		3		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Q_{gs}	Gate to Source Charge		14		nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 13.2\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		14				
Q_g	Total Gate Charge		46				

Note (1): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V

Reverse Diode Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		23	A	$V_{GS} = -4\text{ V}, T_C = 25^\circ\text{C}$	
$I_{S, pulse}$	Diode pulse Current		99	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recover time	20		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $dif/dt = 1200\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	190		nC		
I_{rrm}	Peak Reverse Recovery Current	16		A		
t_{rr}	Reverse Recover time	29		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $dif/dt = 750\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	181		nC		
I_{rrm}	Peak Reverse Recovery Current	9		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.99	$^\circ\text{C}/\text{W}$		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

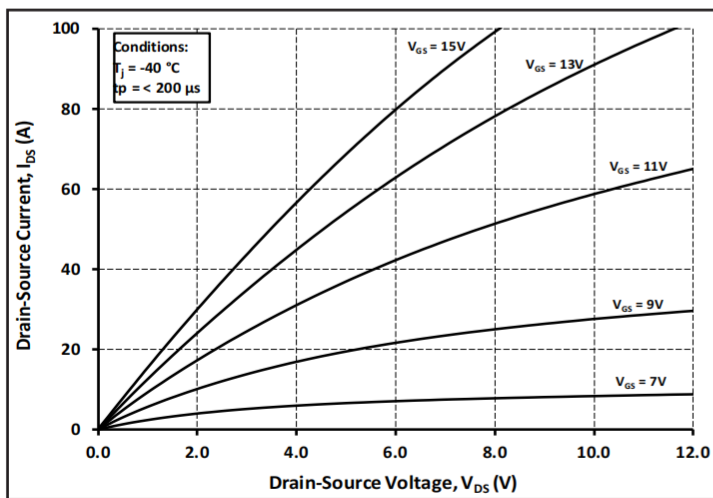


Figure 1. Output Characteristics $T_J = -40^\circ\text{C}$

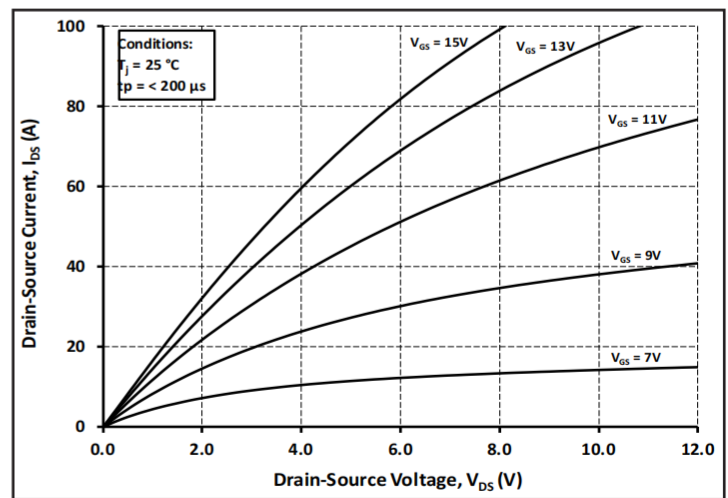


Figure 2. Output Characteristics $T_J = 25^\circ\text{C}$

Typical Performance

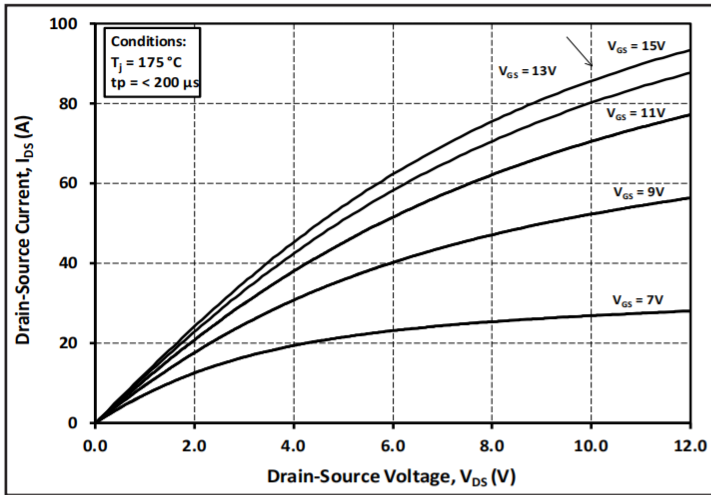


Figure 3. Output Characteristics $T_j = 175\text{ }^\circ\text{C}$

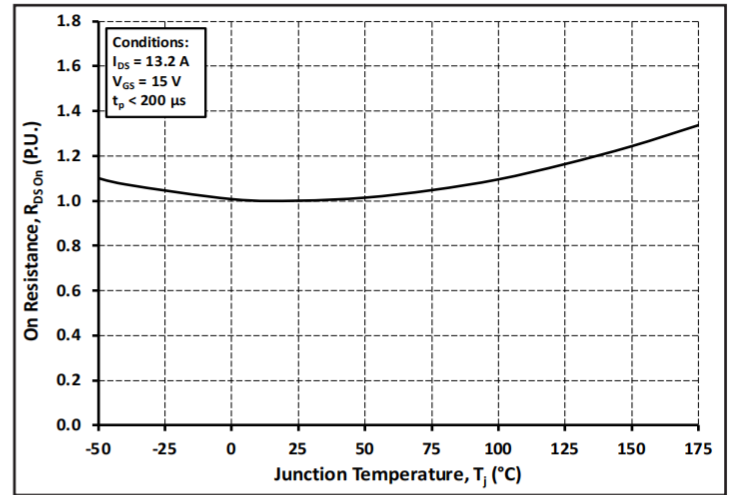


Figure 4. Normalized On-Resistance vs. Temperature

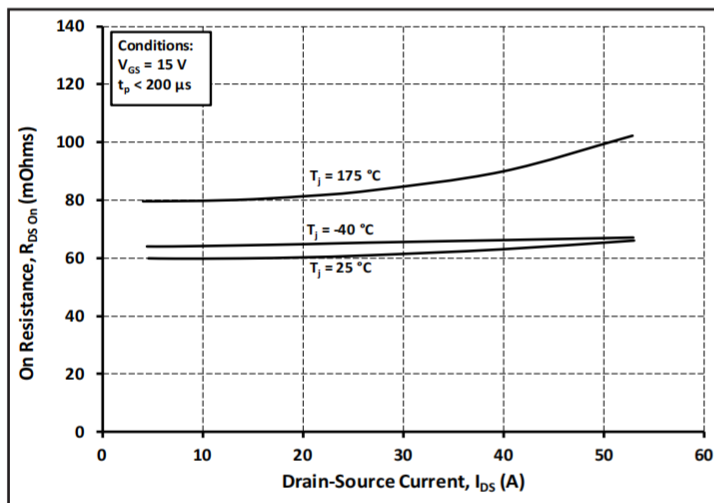


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

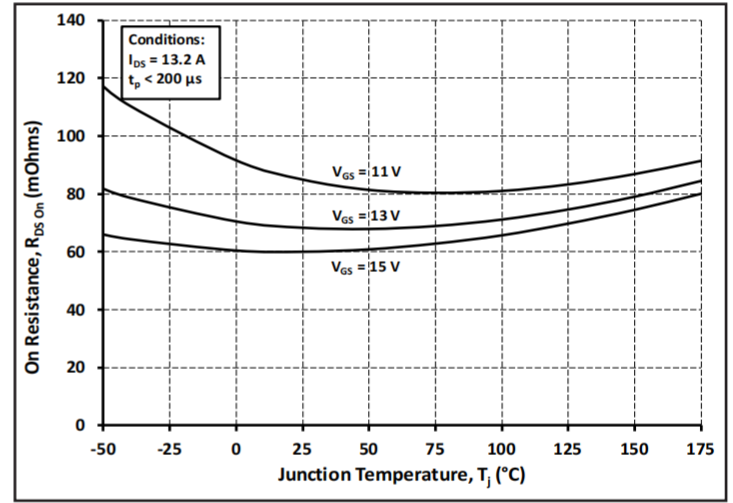


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

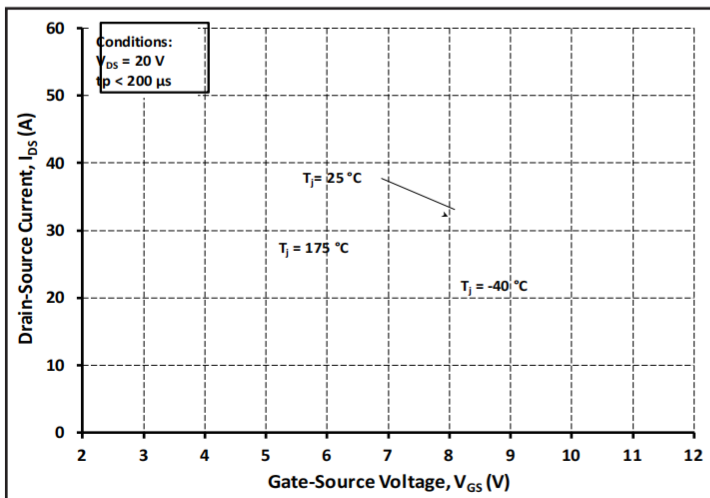


Figure 7. Transfer Characteristic for Various Junction Temperatures

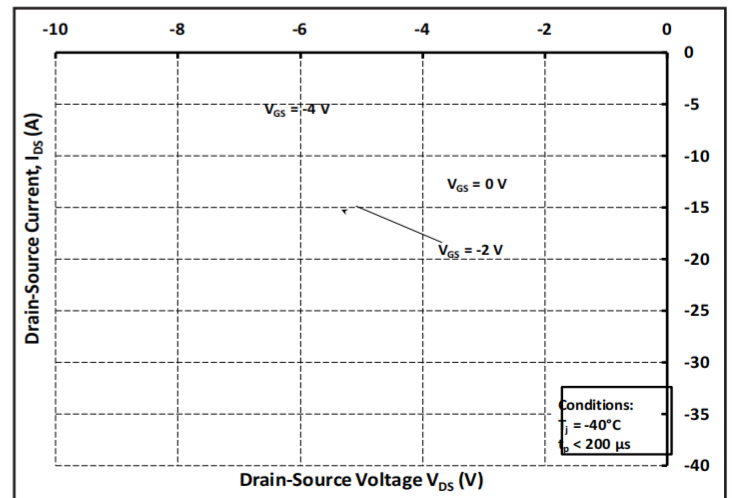


Figure 8. Body Diode Characteristic at $-40\text{ }^\circ\text{C}$

Typical Performance

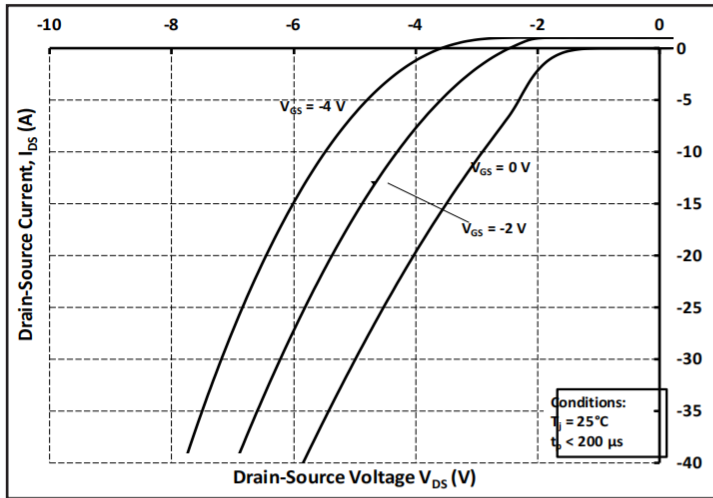


Figure 9. Body Diode Characteristic at 25 °C

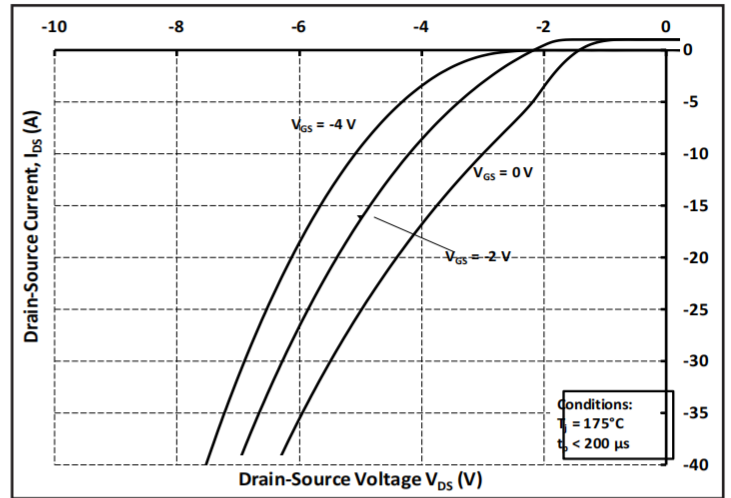


Figure 10. Body Diode Characteristic at 175 °C

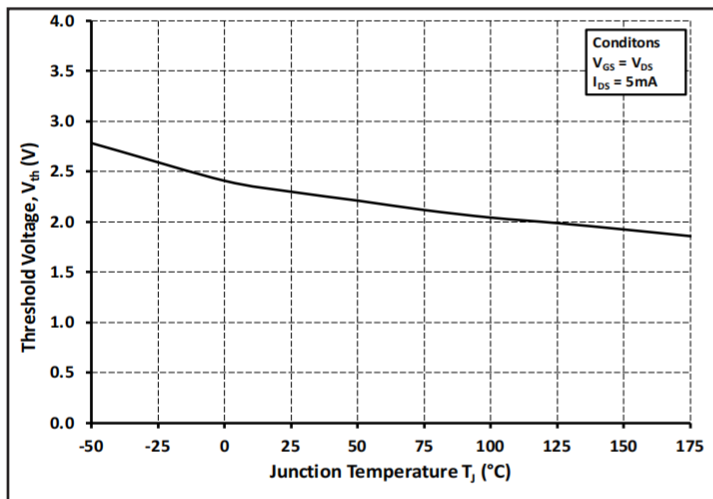


Figure 11. Threshold Voltage vs. Temperature

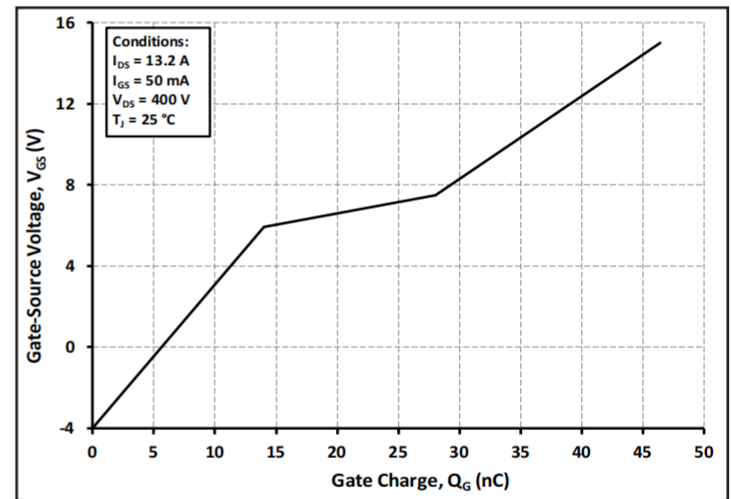


Figure 12. Gate Charge Characteristics

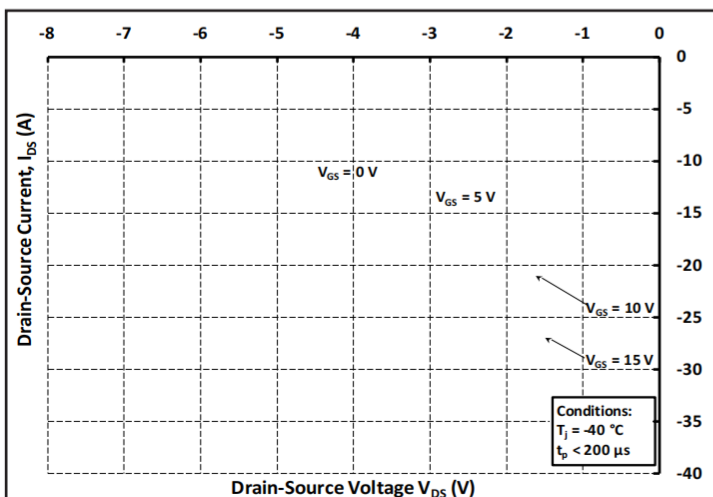


Figure 13. 3rd Quadrant Characteristic at -40 °C

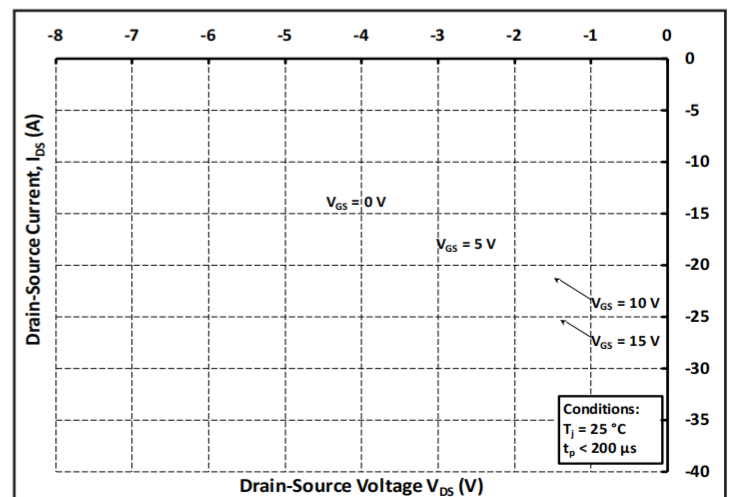


Figure 14. 3rd Quadrant Characteristic at 25 °C

Typical Performance

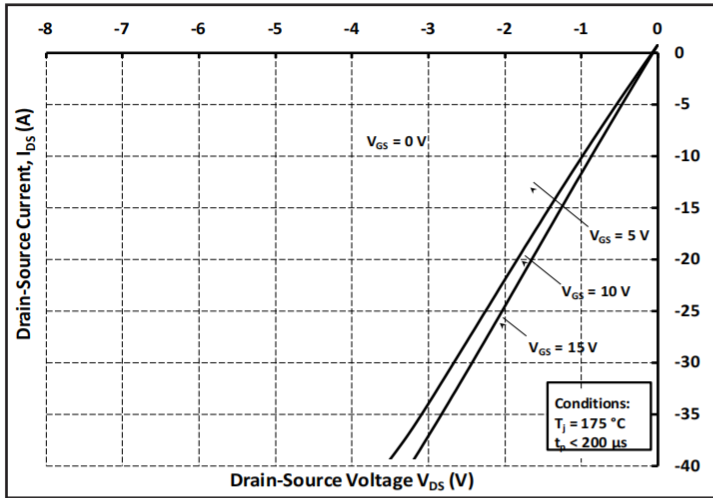


Figure 15. 3rd Quadrant Characteristic at 175 °C

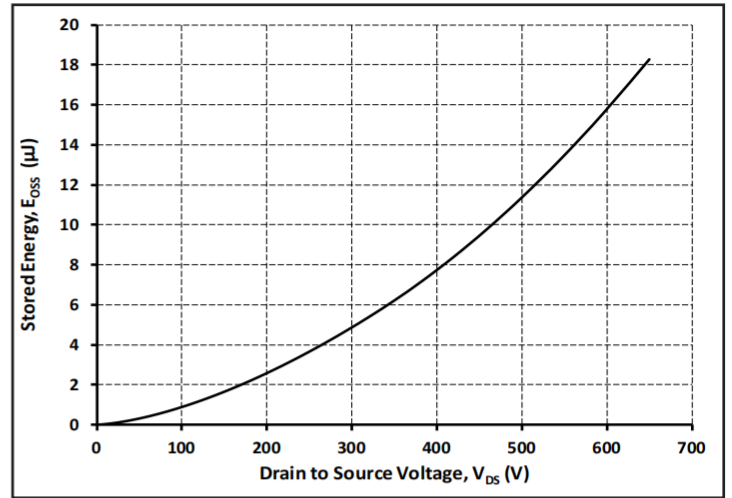


Figure 16. Output Capacitor Stored Energy

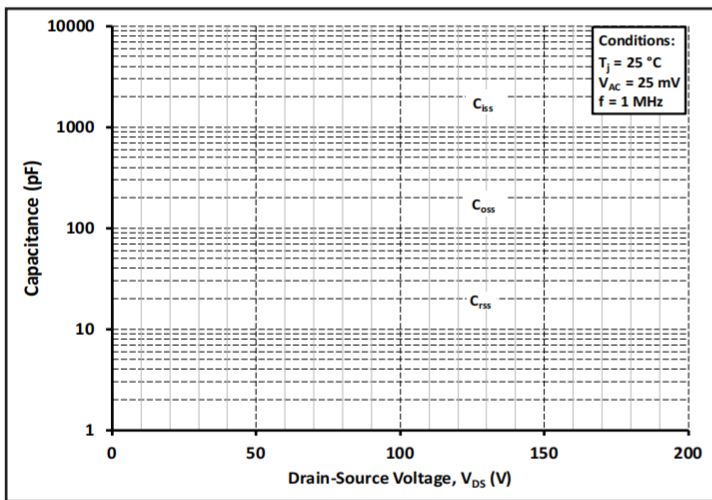


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

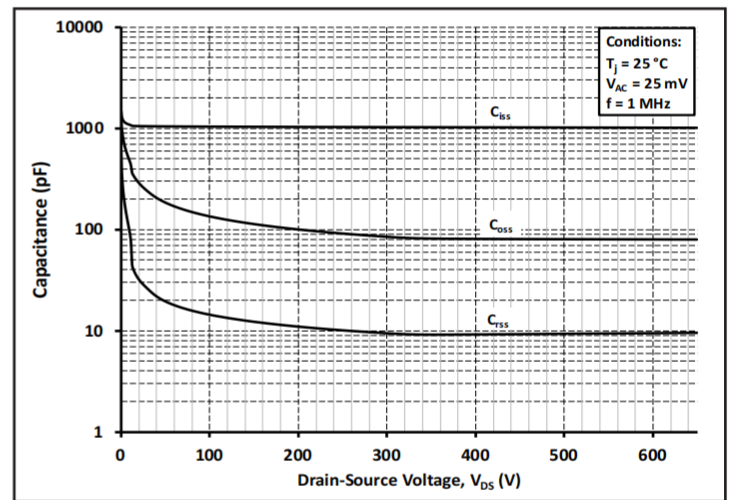


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

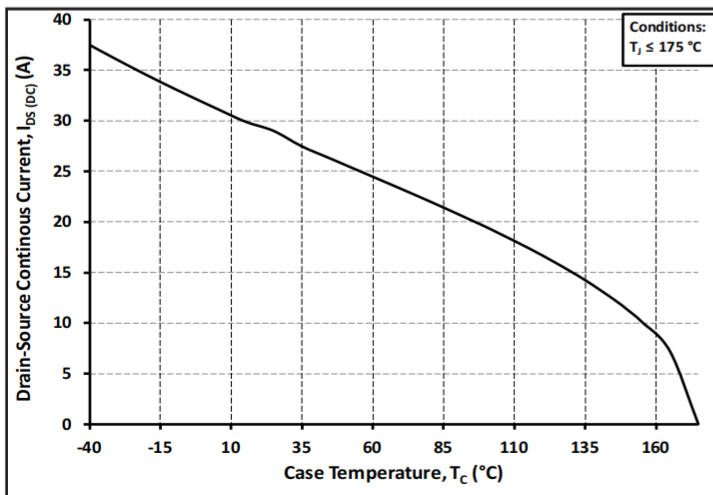


Figure 19. Continuous Drain Current Derating vs. Case Temperature

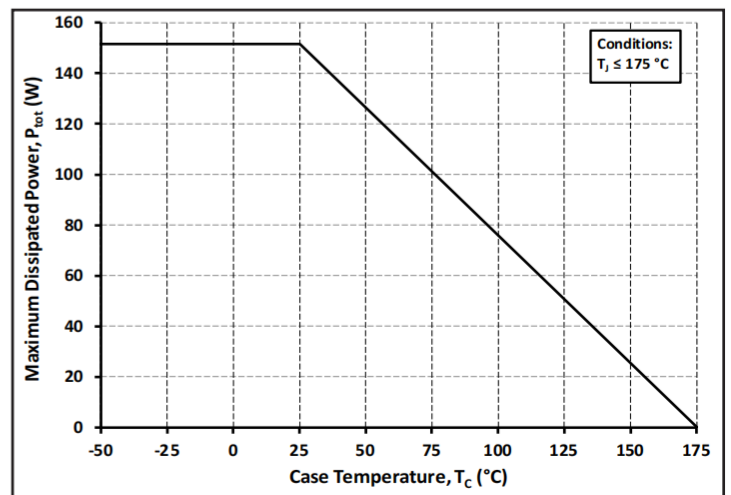


Figure 20. Maximum Power Dissipation Derating Vs Case Temperature

Typical Performance

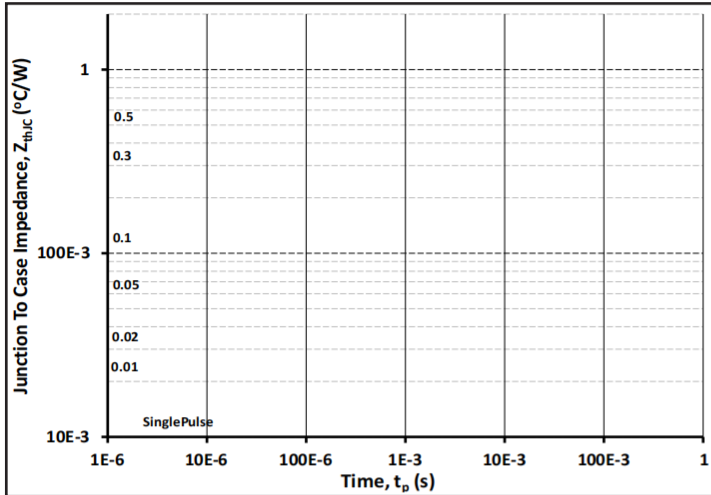


Figure 21. Transient Thermal Impedance (Junction - Case)

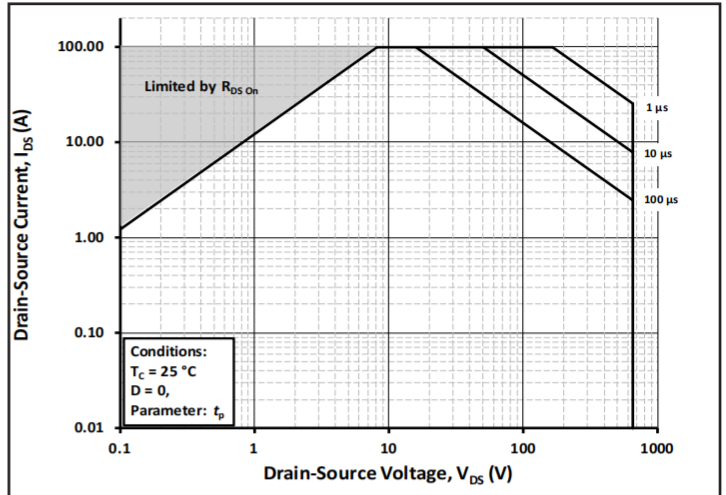


Figure 22. Safe Operating Area

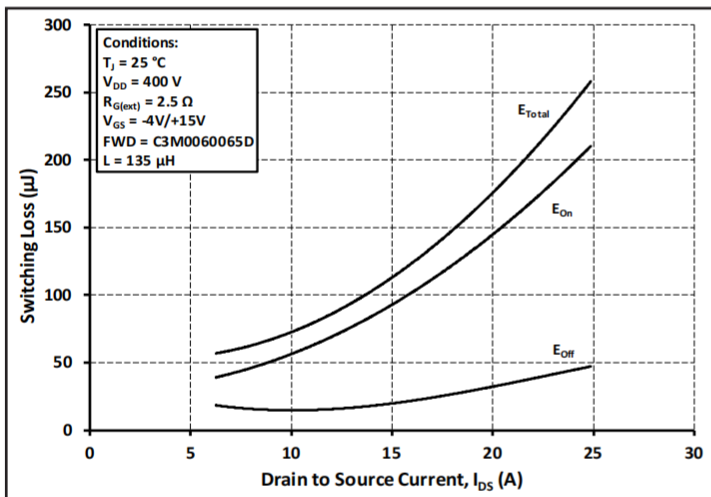


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

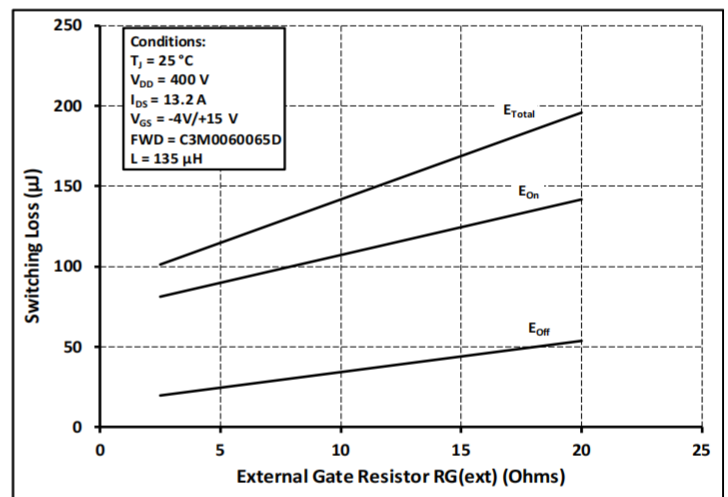


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

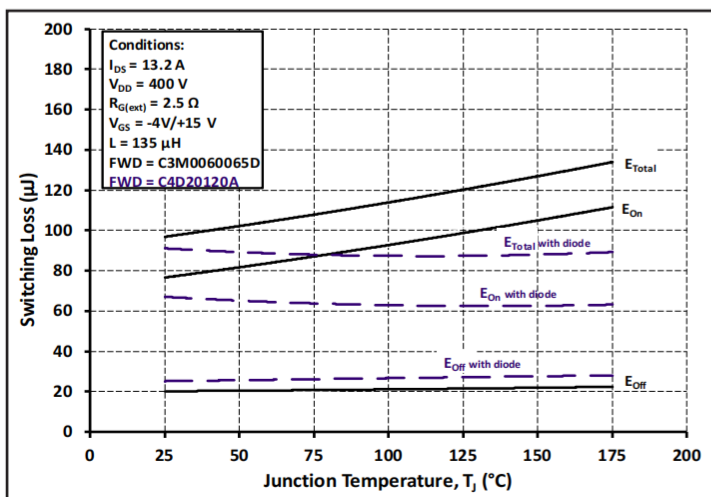


Figure 25. Clamped Inductive Switching Energy vs. Temperature

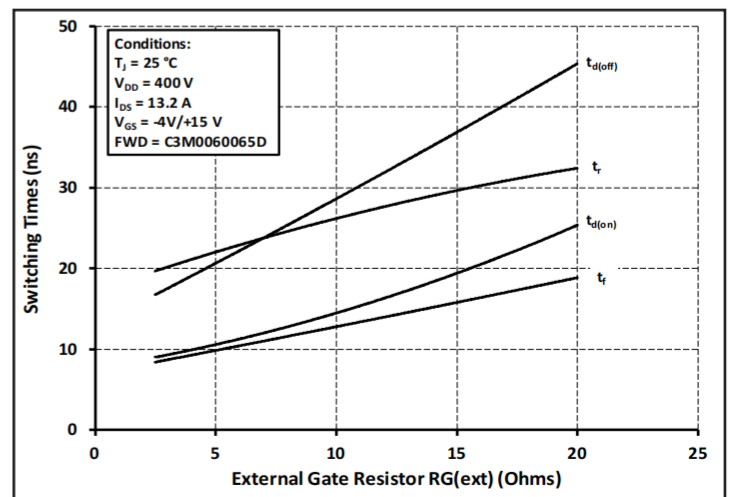


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

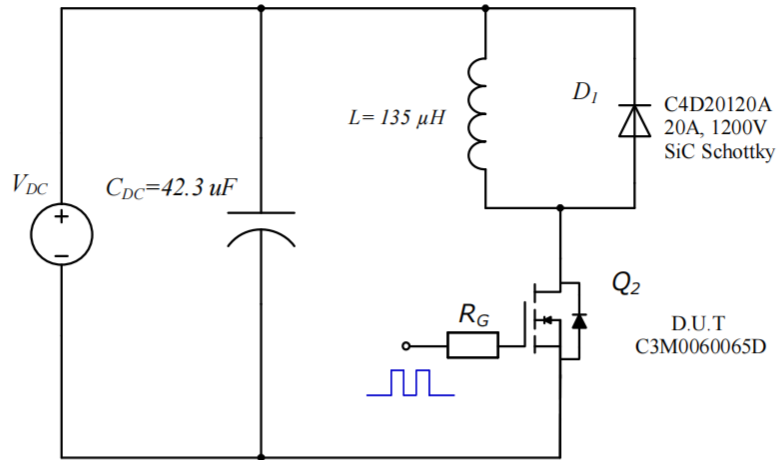


Figure 27. Clamped Inductive Switching Waveform Test Circuit

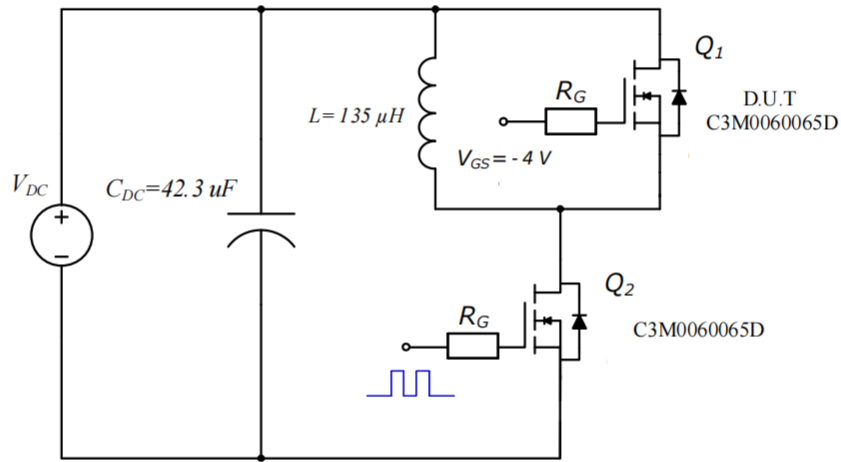


Figure 28. Body Diode Recovery Test Circuit

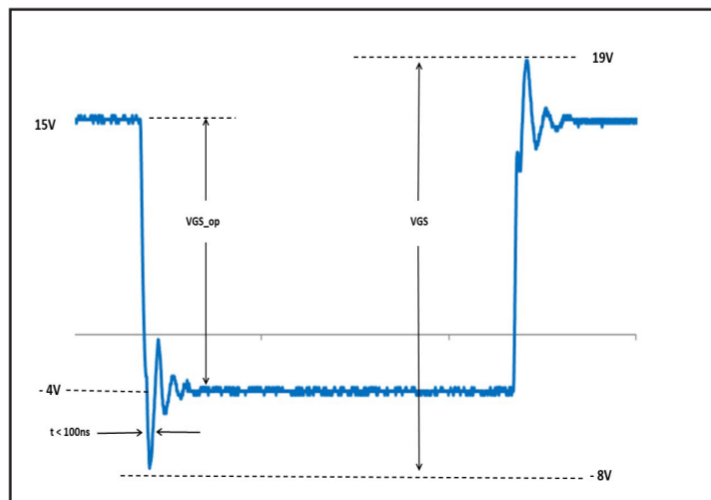
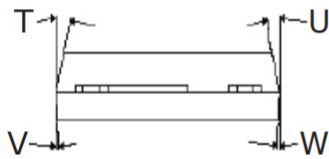
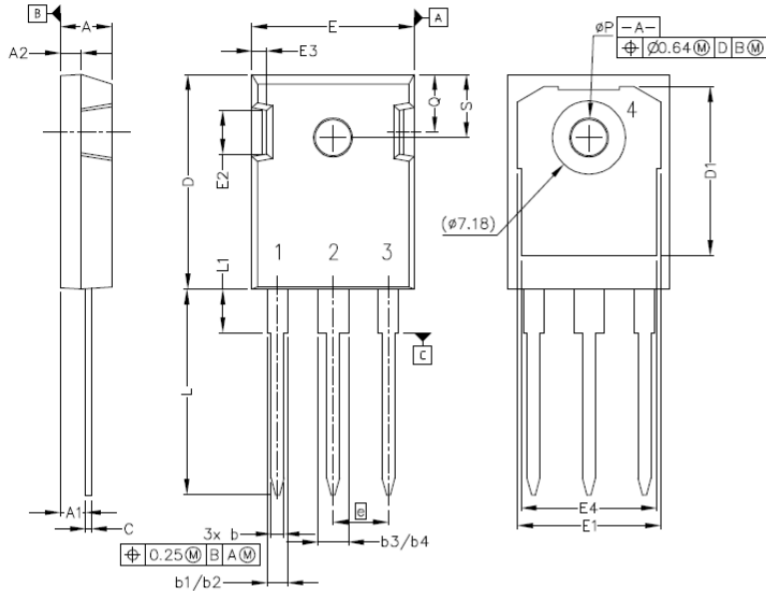


Figure 29. V_{GS} Waveform Example

Package Dimensions

Package TO-247-3

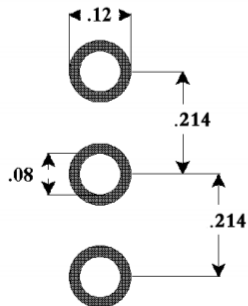


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°

Recommended Solder Pad Layout



TO-247-3

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