

## Silicon Carbide Power MOSFET N-Channel Enhancement Mode

### Features

- ★ 3rd Generation SiC MOSFET technology
- ★ High blocking voltage with low on-resistance
- ★ High-speed switching with low capacitances
- ★ Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- ★ Halogen Free, RoHS Compliant

### Benefits

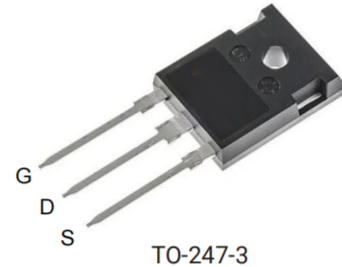
- ★ Higher system efficiency
- ★ Reduced Cooling Requirements
- ★ Increase power density
- ★ Increase system switching frequency
- ★ Easy to parallel and simple to drive
- ★ Enable new hard switching PFC topologies (Totem-Pole)

### Applications

- ★ EV charging
- ★ Solar PV Inverters
- ★ UPS
- ★ SMPS
- ★ DC/DC converters

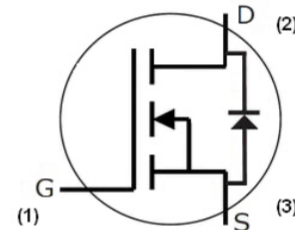
### Product Summary

$V_{DS}$	$R_{DS(on)}$	$I_D @25^\circ$
650V	15m $\Omega$	120A



TO-247-3

Package



### Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note
$V_{DSmax}$	Drain - Source Voltage	650	V	
$V_{GSmax}$	Gate - Source voltage	-8/+19	V	Note 1
$I_D$	Continuous Drain Current, $V_{GS} = 15\text{V}$ , $T_C = 25^\circ\text{C}$	120	A	Fig. 19 Note 2
	Continuous Drain Current, $V_{GS} = 15\text{V}$ , $T_C = 100^\circ\text{C}$	96		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width $t_p$ limited by $T_{Jmax}$	418	A	
$P_D$	Power Dissipation, $T_C = 25^\circ\text{C}$ , $T_J = 175^\circ\text{C}$	416	W	Fig. 20
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$	
$T_L$	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$	
$M_d$	Mounting Torque, (M3 or 6-32 screw)	1 8.8	Nm lbf-in	

Note (1): Recommended turn off / turn on gate voltage  $V_{GS} = -4\text{V} \dots 0\text{V} / +15\text{V}$

Note (2): Package limited to 120 A

**Electrical Characteristics** ( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 15.5\text{ mA}$	Fig. 11
			1.9		V	$V_{DS} = V_{GS}, I_D = 15.5\text{ mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance	10.5	15	21	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 55.8\text{ A}$	Fig. 4, 5, 6
			20			$V_{GS} = 15\text{ V}, I_D = 55.8\text{ A}, T_J = 175^\circ\text{C}$	
$g_{fs}$	Transconductance		42		S	$V_{DS} = 20\text{ V}, I_{DS} = 55.8\text{ A}$	Fig. 7
			40			$V_{DS} = 20\text{ V}, I_{DS} = 55.8\text{ A}, T_J = 175^\circ\text{C}$	
$C_{iss}$	Input Capacitance		5011		pF	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$ $f = 100\text{ KHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		289				
$C_{rss}$	Reverse Transfer Capacitance		31				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		357				Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		516				Note: 3
$E_{oss}$	$C_{oss}$ Stored Energy		29				$\mu\text{J}$
$E_{ON}$	Turn-On Switching Energy (Body Diode)		1500		$\mu\text{J}$	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 55.8\text{ A},$ $R_{G(ext)} = 5\text{ }\Omega, L = 57.6\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
$E_{OFF}$	Turn Off Switching Energy (Body Diode)		700				
$E_{ON}$	Turn-On Switching Energy (External Diode)		1200		$\mu\text{J}$	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 55.8\text{ A},$ $R_{G(ext)} = 5\text{ }\Omega, L = 57.6\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SIC DIODE	Fig. 25
$E_{OFF}$	Turn Off Switching Energy (External Diode)		1000				
$t_{d(on)}$	Turn-On Delay Time		22		ns	$V_{DD} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 55.8\text{ A}, R_{G(ext)} = 5\text{ }\Omega, L = 57.6\text{ }\mu\text{H}$ Timing relative to $V_{DS}$ Inductive load	Fig. 26
$t_r$	Rise Time		125				
$t_{d(off)}$	Turn-Off Delay Time		58				
$t_f$	Fall Time		25				
$R_{G(int)}$	Internal Gate Resistance		1.5		$\Omega$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
$Q_{gs}$	Gate to Source Charge		54		nC	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 55.8\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		62				
$Q_g$	Total Gate Charge		188				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 400V  
 $C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 400V

**Reverse Diode Characteristics** ( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$V_{SD}$	Diode Forward Voltage	4.7		V	$V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 25\text{ }^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 175\text{ }^\circ\text{C}$	
$I_S$	Continuous Diode Forward Current		79	A	$V_{GS} = -4\text{ V}, T_C = 25\text{ }^\circ\text{C}$	
$I_{S,pulse}$	Diode pulse Current		418	A	$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{Jmax}$	
$t_{rr}$	Reverse Recovery time	85		ns	$V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 1500\text{ A}/\mu\text{s}, T_J = 175\text{ }^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	667		nC		
$I_{rrm}$	Peak Reverse Recovery Current	17		A		
$t_{rr}$	Reverse Recovery time	74		ns	$V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 1000\text{ A}/\mu\text{s}, T_J = 175\text{ }^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	562		nC		
$I_{rrm}$	Peak Reverse Recovery Current	14		A		

**Thermal Characteristics**

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.35	$^\circ\text{C}/\text{W}$		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

## Typical Performance

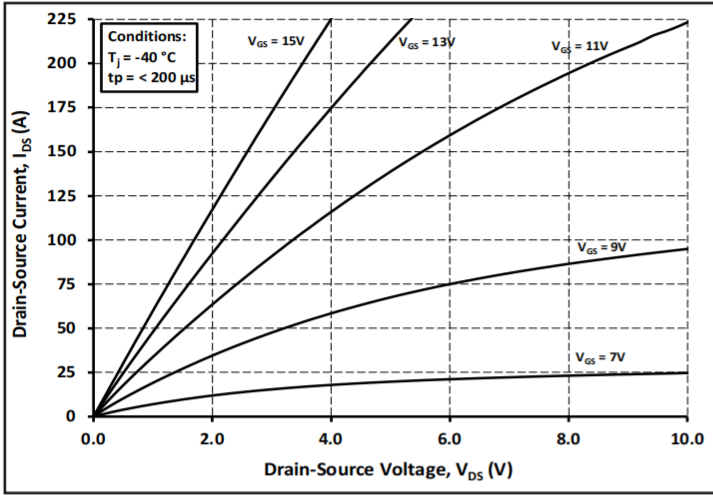


Figure 1. Output Characteristics  $T_j = -40\text{ }^\circ\text{C}$

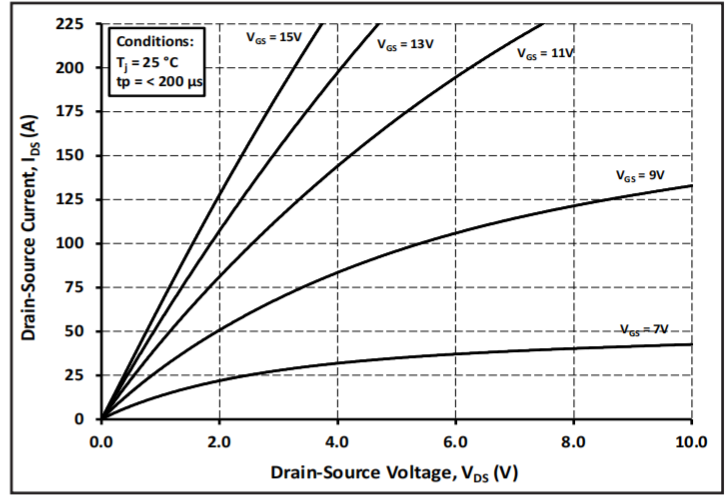


Figure 2. Output Characteristics  $T_j = 25\text{ }^\circ\text{C}$

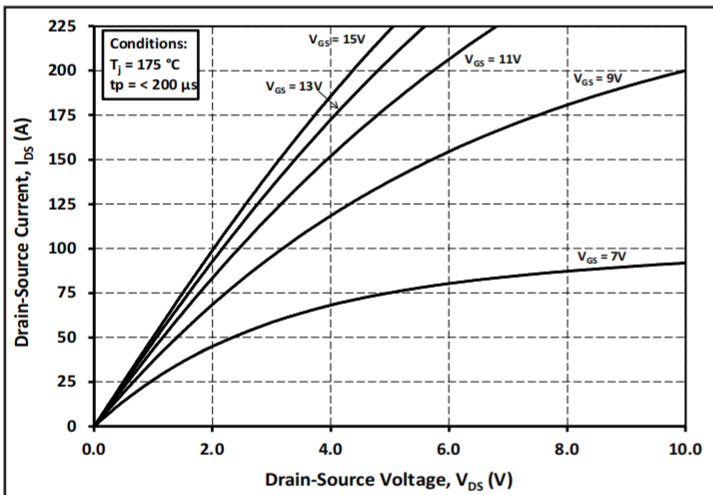


Figure 3. Output Characteristics  $T_j = 175\text{ }^\circ\text{C}$

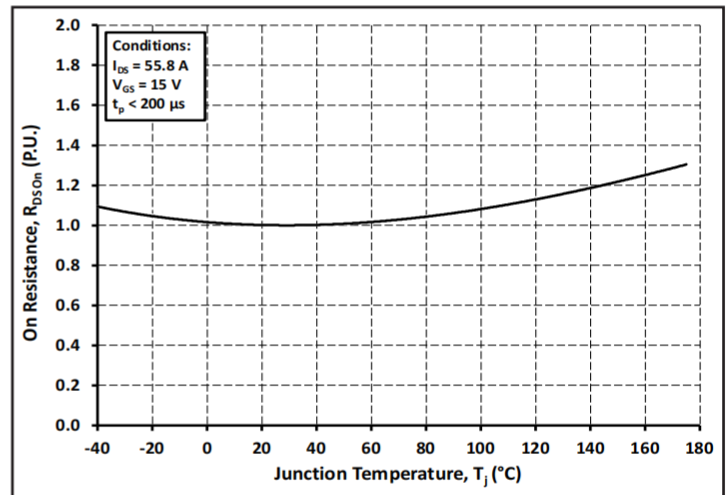


Figure 4. Normalized On-Resistance vs. Temperature

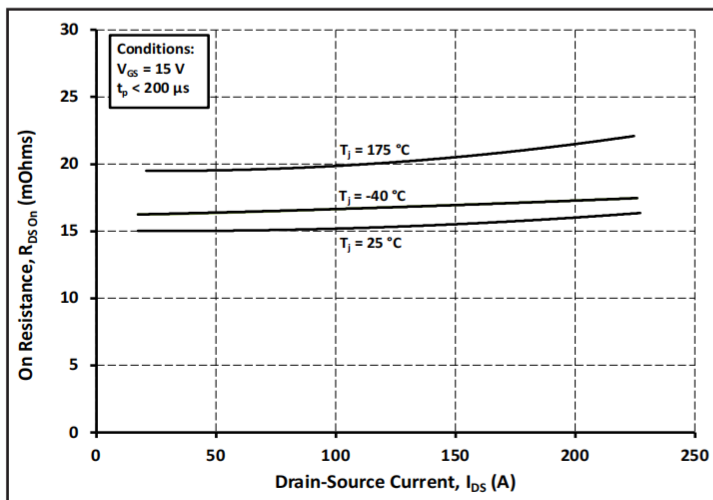


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

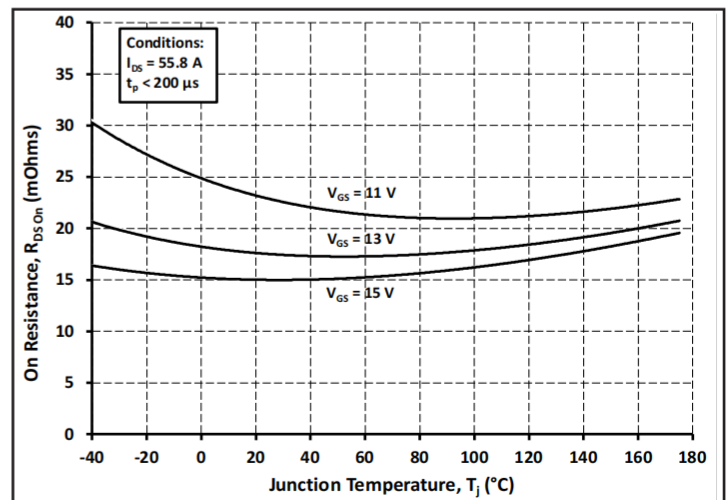


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

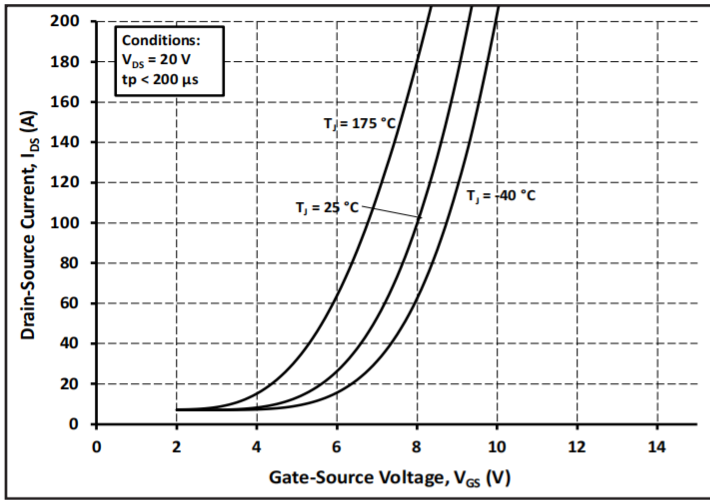


Figure 7. Transfer Characteristic for Various Junction Temperatures

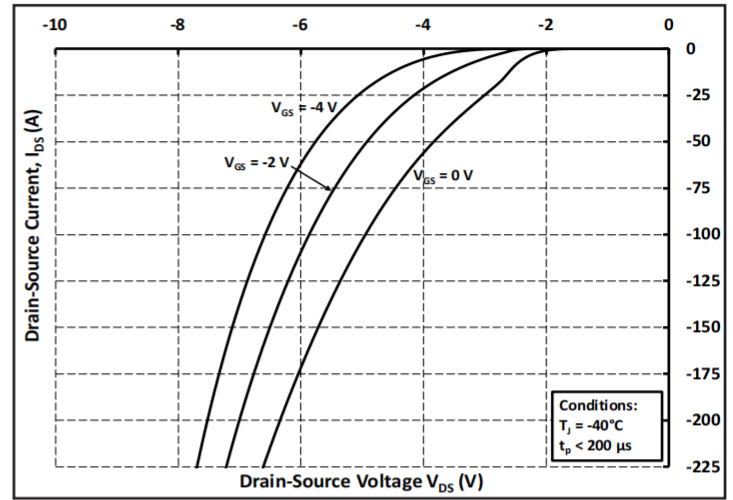


Figure 8. Body Diode Characteristic at -40 °C

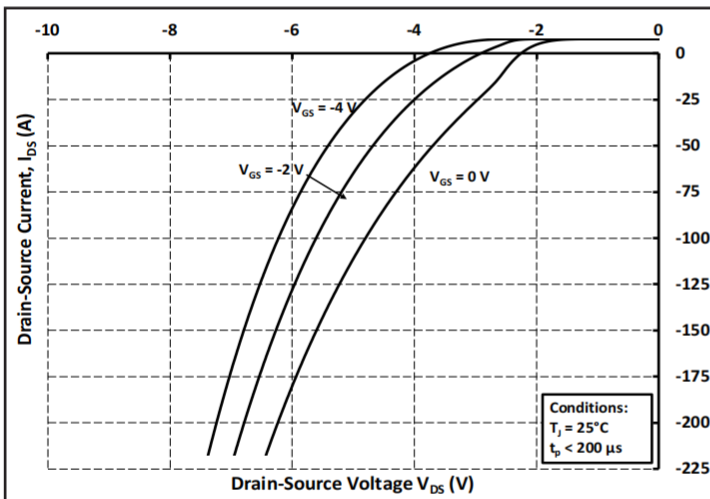


Figure 9. Body Diode Characteristic at 25 °C

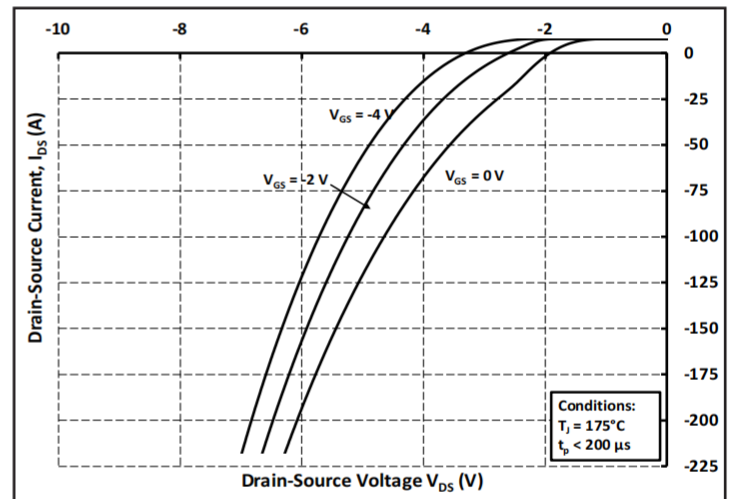


Figure 10. Body Diode Characteristic at 175 °C

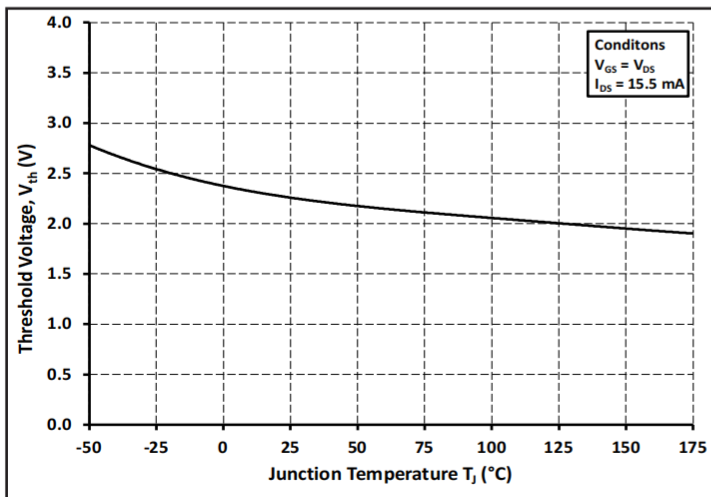


Figure 11. Threshold Voltage vs. Temperature

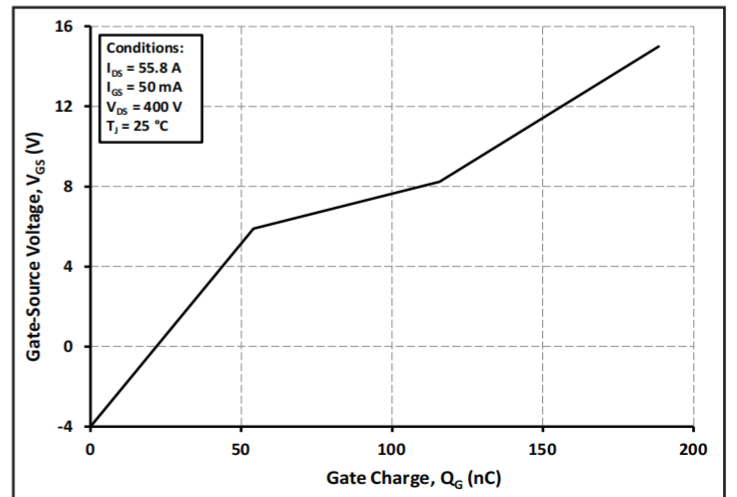


Figure 12. Gate Charge Characteristics

## Typical Performance

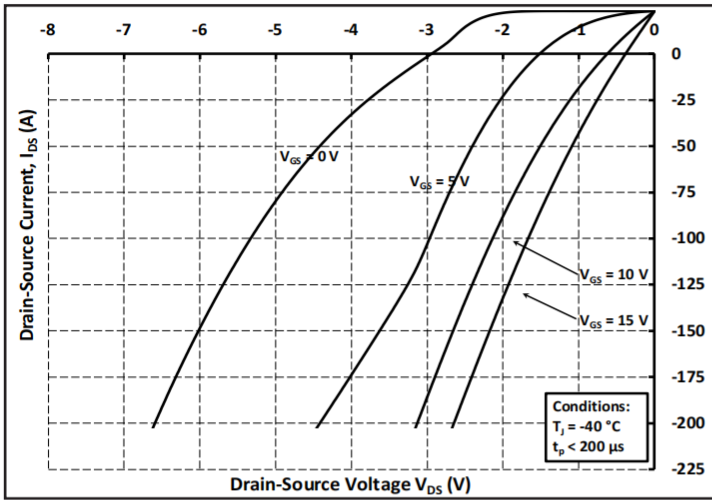


Figure 13. 3rd Quadrant Characteristic at -40 °C

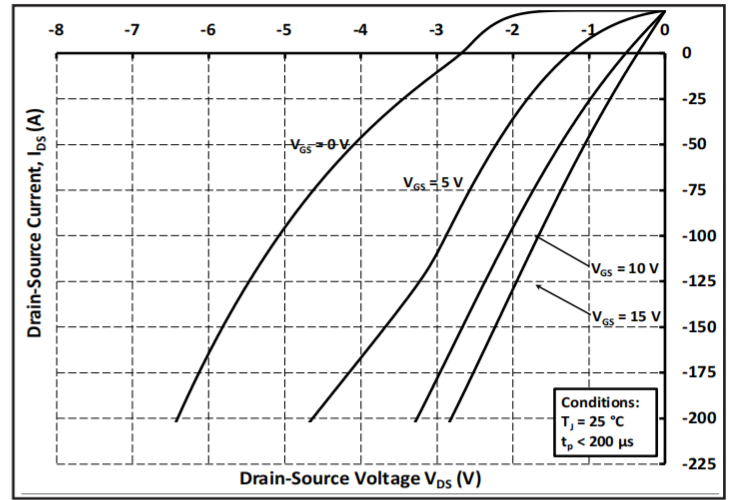


Figure 14. 3rd Quadrant Characteristic at 25 °C

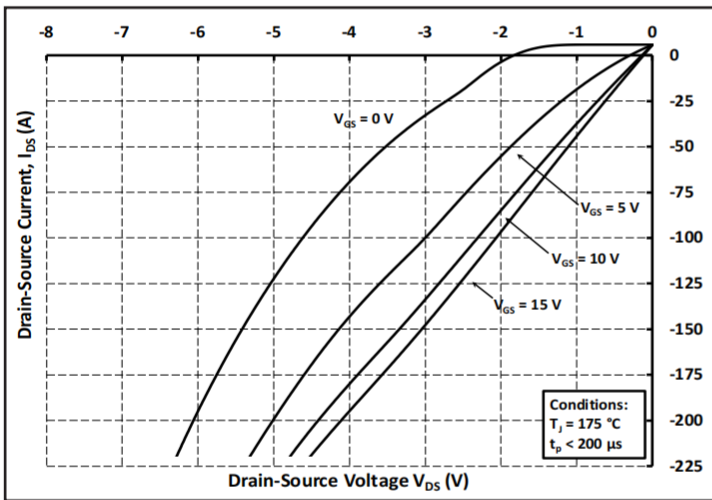


Figure 15. 3rd Quadrant Characteristic at 175 °C

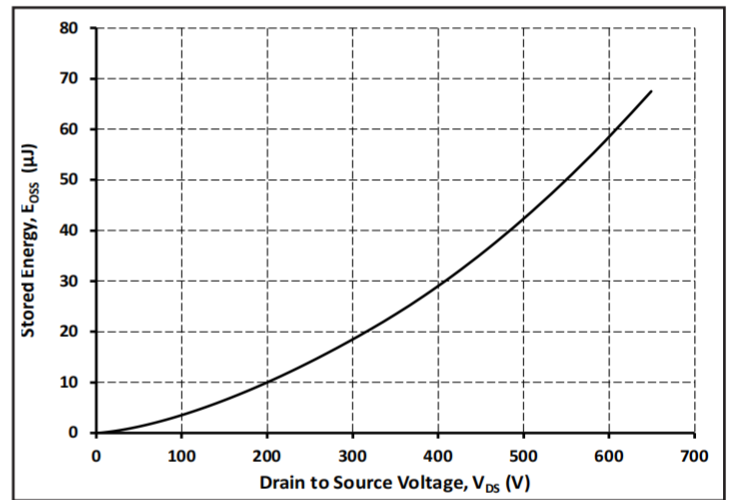


Figure 16. Output Capacitor Stored Energy

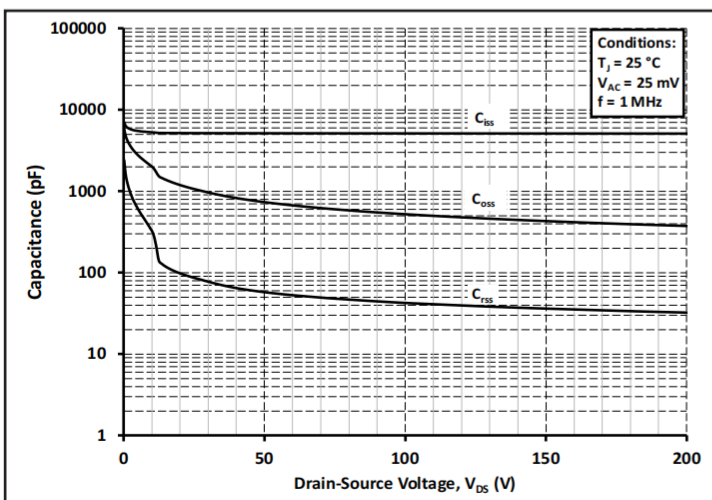


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

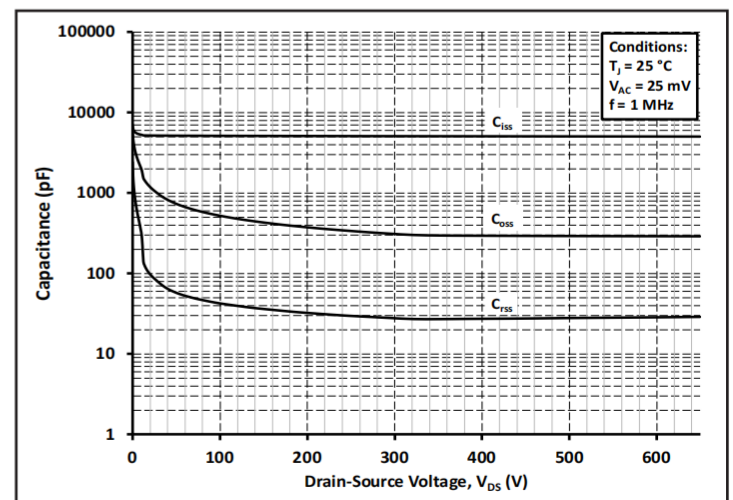


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

## Typical Performance

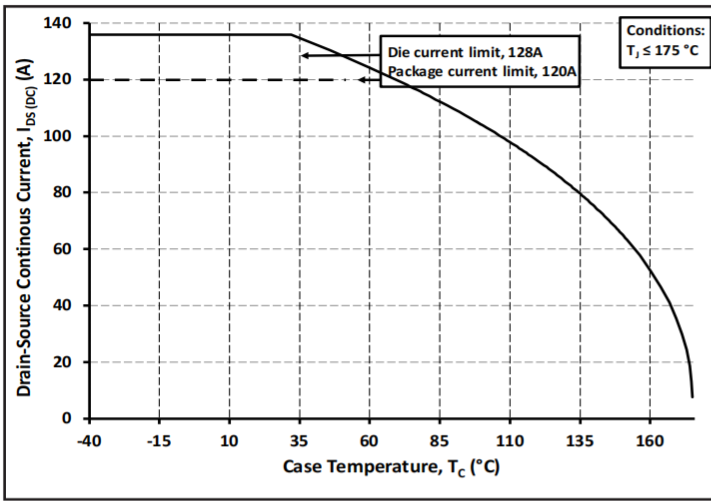


Figure 19. Continuous Drain Current Derating vs. Case Temperature

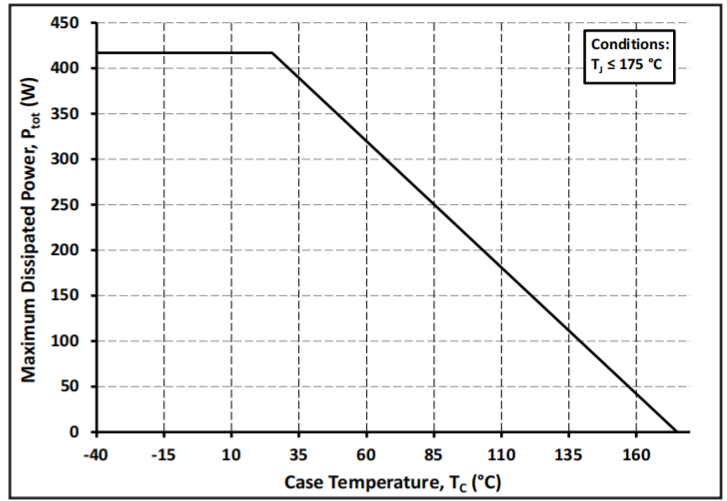


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

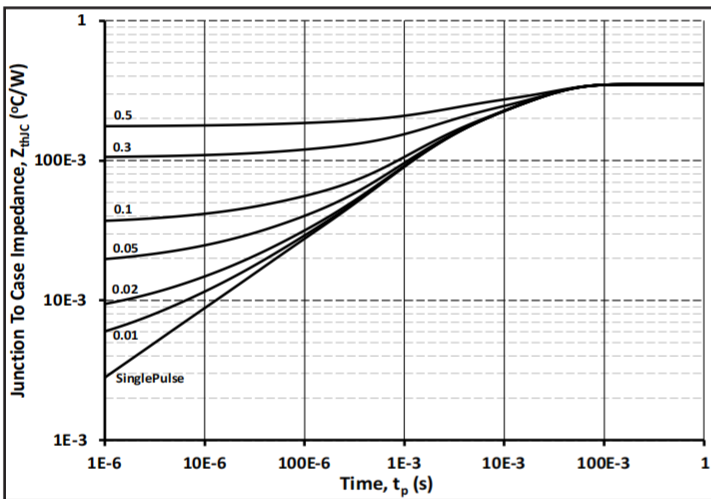


Figure 21. Transient Thermal Impedance (Junction - Case)

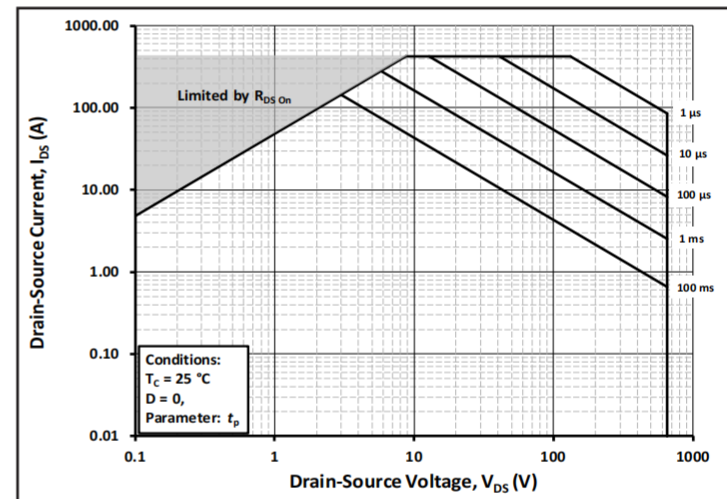


Figure 22. Safe Operating Area

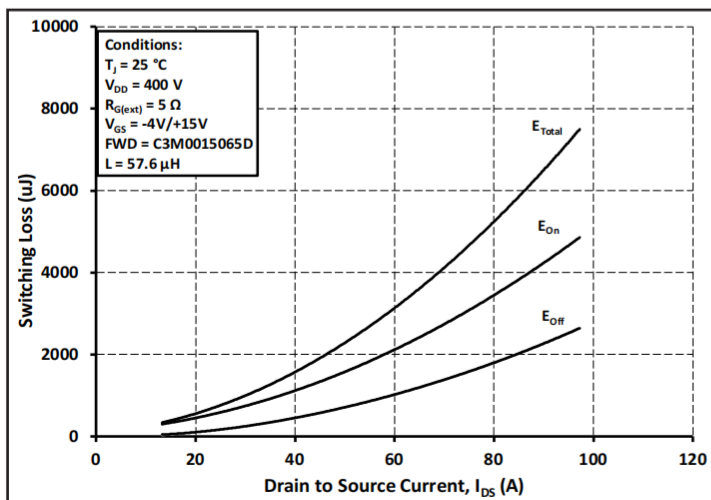


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 400V$ )

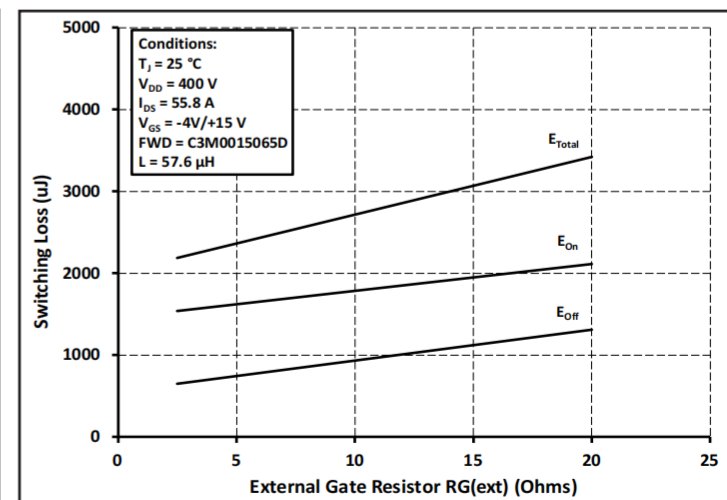


Figure 24. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

## Typical Performance

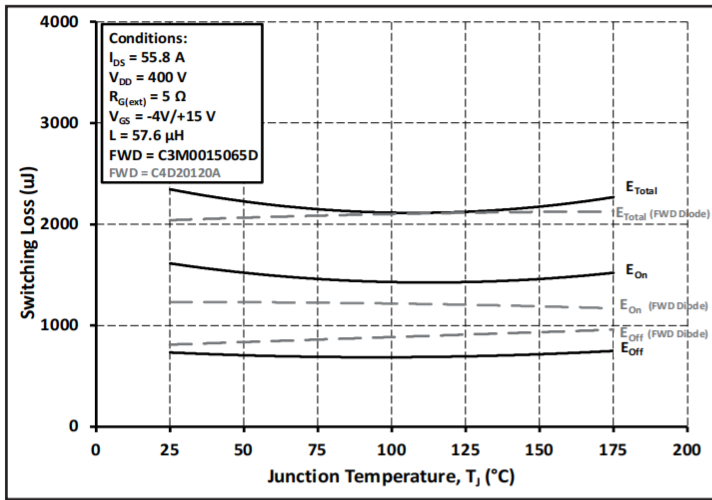


Figure 25. Clamped Inductive Switching Energy vs. Temperature

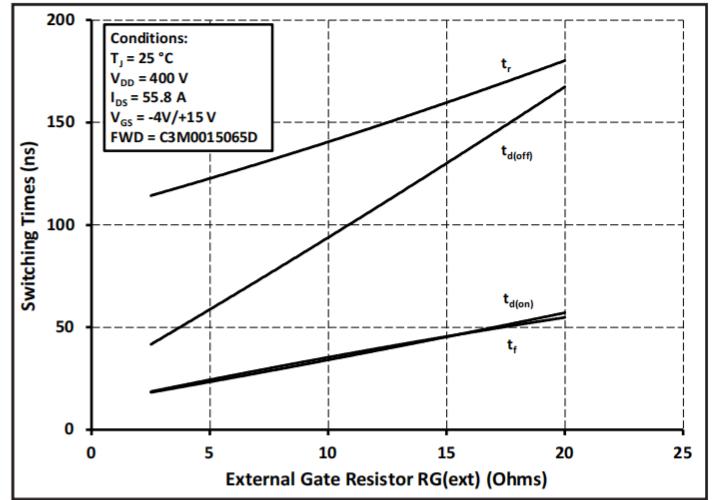


Figure 26. Switching Times vs.  $R_{G(ext)}$

## Test Circuit Schematic

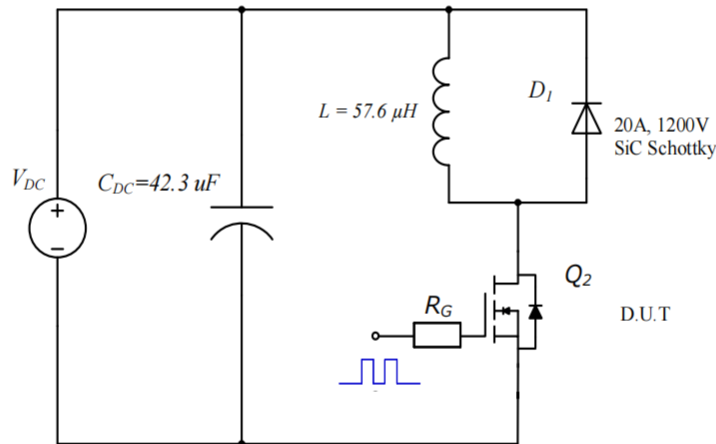


Figure 27. Clamped Inductive Switching Waveform Test Circuit

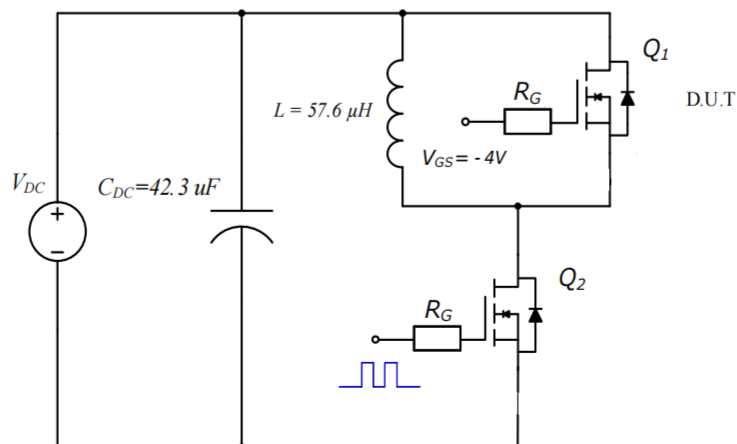
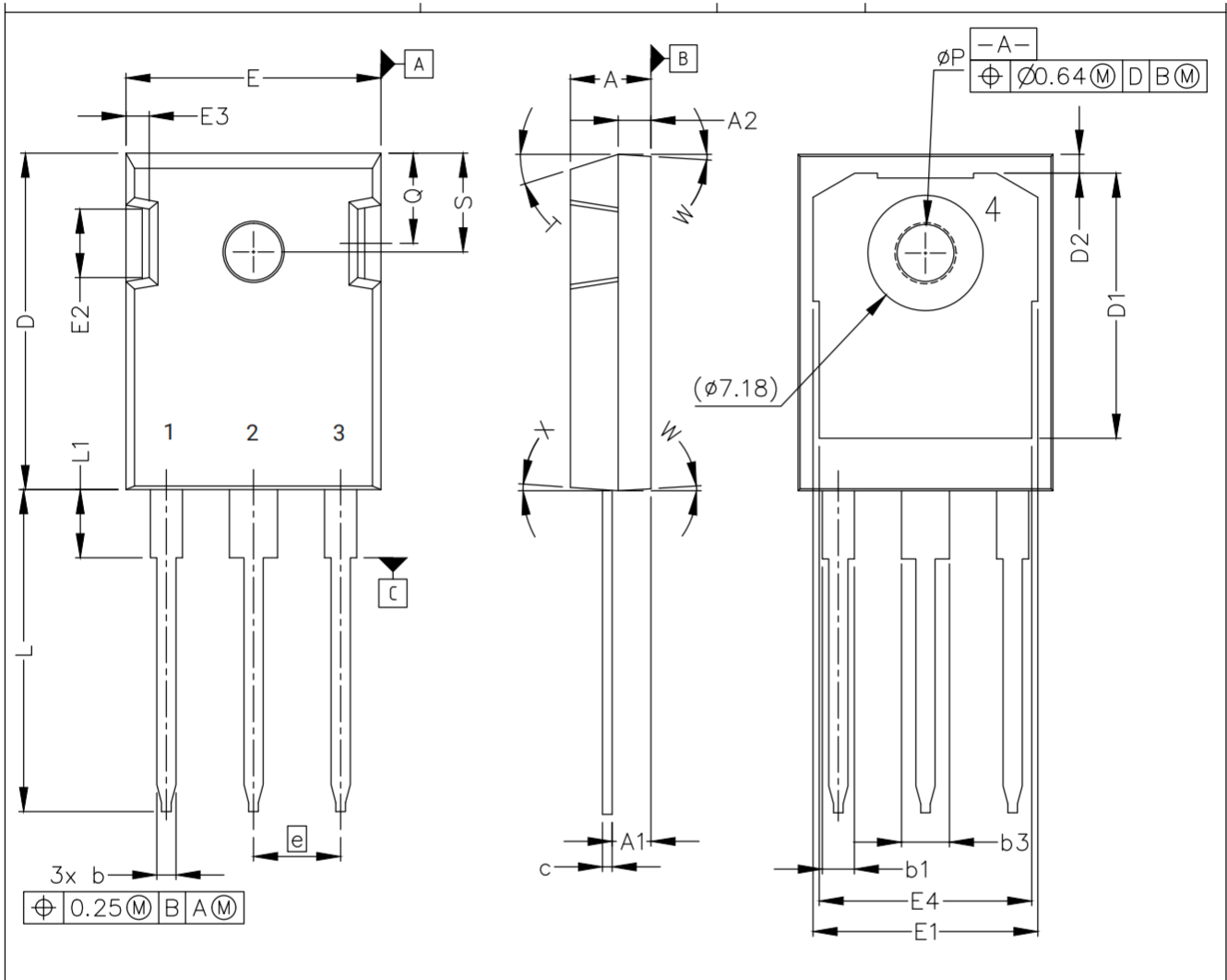


Figure 28. Body Diode Recovery Test Circuit

### Package Dimensions

Package TO-247-3



- NOTE ;
1. ALL METAL SURFACES: TIN PLATED, EXCEPT AREA OF CUT
  2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
  3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
  4. THIS DRAWING WILL MEET ALL DIMENSIONS REQUIREMENT OF JEDEC outlines TO-247 AD.
  5. DIMENSION DO NOT INCLUDE BURR OR MOLD FLASH.

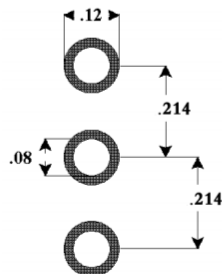
- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - DRAIN (COLLECTOR)

## Package Dimensions

Package TO-247-3

SYM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	.190	.205
A1	2.29	2.54	.090	.100
A2	1.91	2.16	.075	.085
b	1.07	1.33	.042	.052
b1	1.91	2.41	.075	.095
b3	2.87	3.38	.113	.133
c	0.55	0.68	.022	.027
D	20.80	21.10	.819	.831
D1	16.25	17.65	.640	.695
D2	0.95	1.25	.037	.049
E	15.75	16.13	.620	.635
E1	13.10	14.15	.516	.557
E2	3.68	5.10	.145	.201
E3	1.00	1.90	.039	.075
E4	12.38	13.43	.487	.529
e	5.44 BSC		.214 BSC	
N	3		3	
L	19.81	20.32	.780	.800
L1	4.10	4.40	.161	.173
φP	3.51	3.65	.138	.144
Q	5.49	6.00	.216	.236
S	6.04	6.30	.238	.248
T	17.5° REF.			
W	3.5° REF.			
X	4° REF.			

## Recommended Solder Pad Layout



TO-247-3

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[C3M0280090J](#) [SCT2750NYTB](#) [SCT2H12NYTB](#) [CDMS24783-120 SL](#) [C3M0016120K](#) [C3M0045065D](#) [C3M0045065K](#) [E3M0120090J](#)  
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