

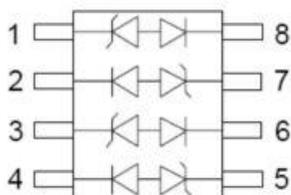
## LCDA03 THRU LCDA24 TVS ARRAY SERIES



### Description

The LCDAXX series of TVS array are designed to protect sensitive electronics from damage or latch-up due to ESD and other voltage-induced transient events. Each device will protect two high-speed lines. They are bi-directed devices and may be used on lines where the signal polarities are above and below ground

### Schematic & Pin Configuration



### Features

- Protects 3.3, 5, 12, 15, 24 V Components
- Bidirectional
- Low capacitance for high-speed data lines
- 300 W @ 8/20 us
- Protect 2 I/O Lines
- SO-8 Packaging
- Solid-state silicon avalanche technology
- “-A” is an AEC-Q101 qualified device
- This is a Pb – Free Device
- All SMC parts are traceable to the wafer lot
- Additional testing can be offered upon request

### Mechanical Characteristics

- SO-8 Surface Mount Package
- Approximate Weight: 0.1 grams
- PIN #1 Indicator: DOT on top of package
- Packaging: Tubes or Tape & Reel per EIA Standard 481

### Application

- High-Speed Data Lines
- Microprocessor Based Equipment
- Universal Serial Bus(USB) Port Protection
- Notebooks, Desktops, & Servers
- Instrumentation
- LAN/WAN Equipment
- Peripherals

### Absolute Maximum Ratings:

| Parameter                                 | Symbol           | Value         | Units |
|---|------------------|---------------|-------|
| Peak Pulse Power, 8/20 $\mu$ s Wave shape | P                | 300           | W     |
| Operating Temperature                     | T <sub>J</sub>   | -55 to +125   | °C    |
| Storage Temperature                       | T <sub>stg</sub> | -55 to +150   | °C    |
| Lead Soldering Temperature                | T <sub>L</sub>   | 260 (10 Sec.) | °C    |

**Electrical Characteristics@25°C**

| Part Number | Stand-off Voltage $V_{wm}$ (V) Max | Breakdown Voltage $V_{BR}$ @1mA (V) Min | Clamping Voltage $V_c$ @ 1 A (V) Max | Leakage Current $I_R$ @ $V_{wm}$ (uA) Max | Capacitance (f = 1MHz) C @ 0V (pF) Max | Temperature Coefficient of $V_{BR}$ a( $V_{BR}$ ) mv/°C Max |
|-------------|------------------------------------|---|--------------------------------------|---|--|---|
| LCDA03      | 3.3                                | 4                                       | 7                                    | 200                                       | 5                                      | -5  |
| LCDA05      | 5.0                                | 6                                       | 9.8                                  | 20  | 5                                      | 1   |
| LCDA12      | 12.0                               | 13.3                                    | 19                                   | 1   | 5                                      | 8   |
| LCDA15      | 15.0                               | 16.7                                    | 24                                   | 1   | 5                                      | 11  |
| LCDA24      | 24.0                               | 26.7                                    | 43                                   | 1   | 5                                      | 28  |

**Ratings and Characteristics Curves**

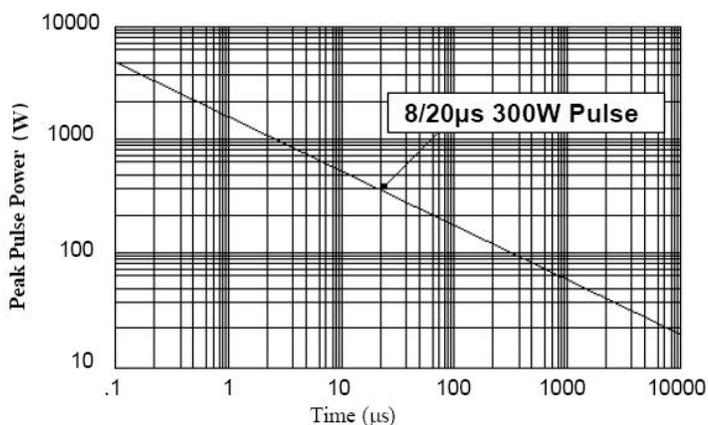


Figure 1. Peak Pulse Power Vs Pulse Time (µs)

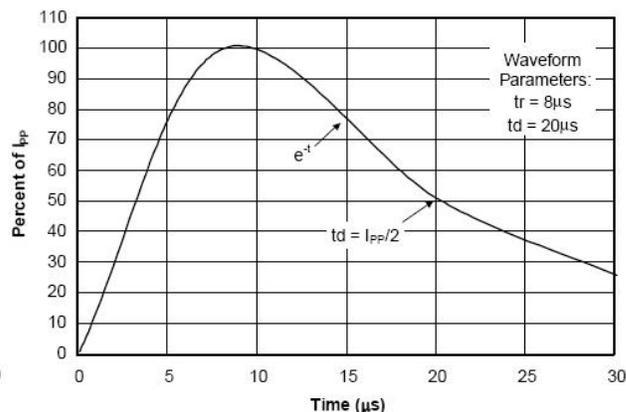


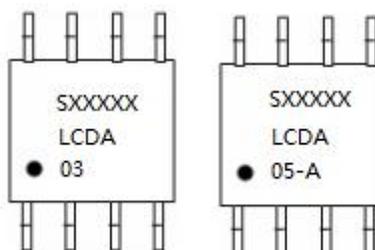
Figure 2. Pulse Wave Form

**Ordering Information**

| Device                       | Package        | Shipping       |
|------------------------------|----------------|----------------|
| LCDA03<br>THRU<br>LCDA24     | SO-8 (Pb-Free) | 2500pcs / reel |
| LCDA03TR<br>THRU<br>LCDA24TR | SO-8 (Pb-Free) | 2500pcs / reel |

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our tape and reel packaging specification.

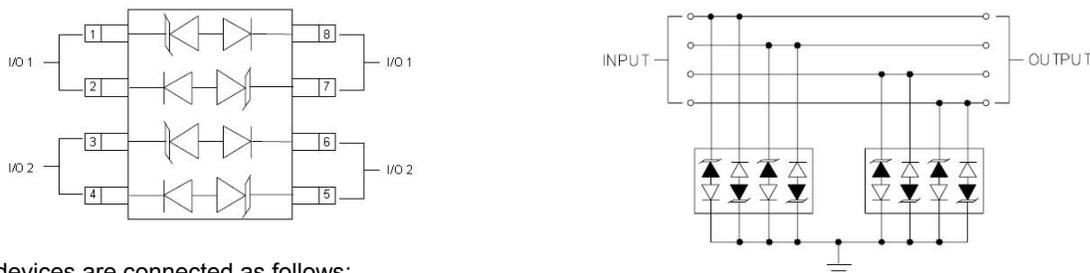
**Marking Diagram**



Where XXXXX is YYWWL

LCDA03 = Part Name  
-A = AEC-Q101  
S = S  
YY = Year  
WW = Weak  
L = Lot Number

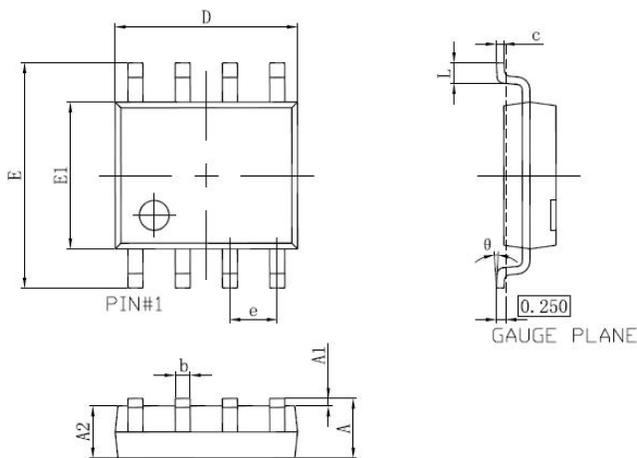
**Circuit Diagram**



The devices are connected as follows:

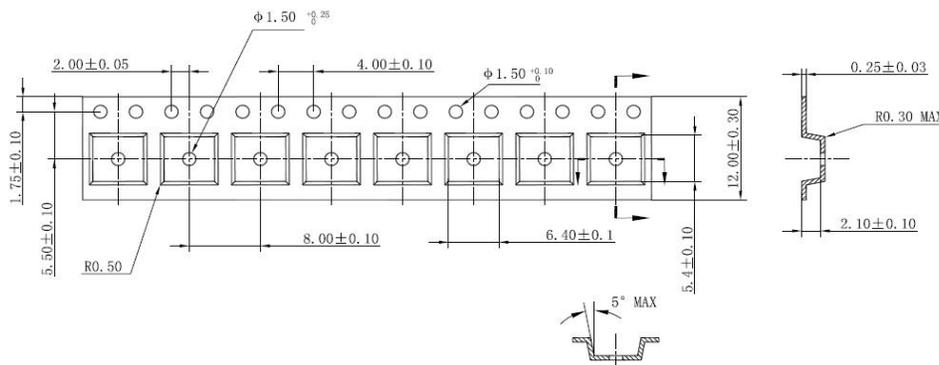
- ✓ Pins 1 and 2 are tied together and pins 7 and 8 are tied together providing the protection circuit for one I/O line. Pins 3 and 4 are tied together and pins 5 and 6 are tied together providing the protection circuit for the second I/O line. Since the device is electrically symmetrical, either side of the connected pairs may be used to protect the lines. The other side of the pair is used to make the ground connection. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

**Mechanical Dimensions SO-8**



| SYMBOL | Millimeters |       | Inches |       |
|--------|-------------|-------|--------|-------|
|        | MIN.        | MAX.  | MIN.   | MAX.  |
| A      | 1.350       | 1.800 | 0.053  | 0.071 |
| A1     | 0.100       | 0.250 | 0.004  | 0.010 |
| A2     | 1.350       | 1.750 | 0.053  | 0.069 |
| b      | 0.306       | 0.510 | 0.012  | 0.020 |
| c      | 0.150       | 0.300 | 0.006  | 0.012 |
| D      | 4.720       | 5.120 | 0.186  | 0.202 |
| e      | 1.140       | 1.400 | 0.045  | 0.055 |
| E      | 5.700       | 6.300 | 0.224  | 0.248 |
| E1     | 3.750       | 4.150 | 0.148  | 0.163 |
| L      | 0.300       | 1.270 | 0.012  | 0.050 |
| θ      | 0°          | 8°    | 0°     | 8°    |

**Carrier Tape Specification SO-8**



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