EFR32MG29 Wireless SoC Family Data Sheet

The EFR32MG29 wireless SoCs are ideal for battery-powered IoT end devices. With support for both buck and boost DC-DC, the device can provide the ultimate in battery flexibility. Buck DC-DC is ideal for devices that run on batteries with voltage range from 1.8 to 3.8 V, such as coin cells and dual alkaline cells. The boost DC-DC operates from 1.2 to 1.7 V and is ideal where smaller form-factor or lower cost batteries such as button cell or single alkaline cells are required.

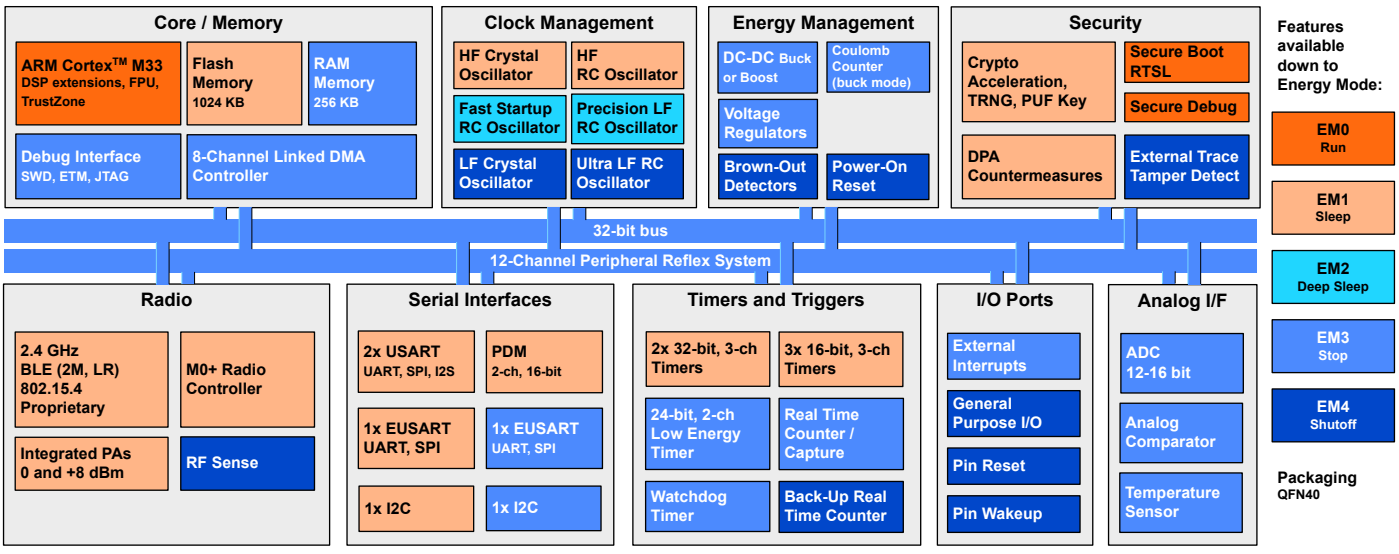
The tri-core device has a Cortex®-M33 running up to 76.8 MHz and dedicated cores for the radio and security, offloading timing critical operations. With key features like high-performance 2.4 GHz RF, low current consumption, and Secure Vault™ High, IoT device makers can create smart, robust, and energy-efficient products that are secure from remote and local cyber-attacks. In addition, 1024 KB of flash and 256 KB of RAM ensures there is enough memory for Zigbee and multiprotocol applications.

EFR32MG29 applications include battery-powered devices for:

- Smart Home
- Building Automation
- Security Systems

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 76.8 MHz maximum operating frequency
- 1024 KB of flash and 256 KB of RAM
- Energy-efficient core with low active and sleep currents
- Integrated PA with up to 8 dBm (2.4 GHz) TX power
- Secure Vault™ High
- DC-DC supporting buck (1.8-3.8 V) or boost (1.2-1.7 V) operation
- Available in QFN packaging



1. Feature List

The EFR32MG29 highlighted features are:

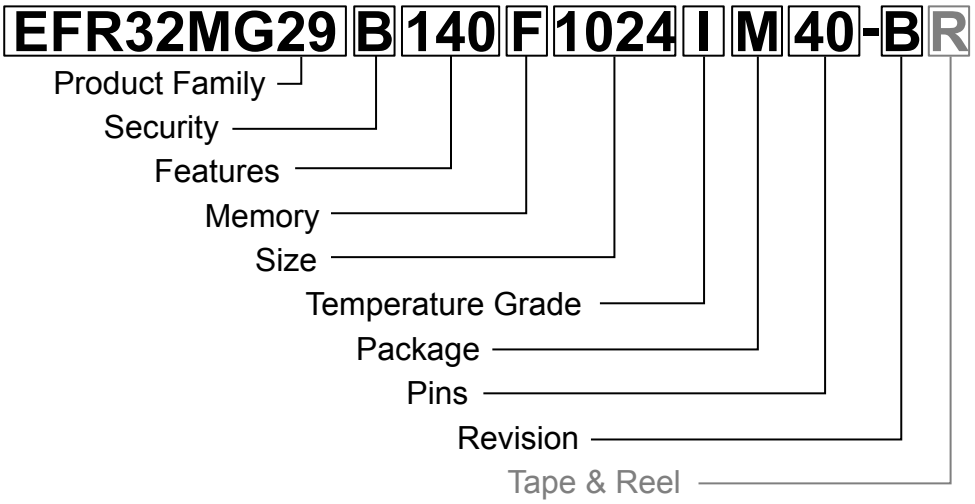
- **Low-Power Wireless System-on-Chip**
  - High-performance 32-bit 76.8 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 1024 KB flash program memory
  - 256 KB RAM data memory
  - 2.4 GHz radio operation
- **Radio Performance**
  - -102.2 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -106.8 dBm sensitivity @ 125 kbps GFSK
  - -99 dBm sensitivity @ 1 Mbit/s GFSK
  - -96.1 dBm sensitivity @ 2 Mbit/s GFSK
  - TX power up to 8 dBm
- **Low System Energy Consumption**
  - 4.1 mA RX current (250 kbps O-QPSK DSSS)
  - 3.6 mA RX current @ 1 Mbps GFSK (Buck DCDC, 3 V)
  - 4 mA TX current @ 0 dBm output power (Buck DCDC, 3 V)
  - 9 mA TX current @ 6 dBm output power (Buck DCDC, 3 V)
  - 11 mA TX current @ 8 dBm output power (Buck DCDC, 3 V)
  - 30 µA/MHz in Active Mode (EM0) at 76.8 MHz (Buck DCDC, 3 V)
  - 3.4 µA EM2 DeepSleep current (256 KB RAM retention and RTC running from LFXO, Buck DCDC, 3 V)
  - 1.5 µA EM2 DeepSleep current (16 KB RAM retention and RTC running from LFXO, Buck DCDC, 3 V)
  - 0.16 µA EM4 current
- **Supported Modulation Format**
  - OQPSK DSSS
  - 2 (G)FSK with fully configurable shaping
  - (G)MSK
- **Protocol Support**
  - Zigbee PRO / Green Power
  - Bluetooth Low Energy
  - Proprietary
- **Secure Vault High**
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
  - Designed for PSA level 3 certification
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - Analog Comparator (ACMP)
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 3 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low-Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 2 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - Precision Low-Frequency RC Oscillator to replace 32 kHz sleep crystal
  - RFSENSE with selective OOK mode
  - Die temperature sensor with +/-1.5 degree C accuracy after single-point calibration
  - Coulomb counter integrated into Buck DC-DC
- **Wide Operating Range**
  - Devices with Buck DC-DC
    - 1.8 to 3.8 V supply range
    - -40 to 125 °C operating temperature
  - Devices with Boost DC-DC
    - 1.2 to 1.7 V supply range
    - -20 to 55 °C operating temperature
- **Packages**
  - **QFN40** 5 × 5 × 0.85 mm, 0.4 mm pitch

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	DC-DC	Flash (KB)	RAM (KB)	GPIO	Package	Temp Range
EFR32MG29B230F1024CM40-B	• Zigbee PRO • Zigbee Green Power • Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	6 dBm	Boost	1024	256	25	QFN40	-20 to 55 °C
EFR32MG29B140F1024IM40-B	• Zigbee PRO • Zigbee Green Power • Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	8 dBm	Buck	1024	256	26	QFN40	-40 to 125 °C

Bluetooth 5.x: As the Bluetooth standard evolves, Silicon Labs is regularly adding new features. For more information on supported Bluetooth capabilities, visit https://www.silabs.com/bluetooth-hardware.



Field	Options
Product Family	• **EFR32MG29**: Wireless SoC Family
Security	• **B**: Secure Vault High

Features [f1][f2][f3]	• f1
	  • **1**: DC-DC Buck Converter
	  • **2**: DC-DC Boost Converter
	• f2
	  • **3**: 6 dBm PA Transmit Power
	  • **4**: 8 dBm PA Transmit Power
	• f3
	  • **0**: 256 KB RAM

Memory	• **F**: Flash
Size	• **Memory Size** in KBytes
Temperature Grade	• **C**: -20 to +55 °C • **I**: -40 to +125 °C
Package	• **M**: QFN
Pins	• **Number of Package Pins**
Revision	• **B**: Revision B
Tape & Reel	• **R**: Tape & Reel (optional)

Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high-performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices which require high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. A detailed functional description is available in the EFR32xG29 Reference Manual.

3.2 Radio

The EFR32MG29 Wireless features a highly configurable radio transceiver which supports Zigbee and Bluetooth Low Energy wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RF2G4_IO). The external components for the antenna interface in typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32MG29 contains a high-performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32MG29 uses a low-IF receiver architecture, which consists of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF Analog-to-Digital Converter (IFADC).

The IF frequency is configurable from 150 to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high-quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, level-based proximity detection, and RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32MG29 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MG29. These algorithms are typically defined by regulatory standards to improve interoperability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32MG29 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32MG29 features an advanced Radio Buffer Controller (BUFC) capable of handling up to four buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or for both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The RAC controls the top level state of the radio subsystem in the EFR32MG29. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing with optional LBT or CSMA-CA

3.2.8 RFSENSE Interface

The RFSENSE block allows the device to remain in EM2, EM3, or EM4 and wake when RF energy above a specified threshold is detected. When operated in selective mode, the RFSENSE block performs OOK preamble and sync word detection, preventing false wake-up events.

3.3 General Purpose Input/Output (GPIO)

EFR32MG29 has up to 26 GPIO pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System (PRS) to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by low-energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have wake functionality down to EM4. These pins are listed in the Alternate Function Table with the function GPIO.EM4WU.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The CMU controls oscillators and clocks in the EFR32MG29. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFR32MG29 supports two crystal oscillators and fully integrates four RC oscillators:

- A high-frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low-energy modes.
- An integrated high-frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 to 76.8 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low-frequency 32.768 kHz RC oscillator (LFRCO) for low-power operation without an external crystal. Precision mode enables periodic recalibration against the 38.4 MHz HFXO crystal to improve accuracy to ±500 ppm, suitable for BLE sleep interval timing.
- An integrated ultra-low-frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low-energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes:

- In capture mode, the counter state is stored in a buffer at a selected input event.
- In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value.
- In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers.

Complementary outputs with dead-time insertion are available on select TIMER output channels.

See 3.13 Configuration Summary for information on the feature set of each timer.

3.5.2 Low-Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.5.3 Real Time Clock with Capture (RTCC)

The RTCC is a 32-bit counter that provides timekeeping down to EM3. The RTCC can be clocked by any of the on-board, low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire, and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The EUSART supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low-energy modes. Not all instances of I^2C are available in all energy modes.

3.6.4 Peripheral Reflex System (PRS)

The PRS provides a communication network between different peripheral modules without software involvement. Peripheral modules producing reflex signals are called producers. The PRS routes reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.6.5 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors, and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

3.7 Security Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFR32MG29 family includes devices with Secure Vault High capabilities, which are summarized in the following table.

Table 3.1. Secure Vault Features

Feature	Secure Vault High
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes
Secure Debug with Lock/Unlock	Yes
DPA Countermeasures	Yes
Anti-Tamper	Yes
Secure Attestation	Yes
Secure Key Management	Yes
Symmetric Encryption	• AES 128 / 192 / 256 bit • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC • ChaCha20
Public Key Encryption - ECDSA / ECDH / EdDSA	• p192, p256, p384 and p521 • Curve25519 (ECDH) • Ed25519 (EdDSA)
Key Derivation	• ECJ-PAKE p192, p256, p384, and p521 • PBKDF2 • HKDF
Hashes	• SHA-1 • SHA-2 256, 384, and 512 • Poly1305

Additionally, the EFR32MG29 includes an External Tamper Detection (ETAMPDET) peripheral which provides additional physical security for the end product.

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192, P-256, P-384, and P-521 for Elliptic Curve Diffie-Hellman (ECDH) key derivation, and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for Edwards-curve Digital Signature Algorithm (EdDSA) sign and verify operations.

Secure Vault also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE) and Password-Based Key Derivation Function 2 (PBKDF2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.7.5 Differential Power Analysis (DPA) Countermeasures

The AES and ECC accelerators have DPA countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.7.6 Secure Key Management with Physically Unclonable Function (PUF)

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a PUF to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.7.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.7.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

3.7.9 External Tamper Detection (ETAMPDET)

The ETAMPDET module enables detection of external tampering, such as unauthorized enclosure opening. ETAMPDET operates in all energy modes down to EM4. Up to two signals can be generated and monitored to identify external tamper events. When a tamper event occurs, an interrupt is generated to allow software to take system-appropriate actions.

3.8 Analog

3.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.2 Analog Comparator (ACMP)

The ACMP is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9 Power

The EFR32MG29 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. Devices are available with an integrated DC-DC buck or DC-DC boost regulator. The DC-DC buck regulator is capable of bucking higher voltages down to 1.8 V, while the DC-DC boost option boosts lower battery voltages up to a higher voltage. The DC-DC boost converter has adjustable output, from 1.8 to 2.4 V in 100 mV steps. If used in an application, the DC-DC regulator requires one external inductor and one external capacitor.

The EFR32MG29 device family includes support for internal supply voltage scaling, as well as different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.9.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.9.2 Voltage Scaling

The EFR32MG29 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.9.3 Buck or Boost DC-DC Converter

Each device in the family includes either a buck DC-DC or boost DC-DC converter. The DC-DC converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2 and EM3 for device and radio operation.

RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. It employs soft switching at boot and DC-DC regulating-to-bypass transitions to limit the max supply slew rate and mitigate inrush current.

The buck DC-DC configuration provides up to 60 mA output current at 1.8 V from a 2.2 - 3.8 V supply in energy modes EM0,EM1, EM2, and EM3. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator, and extend the operating range down to 1.8 V. In bypass mode, the DC-DC operation is shut down and the input supply is switched directly to the output. The bypass mode of the buck DC-DC may be enabled to allow the system to go into EM4 and save energy. An integrated Coulomb Counter may be used to monitor the energy flowing through the buck DC-DC.

The boost DC-DC configuration has an input range of 1.2 to 1.7 V, an adjustable output range of 1.8 to 2.4 V, and up to 25 mA output current, enabling operation directly from single-cell low-voltage batteries. The boost DC-DC converter is operational in energy modes EM0, EM1, EM2, and EM3. It can be completely shut down using the dedicated BOOST_EN pin, saving system power during storage and shipping. BOOST_EN may also be used to re-enable the boost converter and power up the system.

3.9.4 Power Domains

Peripherals may exist on one of several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low-power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low-power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2 Peripheral Power Subdomains on page 17 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 3.2. Peripheral Power Subdomains

Always On in EM2/EM3		Selectively On in EM2/3	
PDHV[1]	**PD0A**	**PD0B**	**PD0C**
LFRCO (Non-precision mode)	RTCC	LETIMER0	LFRCO (Precision Mode)
LFXO	FSRCO	IADC0	
BURTC	WDOG0	ACMP0	
RFSENSE		I2C0	
ULFRCO		EUSART0	
ETAMPDET		PRS	
BURAM		DEBUG	
		GPIO	

Note:
1. Peripherals on PDHV are also available in EM4.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MG29. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1024 KB flash program memory
- Up to 256 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where program code is normally written, the MSC provides an information block where additional information, such as special user information or flash-lock bits, is stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32MG29 memory map is shown in the following figure. RAM and flash sizes are for the largest memory configuration.

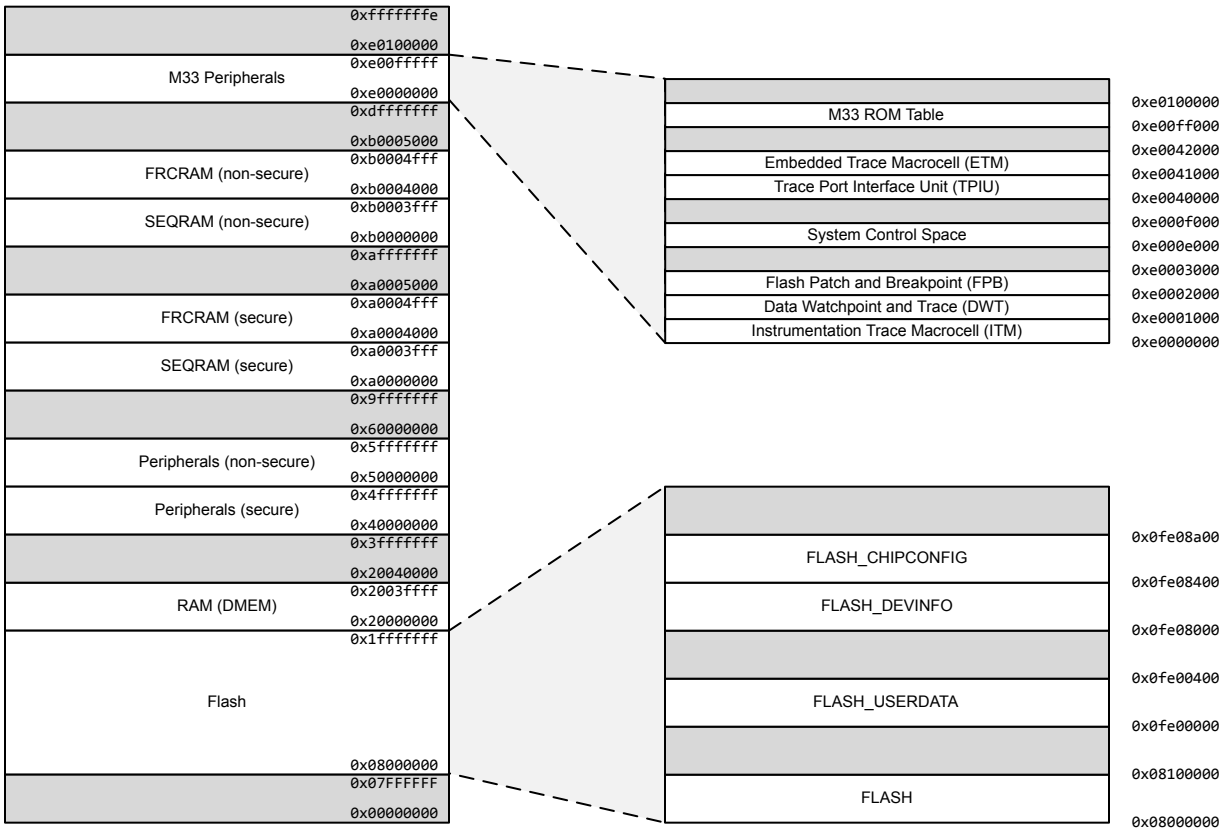


Figure 3.1. EFR32MG29 Memory Map — Core Peripherals and Code Space

3.13 Configuration Summary

The features of the EFR32MG29 are a subset of the feature set described in the device reference manual. The following table describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM3[1]	
I2C1	EM1	
IADC0	EM3	
LETIMER0	EM2[1]	
PDM	EM1	2-channel
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	32-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUSART0	EM1 - Full high-speed operation, all modes EM2[1] - Low-energy UART operation, 9600 Baud EM2 or EM3[1] - Low-energy SPI secondary receiver	
EUSART1	EM1 - Full high-speed operation, all modes	
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry, some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined in the following list. Exceeding these constraints can result in damage to the device and/or increased current draw.

Buck DC-DC or DC-DC not used

- VREGVDD and DVDD
  - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD (VREGVDD ≥ DVDD).
  - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD = DVDD).
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin.

Boost DC-DC

- VBAT: DCDC converter input. Connect to recommended supply and L_{DCDC}.
- DVDD: DVDD is the boost converter output and should be bypassed with the recommended C_{DCDC}, it should not be driven by an off-chip regulator.
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin

4.2 Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Voltage on DVDD, AVDD, IOVDD, RFVDD, PAVDD or VREGVDD supply pins	V_{DDMAX}		-0.3	—	3.8	V
Voltage on VBAT supply pin	$V_{VBATMAX}$		-0.3	—	3.8	V
Junction temperature	T_{JMAX}	-C grade	—	—	55	°C
		-I grade	—	—	125	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.2	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.8	V
Input RF level on RF pins RF2G4_IO	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF2G4_IO	V_{MAX2G4}		-0.3	—	V_{PAVDD} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-C temperature grade [1]	-20	—	+55	°C
		-I temperature grade [1]	-40	—	+125	°C
VREGVDD operating supply voltage (Buck DCDC or DCDC not used)	$V_{VREGVDD}$	Buck Mode DCDC in regulation, 60 mA load	2.2	3.0	3.8	V
		Buck Mode DCDC in bypass, 60 mA load	1.8	3.0	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
VBAT operating supply voltage (Boost DCDC)	V_{VBAT}	Boost Mode DCDC in regulation [2]	1.2	1.5	V_{OUT_BST} - 0.1	V
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4 [3]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDD0 operating supply voltage	V_{IOVDD0}	IOVDD0BODEN = 0 [4]	1.175	3.0	3.8	V
		IOVDD0BODEN = 1 [4]	1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
DECOUPLE output capacitor[5]	$C_{DECOUPLE}$	1.0 µF ± 10% X8L capacitor used for performance characterization.	1.0	—	2.75	µF
HCLK and core frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	80	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
HCLK radio frequency[6]	$f_{HCLKRADIO}$	VSCALE2 or VSCALE1	—	38.4	—	MHz
External clock input	f_{CLKIN}	VSCALE2 or VSCALE1	—	—	40	MHz
DPLL reference clock	$f_{DPLLREFCLK}$	VSCALE2 or VSCALE1	—	—	40	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The VBAT supply may be as high as the Boost DCDC output, but DCDC and RF performance specifications willl degrade.
3. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
4. The IOVDD BOD enable bit is in the EMU_BOD3SENSE register. The BOD is disabled on reset.
5. Murata GCM21BL81C105KA58L used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 µF.
6. The recommended radio crystal frequency is 38.4 MHz and all radio performance is specified at this frequency. See HFXO specifications for more detail on crystal tolerance.

4.4 Buck-Mode DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH, C_{DCDC} = 4.7 µF, $V_{VREGVDD}$ = 3.0 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. Buck-Mode DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin	$V_{VREGVDD}$	DCDC in regulation, I_{LOAD} = 60 mA, EM0/EM1 mode	2.2	3.0	3.8	V
		DCDC in regulation, I_{LOAD} = 5 mA, EM0/EM1 or EM2/EM3 mode	1.8	3.0	3.8	V
		Bypass mode	1.8	3.0	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	3.3	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	14.3	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 60 mA in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V	—	5.5	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and 60 mA in EM0/EM1 mode	—	0.27	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 60 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current[1]	I_{LOAD}	EM0/EM1 mode, DCDC in regulation	—	—	60	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode	—	—	60	mA
Nominal output capacitor	C_{DCDC}	4.7 µF ± 10% X7R capacitor used for performance characterization[2]	4.7	—	10	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	µF
Resistance in bypass mode	R_{BYP}	Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V	—	1.75	3	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V	—	0.86	1.5	Ω
Supply monitor threshold programming range	V_{CMP_RNG}	Programmable in 0.1 V steps	2.0	—	2.3	V
Supply monitor threshold accuracy	V_{CMP_ACC}	Supply falling edge trip point	-5	—	5	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply monitor threshold hysteresis	V_{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	t_{CMP_DELAY}	Supply falling edge at -100 mV / µs	—	0.6	—	µs

Note:

1. I_{LOAD} is the total current sourced by the DCDC, including on-chip and off-chip circuits powered from the DVDD supply rail.
2. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.

4.4.1 Buck DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 4.1 Lifetime Average Load Current limit vs. Maximum Input Voltage on page 27 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, a continuously powered application that sleeps 99% of the time, consumes 2 uA while asleep and 10 mA during the 1% it is active, with an average lifetime load current of about 102 uA.

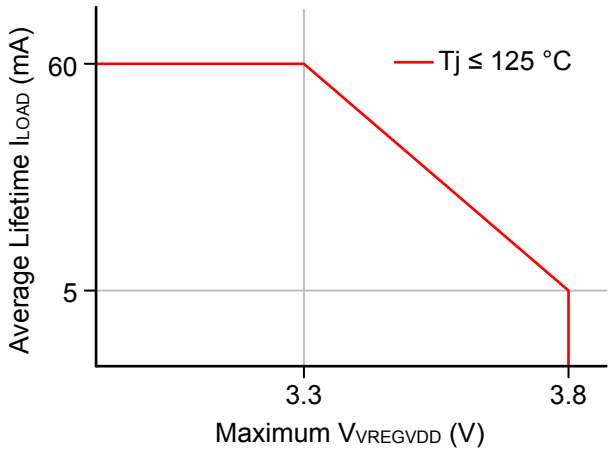


Figure 4.1. Lifetime Average Load Current limit vs. Maximum Input Voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4.2 Transient Maximum Load Current vs. Minimum Input Voltage on page 27 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

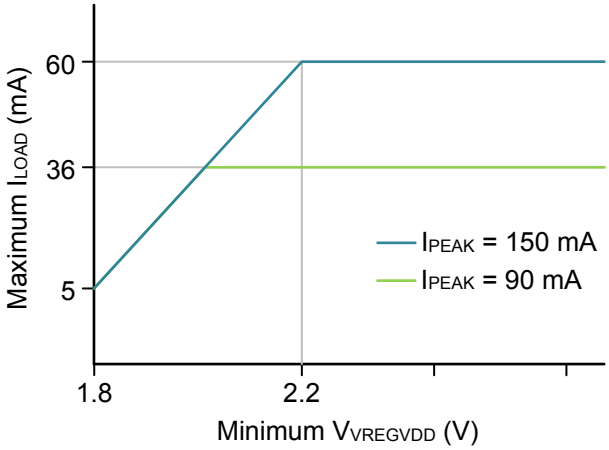


Figure 4.2. Transient Maximum Load Current vs. Minimum Input Voltage

4.5 Boost-Mode DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH, C_{DCDC} = 10 µF, V_{VBAT} = 1.5 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 180 mA, and in EM2/3 modes is set to 150 mA, unless otherwise indicated.

Table 4.4. Boost-Mode DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VBAT pin	V_{VBAT}	C_{LOAD} = 10 µF	1.2	—	1.7	V
Nominal regulated output voltage	V_{OUT_BST}	Adjustable in 100 mV increments	1.8	—	2.4	V
Regulation DC accuracy	ACC_{DC}	1.2 V ≤ V_{VBAT} ≤ 1.7 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2	—	2.5	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	15	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 25 mA in EM0/EM1 mode, 1.2 V ≤ V_{VBAT} ≤ 1.6 V	—	15	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and MAX(I_{LOAD}) in EM0/EM1 mode	—	-0.25	—	mV/mA
Efficiency	EFF	Load current between 100 µA and MAX(I_{LOAD}) mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current[1]	I_{LOAD}	EM0/EM1 mode, DCDC in regulation, V_{OUT} = 1.8 V, V_{VBAT} = 1.2 V	—	—	25	mA
		EM2/EM3 mode, DCDC in regulation, V_{OUT} = 1.8 V, V_{VBAT} = 1.2 V	—	—	5	mA
External load during startup[2]	I_{LOAD_START}	Off-chip load applied at DVDD supply rail	—	—	0.5	mA
Peak current during startup	I_{PEAK_START}	C_{LOAD} = 10 µF	—	—	10	mA
Nominal output capacitor	C_{DCDC}	10 µF ± 10% X8L capacitor used for performance characterization[3]	7.5	10	—	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		4.7	—	—	µF
Time to switch from EM2/3 mode to EM0/1 mode[4]	t_{MODE_SWITCH}		—	16	32	µs
Input high voltage on BOOST_EN	$V_{IH\_BOOST\_EN}$		0.8 * V_{BAT}	—	—	V
Input low voltage on BOOST_EN	$V_{IL\_BOOST\_EN}$		—	—	0.3 * V_{BAT}	V
Hysteresis of input voltage on BOOST_EN	$V_{HYST\_BOOST\_EN}$		0.03 * V_{BAT}	—	—	V
Time from BOOST_EN high to output regulation at 1.8 V	t_{START}	With 500 µA off-chip I_{LOAD_START} on DVDD	—	8	20	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Peak output voltage during startup (during t_{START})	V_{START}		—	2.35	2.8	V

Note:

1. I_{LOAD} is the total current sourced by the DCDC, including on-chip and off-chip circuits powered from the DVDD supply rail. Maximum output load current is a function of input and output voltage.
2. I_{LOAD_START} is the allowable current sourced by the DCDC during startup to off-chip circuits powered from the DVDD supply rail.
3. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 6.7 µF.
4. Mode switch is initiated when a wake event is recognized and occurs in parallel to the normal system wake time. During the mode switch, I_{LOAD} should be limited to 20 mA or less.

4.6 Coulomb Counter Calibration Load (Buck DC-DC Only)

Table 4.5. Coulomb Counter Calibration Load (Buck DC-DC Only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{CCLOAD}		-20	—	70	°C
Load current accuracy vs. production measurement[1]	I_{LOAD_ACC}	CCLVL = LOAD2 (1.0 mA nominal)	-9	—	9	%
		CCLVL = LOAD7 (8.0 mA nominal)	-10	—	10	%

Note:

1. Calibration load currents vary from part-to-part. The magnitude of the calibration load currents at 25 °C are measured in production on each device, and the measurement is written into DEVINFO space in the CCLOADxx locations. Accuracy is specified relative to the measured value across T_{CCLOAD}.

4.7 Thermal Characteristics

Table 4.6. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
40QFN (5x5mm)	JEDEC - High Thermal Cond. (2s2p)[1]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	27.1	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		7.2	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.27	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		15.5	°C/W

Note:

1. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.

4.8 Current Consumption

4.8.1 MCU Current Consumption Using Buck DC-DC at 3.0 V VREGVDD Input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU Current Consumption Using Buck DC-DC at 3.0 V VREGVDD Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	32	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	30	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	40	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	33	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	31	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	41	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	27	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	30	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	36	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	283	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	20	—	µA/MHz
		38.4 MHz crystal	—	21	—	µA/MHz
		38 MHz HFRCO	—	17	—	µA/MHz
		26 MHz HFRCO	—	20	—	µA/MHz
		16 MHz HFRCO	—	26	—	µA/MHz
		1 MHz HFRCO	—	273	—	µA/MHz
Current consumption in EM2 mode, VSCALE1	I_{EM2_VS1}	256 KB RAM retention and RTC running from LFRCO	—	4.6	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	1.9	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 KB RAM retention and RTC running from LFXO	—	3.4	—	µA
		256 KB RAM retention and RTC running from LFRCO	—	3.4	—	µA
		192 KB RAM retention and RTC running from LFXO	—	2.9	—	µA
		192 KB RAM retention and RTC running from LFRCO	—	2.9	—	µA
		192 KB RAM retention with RTC, BURTC, and WDOG running from LFRCO in precision mode	—	3.3	—	µA
		32 KB RAM retention and RTC running from LFXO	—	1.7	—	µA
		32 KB RAM retention and RTC running from LFRCO in precision mode	—	2.0	—	µA
		16 KB RAM retention and RTC running from LFXO	—	1.5	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	1.5	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.3	—	µA
		16 KB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.5	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.3	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	16 KB RAM retention and RTC running from ULFRCO	—	1.35	—	µA
Change in current consumption for retained RAM bank in EM2 or EM3	I_{EM23_RAM}	Per 16 KB RAM bank	—	0.124	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	1.8	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.2 MCU Current Consumption Using Boost DC-DC at 1.5 V VBAT Input

Unless otherwise indicated, typical conditions are: VBAT = 1.5 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.8. MCU Current Consumption Using Boost DC-DC at 1.5 V VBAT Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	50	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	47	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	62	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	52	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	49	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	64	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	41	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	45	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	55	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	429	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	33	—	µA/MHz
		38.4 MHz crystal	—	35	—	µA/MHz
		38 MHz HFRCO	—	27	—	µA/MHz
		26 MHz HFRCO	—	31	—	µA/MHz
		16 MHz HFRCO	—	41	—	µA/MHz
		1 MHz HFRCO	—	415	—	µA/MHz
Current consumption in EM2 mode, VSCALE1	I_{EM2_VS1}	256 KB RAM retention and RTC running from LFRCO	—	5.9	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.8	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 KB RAM retention and RTC running from LFXO	—	4.3	—	µA
		256 KB RAM retention and RTC running from LFRCO	—	4.4	—	µA
		192 KB RAM retention and RTC running from LFXO	—	3.7	—	µA
		192 KB RAM retention and RTC running from LFRCO	—	3.8	—	µA
		192 KB RAM retention with RTC, BURTC, and WDOG running from LFRCO in precision mode	—	4.6	—	µA
		32 KB RAM retention and RTC running from LFXO	—	2.3	—	µA
		32 KB RAM retention and RTC running from LFRCO in precision mode	—	3.0	—	µA
		16 KB RAM retention and RTC running from LFXO	—	2.2	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.2	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.9	—	µA
		16 KB RAM retention and RTC running from LFXO, CPU cache not retained	—	2.1	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.9	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	16 KB RAM retention and RTC running from ULFRCO	—	1.9	—	µA
Current with Boost DCDC shut down (BOOST_EN = 0)	I_{SHDN}	IOVDD, AVDD, RFVDD, and PAVDD connected to DVDD (un-powered)	—	18	30	nA
		IOVDD powered. AVDD, RFVDD, and PAVDD connected to DVDD (unpowered)	—	36	50	nA
Current consumption during reset	I_{RST}	Hard pin reset held	—	516	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	2.1	—	µA
Change in current consumption for retained RAM bank in EM2 or EM3	I_{EM23_RAM}	Per 16 KB RAM bank	—	0.143	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.3 MCU Current Consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = VREGVDD = 3.0 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.9. MCU Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	47	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	44	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	59	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	48	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	45	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	60	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	39	81	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	43	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	53	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	408	1960	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	29	—	µA/MHz
		38.4 MHz crystal	—	31	—	µA/MHz
		38 MHz HFRCO	—	25	67	µA/MHz
		26 MHz HFRCO	—	29	—	µA/MHz
		16 MHz HFRCO	—	38	—	µA/MHz
		1 MHz HFRCO	—	393	1950	µA/MHz
Current consumption in EM2 mode, VSCALE1	I_{EM2_VS1}	256 KB RAM retention and RTC running from LFRCO	—	6.6	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.7	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 KB RAM retention and RTC running from LFXO	—	4.8	—	µA
		256 KB RAM retention and RTC running from LFRCO	—	4.8	16	µA
		192 KB RAM retention and RTC running from LFXO	—	4.1	—	µA
		192 KB RAM retention and RTC running from LFRCO	—	4.1	—	µA
		192 KB RAM retention with RTC, BURTC, and WDOG running from LFRCO in precision mode	—	4.7	—	µA
		32 KB RAM retention and RTC running from LFXO	—	2.3	—	µA
		32 KB RAM retention and RTC running from LFRCO in precision mode	—	2.8	—	µA
		16 KB RAM retention and RTC running from LFXO	—	2.1	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.1	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.7	—	µA
		16 KB RAM retention and RTC running from LFXO, CPU cache not retained	—	2.0	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.7	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	16 KB RAM retention and RTC running from ULFRCO	—	1.8	6	µA
Change in current consumption for retained RAM bank in EM2 or EM3	I_{EM23_RAM}	Per 16 KB RAM bank	—	0.179	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.16	0.4	µA
		BURTC with LFXO	—	0.52	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	536	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	2.7	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.4 MCU Current Consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.10. MCU Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	46	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	44	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	59	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	47	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	45	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	60	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	39	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	43	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	52	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	405	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	29	—	µA/MHz
		38.4 MHz crystal	—	31	—	µA/MHz
		38 MHz HFRCO	—	24	—	µA/MHz
		26 MHz HFRCO	—	29	—	µA/MHz
		16 MHz HFRCO	—	38	—	µA/MHz
		1 MHz HFRCO	—	391	—	µA/MHz
Current consumption in EM2 mode, VSCALE1	I_{EM2_VS1}	256 KB RAM retention and RTC running from LFRCO	—	6.5	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.7	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 KB RAM retention and RTC running from LFXO	—	4.7	—	µA
		256 KB RAM retention and RTC running from LFRCO	—	4.7	—	µA
		192 KB RAM retention and RTC running from LFXO	—	4.0	—	µA
		192 KB RAM retention and RTC running from LFRCO	—	4.0	—	µA
		192 KB RAM retention with RTC, BURTC, and WDOG running from LFRCO in precision mode	—	4.7	—	µA
		32 KB RAM retention and RTC running from LFXO	—	2.2	—	µA
		32 KB RAM retention and RTC running from LFRCO in precision mode	—	2.8	—	µA
		16 KB RAM retention and RTC running from LFXO	—	2.1	—	µA
		16 KB RAM retention and RTC running from LFRCO	—	2.0	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.7	—	µA
		16 KB RAM retention and RTC running from LFXO, CPU cache not retained	—	2.0	—	µA
		16 KB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.7	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	16 KB RAM retention and RTC running from ULFRCO	—	1.8	—	µA
Change in current consumption for retained RAM bank in EM2 or EM3	I_{EM23_RAM}	Per 16 KB RAM bank	—	0.179	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.12	—	µA
		BURTC with LFXO	—	0.44	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	447.31	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	2.7	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.5 Radio Current Consumption at 3.0 V Using Buck-Mode DCDC

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.11. Radio Current Consumption at 3.0 V Using Buck-Mode DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.5	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	4.4	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	4.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.3	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	3.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.3	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.5	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.3	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	4.6	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	4.9	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	4	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	5.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	7.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	9	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	11	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	4.3	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	5.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	7.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	9.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	11.3	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	4.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	6	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	7.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	9.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	11.4	—	mA

4.8.6 Radio Current Consumption at 1.5 V Using Boost-Mode DCDC

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VBAT = 1.5 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.12. Radio Current Consumption at 1.5 V Using Boost-Mode DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.5	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.6	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.2	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.6	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	8	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	8.4	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.6	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.9	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.6	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	7.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	7.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.3	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	8	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	8.4	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	8.8	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	7.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	11.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	14.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	17.3	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	22.2	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	8.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	11.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	15.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	17.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	22.7	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	8.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	11.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	15.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	18	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	22.9	—	mA

4.8.7 Radio Current Consumption at 3.0 V

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.13. Radio Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	5.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.8	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.2	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	6.7	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.5	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	5.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.6	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.9	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.6	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	7.1	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	7.4	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	6.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	8.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	11.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	13.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	16.9	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	6.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	9	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	11.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	14.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	17.3	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	6.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	9.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	11.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	14.3	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	17.6	—	mA

4.8.8 Radio Current Consumption at 1.8 V

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.14. Radio Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.5	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	5.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.8	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.2	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	6.6	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.7	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	5.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	6.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	6.9	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.6	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE1, EM1	—	7	—	mA
		802.15.4 receiving frame, f = 2.4 GHz, VSCALE2, EM1	—	7.4	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	6.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	8.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	11.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	13.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	16.8	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	6.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	8.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	11.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	14.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	17.2	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	6.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	9.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	11.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	14.3	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	17.5	—	mA

4.9 Flash Characteristics

Table 4.15. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Flash erase cycles before failure[1]	EC_{FLASH}		10,000	—	—	cycles
Flash data retention[1]	RET_{FLASH}		10	—	—	years
Program time	t_{PROG}	one word (32-bits)	40	44	48	uSec
		average per word over 128 words	10	11	12	uSec
Page erase time	t_{PERASE}		11	13	15	ms
Mass erase time	t_{MERASE}	Erases all of User Code area	94	101	117	ms
Program current	I_{WRITE}	T_A = 25 °C	—	—	2.6	mA
Page erase current	I_{ERASE}	T_A = 25 °C	—	—	1.2	mA
Mass erase current	I_{MERASE}	T_A = 25 °C	—	—	1.2	mA

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.

4.10 Energy Mode Wake-up and Entry Times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.16. Energy Mode Wake-up and Entry Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake-up time from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.39	—	µs
Wake-up time from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.3	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.3	—	µs
		Voltage scaling up one level[1]	—	37.9	—	µs
		Voltage scaling up two levels[2]	—	50.3	—	µs
Wake-up time from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.3	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.3	—	µs
		Voltage scaling up one level[1]	—	37.9	—	µs
		Voltage scaling up two levels[2]	—	50.3	—	µs
Wake-up time from EM4	t_{EM4_WU}	Code execution from flash	—	34	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.27	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.8	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.9	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	10.5	—	µs
Voltage scaling time in EM0[3]	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	µs
		Down from VSCALE2 to VSCALE1	—	172	—	µs

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.11 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash (which is proportional to the size of the image) and the verification of the image signature (which is independent of image size).

The duration for the root code to authenticate the bootloader depends on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application depends on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The following table provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version 2.2.6
- Gecko Bootloader size 13 KB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.17. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time[1]	t_{BOOT}	Secure boot application check disabled, no bootloader	—	25.2	—	ms
		Secure boot application check disabled, second stage bootloader check enabled[2], 50 KB application size	—	32.9	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 50 KB application size	—	45.0	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 150 KB application size	—	48.1	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 350 KB application size	—	54.6	—	ms

Note:

1. Excludes boost DCDC startup time.
2. Timing is measured with the specified bootloader size. Actual bootloader size will impact the boot timing slightly, with a similar µs / KB ratio as application size.

4.12 Crypto Operation Timing for SE Manager API

Values in the following table represent the timing from the SE Manager API call to return. The Cortex-M33 HCLK frequency is 38.4 MHz. The timing specifications are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version 2.2.6

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.18. Crypto Operation Timing for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 KB	—	643	—	µs
		AES-128 CCM encryption, PT 32 KB	—	1832	—	µs
		AES-128 CTR encryption, PT 1 KB	—	524	—	µs
		AES-128 CTR encryption, PT 32 KB	—	1095	—	µs
		AES-128 GCM encryption, PT 1 KB	—	583	—	µs
		AES-128 GCM encryption, PT 32 KB	—	1158	—	µs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 KB	—	656	—	µs
		AES-256 CCM encryption, PT 32 KB	—	2240	—	µs
		AES-256 CTR encryption, PT 1 KB	—	531	—	µs
		AES-256 CTR encryption, PT 32 KB	—	1314	—	µs
		AES-256 GCM encryption, PT 1 KB	—	591	—	µs
		AES-256 GCM encryption, PT 32 KB	—	1360	—	µs
ECC P-256 timing	t_{ECC_P256}	ECC key generation, P-256	—	5.6	—	ms
		ECC signing, P-256	—	5.9	—	ms
		ECC verification, P-256	—	6.2	—	ms
ECC P-521 timing[1]	t_{ECC_P521}	ECC key generation, P-521	—	30.5	—	ms
		ECC signing, P-521	—	30.8	—	ms
		ECC verification, P-521	—	36.6	—	ms
ECC P-25519 timing	t_{ECC_P25519}	ECC key generation, P-25519	—	4.6	—	ms
		ECC signing, P-25519	—	8.9	—	ms
		ECC verification, P-25519	—	6.3	—	ms
ECDH compute secret timing	t_{ECDH}	ECDH compute secret, P-521[1]	—	30.7	—	ms
		ECDH compute secret, P-25519[2]	—	4.6	—	ms
		ECDH compute secret, P-256	—	5.7	—	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE client timing	$t_{ECJPAKE\_C}$	ECJPAKE client write round one	—	21.8	—	ms
		ECJPAKE client read round one	—	11.8	—	ms
		ECJPAKE client write round two	—	15.6	—	ms
		ECJPAKE client read round two	—	6.5	—	ms
		ECJPAKE client derive secret	—	9.0	—	ms
ECJPAKE server timing	$t_{ECJPAKE\_S}$	ECJPAKE server write round one	—	21.8	—	ms
		ECJPAKE server read round one	—	11.8	—	ms
		ECJPAKE server write round two	—	15.5	—	ms
		ECJPAKE server read round two	—	6.5	—	ms
		ECJPAKE server derive secret	—	9.0	—	ms
POLY-1305 timing[1]	$t_{POLY1305}$	POLY-1305, PT 1 KB	—	564	—	µs
		POLY-1305, PT 32 KB	—	1233	—	µs
SHA-256 timing	t_{SHA256}	SHA-256, PT 1 KB	—	340	—	µs
		SHA-256, PT 32 KB	—	769	—	µs
SHA-512 timing[1]	t_{SHA512}	SHA-512, PT 1 KB	—	338	—	µs
		SHA-512, PT 32 KB	—	654	—	µs

Note:

1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

4.13 Crypto Operation Average Current for SE Manager API

Values in the following table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents might be higher.

Conditions:

- SE firmware version 2.2.6

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.19. Crypto Operation Average Current for SE Manager API (Direct supply)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 current	I_{AES128}	AES-128 CCM encryption, PT 1 KB	—	1.95	—	mA
		AES-128 CCM encryption, PT 32 KB	—	4.18	—	mA
		AES-128 CTR encryption, PT 1 KB	—	1.85	—	mA
		AES-128 CTR encryption, PT 32 KB	—	4.22	—	mA
		AES-128 GCM encryption, PT 1 KB	—	1.86	—	mA
		AES-128 GCM encryption, PT 32 KB	—	4.19	—	mA
AES-256 current	I_{AES256}	AES-256 CCM encryption, PT 1 KB	—	2.02	—	mA
		AES-256 CCM encryption, PT 32 KB	—	4.28	—	mA
		AES-256 CTR encryption, PT 1 KB	—	1.9	—	mA
		AES-256 CTR encryption, PT 32 KB	—	4.3	—	mA
		AES-256 GCM encryption, PT 1 KB	—	1.9	—	mA
		AES-256 GCM encryption, PT 32 KB	—	4.28	—	mA
ECC P-256 current	$I_{ECCP256}$	ECC key generation, P-256	—	2.46	—	mA
		ECC signing, P-256	—	2.45	—	mA
		ECC verification, P-256	—	2.48	—	mA
ECC P-521 current[1]	$I_{ECCP521}$	ECC key generation, P-521	—	2.61	—	mA
		ECC signing, P-521	—	2.6	—	mA
		ECC verification, P-521	—	2.6	—	mA
ECC P-25519 current	$I_{ECCP25519}$	ECC key generation, P-25519	—	2.42	—	mA
		ECC signing, P-25519	—	2.45	—	mA
		ECC verification, P-25519	—	2.41	—	mA
ECDH compute secret current	I_{ECDH}	ECDH compute secret, P-521[1]	—	2.59	—	mA
		ECDH compute secret, P-25519[2]	—	2.33	—	mA
		ECDH compute secret, P-256	—	2.43	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE client current	$I_{ECJPAKE\_C}$	ECJPAKE client write round one	—	2.49	—	mA
		ECJPAKE client read round one	—	2.5	—	mA
		ECJPAKE client write round two	—	2.5	—	mA
		ECJPAKE client read round two	—	2.44	—	mA
		ECJPAKE client derive secret	—	2.5	—	mA
ECJPAKE server current	$I_{ECJPAKE\_S}$	ECJPAKE server write round one	—	2.51	—	mA
		ECJPAKE server read round one	—	2.5	—	mA
		ECJPAKE server write round two	—	2.5	—	mA
		ECJPAKE server read round two	—	2.44	—	mA
		ECJPAKE server derive secret	—	2.5	—	mA
POLY-1305 current[1]	$I_{POLY1305}$	POLY-1305, PT 1 KB	—	1.75	—	mA
		POLY-1305, PT 32 KB	—	2.5	—	mA
SHA-256 current	I_{SHA256}	SHA-256, PT 1 KB	—	1.79	—	mA
		SHA-256, PT 32 KB	—	3.07	—	mA
SHA-512 current[1]	I_{SHA512}	SHA-512, PT 1 KB	—	1.77	—	mA
		SHA-512, PT 32 KB	—	2.76	—	mA

Note:

1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

4.14 RFSENSE Low-energy Wake-on-RF

Table 4.20. RFSENSE Low-energy Wake-on-RF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Average current	$I_{RFSENSE}$	RF energy below wake threshold	—	138	—	nA
		Selective mode, RF energy above threshold but no OOK sync detected	—	131	—	nA
RF level above which RFSENSE will detect signal[1]	$THRES_{TRIG}$	Threshold set to -34 dBm	-28	—	—	dBm
		Threshold set to -22 dBm	-19	—	—	dBm
RF level below which RFSENSE will not detect signal[1]	$THRES_{NOTRIG}$	Threshold set to -34 dBm	—	—	-40	dBm
		Threshold set to -22 dBm	—	—	-26	dBm
Sensitivity in selective OOK mode[1]	$SENS_{OOK}$	Sensitivity for > 90% probability of OOK detection[2], threshold set to -34 dBm	-28	—	—	dBm
		Sensitivity for > 90% probability of OOK detection[2], threshold set to -22 dBm	-19	—	—	dBm

Note:

1. Values collected with conducted measurements performed at the end of the matching network.
2. Selective wake signal is 1 kHz OOK Manchester-coded, 8 bits of preamble, 32-bit sync word.

4.15 2.4 GHz RF Transceiver Characteristics for QFN40 Package

4.15.1 RF Transmitter Characteristics for QFN40 Package

4.15.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.21. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power[1]	$POUT_{MAX}$	High-power PA	—	8.2	—	dBm
		0 dBm PA	—	-0.4	—	dBm
Minimum active TX power	$POUT_{MIN}$	High-power PA	—	-31.2	—	dBm
		0 dBm PA	—	-29.3	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	8 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
		0 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
Output power variation vs temperature, frequency = 2450 MHz	$POUT_{VAR\_T}$	High-power PA at 8 dBm, (-40 to +125 °C)	—	1.0	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	1.4	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	High-power PA, 8 dBm	—	0.2	—	dB
		0 dBm PA, 0 dBm	—	0.3	—	dB
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-60	-54	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-42	-36	dBm
		1G-14G, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.15.1.2 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.22. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	665.7	—	kHz
		P_{out} = 0 dBm	—	665.1	—	kHz
Power spectral density limit, peak per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method PKPSD-1	PSD_{LIMIT_PEAK}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-8.3	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-16.8	—	dBm/ 3kHz
Power spectral density limit, average per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method AVGPSD-1	PSD_{LIMIT_AVG}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-11.9	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-20.5	—	dBm/ 3kHz
Power spectral density limit, per ETSI 300.328 option 2	PSD_{LIMIT_OPT2}	P_{out} = 8 dBm, Per ETSI 300.328 at 10 dBm/1 MHz	—	7.8	—	dBm/ 1MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-43.3	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-52.3	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-48.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-57.0	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-36	—	dBm

Note:

1. As per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.15.1.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.23. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	1372.1	—	kHz
		P_{out} = 0 dBm	—	1372.6	—	kHz
Power spectral density limit, peak per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method PKPSD-1	PSD_{LIMIT_PEAK}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-14.4	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-22.9	—	dBm/ 3kHz
Power spectral density limit, average per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method AVGPSD-1	PSD_{LIMIT_AVG}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-16.5	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-25.0	—	dBm/ 3kHz
Power spectral density limit, per ETSI 300.328 option 2	PSD_{LIMIT_OPT2}	P_{out} = 8 dBm, Per ETSI 300.328 at 10 dBm/1 MHz	—	6.8	—	dBm/ 1MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	2.0	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	2.0	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 4 MHz	—	-42.6	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 4 MHz	—	-51.7	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 6 MHz	—	-48.9	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 6 MHz	—	-57.6	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-36	—	dBm

Note:

1. As per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.15.1.4 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.24. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	693.3	—	kHz
		P_{out} = 0 dBm	—	688.1	—	kHz
Power spectral density limit, peak per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method PKPSD-1	PSD_{LIMIT_PEAK}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-9.1	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-17.6	—	dBm/ 3kHz
Power spectral density limit, average per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method AVGPSD-1	PSD_{LIMIT_AVG}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-13.6	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-22.1	—	dBm/ 3kHz
Power spectral density limit, per ETSI 300.328 option 2	PSD_{LIMIT_OPT2}	P_{out} = 8 dBm, Per ETSI 300.328 at 10 dBm/1 MHz	—	7.8	—	dBm/ 1MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-43.3	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-52.3	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-48.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-57.0	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-36	—	dBm

Note:

1. As per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.15.1.5 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.25. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	680.5	—	kHz
		P_{out} = 0 dBm	—	680.1	—	kHz
Power spectral density limit, peak per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method PKPSD-1	PSD_{LIMIT_PEAK}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	1.8	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-6.7	—	dBm/ 3kHz
Power spectral density limit, average per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method AVGPSD-1	PSD_{LIMIT_AVG}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	1.0	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-7.5	—	dBm/ 3kHz
Power spectral density limit, per ETSI 300.328 option 2	PSD_{LIMIT_OPT2}	P_{out} = 8 dBm, Per ETSI 300.328 at 10 dBm/1 MHz	—	7.7	—	dBm/ 1MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.0	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-43.3	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-52.3	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-48.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-57.0	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-36	—	dBm

Note:

1. As per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.15.1.6 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.26. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude per 802.15.4-2011	EVM	Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 8 dBm	—	2.9	—	% rms
		Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 0 dBm	—	2.9	—	% rms
Power spectral density limit, peak per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method PKPSD-1	PSD_{LIMIT_PEAK}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-7.5	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-16.1	—	dBm/ 3kHz
Power spectral density limit, average per FCC 15.247 / ANSI C63.10-2020 11.10.2 Method AVGPSD-1	PSD_{LIMIT_AVG}	P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-24.1	—	dBm/ 3kHz
Power spectral density limit, per ETSI 300.328 option 2	PSD_{LIMIT_OPT2}	P_{out} = 8 dBm, Per ETSI 300.328 at 10 dBm/1 MHz	—	6.0	—	dBm/ 1MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band, P_{out} = 8 dBm	—	2.2	—	MHz
		99% BW at highest and lowest channels in band, P_{out} = 0 dBm	—	2.2	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$. Test frequency = 2440 MHz.	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test frequency = 2440 MHz	—	-36	—	dBm

4.15.2 RF Receiver Characteristics for QFN40 Package

4.15.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.27. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-92.7	—	dBm
		1 GHz to 12 GHz	—	-68.5	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-47	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal[1], 1% PER	—	-93.3	—	dBm
		250 kbps 2GFSK signal[2], 0.1% BER	—	-104.8	—	dBm

Note:

1. Reference signal is 2 Mbps 2GFSK, BT = 0.5, mi = 1.0, Δf = ± 1 MHz, Channel bandwidth = 2.4 MHz.
2. Reference signal is 250 kbps 2GFSK, BT = 0.5, mi = 1.0, Δf = ± 125 kHz, Channel bandwidth = 350 kHz.

4.15.2.2 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz, Packet length is 37 bytes.

Table 4.28. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-99	—	dBm
		Signal is reference signal, 255 byte payload[2]	—	-97.4	—	dBm
		With non-ideal signals[3] [1]	—	-98.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	6.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-7.9	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-8.1	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-43.8	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-46.3	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-49.4	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-51	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-24.9	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-43.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-7.9	—	dB
Intermodulation performance	IM	n = 3[7]	—	-15.5	—	dBm

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4.

4.15.2.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz, Packet length is 37 bytes.

Table 4.29. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-96.1	—	dBm
		Signal is reference signal, 255 byte payload[2]	—	-94.6	—	dBm
		With non-ideal signals[3] [1]	—	-95.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	6.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-7.7	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-8.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1] [5] [4] [6]	—	-44.1	—	dB
		Interferer is reference signal at -4 MHz offset[1] [5] [4] [6]	—	-49.1	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1] [5] [4] [6]	—	-51	—	dB
		Interferer is reference signal at -6 MHz offset[1] [5] [4] [6]	—	-53.4	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-24.1	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1] [6]	—	-44.1	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1] [6]	—	-7.7	—	dB
Intermodulation performance	IM	n = 3[7]	—	-14.5	—	dBm

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency 2404 MHz ≤ Fc ≤ 2478 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4.

4.15.2.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz, Packet length is 37 bytes.

Table 4.30. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-102.6	—	dBm
		Signal is reference signal, 255 byte payload[2]	—	-101.2	—	dBm
		With non-ideal signals[3 1]	—	-101.9	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	2.1	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-9.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-9.3	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-47.8	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-51.4	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-48.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-54.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-48.8	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-48.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-47.8	—	dB

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.15.2.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz, Packet length is 37 bytes.

Table 4.31. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-106.8	—	dBm
		Signal is reference signal, 255 byte payload[2]	—	-106.4	—	dBm
		With non-ideal signals[3] [1]	—	-106.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-13.2	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-13.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-52.7	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-55.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-52.8	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-60.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-52.1	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-52.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-52.7	—	dB

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.15.2.6 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency = 38.4 MHz. RF center frequency 2.44 GHz.

Table 4.32. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Signal is reference signal[1]. Packet length is 20 octets	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets	—	-102.2	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	1.9	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{P1}	Interferer is reference signal at +1 channel-spacing	—	34.9	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{M1}	Interferer is reference signal at -1 channel-spacing	—	35.5	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ± 2 channel-spacing	—	47.9	—	dB
Image rejection , 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	IR	Interferer is CW in image band[3]	—	38.9	—	dB
Blocking rejection of all other channels, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]. Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	53.8	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	53.9	—	dB
RSSI resolution	$RSSI_{RES}$	-100 dBm to +5 dBm	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2020	$RSSI_{LIN}$		—	+/-6	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, frequency range = 2400-2483.5 MHz, symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the desired signal carrier, regardless of the channel raster.

4.16 Oscillators

4.16.1 High-Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.33. High-Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	F_{HFXO}	see note[1] [2]	—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, C_L = 10 pF[3] [4]	—	40	60	Ω
Supported range of crystal load capacitance[5]	C_{L_HFXO}	38.4 MHz, ESR = 40 Ohm[4]	—	10	—	pF
Supply current	I_{HFXO}		—	415	—	µA
Startup time[6]	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ω, C_L = 10 pF	—	160	—	µs
On-chip tuning cap step size[7]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The BLE radio requires a 38.4 MHz crystal with a tolerance of ± 50 ppm over temperature and aging. Use a crystal with the recommended frequency and tolerance.
2. The ZigBee radio requires a 38.4 MHz crystal with a tolerance of ± 40 ppm over temperature and aging. Use a crystal with the recommended frequency and tolerance.
3. The crystal should have a maximum ESR less than or equal to this maximum rating.
4. RF performance characteristics have been determined using crystals with an ESR of 40 Ω and C_L of 10 pF.
5. Total load capacitance as seen by the crystal.
6. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
7. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.16.2 Low-Frequency Crystal Oscillator

Table 4.34. Low-Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	F_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, C_L = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	254	—	nA
Startup time	$T_{STARTUP}$	ESR = 70 kΩ, C_L = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	43	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal.
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register.
4. In LFXO_CFG Register.
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.16.3 High-Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.35. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies[1]	I_{HFRCO}	F_{HFRCO} = 4 MHz	—	28	—	µA
		F_{HFRCO} = 5 MHz	—	30	—	µA
		F_{HFRCO} = 7 MHz	—	60	—	µA
		F_{HFRCO} = 10 MHz	—	66	—	µA
		F_{HFRCO} = 13 MHz	—	79	—	µA
		F_{HFRCO} = 16 MHz	—	88	—	µA
		F_{HFRCO} = 19 MHz	—	92	—	µA
		F_{HFRCO} = 20 MHz	—	105	—	µA
		F_{HFRCO} = 26 MHz	—	118	—	µA
		F_{HFRCO} = 32 MHz	—	141	—	µA
		F_{HFRCO} = 38 MHz	—	172	—	µA
		F_{HFRCO} = 80 MHz	—	289	—	µA
Clock out current for HFRCODPLL[2]	$I_{CLKOUT\_HFRCODPLL}$	FORCEEN bit of HFRCO0_CTRL = 1	—	3.0	—	µA/MHz
Startup time[3]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	1.2	—	µs
		FREQRANGE = 8 to 15	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band frequency limits[4]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
3. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
4. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.16.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.36. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.16.5 Precision Low-Frequency RC Oscillator (LFRCO)

Table 4.37. Precision Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	211	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	183	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	664	—	nA

Note:
1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.16.6 Ultra Low-Frequency RC Oscillator

Table 4.38. Ultra Low-Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.17 GPIO with 3 V Nominal IOVDD

Table 4.39. GPIO with 3 V Nominal IOVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IOVDD supply range	V_{IO}		1.71	3.0	3.8	V
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	250	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * IOVDD	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8 mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8 mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT = 1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	34	44	60	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.18 GPIO with 1.5 V Nominal IOVDD

Table 4.40. GPIO with 1.5 V Nominal IOVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IOVDD supply range	V_{IO}	IOVDD BOD Disabled	1.175	1.5	1.85	V
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.175 V	—	1.4	—	nA
		MODEx = DISABLED, IOVDD = 1.5 V	—	1.5	—	nA
		MODEx = DISABLED, IOVDD = 1.71 V T_A = 55 °C	—	—	90	nA
		MODEx = DISABLED, IOVDD = 1.71 V T_A = 125 °C	—	—	200	nA
Input low voltage	V_{IL}		—	—	0.35 * IOVDD	V
Input high voltage	V_{IH}		0.65 * IOVDD	—	—	V
Hysteresis of input voltage	V_{HYS}		0.05 * IOVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 8 mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
		Sourcing 4 mA, IOVDD ≥ 1.175 V	0.6 * IOVDD	—	—	V
		Sourcing 0.5 mA, IOVDD ≥ 1.175 V	0.95 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 8 mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
		Sinking 4 mA, IOVDD ≥ 1.175 V	—	—	0.4 * IOVDD	V
		Sinking 0.5 mA, IOVDD ≥ 1.175 V	—	—	0.05 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 1.5 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	11.9	—	ns
		IOVDD = 1.175 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	17.0	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 1.5 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	12.5	—	ns
		IOVDD = 1.175 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	17.8	—	ns
Pull up/down resistance	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT = 1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

4.19 Analog to Digital Converter (IADC)

Unless otherwise indicated, specified at 1 Msps, ADCCLK = 10 MHz, OSR = 2.

Table 4.41. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V_{AVDD}	Normal Mode	1.71	—	3.8	V
Maximum input range[1]	V_{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-scale voltage	V_{FS}	Voltage required for full-scale measurement	—	V_{REF} / Gain	—	V
Input measurement range	V_{IN}	Differential mode - plus and minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single ended mode - one input tied to ground	0	—	V_{FS}	V
Input sampling capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 3x	—	5.4	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f_{ADC_CLK}	Gain = 1x or 0.5x	—	—	10	MHz
		Gain = 2x	—	—	5	MHz
		Gain = 3x or 4x	—	—	2.5	MHz
Input sampling frequency	f_S		—	$f_{ADC\_CLK}/4$	—	MHz
Throughput rate	f_{SAMPLE}	f_{ADC_CLK} = 10 MHz, OSR = 2	—	—	1	Msps
		f_{ADC_CLK} = 10 MHz, OSR = 32	—	—	76.9	ksps
Current from all supplies, Continuous operation	I_{ADC_CONT}	1 Msps, OSR = 2, f_{ADC_CLK} = 10 MHz	—	290	385	µA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I_{STBY}		—	16	—	µA
ADC startup time	$t_{startup}$	From power down state	—	5	—	µs
		From standby state	—	1	—	µs
ADC resolution[2]	Resolution		—	12	—	bits
Differential Nonlinearity	DNL	Differential Input, OSR = 2, (No missing codes) .	-0.998	+/- 0.25	1.5	LSB12
Integral Nonlinearity	INL	Differential Input, OSR = 2.	-2.5	+/- 0.65	2.5	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Effective number of bits[3]	ENOB	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V. OSR = 2	10.5	11.7	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	—	13.5	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	—	14.3	—	bits
Signal to noise + distortion ratio[3]	SNDR	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	65	72.3	—	dB
		Differential Input. Gain = 2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	72.3	—	dB
		Differential Input. Gain = 4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	68.8	—	dB
		Differential Input. Gain = 0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	72.5	—	dB
Total harmonic distortion	THD	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	-80.8	-70	dB
Spurious-free dynamic range	SFDR	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	72	86.5	—	dB
Common mode rejection ratio	CMRR	DC to 100 Hz	—	87.0	—	dB
		AC high frequency	—	68.6	—	dB
Power supply rejection ratio	PSRR	DC to 100 Hz	—	80.4	—	dB
		AC high frequency, using VREF pad.	—	33.4	—	dB
		AC high frequency, using internal VBGR.	—	65.2	—	dB
Gain error	GE	GAIN = 1 and 0.5, using external VREF	-0.3	0.0165	0.3	%
		GAIN = 2, using external VREF	-0.4	0.0426	0.4	%
		GAIN = 3, using external VREF	-0.7	0.0864	0.7	%
		GAIN = 4, using external VREF	-1.1	0.107	1.1	%
		Internal VREF[4], all GAIN settings	-1.5	0.064	1.5	%
Offset error	OFFSET	GAIN = 1 and 0.5, Differential Input	-3	-0.45	3	LSB12
		GAIN = 2, Differential Input	-4	-0.44	4	LSB12
		GAIN = 3, Differential Input	-4	-0.47	4	LSB12
		GAIN = 4, Differential Input	-4	-0.47	4	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External reference voltage range[1]	V_{EVREF}		1.0	—	AVDD	V
Internal reference voltage	V_{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR = 2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32, and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

4.20 Analog Comparator (ACMP)

Table 4.42. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP supply current	I_{ACMP}	BIAS = 0 [1], HYST = DISABLED (100 °C max)	—	63	—	nA
		BIAS = 1 [1], HYST = DISABLED	—	252	—	nA
		BIAS = 2 [1], HYST = DISABLED	—	628	—	nA
		BIAS = 3 [1], HYST = DISABLED	—	2.3	—	µA
		BIAS = 4, HYST = DISABLED	—	5.2	—	µA
		BIAS = 5, HYST = DISABLED	—	10	—	µA
		BIAS = 6, HYST = DISABLED	—	25	—	µA
		BIAS = 7, HYST = DISABLED	—	47	80	µA
ACMP supply current with hysteresis	I_{ACMP_WHYS}	BIAS = 0 [1], HYST = SYM30MV (100 °C max)	—	81	—	nA
		BIAS = 1 [1], HYST = SYM30MV	—	346	—	nA
		BIAS = 2 [1], HYST = SYM30MV	—	871	—	nA
		BIAS = 3 [1], HYST = SYM30MV	—	3.23	—	µA
		BIAS = 4, HYST = SYM30MV	—	7.1	—	µA
		BIAS = 5, HYST = SYM30MV	—	15	—	µA
		BIAS = 6, HYST = SYM30MV	—	36	—	µA
		BIAS = 7, HYST = SYM30MV	—	67	—	µA
Current consumption from VREFDIV in continuous mode	$I_{VREFDIV}$	NEGSEL = VREFDIVAVDD	—	3.2	—	µA
		NEGSEL = VREFDIV1V25	—	4.2	—	µA
		NEGSEL = VREFDIV2V5	—	7.0	—	µA
Current consumption from VREFDIV in sample/hold mode	$I_{VREFDIV\_SH}$	NEGSEL = VREFDIV2V5LP	—	72	—	nA
		NEGSEL = VREFDIV1V25LP	—	66	—	nA
		NEGSEL = VREFDIVAVDDLP	—	68	—	nA
Current consumption from VSENSEDIV in continuous mode	$I_{VSENSEDIV}$	NEGSEL = VSENSE01DIV4	—	1.7	—	µA
Current consumption from VSENSEDIV in sample/hold mode	$I_{VSENSEDIV\_SH}$	NEGSEL = VSENSE01DIV4LP	—	55	—	nA
Hysteresis (BIAS = 0)	V_{HYST_0}	HYST = SYM10MV[2]	—	20	—	mV
		HYST = SYM20MV[2]	—	38	—	mV
		HYST = SYM30MV[2]	—	54	—	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V Reference	1.18	1.25	1.3	V
		Internal 2.5 V Reference	2.36	2.5	2.61	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	BIAS = 0, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 2, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 4, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 7, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
Input range	V_{IN}	Input Voltage Range	0	—	AVDD	V
Comparator delay with 100 mV overdrive	T_{DELAY}	BIAS = 0, (100 °C max)	—	11	—	µs
		BIAS = 1	—	2.9	—	µs
		BIAS = 2	—	1.4	—	µs
		BIAS = 3	—	0.56	—	µs
		BIAS = 4	—	211	—	ns
		BIAS = 5	—	120	—	ns
		BIAS = 6	—	70	—	ns
		BIAS = 7	—	51	—	ns

Note:

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 µA of supply current is required.
2. V_{CM} = 1.25 V

4.21 External Trace Tamper Detection Supply Current

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V. T_A = 25 °C.

Table 4.43. External Trace Tamper Detection Supply Current

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current consumption	$I_{ETAMPDET}$	One channel, operating from 1 kHz ULFRCO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	81	—	nA
		One channel, operating from 32.768 kHz LFXO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	154	—	nA
		One channel, operating from 32.768 kHz LFRCO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	154	—	nA

4.22 Temperature Sensor

Table 4.44. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range[1]	T_{RANGE}		-40	—	125	°C
Temperature sensor resolution	$T_{RESOLUTION}$		—	0.25	—	°C
Measurement noise (RMS)	T_{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVGNUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVGNUM = 1)	—	0.12	—	°C
Temperature offset	T_{OFF}	Mean error of uncorrected output across full temperature range	—	2.4	—	°C
Temperature sensor accuracy[2] [3]	T_{ACC}	Direct output accuracy after mean error (T_{OFF}) removed	—	+/-3	—	°C
		After linearization in software, no calibration	—	+/-2	—	°C
		After linearization in software, with single-temperature calibration at 25 °C[4]	—	+/-1.5	—	°C
Measurement interval	t_{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.23 Brown Out Detectors

4.23.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.45. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply rising	—	1.67	1.71	V
		Supply falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100 mV / µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example if the supply ramps down and then back up at a very fast rate).

4.23.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 and lower, unless otherwise noted.

Table 4.46. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2 mV / µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example if the supply ramps down and then back up at a very fast rate).

4.23.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.47. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV / µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example if the supply ramps down and then back up at a very fast rate).

4.24 PDM Timing Specifications

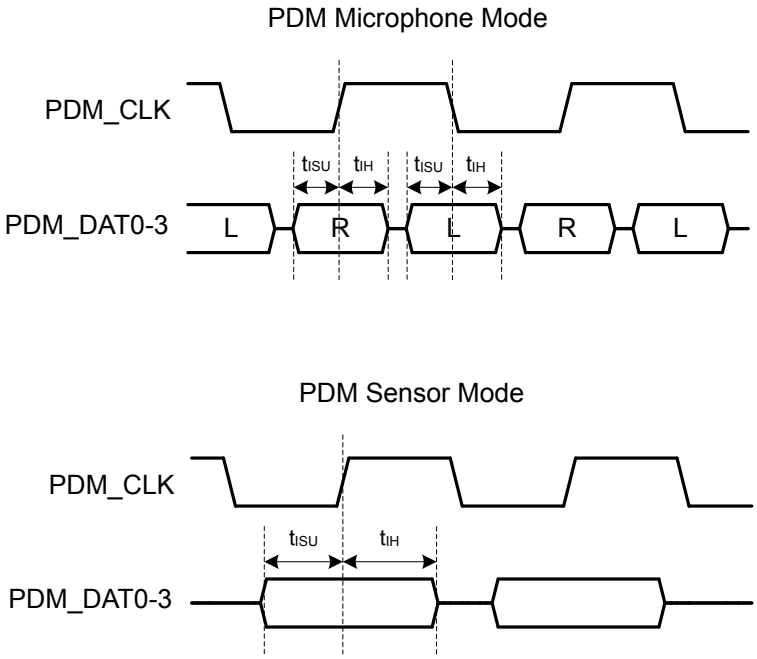


Figure 4.3. PDM Timing Diagrams

4.24.1 Pulse Density Modulator (PDM), Common DBUS

Timing specifications are for all PDM signals routed to the same DBUS (DBUSAB or DBUSCD), though routing to the same GPIO port is the optimal configuration. C_{LOAD} < 20 pF. System voltage scaling = VSCALE1 or VSCALE2. All GPIO set to slew rate = 6. Data delay (PDM_CFG1_DLYMUXSEL) = 0.

Table 4.48. Pulse Density Modulator (PDM), Common DBUS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PDM_CLK frequency during data transfer	F_{PDM_CLK}	Microphone mode	—	—	5	MHz
		Sensor mode	—	—	20	MHz
PDM_CLK duty cycle	DC_{PDM_CLK}		47.5	—	52.5	%
PDM_CLK rise time	t_R		—	—	5.5	ns
PDM_CLK fall time	t_F		—	—	5.5	ns
Input setup time	t_{ISU}	Microphone mode	30	—	—	ns
		Sensor mode	20	—	—	ns
Input hold time	t_{IH}		3	—	—	ns

4.25 USART SPI Main Timing

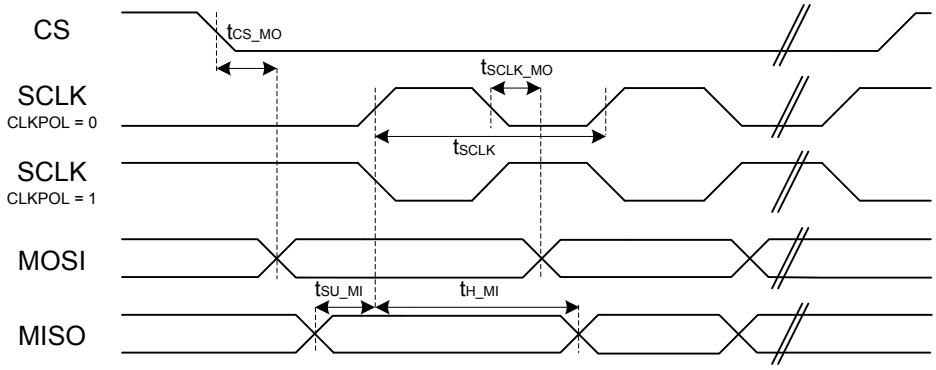


Figure 4.4. SPI Main Timing (SMSDELAY = 0)

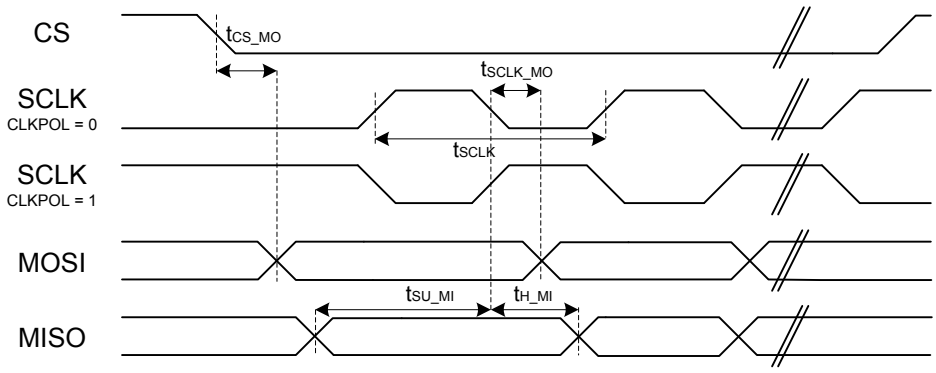


Figure 4.5. SPI Main Timing (SMSDELAY = 1)

4.25.1 USART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.49. USART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		2*t_{PCLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-14	—	14	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-4	—	13	ns
MISO setup time[1 2]	t_{SU_MI}	IOVDD = 1.8 V	37	—	—	ns
		IOVDD = 3.0 V	27	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-8	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.25.2 USART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.50. USART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		2*t_{PCLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-25	—	25	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-7	—	22	ns
MISO setup time[1 2]	t_{SU_MI}	IOVDD = 1.8 V	44	—	—	ns
		IOVDD = 3.0 V	36	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-9	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.25.3 USART SPI Main Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.51. USART SPI Main Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-17	—	17	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-4	—	15	ns
MISO setup time[1 2]	t_{SU_MI}		57	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-31	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.25.4 USART SPI Main Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.52. USART SPI Main Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-28	—	28	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-8	—	25	ns
MISO setup time[1 2]	t_{SU_MI}		66	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-34	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.26 USART SPI Secondary Timing

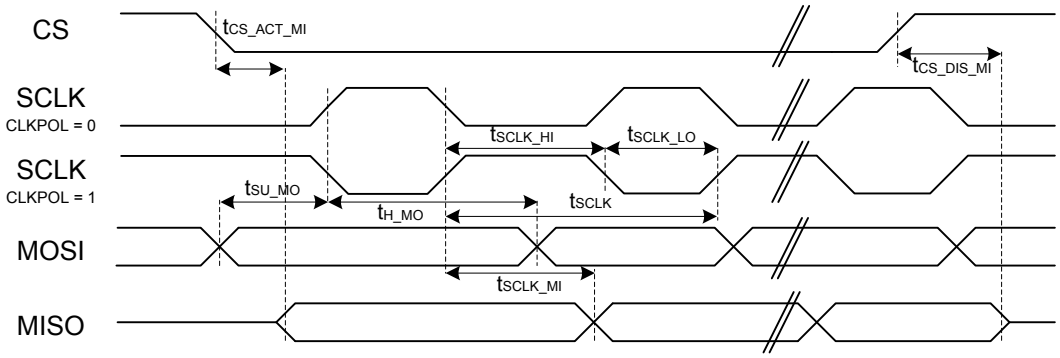


Figure 4.6. SPI Secondary Timing

4.26.1 USART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.53. USART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		19	—	54	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		18	—	46	ns
MOSI setup time[1 2]	t_{SU_MO}		6	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		8	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		15 + 1.5*t_{PCLK}	—	33 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.26.2 USART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.54. USART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		24	—	65	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		26	—	64	ns
MOSI setup time[1 2]	t_{SU_MO}		9	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		14	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		18 + 1.5*t_{PCLK}	—	46 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.26.3 USART SPI Secondary Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.55. USART SPI Secondary Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		32	—	73	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		24	—	55	ns
MOSI setup time[1 2]	t_{SU_MO}		7	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		9	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		28 + 1.5*t_{PCLK}	—	51 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.26.4 USART SPI Secondary Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.56. USART SPI Secondary Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		$6*t_{PCLK}$	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		$2.5*t_{PCLK}$	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		$2.5*t_{PCLK}$	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		37	—	88	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		32	—	74	ns
MOSI setup time[1 2]	t_{SU_MO}		10	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		14	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		$31 + 1.5*t_{PCLK}$	—	$65 + 2.5*t_{PCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.27 EUSART SPI Main Timing

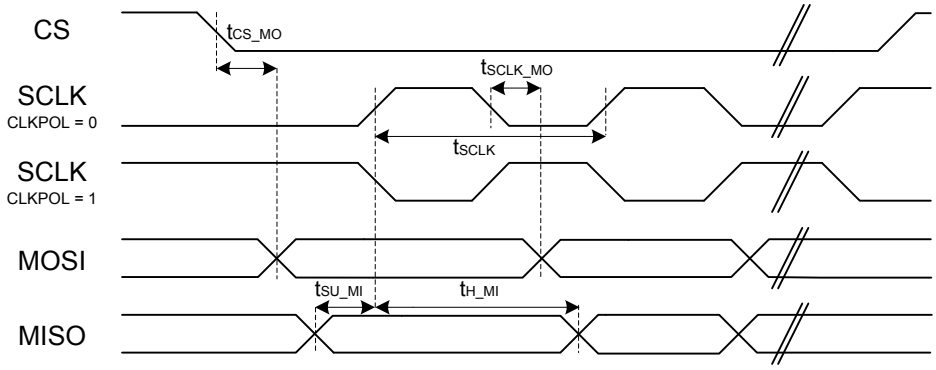


Figure 4.7. SPI Main Timing

4.27.1 EUSART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.57. EUSART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-13	—	11	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-4	—	10	ns
MISO setup time [1 2]	t_{SU_MI}		3	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-7	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.27.2 EUSART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.58. EUSART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-24	—	19	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-7	—	17	ns
MISO setup time [1 2]	t_{SU_MI}		12	—	—	ns
MISO hold time[1 2]	t_{H_MI}		7	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.27.3 EUSART SPI Main Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.59. EUSART SPI Main Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-16	—	16	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-4	—	13	ns
MISO setup time[1 2]	t_{SU_MI}		5	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-8	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.27.4 EUSART SPI Main Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.60. EUSART SPI Main Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-27	—	24	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-7	—	19	ns
MISO setup time[1 2]	t_{SU_MI}		14	—	—	ns
MISO hold time[1 2]	t_{H_MI}		6	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.28 EUSART SPI Secondary Timing

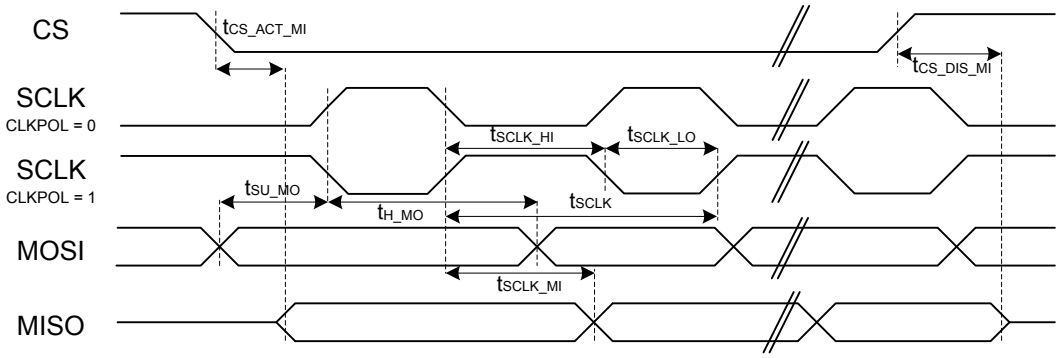


Figure 4.8. SPI Secondary Timing

4.28.1 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.61. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1] [2]	t_{SCLK_HI}		50	—	—	ns
SCLK low time[1] [2]	t_{SCLK_LO}		50	—	—	ns
CS active to MISO[1] [2]	$t_{CS\_ACT\_MI}$		4	—	51	ns
CS disable to MISO[1] [2]	$t_{CS\_DIS\_MI}$		5	—	35	ns
MOSI setup time[1] [2]	t_{SU_MO}		8	—	—	ns
MOSI hold time[1] [2]	t_{H_MO}		7	—	—	ns
SCLK to MISO[1] [2]	t_{SCLK_MI}	IOVDD = 1.8 V	9	—	41	ns
		IOVDD = 3.3 V	9	—	31	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.28.2 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.62. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		50	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		50	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		5	—	78	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		5	—	56	ns
MOSI setup time[1 2]	t_{SU_MO}		12	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		12	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}	IOVDD = 1.8 V	10	—	51	ns
		IOVDD = 3.3 V	10	—	43	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.28.3 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.63. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		100	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		100	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		8	—	112	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		7	—	83	ns
MOSI setup time[1 2]	t_{SU_MO}		12	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		33	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}	IOVDD = 1.8 V	11	—	92	ns
		IOVDD = 3.3 V	11	—	83	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.28.4 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.64. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1] [2]	t_{SCLK_HI}		100	—	—	ns
SCLK low time[1] [2]	t_{SCLK_LO}		100	—	—	ns
CS active to MISO[1] [2]	$t_{CS\_ACT\_MI}$		16	—	56	ns
CS disable to MISO[1] [2]	$t_{CS\_DIS\_MI}$		14	—	39	ns
MOSI setup time[1] [2]	t_{SU_MO}		8	—	—	ns
MOSI hold time[1] [2]	t_{H_MO}		7	—	—	ns
SCLK to MISO[1] [2]	t_{SCLK_MI}		34	—	63	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.28.5 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.65. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, 1.2 V ≤ IOVDD < 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1] [2]	t_{SCLK_HI}		100	—	—	ns
SCLK low time[1] [2]	t_{SCLK_LO}		100	—	—	ns
CS active to MISO[1] [2]	$t_{CS\_ACT\_MI}$		20	—	83	ns
CS disable to MISO[1] [2]	$t_{CS\_DIS\_MI}$		17	—	60	ns
MOSI setup time[1] [2]	t_{SU_MO}		13	—	—	ns
MOSI hold time[1] [2]	t_{H_MO}		12	—	—	ns
SCLK to MISO[1] [2]	t_{SCLK_MI}		38	—	75	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.29 I2C Electrical Specifications

4.29.1 I2C Standard-mode (Sm)

CLHR is set to 0 in the I2Cn_CTRL register.

Table 4.66. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.29.2 I2C Fast-mode (Fm)

CLHR is set to 1 in the I2Cn_CTRL register.

Table 4.67. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.29.3 I2C Fast-mode Plus (Fm+)

CLHR is set to 1 in the I2Cn_CTRL register.

Table 4.68. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.30 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.30.1 Supply Current

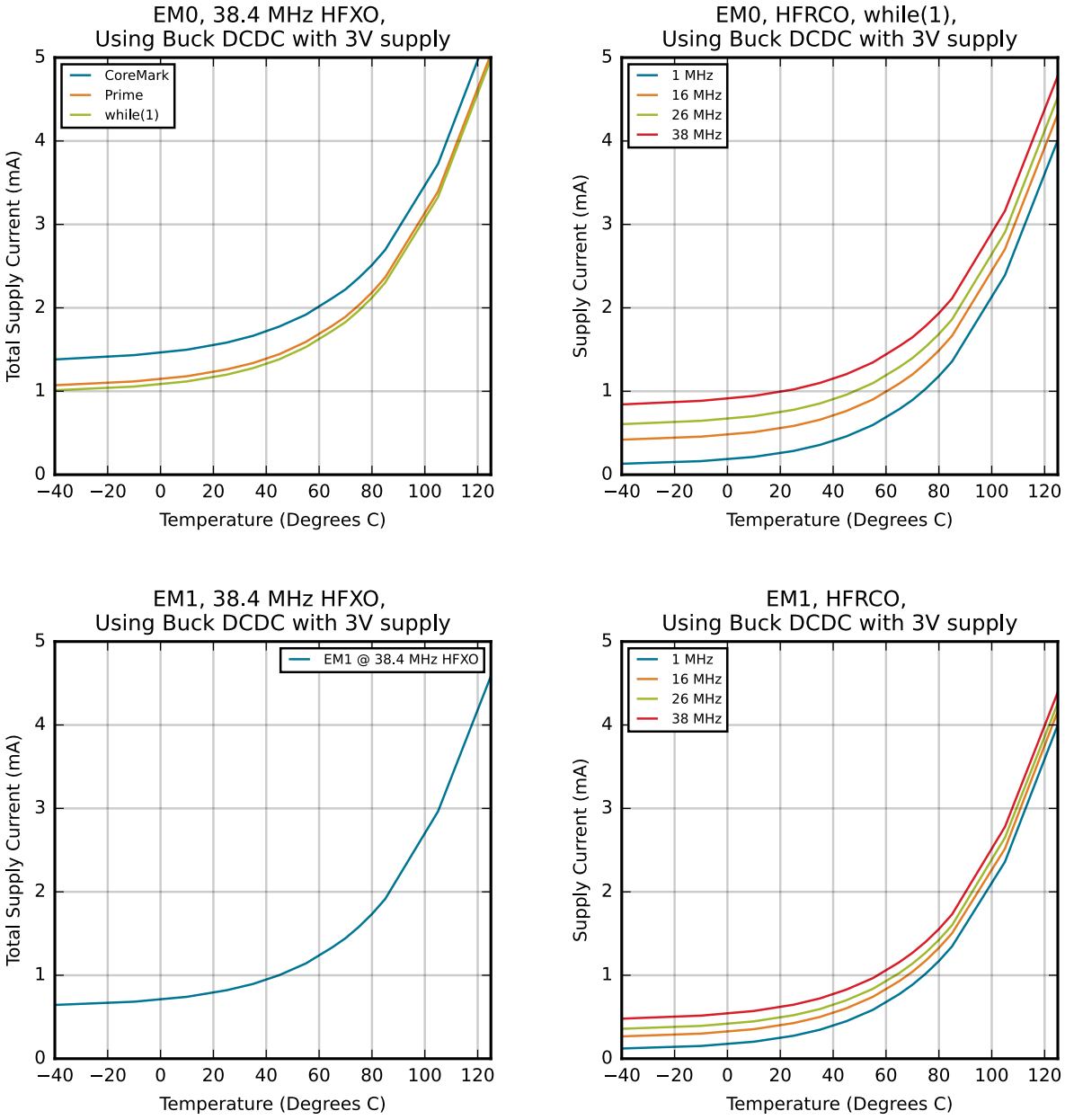


Figure 4.9. EM0 and EM1 Typical Supply Current vs. Temperature (Buck DCDC)

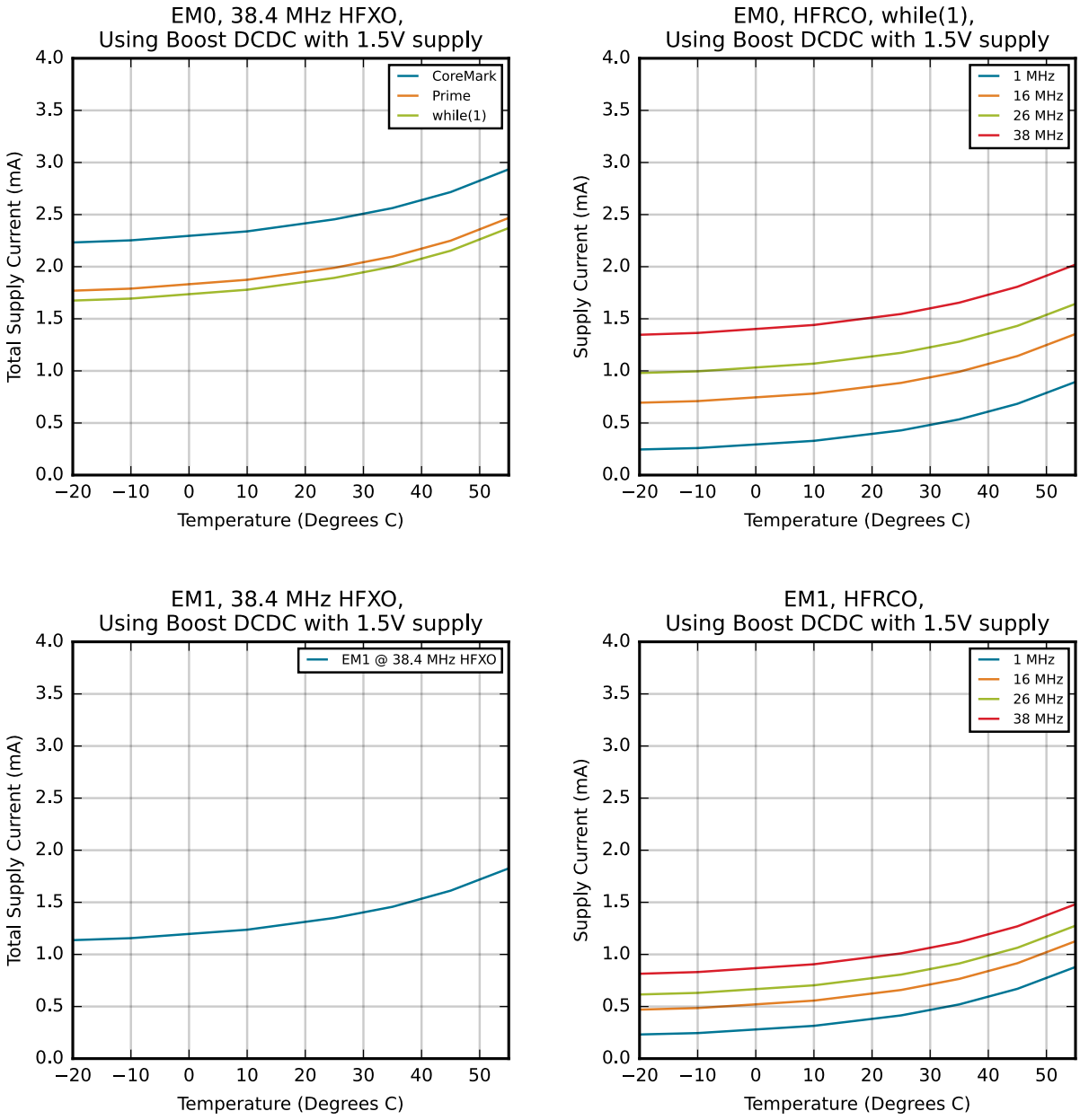


Figure 4.10. EM0 and EM1 Typical Supply Current vs. Temperature (Boost DCDC)

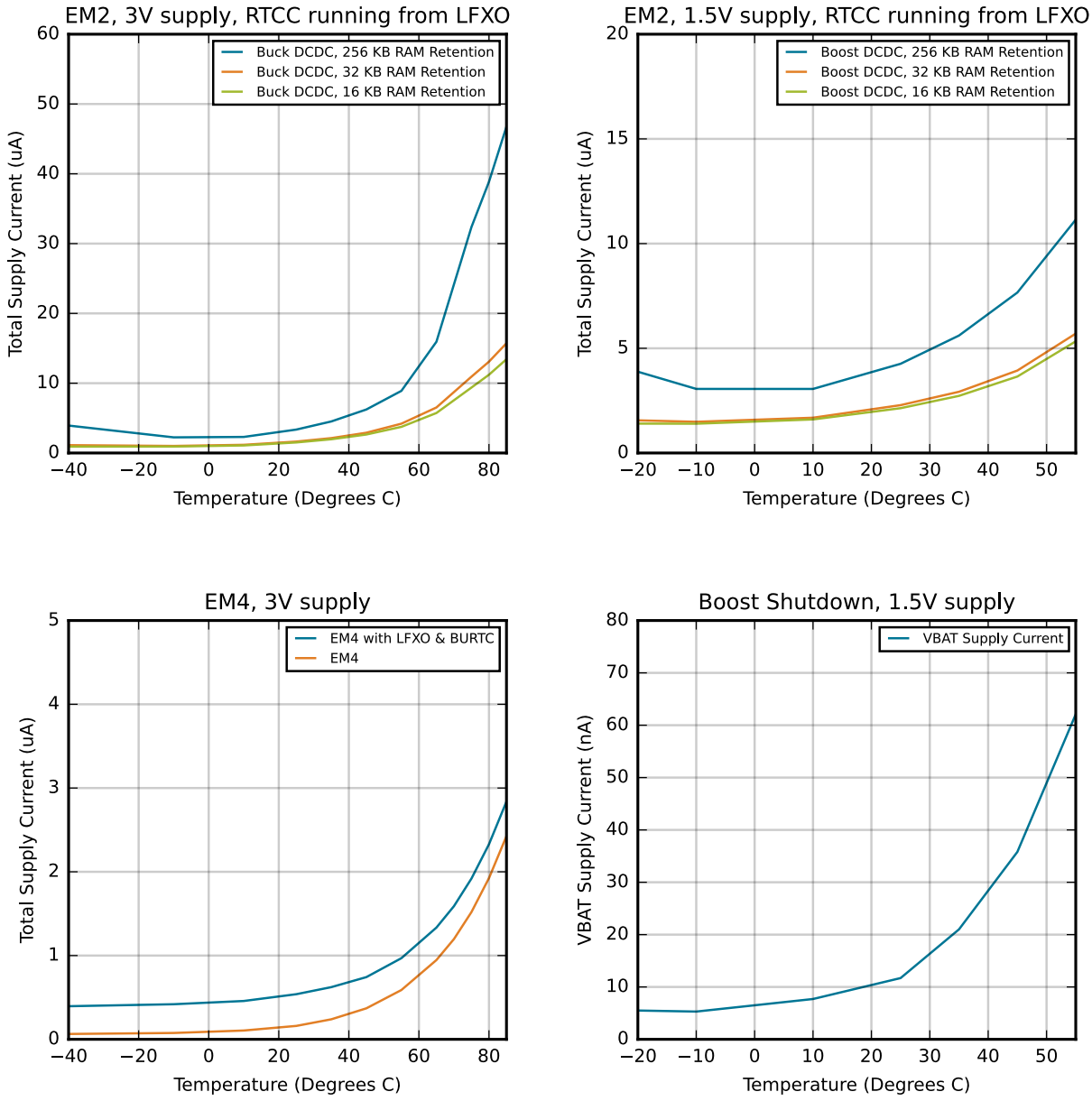


Figure 4.11. EM2, EM4, and Boost Shutdown Typical Supply Current vs. Temperature

4.30.2 RF Characteristics

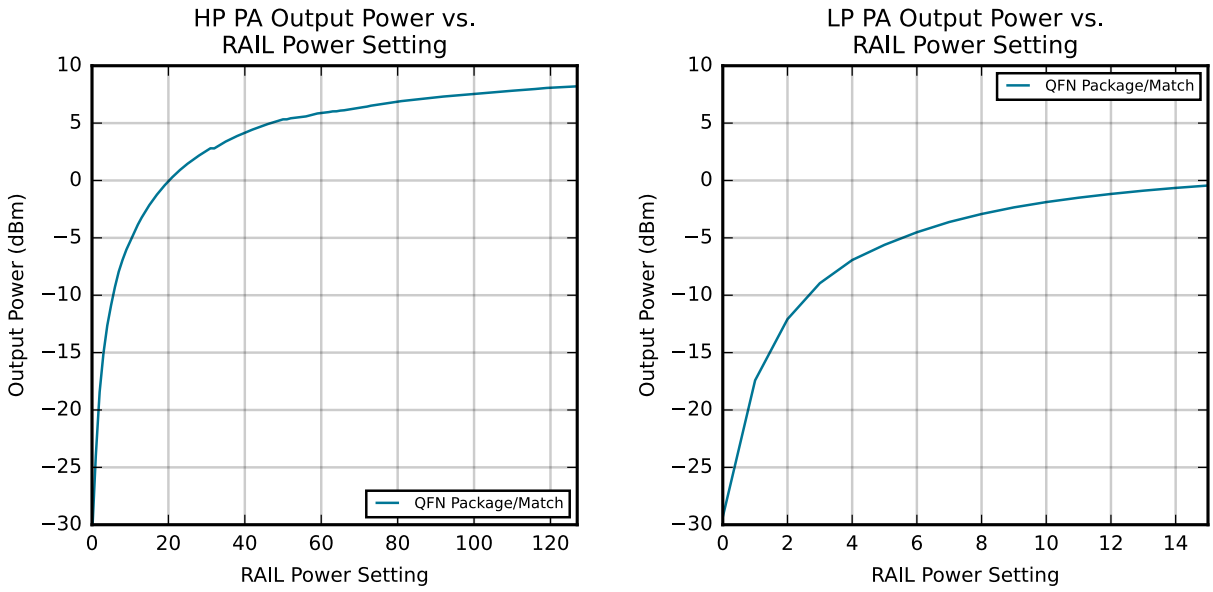


Figure 4.12. Transmitter Output Power, QFN Package / Matching

4.30.3 DC-DC Converter

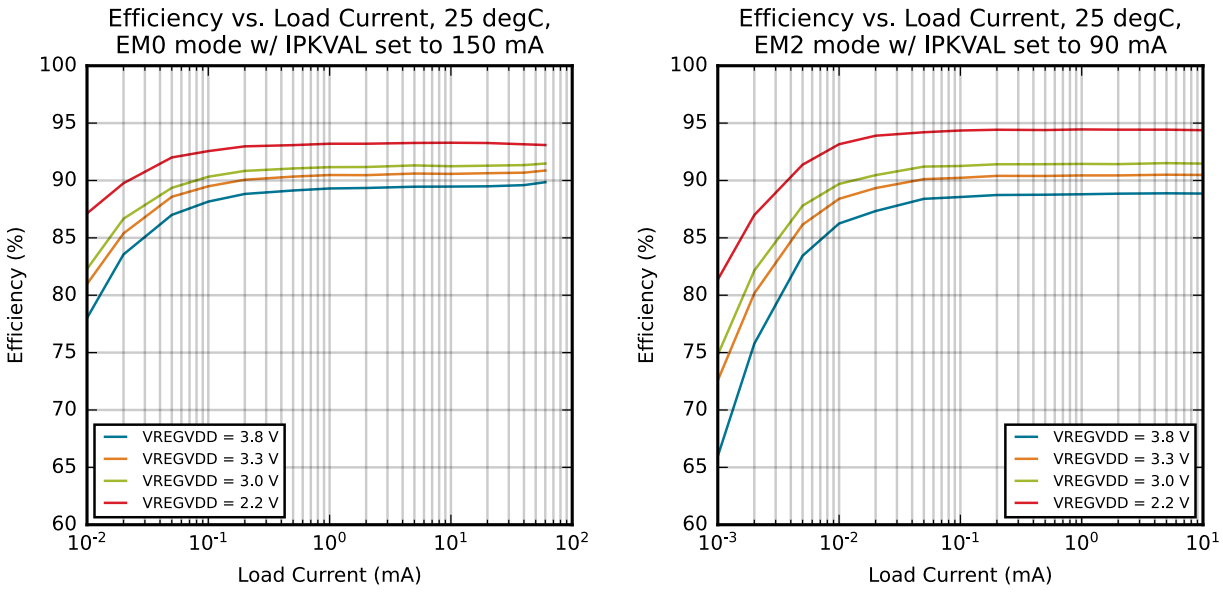


Figure 4.13. Buck DC-DC Efficiency

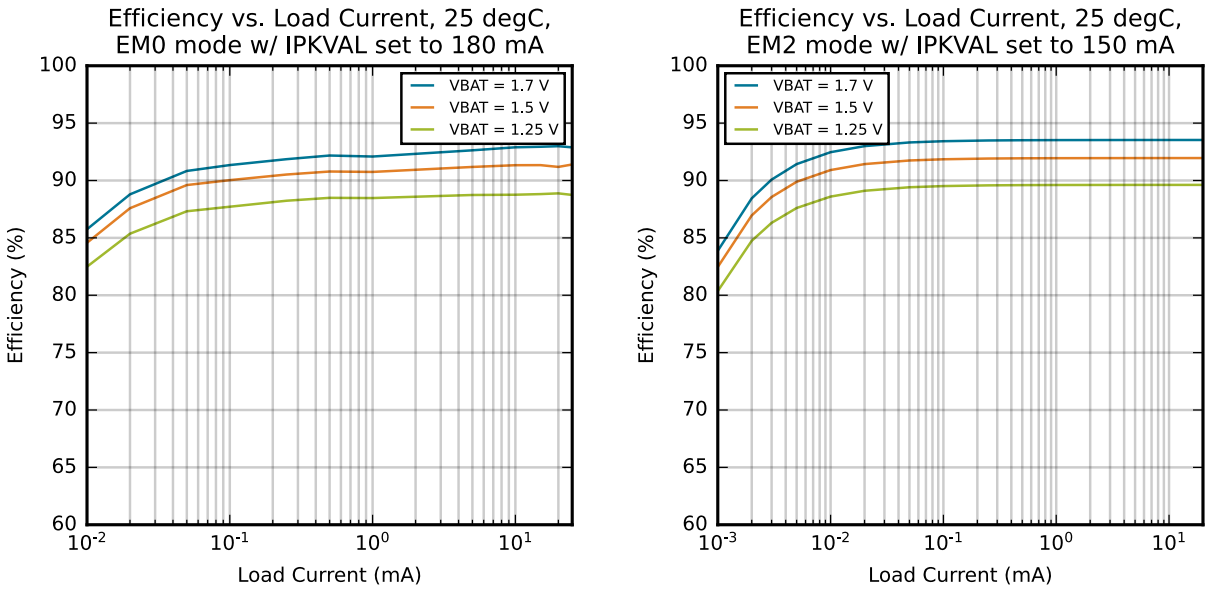


Figure 4.14. Boost DC-DC Efficiency

4.30.4 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

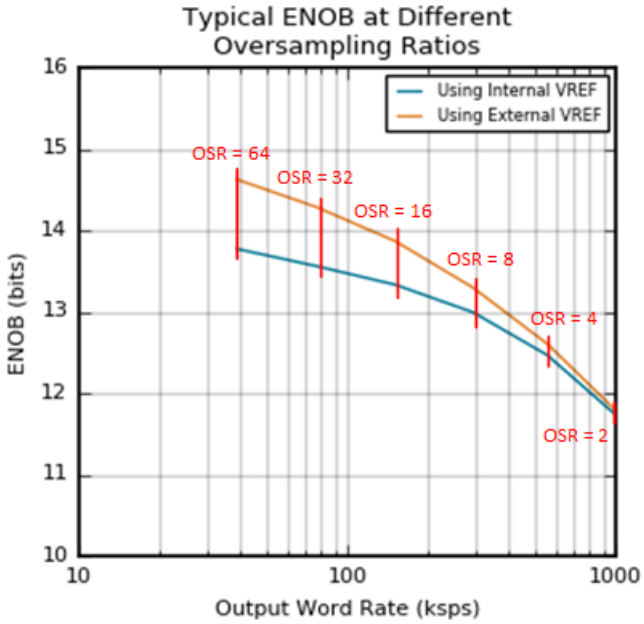


Figure 4.15. Typical ENOB vs. Oversampling Ratio

4.30.5 GPIO

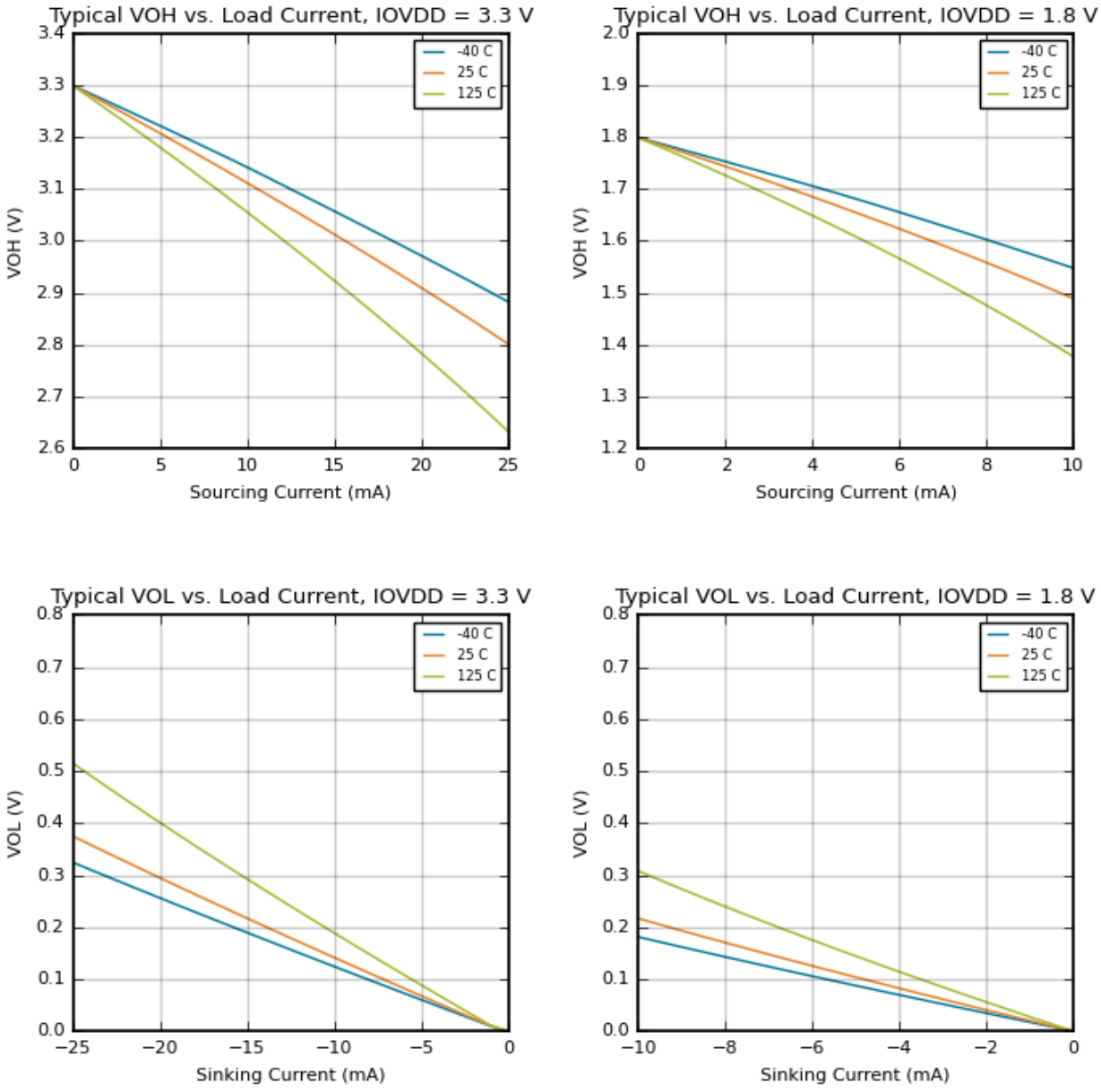


Figure 4.16. VOH and VOL vs. Load Current at 3.3 V and 1.8 V

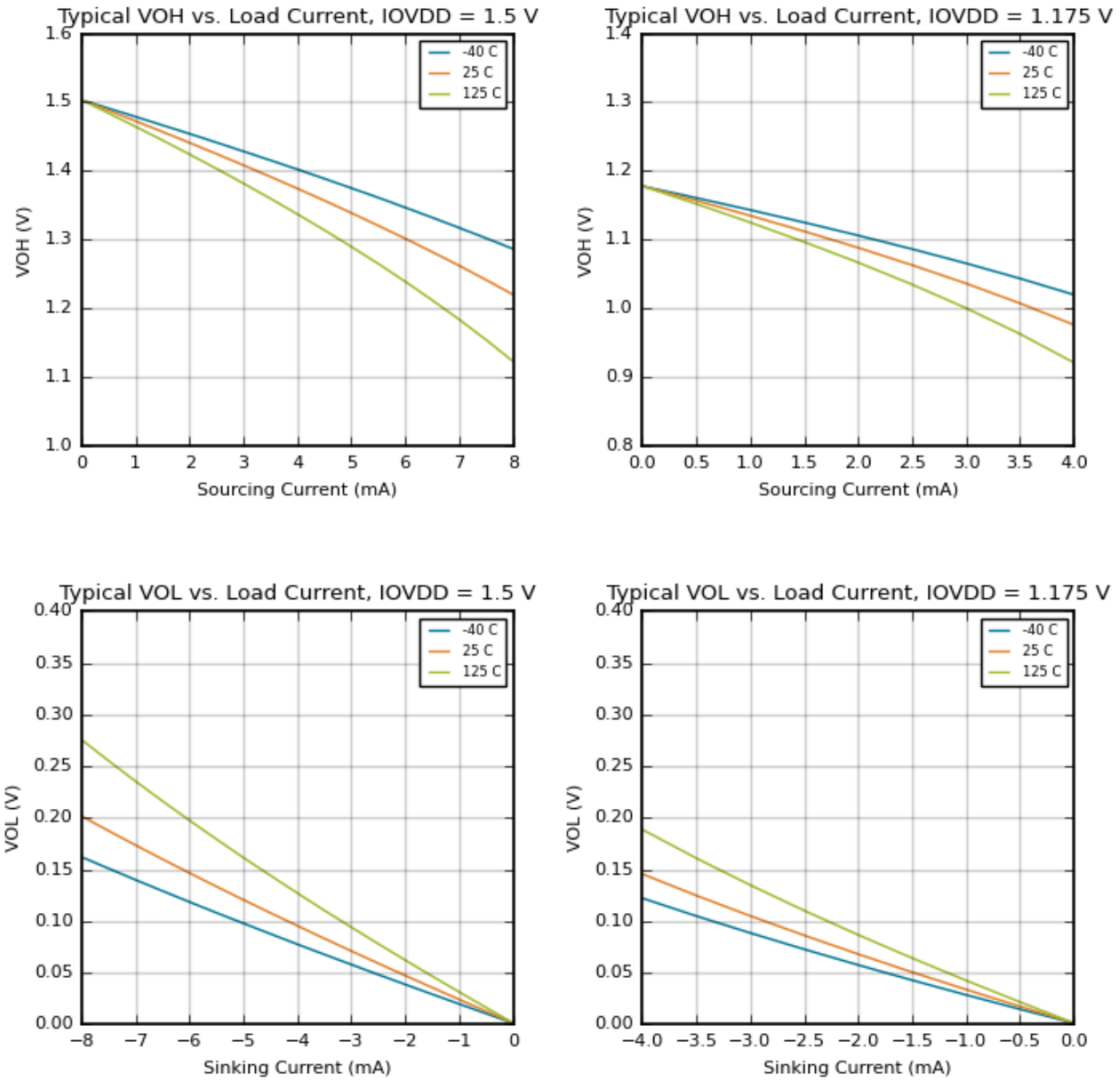


Figure 4.17. VOH and VOL vs. Load Current at 1.5 V and 1.175 V

5. Typical Connections

5.1 Power

Typical power supply connections are shown in the following figures.

Note: PAVDD, RFVDD, AVDD, and IOVDD supply connections are flexible. They may be connected in other configurations or to external supplies as long as the supply limits described in 4.1 Electrical Characteristics are met.

QFN40 Package Connections

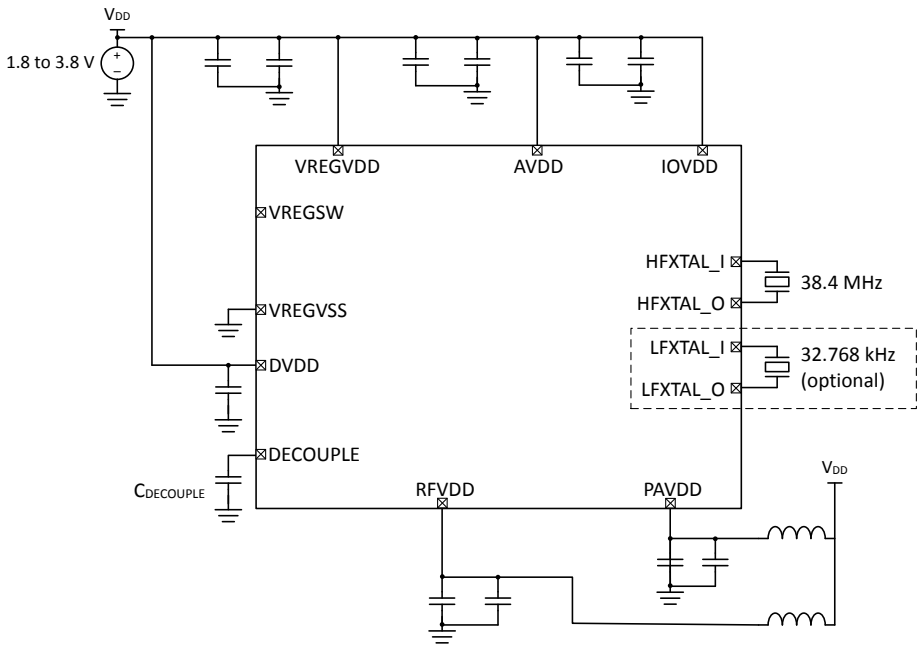


Figure 5.1. Typical Application Circuit: Direct Supply Configuration without DCDC (EFR32xG29B14x)

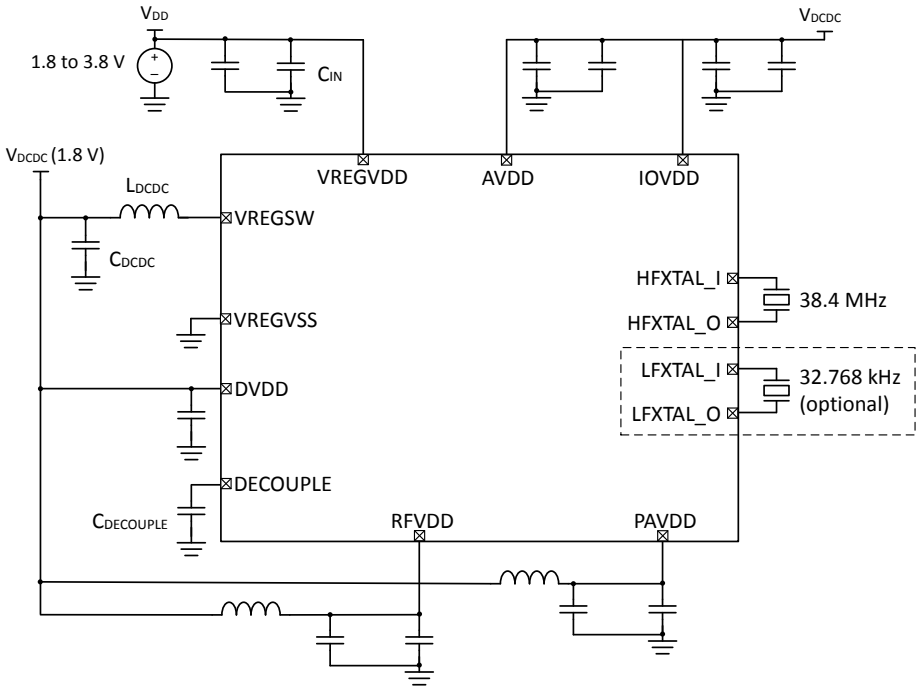


Figure 5.2. Typical Application Circuit: Buck DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output (EFR32xG29B14x)

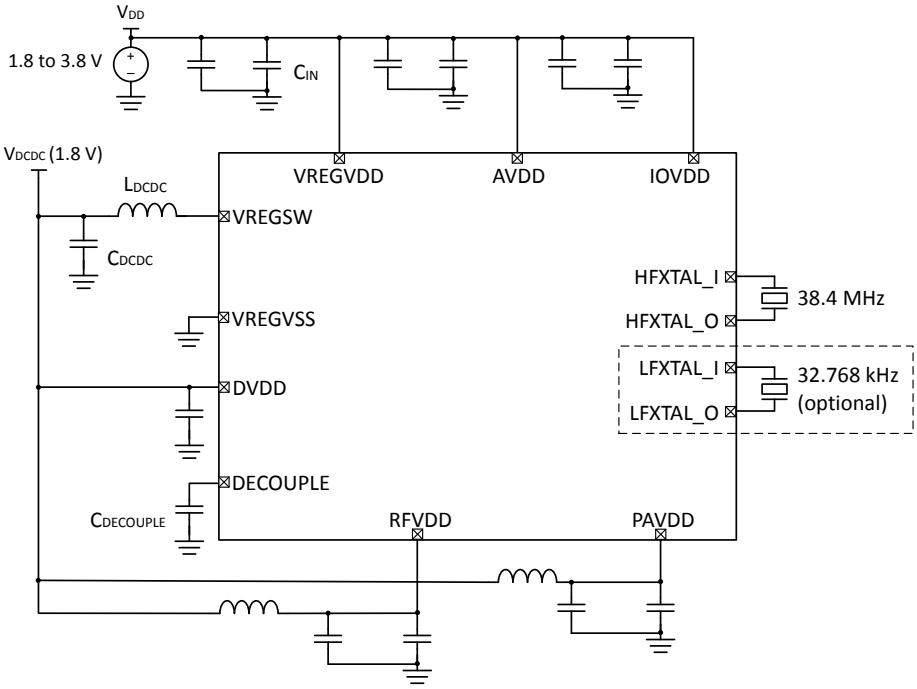
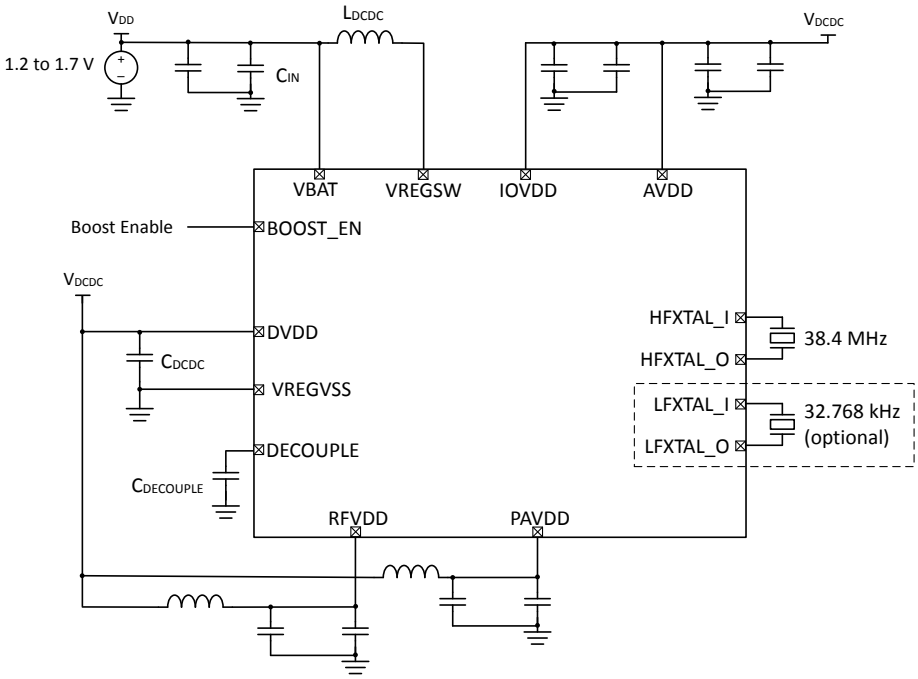
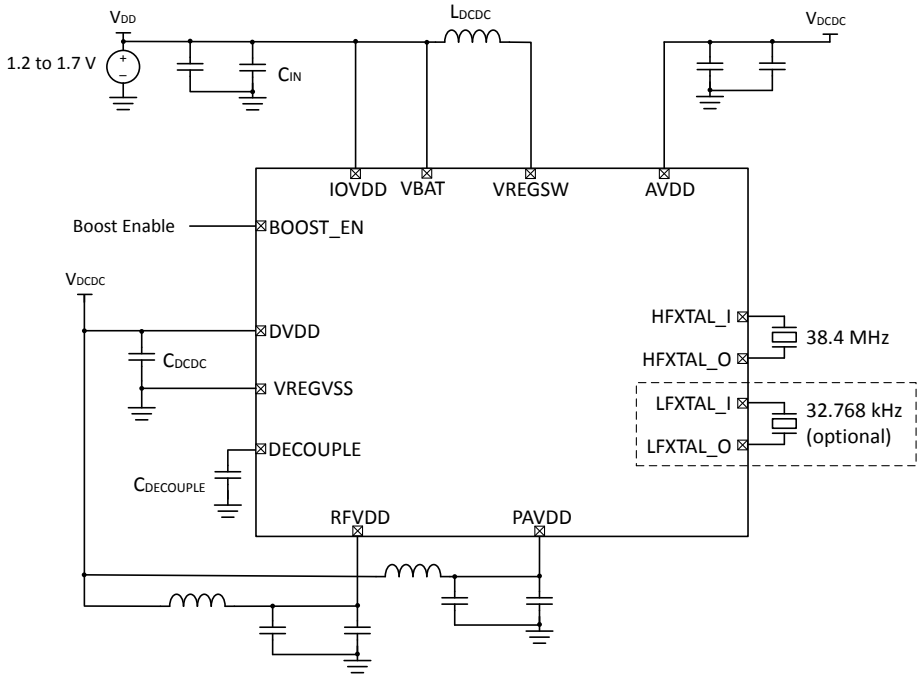


Figure 5.3. Typical Application Circuit: Buck DCDC Configuration with PAVDD and RFVDD from DCDC output (EFR32xG29B14x)



For DCDC always-on configuration, tie BOOST_EN to VBAT.

Figure 5.4. Typical Application Circuit: Boost DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output (EFR32xG29B23x)



For DCDC always-on configuration, tie BOOST_EN to VBAT.

Figure 5.5. Typical Application Circuit: Boost DCDC Configuration with PAVDD, RFVDD and AVDD from DCDC output, IOVDD from VBAT (EFR32xG29B23x)

5.2 RF Matching Networks

5.2.1 2.4 GHz Matching Network

The RF matching network circuit diagram used for RF characterization is shown in Figure 5.6 Typical RF impedance-matching network circuit on page 119. Typical component values are shown in Table 5.1 Component Values for QFN40 package on page 119. Refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

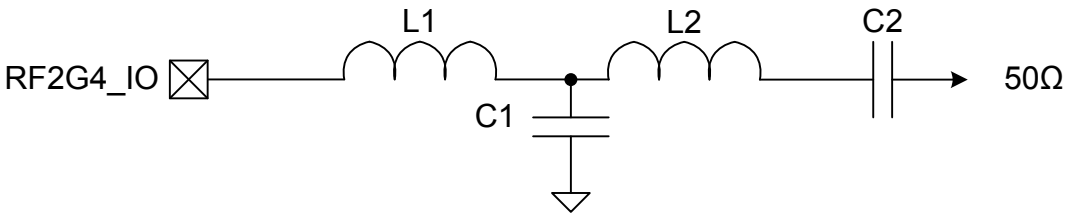


Figure 5.6. Typical RF impedance-matching network circuit

Table 5.1. Component Values for QFN40 package

Designator	Value
L1	2.0 nH
C1	1.6 pF
L2	3.2 nH
C2	18 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN40 with Buck DC-DC Device Pinout

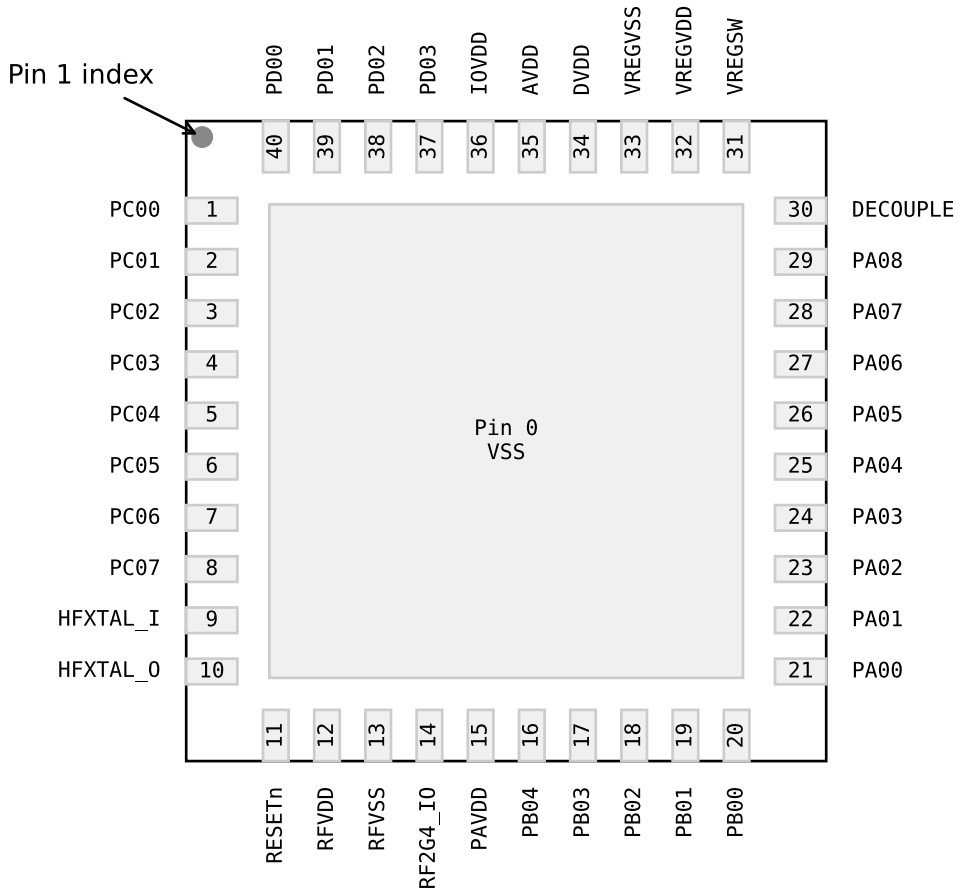


Figure 6.1. QFN40 with Buck DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.1. QFN40 with Buck DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High-frequency crystal input	HFXTAL_O	10	High-frequency crystal output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	11	Reset. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz Single-ended RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	31	DCDC regulator switching node	VREGVDD	32	DCDC Buck regulator input supply
VREGVSS	33	DCDC ground	DVDD	34	Digital power supply
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.2 QFN40 with Boost DC-DC Device Pinout

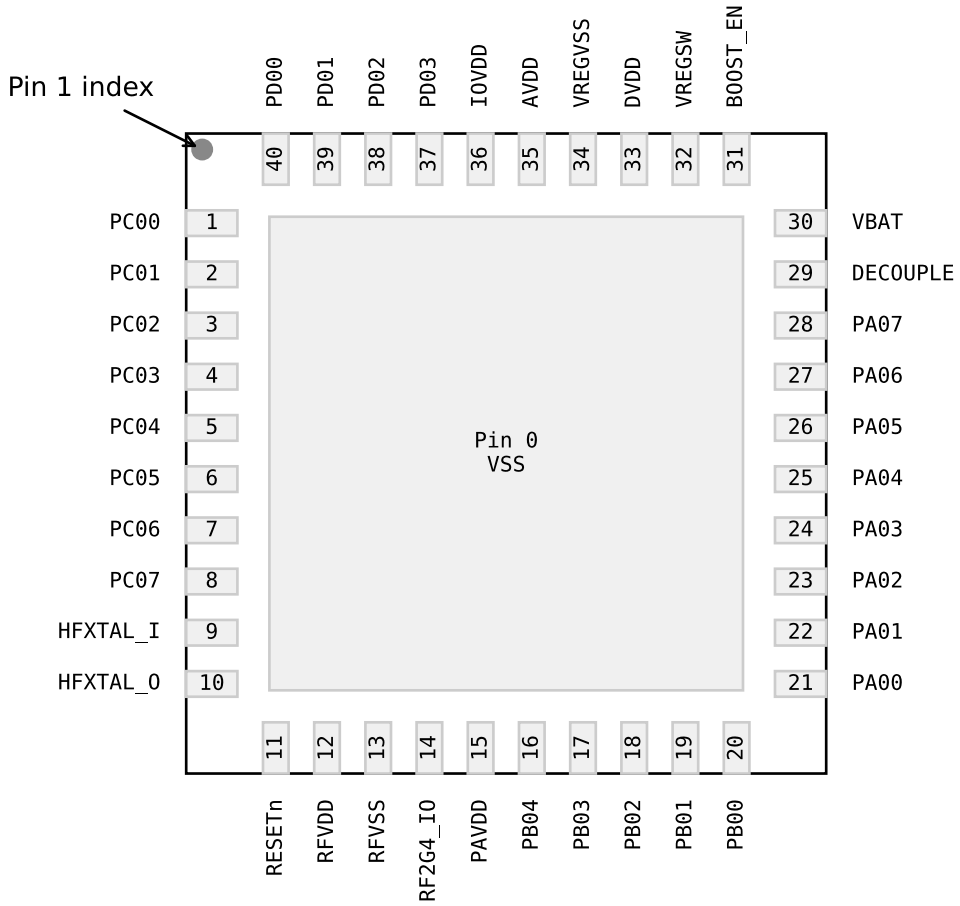


Figure 6.2. QFN40 with Boost DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

Table 6.2. QFN40 with Boost DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High-frequency crystal input	HFXTAL_O	10	High-frequency crystal output
RESETn	11	Reset. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	13	Radio ground	RF2G4_IO	14	2.4 GHz Single-ended RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	VBAT	30	DCDC boost regulator input supply
BOOST_EN	31	Boost DCDC enable	VREGSW	32	DCDC regulator switching node
DVDD	33	Digital power supply	VREGVSS	34	DCDC ground
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.3 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

Table 6.3. GPIO Alternate Function Table

GPIO	Alternate Functions	QFN40 with Buck DC-DC Package[1]	QFN40 with Boost DC-DC Package[2]
PA00	IADC0.VREFP	Yes	Yes
PA01	GPIO.SWCLK	Yes	Yes
PA02	GPIO.SWDIO	Yes	Yes
PA03	GPIO.SWV	Yes	Yes
	GPIO.TDO	Yes	Yes
	GPIO.TRACEDATA0	Yes	Yes
PA04	GPIO.TDI	Yes	Yes
	GPIO.TRACECLK	Yes	Yes
PA05	GPIO.TRACEDATA1	Yes	Yes
	GPIO.EM4WU0	Yes	Yes
PA06	GPIO.TRACEDATA2	Yes	Yes
PA07	GPIO.TRACEDATA3	Yes	Yes
PB01	ETAMPDET.ETAMPIN0	Yes	Yes
	GPIO.EM4WU3	Yes	Yes
PB03	GPIO.EM4WU4	Yes	Yes
PC00	ETAMPDET.ETAMPIN1	Yes	Yes
	GPIO.EM4WU6	Yes	Yes
	GPIO.THMSW_EN	Yes	Yes
	GPIO.THMSW_HALFSWITCH	Yes	Yes
PC01	ETAMPDET.ETAMPOUT0	Yes	Yes
	GPIO.EFP_TX_SDA	Yes	Yes
PC02	ETAMPDET.ETAMPOUT1	Yes	Yes
	GPIO.EFP_TX_SCL	Yes	Yes
PC05	GPIO.EFP_INT	Yes	Yes
	GPIO.EM4WU7	Yes	Yes
PC07	GPIO.EM4WU8	Yes	Yes
PD00	LFXO.LFXTAL_O	Yes	Yes
PD01	LFXO.LFXTAL_I	Yes	Yes
	LFXO.LF_EXTCLK	Yes	Yes
PD02	GPIO.EM4WU9	Yes	Yes

GPIO	Alternate Functions	QFN40 with Buck DC-DC Package[1]	QFN40 with Boost DC-DC Package[2]

Note:

1. QFN40 with Buck DC-DC Package includes OPN EFR32MG29B140F1024IM40-B
2. QFN40 with Boost DC-DC Package includes OPN EFR32MG29B230F1024CM40-B

6.4 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single-ended connection is being used, positive input is available on all pins. See the device reference manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.4. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.5 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.5. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available	Available	Available
EUSART0.CTS	Available	Available	Available	Available
EUSART0.RTS	Available	Available	Available	Available
EUSART0.RX	Available	Available	Available	Available
EUSART0.SCLK	Available	Available	Available	Available
EUSART0.TX	Available	Available	Available	Available
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7. QFN40 Package Specifications

7.1 QFN40 Package Dimensions

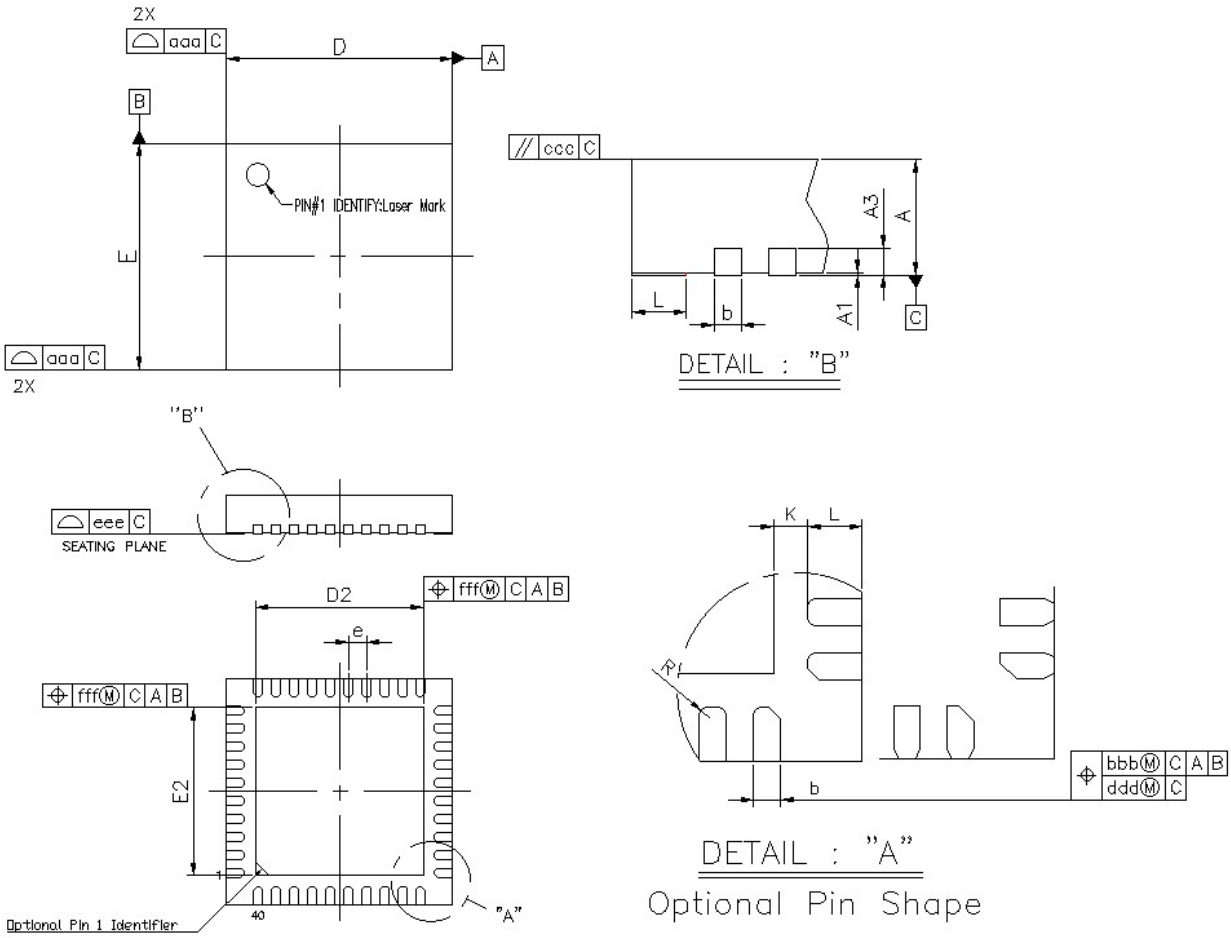


Figure 7.1. QFN40 Package Drawing

Table 7.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

7.2 QFN40 PCB Land Pattern

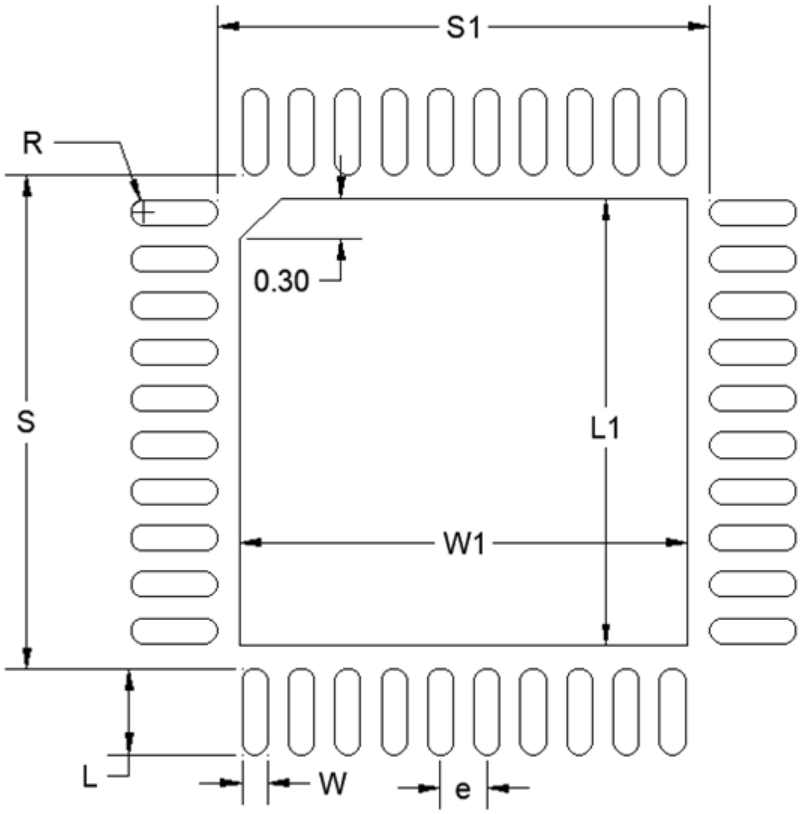


Figure 7.2. QFN40 PCB Land Pattern Drawing

Table 7.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Dimension	Typ

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN40 Package Marking

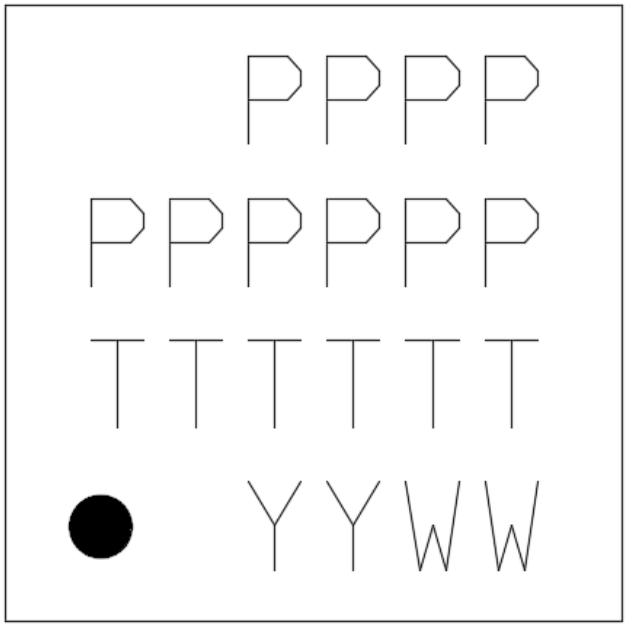


Figure 7.3. QFN40 Package Marking

The package marking consists of:

- FFFF – The product family codes (BG29 | MG29)
- PPPPPP – The product option codes:
  - 1) Security (B = Secure Vault High)
  - 2-4) Product Feature Codes
  - 5) Flash (J = 1024K)
  - 6) Temperature grade (C = -20 to 55 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. Revision History

Revision 1.0

May, 2025

Initial release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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