

Description

RClamp2271ZC is specifically designed to protect sensitive electronics from damage or latch-up due to ESD. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp2271ZC is in a DFN 0.60 x 0.30 x 0.25mm 2-Lead package. Leads are finished with lead-free NiAu. Each device will protect one high-speed data line operating up to 22V. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications.

Applications

- RF Antenna
- FM Antenna
- Near Field Communication (NFC) lines
- IoT Devices
- USB Type-C

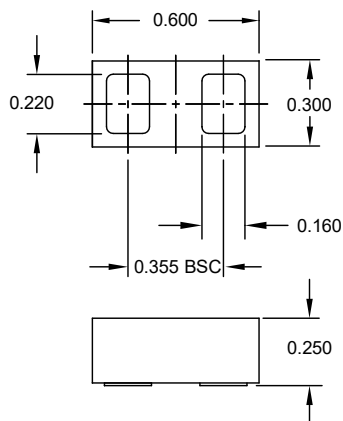
Features

- High ESD withstand Voltage
 - IEC 61000-4-2 (ESD): 8kV (Contact), 15kV (Air)
 - IEC 61000-4-5 (Lightning): 2A ($t_p = 8/20\mu s$)
- Ultra-small package
- Protects one data line
- Working voltage: $\pm 22V$
- Low ESD clamping voltage
- Low capacitance: 0.2pF maximum
- Low dynamic resistance: 0.4 Ω typical
- Solid-state silicon-avalanche technology

Mechanical Characteristics

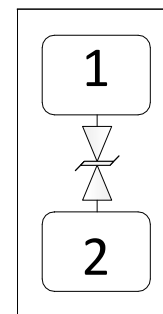
- Package: DFN 0.60 x 0.30 x 0.25mm 2-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking: Marking Code
- Packaging: Tape and Reel

Package Dimension



Nominal Dimensions in mm

Schematic & Pin Configuration



DFN 0.60 x 0.30 x 0.25mm 2-Lead (Bottom View)

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs)	P _{PK}	12	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	2	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±8	kV
ESD per IEC 61000-4-2 (Air) ^{(1),(2)}		±15	
Operating Temperature	T _{OP}	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V _{RWM}				22	V
Reverse Breakdown Voltage	V _{BR}	I _t = 10uA	24	28	32	V
Trigger Voltage ⁽³⁾	V _{Trigger}	tp = 0.2/100ns	24			V
Reverse Leakage Current	I _R	V _{RWM} = 22V		<1	50	nA
Clamping Voltage ⁽⁴⁾	V _C	tp = 1.2/50μs (Voltage), 8/20μs (Current) Combination Waveform, R _s = 12Ω	I _{PP} = 1A	4.9	5.5	V
				5.5	6.0	
ESD Clamping Voltage ⁽⁵⁾	V _C	t _p = 0.2/100ns (TLP)	I _{TLP} = 4A	6.9		V
		t _p = 0.2/100ns (TLP)	I _{TLP} = 12A	11		
Dynamic Resistance ^{(5),(6)}	R _{DYN}	t _p = 0.2/100ns (TLP)		0.5		Ω
Junction Capacitance	C _J	V _R = 0V, f = 1MHz		0.15	0.2	pF

Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP).

(2): Air discharge rated for in system withstand voltage.

(3): Guaranteed by design, not production tested.

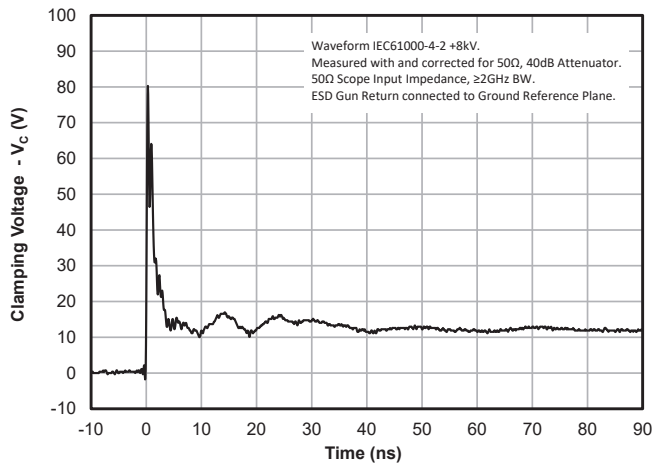
(4): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R_s = 12Ω. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(5): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns.

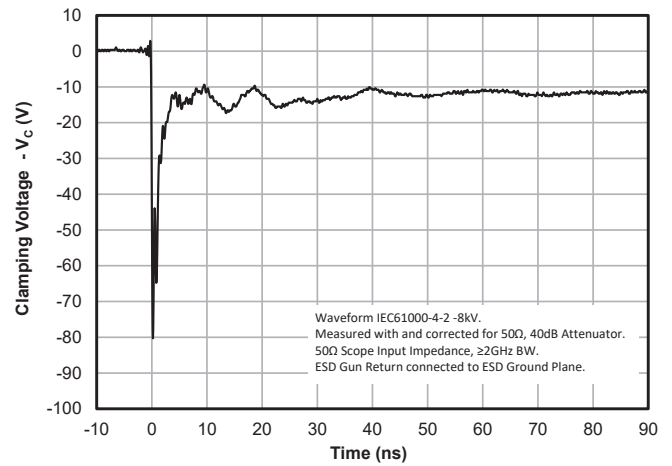
(6): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 12A.

Typical Characteristics

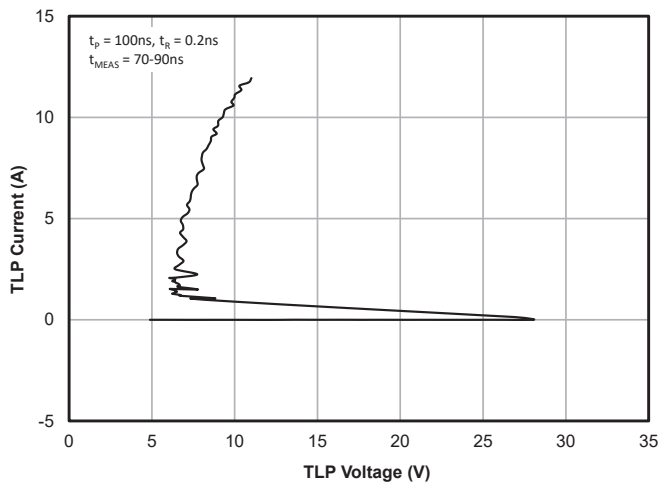
ESD Clamping (8kV Contact per IEC 61000-4-2)



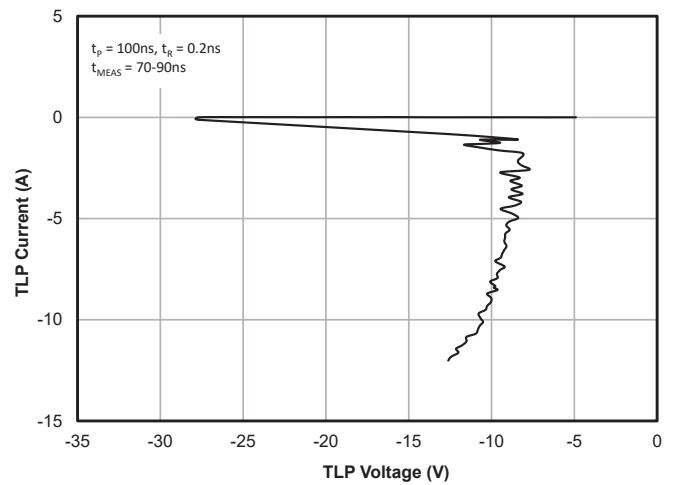
ESD Clamping (-8kV Contact per IEC 61000-4-2)



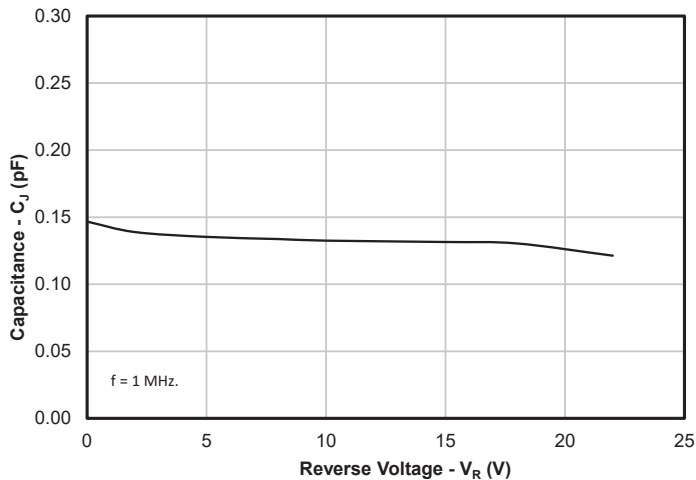
TLP Characteristics (Positive Pulse)



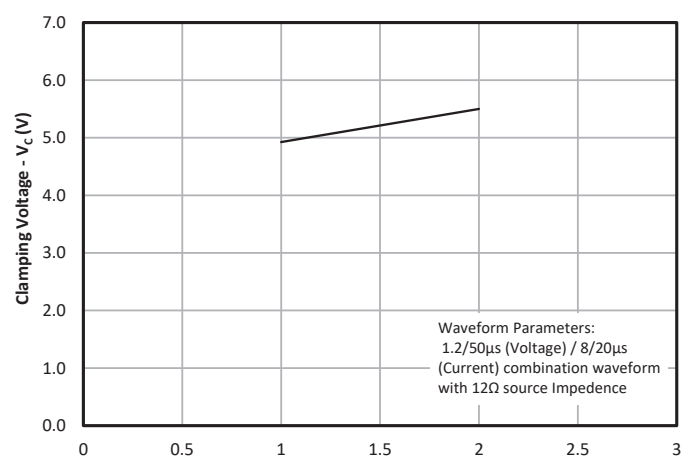
TLP Characteristics (Negative Pulse)



Capacitance vs. Reverse Voltage



Clamping Voltage vs. Peak Pulse Current



Applications Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

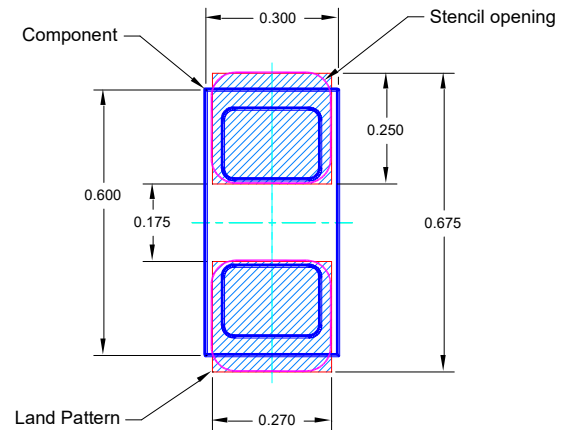
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern



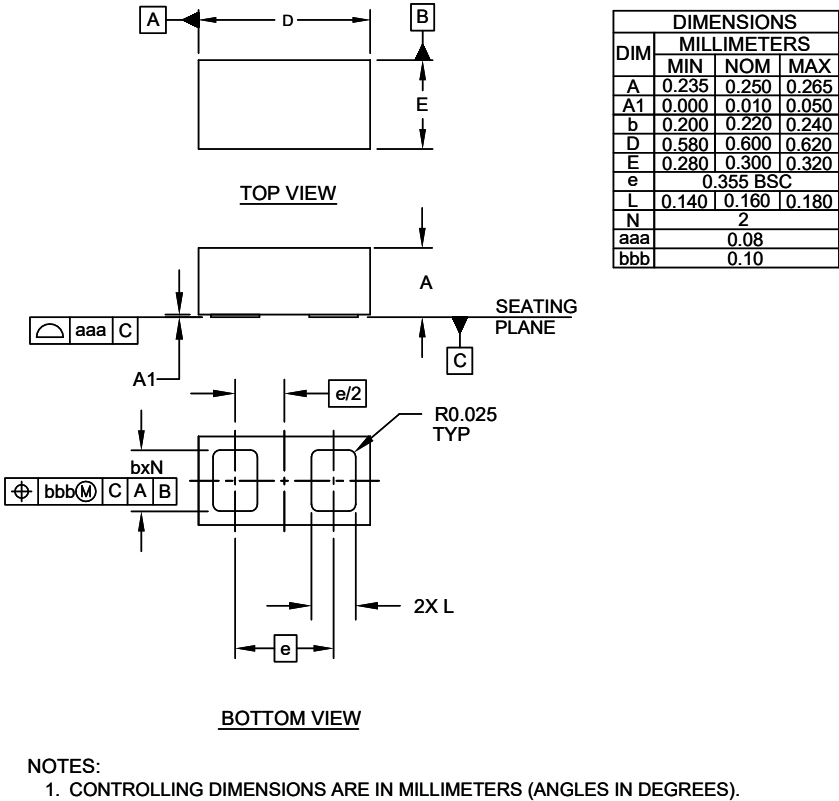
All Dimensions are in mm.

Land Pad. Stencil opening Component

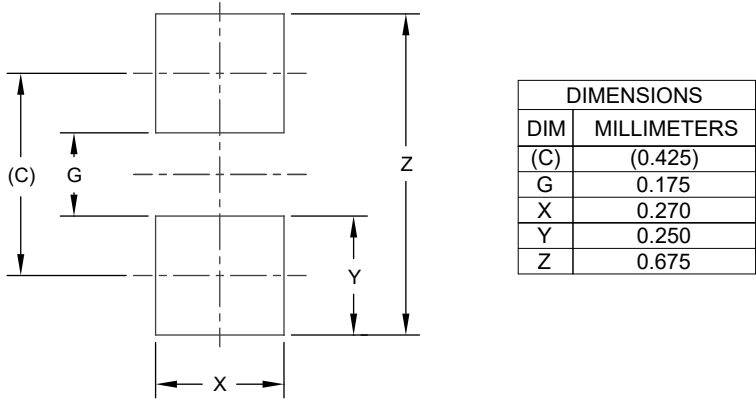
Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003") or 0.100mm (0.004")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 0.60 x 0.30 x 0.25mm 2-Lead



Landing Pattern - DFN 0.60 x 0.30 x 0.25mm 2-Lead



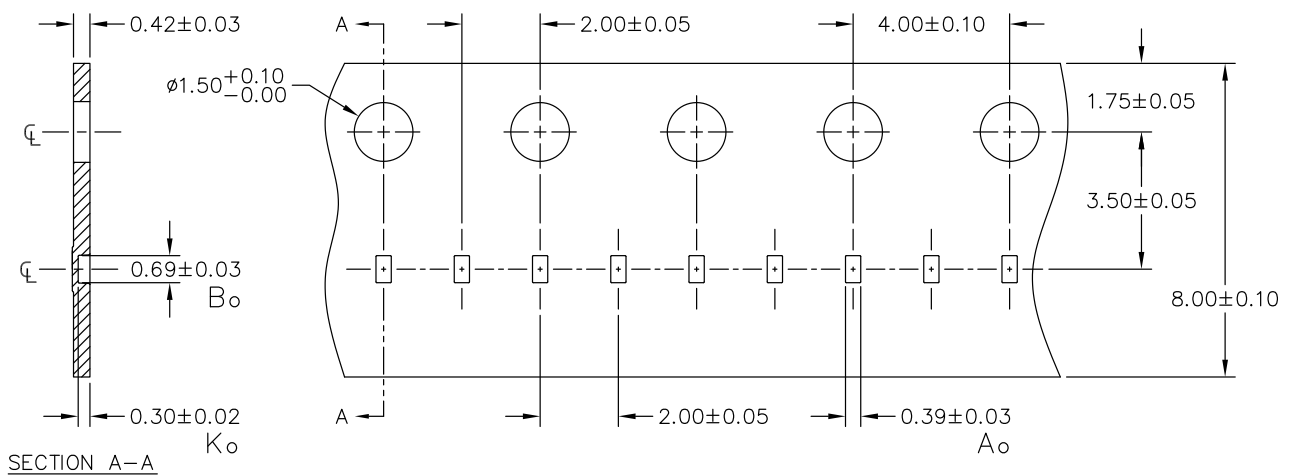
- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

71

Note: Device is electrically symmetrical.

Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

Order Information

PART NUMBER	QTY PER REEL	REEL SIZE
RClamp2271ZC.F	15,000	7"

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