



# LTDC-X3

## 2-Channel LiDAR Time-to-Digital Converter

**LTDC-X3 datasheet**

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LTDC-X3 is a high-performance 2-channel time-to-digital converter specifically designed for single-beam LIDAR systems. It has a separate START channel, two STOP channels, measures up to 8 pulses on rising and/or falling edges, has a pulse-pair resolution as low as 5 ns, a typical rms resolution of 20 ps and a range up to 16  $\mu$ s. It integrates a start pulse generator for generation of trigger signals to an external laser diode driver.

Equipped with a quad SPI interface, the data rate can be as high as 50MHz / 200MBPS.

It comes in a 4x4 QFN32 package and works in the industrial temperature range.

## Key Benefits

- Simple data post-processing thanks to calibrated results
- Optimized for LiDAR applications
- High efficiency thanks high sample rate
- Compact design thanks to small package and low number of external components
- Reduced cooling thanks to low power consumption

## Key Features

- Two TDC stop channels, one separate TDC start channel
- Pulse measurements on rising and falling edge
- Minimum pulse width 2 ns
- Minimum pulse-to-pulse spacing 3 ns (combined channels)
- Stop measurement of up to 8 pulses on rising and falling edge
- Stop mask window
- Maximum measuring range 16  $\mu$ s
- Typical rms resolution 30 ps, 20 ps with HighRes = 4
- Stop input comparator compatible with LVDS
- 50MHz/200MBPS Quad SPI interface
- Start pulse generator including configurable phase noise

## Applications

- Robotics LiDAR
- Range finders
- Door scanners
- Safety scanners

## Properties

- Supply voltage 3.3 V
- Temperature range -40°C to +105°C
- QFN32 package

## Content Guide

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## 1 Block Diagram

The functional blocks of this device are shown below.

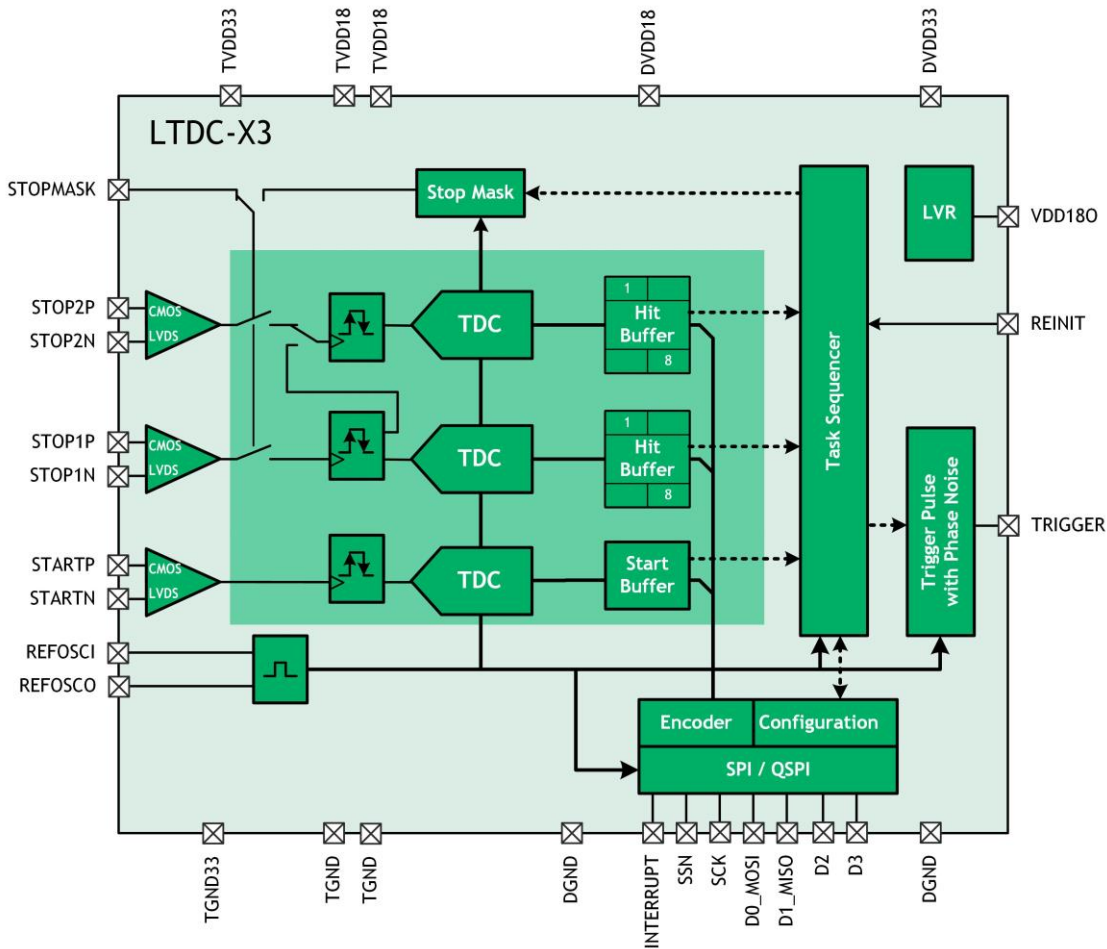


Figure 1: Functional Blocks

## 2 Pin Assignment

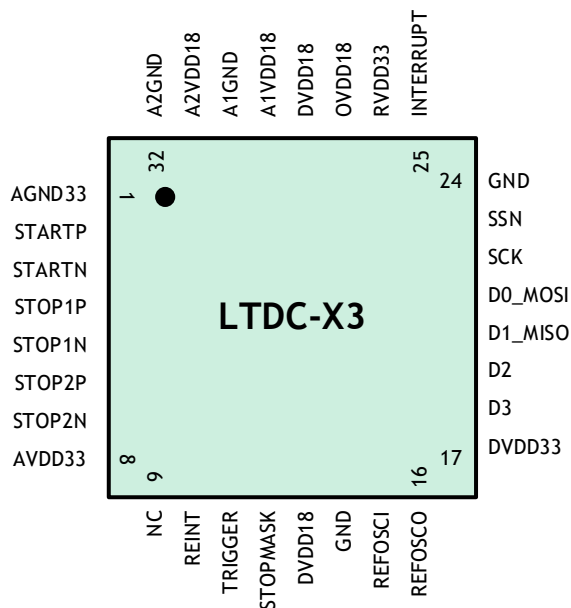


Figure 2: Pin diagram

Table 1: Pin description

| Pins | Pin Name | Pin Type <sup>1</sup> | Description                                   | If not used |
|------|----------|-----------------------|-----------------------------------------------|-------------|
| 1    | AGND33   | S                     | Ground supply for time front-end              |             |
| 2    | STARTP   | LVDS <sub>DI</sub>    | Positive LVDS / CMOS start input              |             |
| 3    | STARTN   | LVDS <sub>N</sub>     | Negative LVDS start input                     |             |
| 4    | STOP1P   | LVDS <sub>DI</sub>    | Positive LVDS / CMOS input for stop channel 1 |             |
| 5    | STOP1N   | LVDS <sub>N</sub>     | Negative LVDS input for stop channel 1        |             |
| 6    | STOP2P   | LVDS <sub>DI</sub>    | Positive LVDS / CMOS input for stop channel 2 |             |
| 7    | STOP2N   | LVDS <sub>N</sub>     | Negative LVDS input for stop channel 2        |             |
| 8    | AVDD33   | S                     | 3.3V positive supply for time front-end       |             |
| 9    | NC       | IO                    | Not connected                                 | GND         |
| 10   | REINIT   | DI <sub>PD</sub>      | Re-init TDC command                           |             |
| 11   | TRIGGER  | DO                    | Trigger pulses with phase noise               |             |
| 12   | STOPMASK | DI <sub>PD</sub>      | Input signal to mask the stop inputs          |             |
| 13   | DVDD18   | S                     | 1.8V supply for digital and IO units          |             |

<sup>1</sup> S supply pad, AIO analog I/O, DI digital input, LVDS<sub>DI</sub> LVDS positive input / CMOS digital input, LVDS<sub>N</sub> LVDS negative input, DI<sub>PU</sub> digital input with pull-up, DI<sub>PD</sub> digital input with pull-down, DI<sub>PU\_ST</sub> digital Schmitt trigger input with pull-up, DI<sub>PD\_ST</sub> digital Schmitt trigger input with pull-down, DIO<sub>PU</sub> I/O with pull-up, DIO<sub>PD</sub> digital I/O with pull-down, DIO<sub>T</sub> digital I/O / tristate, DO digital output, DO<sub>PD</sub> digital output with pull-down, DO<sub>ODPU</sub> digital output open drain with pull-up, DO<sub>ODPD</sub> digital output open drain with pull-down

|    |           |       |                                                        |  |
|----|-----------|-------|--------------------------------------------------------|--|
| 14 | GND       | S     | Ground for digital blocks and IO units                 |  |
| 15 | REFOSCI   | AIO   | Input for quartz as reference clock                    |  |
| 16 | REFOSCO   | AIO   | Output for quartz as reference clock                   |  |
| 17 | DVDD33    | S     | 3.3V supply for digital and IO units                   |  |
| 18 | D3        | DIO_T | QSPI/SPI Data Output 3                                 |  |
| 19 | D2        | DIO_T | QSPI/SPI Data Output 2                                 |  |
| 20 | D1        | DIO_T | QSPI/SPI Data Output 1 / Master Input Slave Output     |  |
| 21 | D0        | DIO_T | QSPI/SPI Data Output 0 / Master Output Slave Input     |  |
| 22 | SCK       | DI    | QSPI/SPI clock                                         |  |
| 23 | SSN       | DI_PU | QSPI/SPI chip select                                   |  |
| 24 | GND       | S     | Ground for digital blocks and IO units                 |  |
| 25 | INTERRUPT | DO    | Interrupt output                                       |  |
| 26 | RVDD33    | S     | 3.3V positive supply for LDO                           |  |
| 27 | OVDD18    | S     | 1.8V supply for digital and IO units, regulator output |  |
| 28 | DVDD18    | S     | 1.8V supply for digital and IO units                   |  |
| 29 | A1VDD18   | S     | 1.8V supply for analog block                           |  |
| 30 | GND1      | S     | Ground for analog 1.8V block                           |  |
| 31 | A2VDD18   | S     | 1.8V supply for analog block                           |  |
| 32 | A2GND18   | S     | Ground for analog 1.8V block                           |  |

### 3 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2: Absolute Maximum Ratings*

| Symbol                                    | Parameter                                                                    | Min    | Max       | Units | Comments                         |
|-------------------------------------------|------------------------------------------------------------------------------|--------|-----------|-------|----------------------------------|
| Electrical Parameters                     |                                                                              |        |           |       |                                  |
| VDD33                                     | 3.3V Supply Voltage to Ground                                                | -0.3   | 4.0       | V     |                                  |
| VDD18                                     | 1.8V Supply Voltage to Ground                                                | -0.3   | 2.3       | V     |                                  |
| V <sub>DLVDS</sub>                        | DC Voltage at LVDS START and STOP pins                                       | -0.3   | VDD33+0.3 | V     |                                  |
| V <sub>DIO</sub>                          | DC Voltage at D0, D1, D2, D3, SSN, SCK, INTERRUPT, STOPMASK and TRIGGER pins | -0.3   | VDD33+0.3 | V     |                                  |
| I <sub>SCR</sub>                          | Input current (latch-up immunity)                                            | -100   | 100       | mA    | JESD78E                          |
| P <sub>tot</sub>                          | Total Power Dissipation                                                      |        | 150       | mW    |                                  |
| Electrostatic Discharge                   |                                                                              |        |           |       |                                  |
| ESD <sub>HBM</sub>                        | Electrostatic Discharge HBM                                                  | ± 1000 |           | V     | JS-001-2017                      |
| ESD <sub>CDM</sub>                        | Electrostatic Discharge CDM                                                  | ± 500  |           | V     | JS-002-2018                      |
| Temperature Ranges and Storage Conditions |                                                                              |        |           |       |                                  |
| T <sub>J</sub>                            | Operating Junction Temperature                                               | -40    | 125       | °C    |                                  |
| T <sub>STRG</sub>                         | Storage Temperature Range                                                    | - 65   | 150       | °C    |                                  |
| T <sub>BODY</sub>                         | Package Body Temperature                                                     |        | 260       | °C    | IPC/JEDEC J-STD-020 <sup>2</sup> |
| RH <sub>NC</sub>                          | Relative Humidity (non-condensing)                                           | 5      | 85        | %     |                                  |
| MSL                                       | Moisture Sensitivity Level                                                   | 3      |           |       | Maximum floor life time of 168h  |

<sup>2</sup> The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb free leaded packages is “Matte Tin” (100 % Sn)

## 4 Recommended Operating Conditions

*Recommended operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are expressly denoted.*

Table 3: Recommended operation conditions

| Symbol                     | Parameter                                   | Conditions               | Min                  | Typ  | Max                      | Unit |
|----------------------------|---------------------------------------------|--------------------------|----------------------|------|--------------------------|------|
| Power Supply               |                                             |                          |                      |      |                          |      |
| VDD33                      | DC supply voltage VDD33                     |                          | 3.0                  | 3.3  | 3.6                      | V    |
| VDD18                      | DC voltage at VDD18 pin                     | Supplied from chip       | 1.62                 | 1.8  | 1.98                     | V    |
| t <sub>POR</sub>           | Startup time                                |                          |                      | 10   |                          | ms   |
| Temperature                |                                             |                          |                      |      |                          |      |
| T <sub>A</sub>             | Operating free air temperature <sup>3</sup> |                          | -25                  | 25   | 105                      | °C   |
| LVDS Input                 |                                             |                          |                      |      |                          |      |
| V <sub>ID</sub>            | LVDS differential input voltage             |                          | 100                  |      |                          | mV   |
| V <sub>ICM</sub>           | LVDC common mode input voltage              |                          | V <sub>ID</sub> /2   | 1.25 | 2.4 – V <sub>ID</sub> /2 | mV   |
| t <sub>pmin_LVDS</sub>     | Minimum pulse width                         |                          |                      | 2    | 3                        | ns   |
| Digital Inputs and Outputs |                                             |                          |                      |      |                          |      |
| V <sub>IL,CMOS</sub>       | CMOS input low voltage                      |                          |                      |      | 0.4                      | V    |
| V <sub>IH,CMOS</sub>       | CMOS input high voltage                     |                          | VDD33 – 0.4          |      |                          |      |
| t <sub>p,minCMOS</sub>     | Pulse width for detection                   |                          |                      | 5    |                          | ns   |
| I <sub>leak</sub>          | Input leakage current                       |                          | -10                  |      | 10                       | μA   |
| C <sub>in</sub>            | Input capacitance                           |                          |                      |      | 10                       | pF   |
| V <sub>OH</sub>            | High level output voltage                   | I <sub>out</sub> = 24 mA | 0.8 * VDD33          |      |                          | V    |
| V <sub>OL</sub>            | Low level output voltage                    | I <sub>out</sub> = 24 mA |                      |      | 0.4                      | V    |
| I <sub>LEAKTS</sub>        | Tri-state output leakage current            | V <sub>out</sub> = VDD33 | -10                  |      | 10                       | μA   |
| V <sub>ID</sub>            | Minimum differential input voltage          |                          | 100                  |      |                          | mV   |
| V <sub>hys</sub>           | Hysteresis                                  | LVDS<br>CMOS             | 40<br>0.2*AVDD<br>33 |      |                          | mV   |
| V <sub>ICM</sub>           | Common input voltage                        | GND2 = A2GND18           | V <sub>ID</sub> /2   | 1.25 | 2.4-V <sub>ID</sub> /2   | V    |
| t <sub>p,min</sub>         | Pulse width for detection                   |                          | 2                    |      |                          | ns   |
| Oscillator                 |                                             |                          |                      |      |                          |      |

<sup>3</sup> Recommended Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are explicitly denoted.

|                     |                              |                                           |    |    |                 |            |
|---------------------|------------------------------|-------------------------------------------|----|----|-----------------|------------|
| F <sub>OSC</sub>    | Oscillator Frequency         |                                           | 4  | 10 | 12.5            | MHz        |
| DC                  | Duty cycle                   |                                           | 40 |    | 60              | %          |
| I <sub>CC</sub>     | Current on V <sub>CC</sub>   | After initial startup                     |    |    | 0.9             | mA         |
| I <sub>DD</sub>     | Current on V <sub>DD</sub>   |                                           |    |    | 0.1             | mA         |
| T <sub>STUP</sub>   | Startup time                 | Settling at target frequency $\pm 0.01\%$ |    |    | 10              | ms         |
| R <sub>START</sub>  | Internal feedback resistance |                                           |    | 1  |                 | M $\Omega$ |
| Current Consumption |                              |                                           |    |    |                 |            |
|                     | Standby current              |                                           |    |    | 100             | $\mu$ A    |
|                     | Current after INIT           | No hits                                   |    |    |                 | mA         |
|                     | Measurement current          | 100 ksps                                  |    |    | 50 <sup>4</sup> | mA         |

<sup>4</sup> Simulated, to be confirmed.

## 5 Typical Characteristics

The following test levels apply to all following characteristics.

Table 4: Test levels

| Test Level | Description                                                                          |
|------------|--------------------------------------------------------------------------------------|
| I          | 100% production tested.                                                              |
| II         | 100% production tested at 25°C and guaranteed by design and characterization testing |
| III        | Parameter is guaranteed by design and characterization testing                       |
| IV         | Sample tested                                                                        |
| V          | Parameter is a typical value only.                                                   |

### 5.1 Converter Characteristics

General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T<sub>A</sub> = 0 °C to 80 °C.

Table 5: Characteristics

| Symbol                        | Description                                           | Conditions                                                                                              | TL  | Min     | Typ                 | Max            | Unit |
|-------------------------------|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------|-----|---------|---------------------|----------------|------|
| Accuracy of Time Measurements |                                                       |                                                                                                         |     |         |                     |                |      |
| RMS                           | Single-shot RMS resolution                            | -25 to +85° C<br>High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x)      | IV  |         | 30<br>25<br>20      | 45<br>37<br>30 | ps   |
| INL                           | Integral non-linearity                                |                                                                                                         | IV  |         |                     | 20             | ps   |
| DNL                           | Differential non-linearity                            |                                                                                                         | V   |         | 5                   |                | ps   |
|                               | No missing code                                       | At time quantization level                                                                              | III | Assured |                     |                |      |
|                               | Channel to channel isolation                          | At same times measured                                                                                  | IV  |         | 100                 | 200            | ps   |
|                               | Offset between START and STOP1                        |                                                                                                         | IV  |         | 500                 | 1000           | ps   |
|                               | Offset drift between START and STOP1                  |                                                                                                         |     |         | t.b.d.              |                | ps/K |
|                               | Offset error between STOP1 and STOP2                  | High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x)                       | V   |         | 100<br>150<br>200   |                | ps   |
|                               | Offset drift between STOP1 and STOP2 over temperature | High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x)                       | IV  |         | 0.5<br>1<br>1.5     | 3              | ps/K |
| P2P                           | Pulse-to-pulse spacing                                | High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x)<br>Channel_Chain = on |     |         | 15<br>30<br>45<br>3 |                | ns   |
| Switching Performance         |                                                       |                                                                                                         |     |         |                     |                |      |

|            |                             |                                                                                   |     |     |        |                |       |
|------------|-----------------------------|-----------------------------------------------------------------------------------|-----|-----|--------|----------------|-------|
| $t_{CONV}$ | Converter latency (INT set) | High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x) | III |     | t.b.d. |                | ns    |
|            | Peak conversion rate        | High_Resolution = 0 (off)<br>High_Resolution = 1 (2x)<br>High_Resolution = 2 (4x) | III |     |        | 50<br>20<br>10 | Msp/s |
|            | Maximum read-out rate       | SCK = 50MHz<br>Opcode + 48-Bit<br>Opcode + 16-Bit                                 | III | 0.9 |        | 2.1            | Msp/s |

## 5.2 SPI Timings

SPI slave timing values are described in the following table (the measurement points are done at  $0.2 \cdot V_{DD}$  and  $0.8 \cdot V_{DD}$ ):

Table 6: SPI characteristics

| Symbol        | Parameter                            | Min   | Max | Units |
|---------------|--------------------------------------|-------|-----|-------|
| $f_{sck}$     | Serial clock frequency               |       | 50  | MHz   |
| $t_{pwh,sck}$ | Serial clock pulse width HI state    | 10-5% |     | ns    |
| $t_{pwl,sck}$ | Serial clock pulse width LO state    | 10-5% |     | ns    |
| $t_{pwh,ssn}$ | SSN pulse width between write cycles | 20    |     | ns    |
| $t_{su,ssn}$  | SSN setup time before SCK rising     | 3     |     | ns    |
| $t_{hd,ssn}$  | SSN hold time after SCK rising       | 3     |     | ns    |
| $t_{su,mosi}$ | Data setup time prior to clock edge  | 2     |     | ns    |
| $t_{hd,mosi}$ | Data hold time after clock edge      | 2     |     | ns    |
| $t_{dv,mosi}$ | Data valid after falling clock edge  |       | 8   | ns    |
| $t_{zx,miso}$ | HighZ to output time                 |       | 8   | ns    |
| $t_{xz,miso}$ | Output to HighZ time                 |       | 8   | ns    |

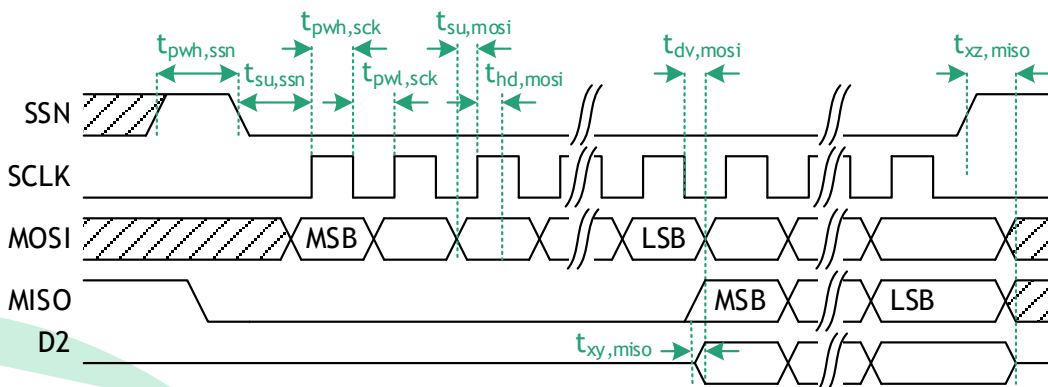


Figure 3: SPI Timings

## 6 Register Description

This section describes the registers of the LTDC-X3, which enable the host system to

- Configure the LTDC-X3 and set the operating mode
- Read back the timing information
- Read back STATUS information

### 6.1 Register Overview

*Table 7: Register Overview*

| Address      | Name                 | Access | Description                  |
|--------------|----------------------|--------|------------------------------|
| 0x00 to 0x0F | <b>CFG0 TO CFG15</b> | RW     | TDC configuration registers  |
| 0x11         | <b>WRN_LOCK</b>      |        | QSPI configuration registers |
| 0x12         | <b>ENC_SET</b>       |        |                              |
| 0x13         | <b>COM_SET</b>       |        |                              |
| 0x14         | <b>CH_CFG20</b>      |        |                              |
| 0x15 to 0x17 | <b>TOF_CH1</b>       |        | Result registers:            |
| 0x18 to 0x1A | <b>PW_CH1</b>        |        | Time of flight channel 1     |
| 0x1B to 0x1D | <b>TOF_CH2</b>       |        | Pulse width channel 1        |
| 0x1E to 0x20 | <b>PW_CH2</b>        |        | Time of flight channel 2     |
|              |                      |        | Pulse width channel          |
| 0x21         | <b>DEV_STATE</b>     |        | Reserved                     |
| 0x22         | <b>TDC_STAT_REG1</b> |        | TDC status                   |
| 0x23         | <b>TDC_STAT_REG2</b> |        |                              |
| 0x24         | <b>TDC_STAT_REG3</b> |        |                              |
| 0x25         | <b>TDC_STAT_REG4</b> |        |                              |
| 0x26 to 0x28 | <b>N.C.</b>          |        |                              |
| 0x2A to 0x2F | <b>ANALOG_CFGX</b>   |        | Analog configuration         |
| 0x30 to 0x33 | <b>CALIB_CFGX</b>    |        | Delay line calibration       |
|              | <b>TRIG_ID</b>       |        | Trigger configuration        |
|              | <b>TRIG_NOISE</b>    |        |                              |
|              | <b>TRIG_PERIOD</b>   |        |                              |
| 0x40 to 0x46 | <b>N.C.</b>          |        | Not used                     |

Note: register addresses that are not listed here are not used and set by default to 0.

## 6.2 Detailed Register Description

### 6.2.1 CFG0 (Address 0x00)

Table 8: Register CFG0

| Address 0x00 |                        | CFG0    |        |                                                                                                                                                                                                                                        |
|--------------|------------------------|---------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name             | Default | Access | Field Description                                                                                                                                                                                                                      |
| 7            |                        |         |        | reserved                                                                                                                                                                                                                               |
| 6            | <b>SSN_INIT_ENA</b>    | 0x00    | RW     | Selects source of re-initialization of the TDC:<br>0: SINGLE ACCESS, restart by opcode TDC_REINIT or pin REINIT<br>1: DMA AUTOMATIC ACCESS, SSN constantly at 0 during read-out, TDC is restarted automatically when SSN is high again |
| 5:4          | <b>HIGHRES</b>         | 0x00    | RW     | Settings for higher resolution<br>0: normal resolution<br>1: medium<br>2: high resolution                                                                                                                                              |
| 3            | <b>CHANNEL_COMBINE</b> | 0x00    | RW     | 0: Stop1 measured on one channel only<br>1: Stop1 measured on both stop channels alternately for halving pulse-to-pulse distance                                                                                                       |
| 2            |                        |         |        | Set 1. reserved                                                                                                                                                                                                                        |
| 1            | <b>HIT_ENA_STOP2</b>   | 0x00    | RW     | Software enable of Stop2 input                                                                                                                                                                                                         |
| 0            | <b>HIT_ENA_STOP1</b>   | 0x00    | RW     | Software enable of Stop1 input                                                                                                                                                                                                         |

### 6.2.2 CFG1 (Address 0x01)

Table 9: Register CFG1

| Address 0x01 |                    | CFG1    |        |                       |
|--------------|--------------------|---------|--------|-----------------------|
| Bits         | Field Name         | Default | Access | Field Description     |
| 7:6          |                    |         |        | reserved              |
| 5:3          | <b>HITBUFSIZE2</b> | 0x00    | RW     | Hit buffer size 1...8 |
| 2:0          | <b>HITBUFSIZE1</b> | 0x00    | RW     | Hit buffer size 1...8 |

### 6.2.3 CFG2 (Address 0x02)

Table 10: Register CFG2

| Address 0x02 |                | CFG2    |        |                                                                                                                                                                                                                                                                                          |
|--------------|----------------|---------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name     | Default | Access | Field Description                                                                                                                                                                                                                                                                        |
| 7:0          | <b>TIMEOUT</b> | 0x00    | RW     | 8-bit timeout counter which is synchronized to the start pulse (100 ns uncertainty) and used for timeout of TDC, ToF and conversion.<br>0: timeout generation off<br>1: period of the reference clock<br>2: periods of the reference clock<br>...<br>255: periods of the reference clock |

### 6.2.4 CFG3 (Address 0x03)

Table 11: Register CFG3

| Address 0x03 |                            | CFG3    |        |                                                    |
|--------------|----------------------------|---------|--------|----------------------------------------------------|
| Bits         | Field Name                 | Default | Access | Command                                            |
| 7:0          | <b>DELSTM_DLY</b><br>[7:0] | 0x00    | RW     | Delay for STOP mask. Counted in <b>DELTRIG_LSB</b> |

### 6.2.5 CFG4 (Address 0x04)

Table 12: Register CFG4

| Address 0x04 |                             | CFG4    |        |                                                    |
|--------------|-----------------------------|---------|--------|----------------------------------------------------|
| Bits         | Field Name                  | Default | Access | Command                                            |
| 7:4          |                             |         |        | reserved                                           |
| 3:0          | <b>DELSTM_DLY</b><br>[11:8] | 0x00    | RW     | Delay for STOP mask. Counted in <b>DELTRIG_LSB</b> |

## CFG5 to CFG7 (Address 0x05 to 0x07)

Table 13: Register CFG3

| Address 0x03 |                   | CFG5    |        |                                                                                              |
|--------------|-------------------|---------|--------|----------------------------------------------------------------------------------------------|
| Bits         | Field Name        | Default | Access | Command                                                                                      |
| 7:0          | REFCLKDIV [7:0]   | 0x00    | RW     | Low word. Defines the LSB at the output interface as fraction of the reference clock period  |
| Address 0x06 |                   | CFG6    |        |                                                                                              |
| 7:0          | REFCLKDIV [15:8]  | 0x00    | RW     | Mid word. Defines the LSB at the output interface as fraction of the reference clock period  |
| Address 0x07 |                   | CFG7    |        |                                                                                              |
| 7:0          | REFCLKDIV [23:16] | 0x00    | RW     | HIGH WORD. Defines the LSB at the output interface as fraction of the reference clock period |

## 6.2.6 CFG8 (Address 0x08)

Table 14: Register CFG8

| Address 0x08 |               | CFG8    |        |                                                                                                                                                                                                                                                                               |
|--------------|---------------|---------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name    | Default | Access | Command                                                                                                                                                                                                                                                                       |
| 7:6          | NOT USED      | 0x00    | RW     | Not used                                                                                                                                                                                                                                                                      |
| 5            | STOP_MASK_ENA | 0x00    | RW     | Enables noise mask or pin STOP_MASK for stop hits after hit on start input a configured time is wait, until the first stop hit is accepted<br>0: stops enabled<br>1: stops masked                                                                                             |
| 4            | STOP_MASK_EXT | 0x00    | RW     | Selects source of noise mask 0: by noise mask delay line 1: by noise mask pin                                                                                                                                                                                                 |
| 3:2          | DELSTM_LSB    | 0x00    | RW     | Length of LSB of stop mask as a fraction of the reference clock period:<br>0: $1/1024 * T_{ref}$ (e.g.0.097 ns @ 10 MHz)<br>1: $2/1024 * T_{ref}$ (e.g.0.195 ns @ 10 MHz)<br>2: $5/1024 * T_{ref}$ (e.g.0.488 ns @ 10 MHz)<br>3: $10/1024 * T_{ref}$ (e.g..0.976 ns @ 10 MHz) |
| 1:0          | DELTRIG_LSB   | 0x00    | RW     | Length of LSB of trigger delay as a fraction of the reference clock period. Same setting as DELSTM_LSB                                                                                                                                                                        |

### 6.2.7 CFG9 (Address 0x09)

Table 15: Register CFG9

| Address 0x09 |              | CFG9    |        |                                                                |
|--------------|--------------|---------|--------|----------------------------------------------------------------|
| Bits         | Field Name   | Default | Access | Command                                                        |
| 7:0          | TRIG_MAX_DEL | 0x00    | RW     | Maximum delay count for trigger output in units of DELTRIG_LSB |

### 6.2.8 CFG10 to14 (Address 0x0A to 0x0D)

Address 0x0A: 63 or 0x3F

Address 0x0B: 224 or E0

Address 0x0C: 101 or 0x65

Address 0x0D: 222 or 0xDE

Address 0x0A: 227 or 0xE3

### 6.2.9 CFG15 (Address 0x0F)

Table 16: Register CFGF3

| Address 0x0F |            | CFG15   |        |                    |
|--------------|------------|---------|--------|--------------------|
| Bits         | Field Name | Default | Access | Command            |
| 7:0          | NOT USED   |         |        | Reserved, set 0x27 |

### 6.2.10 WRN\_LOCK (Address 0x11)

Table 17: Register WRN\_LOCK

| Address 0x11 |            | WRN_LOCK |        |                                                                                                                |
|--------------|------------|----------|--------|----------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name | Default  | Access | Command                                                                                                        |
| 0            | WRN_LOCK   | 0x1      | RW     | Write lock/unlock register<br>0: Functional registers are not writable<br>1: Functional registers are writable |

### 6.2.11 COM\_SET (Address 0x13)

Table 18: Register COM\_SET

| Address 0x13 |             | COM_SET |        |                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------|-------------|---------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name  | Default | Access | Command                                                                                                                                                                                                                                                                                                                                                                                                    |
| 7:4          | DUMMY_CYCLE | 0x0     | RW     | Sets the number of dummy cycles inserted in the Dual SPI and Quad SPI communication. Values can range from 0 to up to 15 clock cycles 1 is typically recommended..                                                                                                                                                                                                                                         |
| 3:2          | TR_MODE     | 0x0     | RW     | Transfer mode for reading from hit buffer:<br>0: Default mode. The slave reads three bytes of TOF and three bytes of PWSTOP<br>1: In this mode, the least significant bytes of TOF and PWSTOP are discarded, this leads to an increase in transmission speed at the expense of measurement accuracy.<br>2: In this mode, only the TOF is read and the PWSTOP is discarded. It is the fastest reading mode. |
| 1            | EN_DUAL     | 0x0     | RW     | Enables dual mode for the QSPI interface                                                                                                                                                                                                                                                                                                                                                                   |
| 0            | EN_QUAD     | 0x0     | RW     | Enables quad mode for the QSPI interface                                                                                                                                                                                                                                                                                                                                                                   |

### 6.2.12 CH\_CFG20 (Address 0x14)

Table 19: Register CH\_CFG20

| Address 0x14 |            | CH_CFG20 |        |                                                                                                                                                                                                                                           |
|--------------|------------|----------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name | Default  | Access | Command                                                                                                                                                                                                                                   |
| 7            | MASK_OV    | 0x1      | RW     | Overflow time (0xFFFFFE) in TOF will also mask PW with 0xFFFFE                                                                                                                                                                            |
| 6:3          | BUFF_SIZE  | 0xf      | RW     | Set to 15                                                                                                                                                                                                                                 |
| 2:1          | CH_CFG     | 0x3      | RW     | Channel read out configuration<br>0: OFF<br>1: read channel 1 only<br>2: read channel 2 only<br>3: read channel 1 & 2 alternately                                                                                                         |
| 0            | ACCMODE    | 0x1      | RW     | Defines the access mode.<br>0: Single access. only one TOF and PWSTOP. Value is read at a time<br>1: Incremental access. In this mode, the QSPI slave refreshes the TDC data every time it has completed the reading of the previous one. |

### 6.2.13 TOF\_CH1\_H (Address 0x15)

Table 20: Register TOF\_CH1\_H

| Address 0x15 |                 | TOF_CH1_H |        |                                           |
|--------------|-----------------|-----------|--------|-------------------------------------------|
| Bits         | Field Name      | Default   | Access | Command                                   |
| 7:0          | TOF_CH1 [23:16] | 0x00      | RO     | TDC channel 1 time-of-flight data [23:16] |

### 6.2.14 TOF\_CH1\_M (Address 0x16)

Table 21: Register TOF\_CH1\_M

| Address 0x16 |                | TOF_CH1_M |        |                                          |
|--------------|----------------|-----------|--------|------------------------------------------|
| Bits         | Field Name     | Default   | Access | Command                                  |
| 7:0          | TOF_CH1 [15:8] | 0x00      | RO     | TDC channel 1 time-of-flight data [15:8] |

### 6.2.15 TOF\_CH1\_L (Address 0x17)

Table 22: Register TOF\_CH1\_L

| Address 0x17 |               | TOF_CH1_L |        |                                         |
|--------------|---------------|-----------|--------|-----------------------------------------|
| Bits         | Field Name    | Default   | Access | Command                                 |
| 7:0          | TOF_CH1 [7:0] | 0x00      | RO     | TDC channel 1 time-of-flight data [7:0] |

### 6.2.16 PW\_CH1\_H (Address 0x18)

Table 23: Register PW\_CH1\_H

| Address 0x18 |                | PW_CH1_H |        |                                        |
|--------------|----------------|----------|--------|----------------------------------------|
| Bits         | Field Name     | Default  | Access | Command                                |
| 7:0          | PW_CH1 [23:16] | 0x00     | RO     | TDC channel 1 pulse width data [23:16] |

### 6.2.17 PW\_CH1\_M (Address 0x19)

Table 24: Register PW\_CH1\_M

| Address 0x19 |               | PW_CH1_L |        |                                       |
|--------------|---------------|----------|--------|---------------------------------------|
| Bits         | Field Name    | Default  | Access | Command                               |
| 7:0          | PW_CH1 [15:8] | 0x00     | RO     | TDC channel 1 pulse width data [15:8] |

### 6.2.18 PW\_CH1\_L (Address 0x1A)

Table 25: Register PW\_CH1\_L

| Address 0x1A |              | PW_CH1_L |        |                                      |
|--------------|--------------|----------|--------|--------------------------------------|
| Bits         | Field Name   | Default  | Access | Command                              |
| 7:0          | PW_CH1 [7:0] | 0x00     | RO     | TDC channel 1 pulse width data [7:0] |

### 6.2.19 TOF\_CH2\_H (Address 0x1B)

Table 26: Register TOF\_CH2\_H

| Address 0x1B |                 | TOF_CH2_H |        |                                           |
|--------------|-----------------|-----------|--------|-------------------------------------------|
| Bits         | Field Name      | Default   | Access | Command                                   |
| 7:0          | TOF_CH2 [23:16] | 0x00      | RO     | TDC channel 2 time-of-flight data [23:16] |

### 6.2.20 TOF\_CH2\_M (Address 0x1C)

Table 27: Register TOF\_CH2\_M

| Address 0x1C |                | TOF_CH2_L |        |                                          |
|--------------|----------------|-----------|--------|------------------------------------------|
| Bits         | Field Name     | Default   | Access | Command                                  |
| 7:0          | TOF_CH2 [15:8] | 0x00      | RO     | TDC channel 2 time-of-flight data [15:8] |

#### 6.2.21 TOF\_CH2\_L (Address 0x1D)

Table 28: Register TOF\_CH2\_L

| Address 0x1D |              | TOF_CH2_L |        |                                         |
|--------------|--------------|-----------|--------|-----------------------------------------|
| Bits         | Field Name   | Default   | Access | Command                                 |
| 7:0          | TOF_C2 [7:0] | 0x00      | RO     | TDC channel 2 time-of-flight data [7:0] |

#### 6.2.22 PW\_CH2\_H (Address 0x1E)

Table 29: Register PW\_CH2\_H

| Address 0x1E |                | PW_CH2_H |        |                                        |
|--------------|----------------|----------|--------|----------------------------------------|
| Bits         | Field Name     | Default  | Access | Command                                |
| 7:0          | PW_CH2 [23:16] | 0x00     | RO     | TDC channel 2 pulse width data [23:16] |

#### 6.2.23 PW\_CH2\_M (Address 0x1F)

Table 30: Register PW\_CH2\_M

| Address 0x1F |               | PW_CH2_L |        |                                       |
|--------------|---------------|----------|--------|---------------------------------------|
| Bits         | Field Name    | Default  | Access | Command                               |
| 7:0          | PW_CH2 [15:8] | 0x00     | RO     | TDC channel 2 pulse width data [15:8] |

#### 6.2.24 PW\_CH2\_L (Address 0x20)

Table 31: Register PW\_CH2\_L

| Address 0x20 |              | PW_CH2_L |        |                                      |
|--------------|--------------|----------|--------|--------------------------------------|
| Bits         | Field Name   | Default  | Access | Command                              |
| 7:0          | PW_CH2 [7:0] | 0x00     | RO     | TDC channel 2 pulse width data [7:0] |

### 6.2.25 DEV\_STATE (Address 0x21)

Table 32: Register DEV\_STATE

| Address 0x21 |            | DEV_STATE |        |                                                                                                                                                    |
|--------------|------------|-----------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name | Default   | Access | Command                                                                                                                                            |
| 1:0          | DEV_STATE  | 0x00      | RO     | Device status bits<br>1: Power-on reset was released<br>2: Configuration registers need to be written<br>3: Calibration is done, start measurement |

### 6.2.26 TDC\_STAT\_REG1 (Address 0x22)

Table 33: Register TDC\_STAT\_REG1

| Address 0x22 |            | TDC_STAT_REG1 |        |                             |
|--------------|------------|---------------|--------|-----------------------------|
| Bits         | Field Name | Default       | Access | Command                     |
| 5            | EF_STO2_R  | 0x00          | RO     | Stop rise 2 FIFO flag empty |
| 4            | FF_STO2_R  | 0x00          | RO     | Stop rise 2 FIFO flag full  |
| 3            | EF_STO1_R  | 0x00          | RO     | Stop rise 1 FIFO flag empty |
| 2            | FF_STO1_R  | 0x00          | RO     | Stop rise 1 FIFO flag full  |
| 1            | EF_STA_R   | 0x00          | RO     | Start FIFO flag empty       |
| 0            | NOT USED   |               |        |                             |

### 6.2.27 TDC\_STAT\_REG2 (Address 0x23)

Table 34: Register TDC\_STAT\_REG2

| Address 0x23 |            | TDC_STAT_REG2 |        |                             |
|--------------|------------|---------------|--------|-----------------------------|
| Bits         | Field Name | Default       | Access | Command                     |
| 3            | EF_STO2_F  | 0x00          | RO     | Stop fall 2 FIFO flag empty |
| 2            | FF_STO2_F  | 0x00          | RO     | Stop fall 2 FIFO flag full  |
| 1            | EF_STO1_F  | 0x00          | RO     | Stop fall 1 FIFO flag empty |
| 0            | FF_STO1_F  | 0x00          | RO     | Stop fall 1 FIFO flag full  |

### 6.2.28 TDC\_STAT\_REG3 (Address 0x24)

Table 35: Register TDC\_STAT\_REG3

| Address 0x24 |             | TDC_STAT_REG3 |        |                                                |
|--------------|-------------|---------------|--------|------------------------------------------------|
| Bits         | Field Name  | Default       | Access | Command                                        |
| 6:4          | HITCNT_CH2R | 0x00          | RO     | Number of hits for rising edge in hit buffer 2 |
| 2:0          | HITCNT_CH1R | 0x00          | RO     | Number of hits for rising edge in hit buffer 1 |

### 6.2.29 TDC\_STAT\_REG4 (Address 0x25)

Table 36: Register TDC\_STAT\_REG4

| Address 0x25 |             | TDC_STAT_REG4 |        |                                                 |
|--------------|-------------|---------------|--------|-------------------------------------------------|
| Bits         | Field Name  | Default       | Access | Command                                         |
| 6:4          | HITCNT_CH2F | 0x00          | RO     | Number of hits for falling edge in hit buffer 2 |
| 2:0          | HITCNT_CH1F | 0x00          | RO     | Number of hits for falling edge in hit buffer 1 |

### 6.2.30 ANALOG\_CFG0 (Address 0x2A)

Table 37: Register ANALOG\_CFG0

| Address 0x2A |            | ANALOG_CFG0 |        |             |
|--------------|------------|-------------|--------|-------------|
| Bits         | Field Name | Default     | Access | Command     |
| 7:0          | DEFAULT    | 0xC0        | RW     | Use default |

### 6.2.31 ANALOG\_CFG1 (Address 0x2B)

Table 38: Register ANALOG\_CFG1

| Address 0x2B |            | ANALOG_CFG1 |        |             |
|--------------|------------|-------------|--------|-------------|
| Bits         | Field Name | Default     | Access | Command     |
| 7:0          | DEFAULT    | 0x04F       | RW     | Use default |

### 6.2.32 ANALOG\_CFG2 (Address 0x2C)

Table 39: Register ANALOG\_CFG2

| Address 0x2A |            | ANALOG_CFG0 |        |             |
|--------------|------------|-------------|--------|-------------|
| Bits         | Field Name | Default     | Access | Command     |
| 7:0          | DEFAULT    | 0x16        | RW     | Use default |

### 6.2.33 ANALOG\_CFG3 (Address 0x2D)

Table 40: Register ANALOG\_CFG3

| Address 0x2D |            | ANALOG_CFG3 |        |             |
|--------------|------------|-------------|--------|-------------|
| Bits         | Field Name | Default     | Access | Command     |
| 7:0          | DEFAULT    | 0x42        | RW     | Use default |

### 6.2.34 ANALOG\_CFG4 (Address 0x2E)

Table 41: Register ANALOG\_CFG4

| Address 0x2E |            | ANALOG_CFG4 |        |          |
|--------------|------------|-------------|--------|----------|
| Bits         | Field Name | Default     | Access | Command  |
| 7:0          | NOT_USED   | 0x00        | RW     | Not used |

### 6.2.35 ANALOG\_CFG5 (Address 0x2F)

Table 42: Register ANALOG\_CFG5

| Address 0x2F |                | ANALOG_CFG5 |        |                                       |
|--------------|----------------|-------------|--------|---------------------------------------|
| Bits         | Field Name     | Default     | Access | Command                               |
| 7            | CMOS_ENA_STOP2 | 0x00        | RW     | Enable CMOS threshold for STOP2 input |
| 6            | CMOS_ENA_STOP1 | 0x00        | RW     | Enable CMOS threshold for STOP1 input |
| 5            | CMOS_ENA_START | 0x00        | RW     | Enable CMOS threshold for START input |
| 4            | LVDS_ENA_STOP2 | 0x00        | RW     | Enable LVDS receiver STOP2            |
| 3            | LVDS_ENA_STOP1 | 0x00        | RW     | Enable LVDS receiver STOP1            |

|   |                |      |    |                                                 |
|---|----------------|------|----|-------------------------------------------------|
| 2 | LVDS_ENA_START | 0x00 | RW | Enable LVDS receiver START                      |
| 1 | OSC_ENA        | 0x00 | RW | Oscillator enable                               |
| 0 | IREF_ENA       | 0x00 | RW | Enable reference current source for LVDS, set 1 |

### 6.2.36 TRIG\_NOISE (Address 0x3CB)

Table 43: Register TRIG\_NOISE

| Address 0x3B |             | TRIG_NOISE |        |                                            |
|--------------|-------------|------------|--------|--------------------------------------------|
| Bits         | Field Name  | Default    | Access | Command                                    |
| 6:5          | TRIG_NOISE  | 0x00       | RW     | Defines the amplitude of the trigger noise |
| 4:1          | TRIG_LENGTH | 0x00       | RW     | Defines the length of the trigger pulse    |
| 0            | TRIG_ON     | 0x00       | RW     | 1: enables the trigger                     |

### 6.2.37 TRIG\_PERIOD (Address 0x3C)

Table 44: Register TRIG\_PERIOD

| Address 0x3C |             | TRIG_PERIOD |        |                                                                                                                                                                                                                                         |
|--------------|-------------|-------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bits         | Field Name  | Default     | Access | Command                                                                                                                                                                                                                                 |
| 7:0          | TRIG_PERIOD | 0x00        | RW     | 8-bit counter which defines the duration of trigger period in multiples of the reference clock period<br>0: off<br>1: one trigger pulse every reference clock period<br>...<br>255: one trigger pulse every 255 reference clock periods |

## 7 Detailed Description

LTDC-X3 is a high-speed, high-resolution TDC designed especially for LiDAR applications. It is based on TDC-GPX2 architecture with a continuously running core, but with a dedicated measurement sequence like a start-stop TDC, starting with the initialization, waiting for hits on the START and STOP inputs, and ending with the interrupt when all hits or a timeout have been detected. It calculates STOP - START time differences and the width of the STOP pulses directly on the chip. LVDS inputs enable an easy integration into fast analog front ends. The QSPI (quad SPI) interface allows high sample rate and data readout via a standard interface.

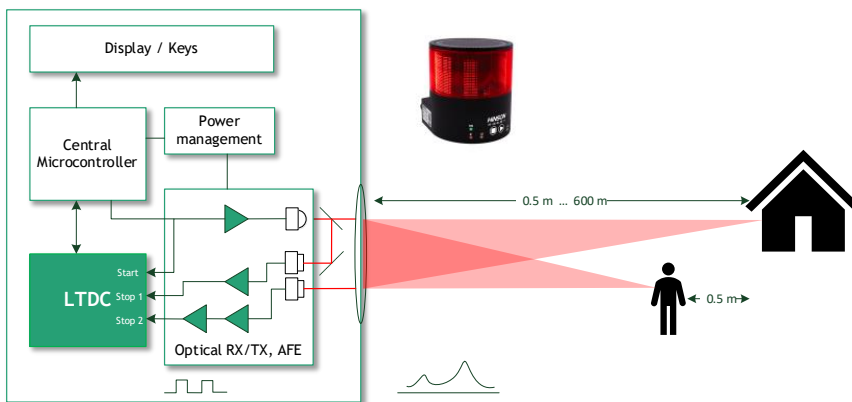


Figure 4: Application diagram

After configuration the chip will be initialized with the receipt of the SPI opcode TDC-INIT. The core is started and the TDC is ready to accept hits. The chip has a START input and two STOP inputs. It calculates the time differences between the STOP channels and the START channel. Time measurements are continuously calibrated against a reference clock which is generated from a 4 to 20 MHz quartz connected to the REFCLK pins. In typical LiDAR designs the START will be triggered by the laser trigger, STOP1 by the reference beam and STOP2 will be the main measurement channel. On both channels the chip measures rising and falling edge and therefore the time-of-flight and the pulse width for each hit.

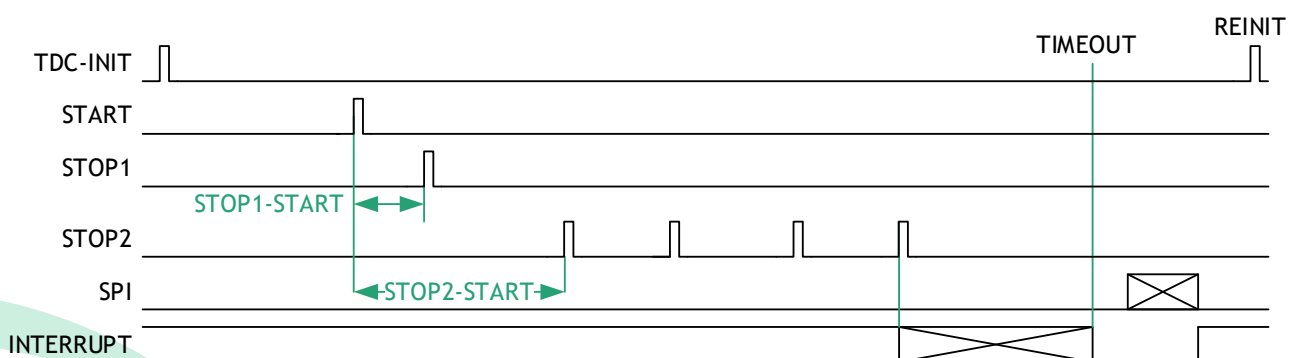


Figure 5: Measurement sequence

The number of expected hits can be configured, and as soon as those are receipt or a timeout occurred an interrupt is set and the external DSP can read the data. The measurement cycle is finished by an automatic or external (SPI or pin) re-initialization which arms the chip for the next measurement.

The reinitialization can be triggered by various sources:

- FIFOs are read: Interrupt and QSPI-SSN are back to high
- Pulse on pin REINIT at any time
- SPI command, resets in addition all internal averaging and calibration units

## 7.1 Input Structure for Time Measurement

The inputs for START, STOP1 and STOP2 are built with LVDS differential line receivers designed for applications requiring high data rates. They accept differential input signals and translate them to CMOS output levels. The 100Ohm differential input termination is not provided internally, therefore 500hm transmission lines and the external termination resistor are needed at pcb level.

The LVDS inputs can be used as single ended receivers to emulate CMOS inputs just connecting the negative input to VDD18 at pcb level. Switching thresholds will be about +/-50 mV around VDD18 without requiring a configuration bit.

The minimum pulse width for the input signals to pass these first comparators is typ. 2 ns for LVDS and 3 ns for CMOS. Shorter pulses might not set the output level high and the hits will be disappear and not trigger the next functional blocks.

### 7.1.1 START

The base value for START should be zero. The first rising edge on pin START after initialization acts as start time for the TDC measurement and the noise mask window. For operation, the pin has to be enabled. Following configuration bits are relevant:

*Table 45: START configuration*

| Register         | Bit | Parameter      | Description                                     |
|------------------|-----|----------------|-------------------------------------------------|
| 0x2E ANALOG_CFG5 | 5   | CMOS_ENA_START | 1: enables the CMOS threshold for the START     |
|                  | 2   | LVDS_ENA_START | 1: enables the LVDS START receiver              |
|                  | 0   | IREF_ENA       | 1: enables the reference in case of LVDS inputs |

### 7.1.2 STOP1, STOP2

The base value of the stop signal inputs should be zero and the stop pulses high active. The rising and falling edges of the stop signals are measured versus rising edge of the start pulse. The chip has two independent stop channels. With CHANNEL\_COMBINE variations of this normal operation mode can be achieved. For operation, the pins have to be enabled. Following configuration bits are relevant:

*Table 46: STOP configuration*

| Register | Bit | Parameter | Description |
|----------|-----|-----------|-------------|
|----------|-----|-----------|-------------|

|                         |   |                        |                                                                                         |
|-------------------------|---|------------------------|-----------------------------------------------------------------------------------------|
| 0x2E <b>ANALOG_CFG5</b> | 7 | <b>CMOS_ENA_STOP2</b>  | 1: Enables the CMOS threshold for the STOP2                                             |
|                         | 6 | <b>CMOS_ENA_STOP1</b>  | 1: Enables the CMOS threshold for the STOP1                                             |
|                         | 4 | <b>LVDS_ENA_STOP2</b>  | 1: Enables the LVDS STOP2 receiver                                                      |
|                         | 3 | <b>LVDS_ENA_STOP1</b>  | 1: Enables the LVDS STOP1 receiver                                                      |
|                         | 0 | <b>IREF_ENA</b>        | 1: Enables the reference in case of LVDS inputs                                         |
| 0x00 <b>CFG0</b>        | 3 | <b>CHANNEL_COMBINE</b> | 1: Stop1 measured on both stop channels alternately for halving pulse-to-pulse distance |
|                         | 2 |                        | Set 1. reserved                                                                         |
|                         | 1 | <b>HIT_ENA_STOP2</b>   | 1: Software enable of STOP2 input                                                       |
|                         | 0 | <b>HIT_ENA_STOP1</b>   | 1: Software enable of STOP1 input                                                       |

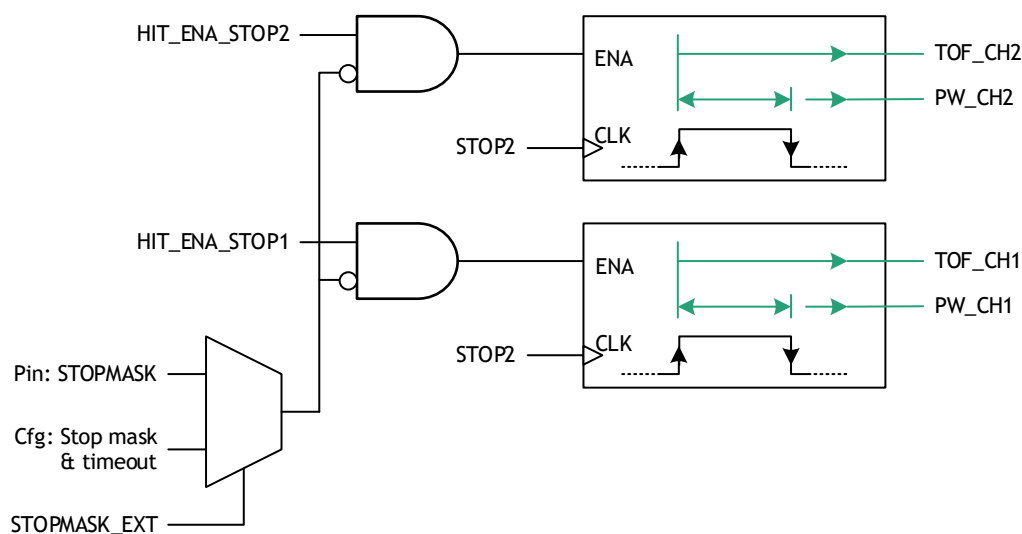


Figure 6: Stop inputs logic

#### 7.1.2.1 Channel Combination for Low Pulse-to-Pulse Spacing

With **CHANNEL\_COMBINE** = 3 the two stop channels 1 & 2 are connected to one input pin STOP1. The stop pulses at the input pin are distributed alternately between the combined channels.

The advantages of combining channels lie in

- Excellent pulse-to-pulse spacing
- Keeping excellent pulse width definition
- Doubled BUFFER depth for stop input pin

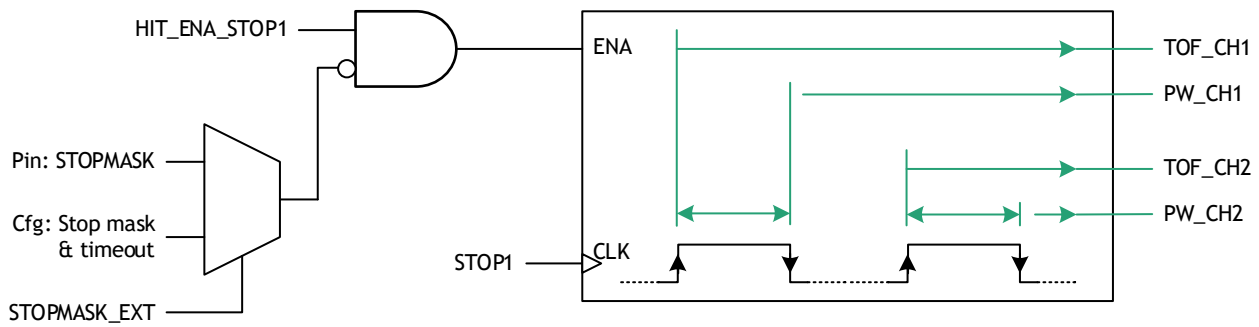


Figure 7: Channels 1 & 2 combined

### 7.1.3 STOPMASK

There is a dedicated CMOS input pin for a stop mask signal. With setting stop mask pin to HIGH the measurement is suppressed on both stops channels. With setting stop mask pin to LOW the measurement is enabled on both stop channels. The STOPMASK pin an alternative for internal stop mask window configured with **STOP\_MASK** and **TIMEOUT**.

Table 47: STOP MASK configuration

| Register         | Bit | Parameter            | Description                                                                                                                                                                       |
|------------------|-----|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x08 <b>CFG8</b> | 5   | <b>STOP_MASK_ENA</b> | Enables noise mask or pin STOP_MASK for stop hits after hit on start input a configured time is wait, until the first stop hit is accepted<br>0: stops enabled<br>1: stops masked |
|                  | 4   | <b>STOP_MASK_EXT</b> | Selects source of noise mask<br>0: by noise mask delay line<br>1: by noise mask pin                                                                                               |

### 7.1.4 REF\_OSC

The oscillator provides the master clock to the digital core. A biasing resistor is used to guarantee proper biasing points at DC. If lower value is needed an external resistor can be added.

Note: the oscillator is meant to deliver full performance in the primary operating range. In the “undervoltage” condition the oscillator will be functional but there could be a degradation of the performances.

The reference clock serves as universal time base. Due to internal averaging, the phase jitter of the reference clock is non-critical. The accuracy and drift of the reference clock will not affect the proper working of LTDC-X3 itself, but it will directly affect the time measurement results as they all are calibrated against the reference clock. It is possible to connect a quartz crystal or a ceramic resonator. But certainly, the selection will directly affect the quality of the time measurement results.

When the crystal driver is disabled, an external oscillator can be used for test purposes. The external clock shall be applied to the XTAL2 pin, while XTAL1 is tied to ground.

Table 48: Oscillator

| Register         | Bit | Parameter | Description           |
|------------------|-----|-----------|-----------------------|
| 0x2F ANALOG_CFG5 | 1   | OSC_ENA   | 1: Oscillator enabled |

## 7.2 Start-up Sequence

- Apply/send POR reset.
- Configure the chip, including reference oscillator enable.
- In case the trigger output is used: send tdc\_cal\_dly2\_tri and wait for 50 ms to calibrate the delay line.
- In case the noise mask is used: send tdc\_cal\_dly1\_stm and wait 50 ms for calibration.
- Start the measuring sequence by sending tdc\_init.
- The chip waits for synchronization of REFCLK
- The chip enables the TDC and waits 19 periods of the reference clock
- The chip enables the START channel

## 7.3 Time Measurements and Results

The reference clock is the framework for all time measurements. Internally, all events (START, rising and falling edges at STOPX) are measured against the reference clock. The TDC automatically calculates the time differences between STOP and START and calibrates those against the reference clock. Optionally, the pulse width can be calculated. The user reads the calibrated 24-bit results as TOF\_CHx and PW\_CHx, where PW could be the pulse width or the time for the falling edge.

- $t_{START}$  is the internal TDC measurement of a start pulse
- $t_{STOP}$  is the internal TDC measurement of a stop pulse
- $t_{REF}$  is the internal TDC measurement of the reference clock period to calibrate the results
- TOF\_CH1 is the time difference from START
- PW\_CH1 is the pulse width of the hit or the time difference to START for the falling edge

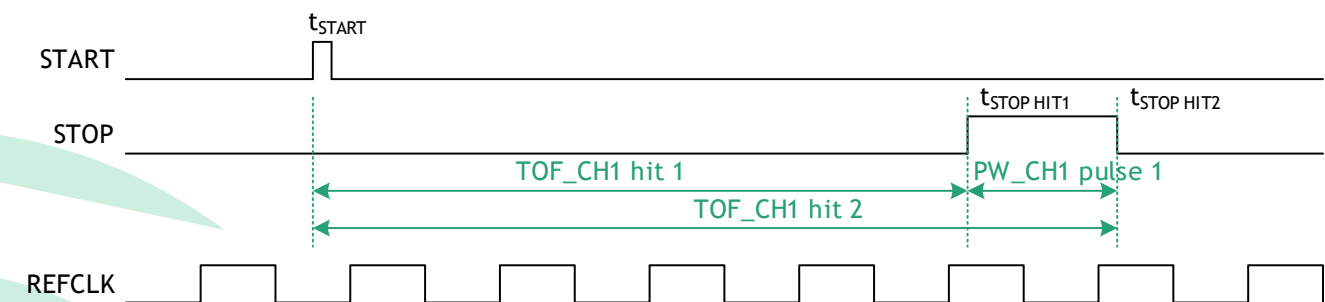


Figure 8: Time Measurement

### 7.3.1 Reinitialization

The LTDC-X3 needs to be re-initialized for each measurement. There are several options to do this:

- Initialization only when all data were read out of the hit buffer and the interrupt went back to high (SSN\_INIT\_EN = 1: EFLAG = 1, SSN="goes back to one" = "rising edge" ). This takes 5 cycles of the reference clock.
- Automatically on a rising edge on SSN pin, even if valid data are still in the buffer . This takes 5 cycles of the reference clock.
- Positive pulse on pin REINIT. This can be done any time and takes 5 cycles of the reference clock.
- Via SPI opcode TDC-REINIT, independent from hit buffer fill state, possible even during an active measuring sequence. This can be sent an time and takes 5 cycles of the reference clock.

### 7.3.2 Stop Mask

Besides the pin STOPMASK there is a digital delay line that can be used to mask stops internally. This stop masks begins with a valid START and releases the STOP input after the configured time interval. This helps to suppress noise or short range signals. The range can be configured from 0 to 255 ns in steps of 1ns.

During start-up delay line has to calibrate by sending opcode tdc\_cal\_dly1\_stm. Calibration should be repeated from time to time, especially if temperature varies. The following parameters are important for the configuration:

*Table 49: Stop mask*

| Register                             | Bit         | Parameter            | Description                                                                                                                                                                                |
|--------------------------------------|-------------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x03 <b>CFG3</b><br>0x04 <b>CFG4</b> | 7:0<br>11:8 | <b>DELSTM_DLY</b>    | Delay for STOP mask. Counted in <b>DELSTM_LSB</b> , 0 to 4095                                                                                                                              |
| 0x08 <b>CFG8</b>                     | 3:2         | <b>DELSTM_LSB</b>    | LSB as fraction of reference clock period<br>0: $1/1024 * T_{ref}$ (e.g. 100 ps @ 10 MHz)<br>1: $2/1024 * T_{ref}$<br>2: $5/1204 * T_{ref}$<br>3: $10/1024 * T_{ref}$ (e.g. 1 ns @ 10 MHz) |
|                                      | 5           | <b>STOP_MASK_ENA</b> | 1:= enable the STOP mask                                                                                                                                                                   |
|                                      | 4           | <b>STOP_MASK_EXT</b> | 0: source is an internal delay line<br>1: mask via STOPMASK pin.                                                                                                                           |

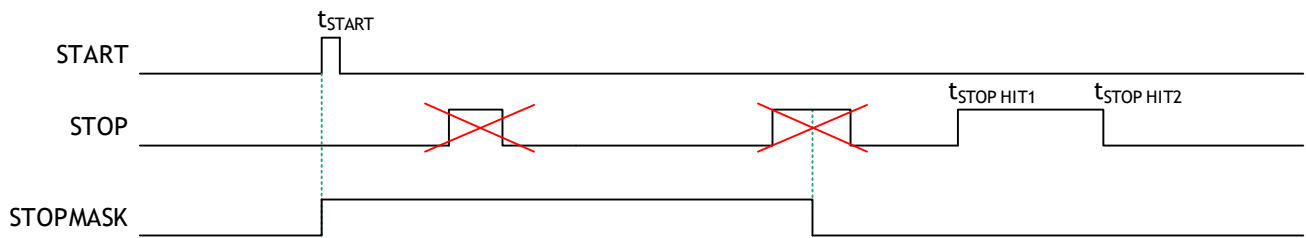


Figure 9: Stop Masking

### 7.3.3 Timeout

The timeout defines the measurement range by setting a time limit before which the set number of hits should have been arrived. If not enough hits are there the timeout sets the interrupt. Typically the limit is 2  $\mu$ s for 300m range. It is set in parameter **TIMEOUT**, register 2.

Table 50: Timeout

| Register         | Bit | Parameter      | Description                                                                                                                                                                  |
|------------------|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x02 <b>CFG2</b> | 7:0 | <b>TIMEOUT</b> | 8-Bit Timeout counter, synchronized to start.<br>0: timeout generation off<br>1: One period of the reference clock<br>...<br>255: maximum 255 periods of the reference clock |

The start of timeout counter is synchronized to start pulse. This means that there is an uncertainty in the timeout window of one period of the reference clock.

### 7.3.4 Interrupt

Each TDC measurement is stored in the internal hit buffer. The buffer size is configurable. A low level at the interrupt pin indicates to the external microcontroller that the measurement is done and valid data are available. This occurs either if the last accepted stop hit has filled the configured buffer space or when a timeout has occurred.

The interrupt is kept low until all data in the data buffer is read out. It is indicated via the interrupt pin.

### 7.3.5 High Resolution Mode

In high resolution mode the stop events are internally delayed and measured several times. The standard deviation is reduced by this method, but as a trade of the pulse-pair resolution is worse.

Table 51: High resolution mode

| Register         | Bit | Parameter      | Description                                                                                                                                                                                               |
|------------------|-----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00 <b>CFG0</b> | 5:4 | <b>HIGHRES</b> | Multiply the STOP hits internally for higher resolution<br>0: off standard resolution with minimum pulse-to-pulse spacing.<br>1: a stop event is measured twice<br>2: a stop event is measured four times |

### 7.3.6 TDC Result

The output result TSTOP is the ratio of the internal measured times of  $t_{STOP}$  over  $t_{REF}$  scaled by the configured REFCLKDIV. These measurements and calculations are done automatically inside of the chip. The read-out result is in multiple of the configured LSB. The LSB is given by the ratio of the reference clock period over the configured REFCLKDIV. The LSB at the output interface should be chosen lower than the single shot resolution of the LTDC-X3. Suitable values are e.g., 1 ps, 5 ps or 10 ps.

$$t_{STOP} = TOF\_CHx \times LSB = TOF\_CHx \times \frac{T_{refclk}[ps]}{REFCLKDIV}$$

or

$$TOF\_CHx = \frac{t_{STOP}}{T_{refclk}} \times REFCLKDIV$$

*Figure: Time Calculation*

### 7.3.7 Hit Buffer

Time measurement data are stored in two hit buffers, each with maximum 16 events. Per channel this means 8 time data and 8 pulse width data can be stored. The hit buffer size can be configured from 1 to 8. When the two channels are combined the buffer size reaches from 2 to 16.

*Table 52: Hit buffer configuration*

| Register         | Bit | Parameter          | Description                                     |
|------------------|-----|--------------------|-------------------------------------------------|
| 0x01 <b>CFG1</b> | 5:3 | <b>HITBUFSIZE2</b> | Number of hits allowed/expected in hit buffer 2 |
|                  | 2:0 | <b>HITBUFSIZE1</b> | Number of hits allowed/expected in hit buffer 1 |

The fill levels of the hit buffers are indicated in the status registers **TDC\_STSA\_REG1** to ...**REG3**.

- **EF\_STA\_R**            Empty flag for START channel with rising edge
- **EF\_STOx\_y**            Empty flag for channel x with slope y
- **FF\_STOx\_y**            Full flag for channel x with slope y
- **FCNT\_STOx\_y**    Hit counter for channel x with slope y

The content of the hit buffers is read from registers 0x15 to 0x20 which hold the values for

- **TOF\_CH1**            Time-of-flight channel 1 rising edge
- **PW\_CH1**            Pulse width channel 1 or second ToF channel 1
- **TOF\_CH2**            Time-of-flight channel 2 rising edge
- **PW\_CH2**            Pulse width channel 2 or second ToF channel 2

Those read registers are refilled from the hit buffer when a TOF & PW combination was read (FIFO principle). Reading can be done in single access mode or incremental mode. For a faster transfer it is further possible discard the LSB of TOF and PW data or to discard PW data at all. For details please see section 7.5.

## 7.4 Trigger Generation Module

The Start Generation Module is an independent module that provides a high configurable start signal which can be used to start the Lidar measurement. Frequency and pulse width are configurable. The signal is available on the TRIGGER pin.

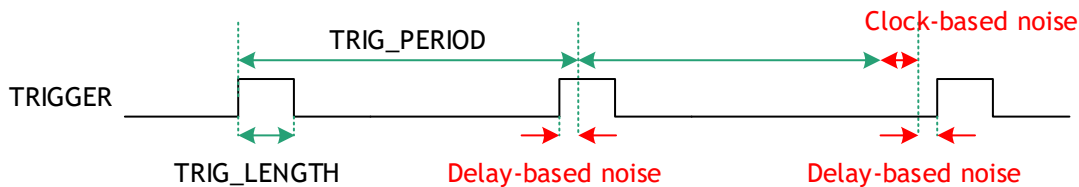


Figure 10: Trigger

The base frequency is given by the reference clock (typical 10MHz, maximum 20MHz). The period has to cover at least the maximum time measuring range of 4us.

A systematic sequence-delay (“Jitter-Sequence”) can be applied to distinguish between different LIDAR systems. Two methods can be used:

- Clock-based: noise is added to the trigger period before every shot and is set in steps of the reference clock period. The main idea is to decorrelate stops received from light sources transmitting on the same frequency. It is also a fallback option to delay-based noise.
- Delay-based: noise is added to the trigger which is based on an internal delay line. The delay can be set in configurable steps of nanoseconds on top of the trigger period and the digital noise. During start-up the delay line has to be calibrated by sending opcode tdc\_cal\_dly2\_tri. The calibration should be repeated from time to time, especially if temperature varies.

Table 53: Trigger configuration

| Register         | Bit | Parameter           | Description                                                                                                                                                                                                                   |
|------------------|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x01 <b>CFG1</b> | 5:3 | <b>TRIG_PERIOD</b>  | Defines the amplitude of trigger noise<br>0 to 7 periods of the reference clock                                                                                                                                               |
|                  | 2:1 | <b>TRIG_LENGTH</b>  | Defines seed of pseudo random sequence 0 to 255                                                                                                                                                                               |
|                  | 0   | <b>TRIG_ON</b>      | Turns on the trigger                                                                                                                                                                                                          |
| 0x08 <b>CFG8</b> | 1:0 | <b>DELTRIG_LSB</b>  | Length of LSB of trigger delay as a fraction of the reference clock period:<br>0: $1/1024 * T_{ref}$ (e.g.97 ps @ 10 MHz)<br>1: $2/1024 * T_{ref}$<br>2: $5/1204 * T_{ref}$<br>3: $10/1024 * T_{ref}$ (e.g.0.976 ns @ 10 MHz) |
| 0x09 <b>CFG9</b> | 7:0 | <b>TRIG_MAX_DEL</b> | Maximum delay count for trigger output in <b>DELTRIG_LSB</b>                                                                                                                                                                  |

## 7.5 QSPI Communication Interface

The QUAD-SPI interface is implemented to

- Reset the chip to power on state
- Write configuration registers
- Verify configuration or status registers
- Initialize and restart measurements
- Byte-wise readout of results from the read registers by standard SPI and quad SPI

The serial interface is compatible with the 4-wire SPI standard in Motorola specification:

- Clock Phase Bit = 0 Clock Polarity Bit = 0
- Clock Phase Bit = 1 Clock Polarity Bit = 1

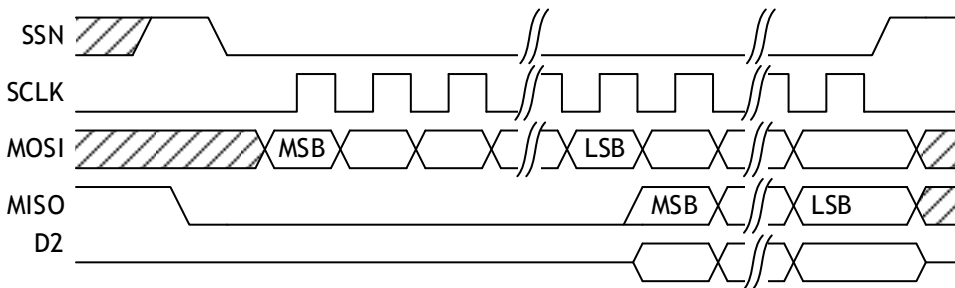


Figure 11: QSPI signals

Table 54: Opcode overview

| Opcode              | Hex  | Description                                                                          |
|---------------------|------|--------------------------------------------------------------------------------------|
| power_up            | 0x30 | Power on reset and stop measurement                                                  |
| init                | 0x18 | Initialize chip and start measurement                                                |
| tdc_reinit          | 0x19 | Re-initialize TDC and hit buffers, TDC waits for next hits afterwards                |
| tdc_stop            | 0x20 | Stops TDC measurement, helps to minimize configuration                               |
| tdc_cal_dly1_stm    | 0x21 | Calibration of delay line for stop mask                                              |
| tdc_cal_dly2_tri    | 0x22 | Calibration of delay line for trigger                                                |
| write_config_std    | 0x80 | Write Configuration register                                                         |
| read_short_sdr      | 0x60 | Read opcode result and configuration by short addressing in standard 4 wire mode     |
| read_24bit_sdr      | 0x61 | Read opcode result and configuration by 24 bit addressing in standard 4 wire mode    |
| read_short_ddr      | 0x62 | Read opcode result and configuration by 24 bit addressing in standard 4 wire mode    |
| read_24bit_ddr      | 0x63 | Read opcode for result and status register in DDR mode                               |
| quad_read_short_sdr | 0x6B | Read opcode for result and status register by quad SPI by 8 bit address in SDR mode  |
| quad_read_24bit_sdr | 0x6C | Read opcode for result and status register by quad SPI by 24 bit address in SDR mode |
| quad_read_short_ddr | 0x6D | Read opcode for result and status register by quad SPI by 8 bit address in DDR mode  |
| quad_read_24bit_ddr | 0x6E | Read opcode for result and status register by quad SPI by 24 bit address in DDR mode |

|                     |      |                                                                                           |
|---------------------|------|-------------------------------------------------------------------------------------------|
| dual_read_short     | 0x6F | Read opcode for result and status register by quad SPI by 8 bit address in SDR mode       |
| dual_read_24bit_sdr | 0x70 | Dual Read opcode for result and status register by dual SPI by 24 bit address in SDR mode |
| dual_read_short_ddr | 0x71 | Read opcode for result and status register by dual read SPI by 8 bit address in DDR mode  |
| dual_read_24bit_ddr | 0x72 | Read opcode for result and status register by dual read SPI by 8 bit address in DDR mode  |

### 7.5.1 Power-on Reset

After stabilization of all VDD33 and VDD18 the device expects the opcode power\_up = 0x30 to be sent via the SPI interface for power on reset. After the last bit of the opcode is sent the reset remains active until SSN goes high ( $t_{por}$ ).

After the reset the measurement stops and the configuration registers are set to internal defaults of the chip.

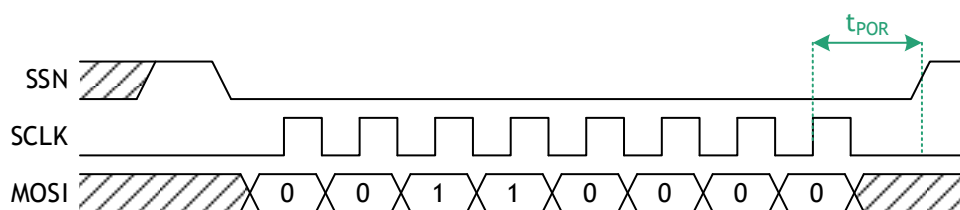


Figure 12: Opcode power\_up

### 7.5.2 Initialization Reset (soft reset)

After the configuration, the initialization opcode init (0x18) resets again the chip to power-on state, but preserves the configuration and starts the measurement. The initialization reset can be send any time while the reference clock is applied or a measurement is running. It takes 19 periods of the reference clock before the stop channels are opened internally.

### 7.5.3 TDC Re-initialization (hit buffer reset)

After the configuration or measurement, the TDC re-initialization opcode tdc\_reinit (0x19) re-initializes hit buffers. The TDC internal counters are not affected. After this command the TDC is ready to wait for the next hits. It takes 5 periods of the reference clock before the stop channels are opened internally.

### 7.5.4 TDC Stop

The opcode tdc\_stop (0x20) stops an ongoing measurement. The configuration registers can be updated partially or totally after receiving of this command.

Afterwards, the TDC is restarted by opcodes tdc\_reinit (0x19) or init (0x18).

### 7.5.5 Write / Incremental Write

Write access is permitted to the configuration registers exclusively. The access starts with the falling edge of SSN and sending the opcode write\_config\_std (0x80). The target register address just follows the opcode, followed then by the data. Incremental write access to the successive registers is possible by sending directly the next data bytes while SSN stays LOW. A complete configuration starts normally at register 0, followed by all register data bytes.

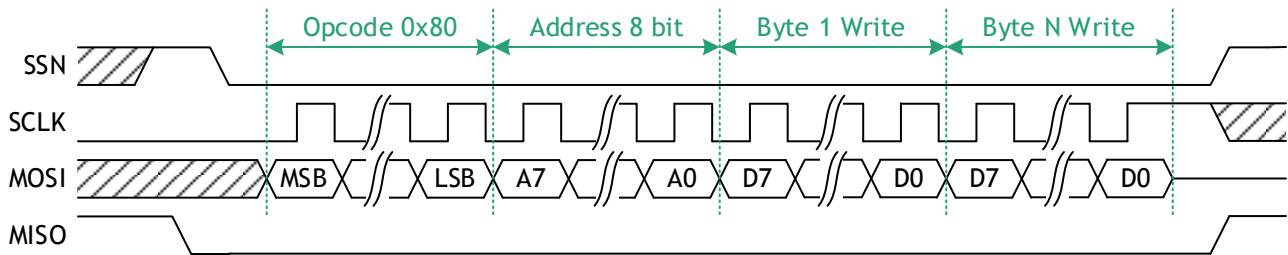


Figure 13: Opcode power\_up

### 7.5.6 Read / Incremental Read in STD & DDR

The read access to the registers starts with the falling edge of SSN followed by sending the opcodes

- read\_short\_sdr (0x60) for an 8-bit address, reading in standard mode, or
- read\_24bit\_sdr (0x61) for a 24-bit address, reading in standard mode, or
- read\_short\_ddr (0x62) for an 8-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock, or
- read\_24bit\_ddr (0x63) for a 24-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock.

The target register address just follows the opcode. Afterwards, the data are clocked out at the MISO line. Incremental read access to the subsequent registers is possible by continuously sending clock cycles. Each register is suitable as start address for an incremental access.

Note: DDR mode is fully usable with 20 MHz bus clock, but is limited in the usable combinations when having 50 MHz bus clock. With 50 MHz the following combinations are possible:

- Quad DDR for dual channel (6 bytes)
- Dual DDR 6,4-bytes transfer mode
- Single DDR

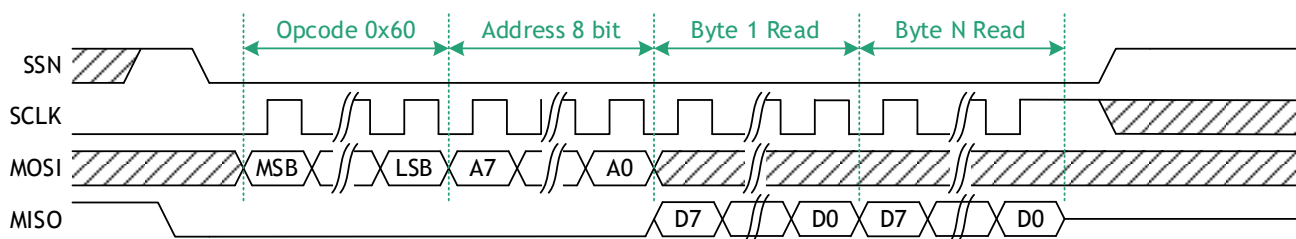


Figure 14: Read results/read incremental results at short address in STD mode

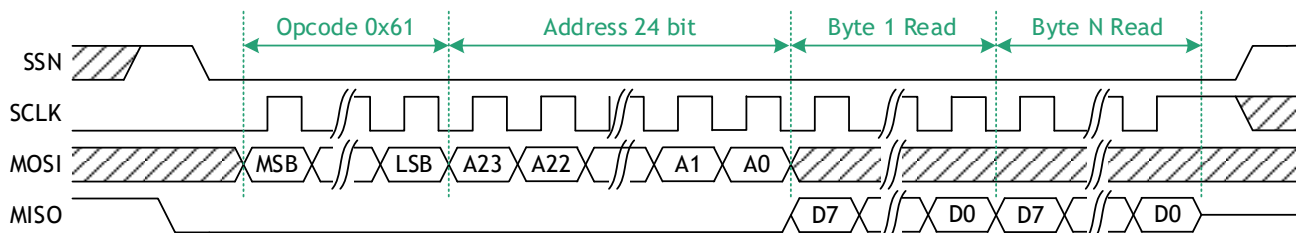


Figure 15: Read results/read incremental results at 24 bits address in STD mode

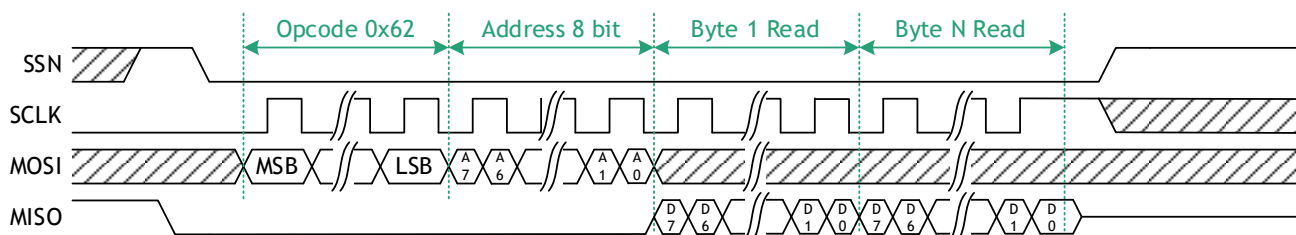


Figure 16: Read results/read incremental results at short address in DDR mode

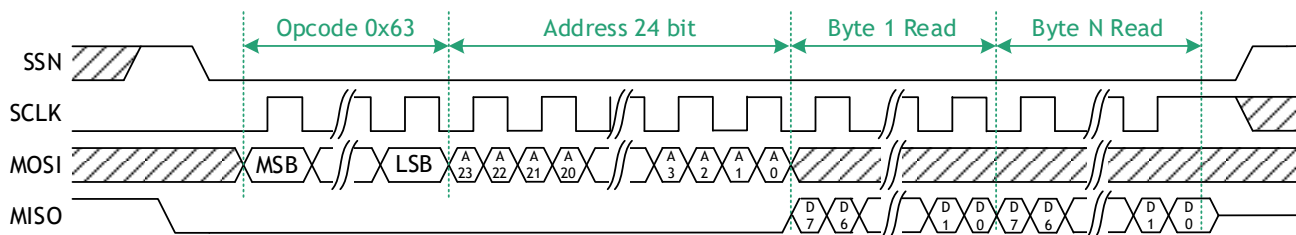


Figure 17: Read results/read incremental results at 24 bits address in DDR mode

### 7.5.7 Quad Read

The QSPI interface allows a quad mode in which address and data are transmitted via 4 data lines. This needs to be enabled by setting parameter EN\_QUAD = 1 in register COM\_SET (0x13). Otherwise, quad-mode-related opcodes are skipped.

The quad read access to the registers starts with setting SSN LOW and sending one of the opcodes

- quad\_read\_short\_sdr (0x6B) for an 8-bit address, reading in standard mode, or
- quad\_read\_24bit\_sdr (0x6C) for a 24-bit address, reading in standard mode, or
- quad\_read\_short\_ddr (0x6D) for an 8-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock, or

- quad\_read\_24bit\_ddr (0x6E) for an 24-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock.

The target register address just follows the opcode. Afterwards, the data are at the lines D0\_MOSI, D1\_MISO, D2 and D3. Incremental read access to the subsequent registers is possible by continuously sending clock cycles. Each register is suitable as start address for an incremental access.

Address bits A23 to A7 are discarded during the read decoding when short addressing is selected (8 bit address instead of 24 bit address).

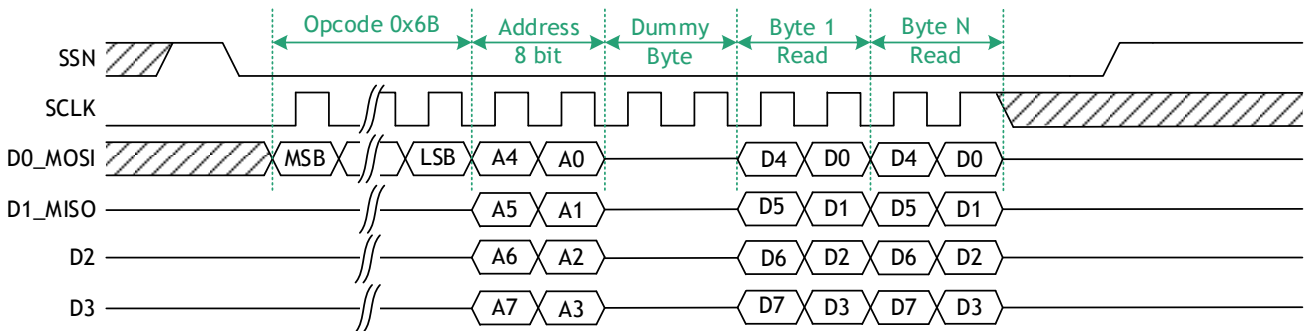


Figure 18: Quad read short address in SDR mode

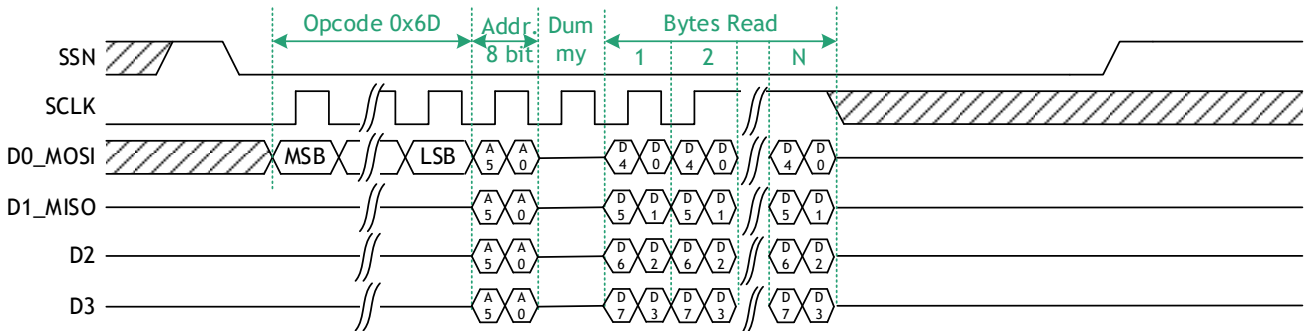


Figure 19: Quad read short address in DDR mode

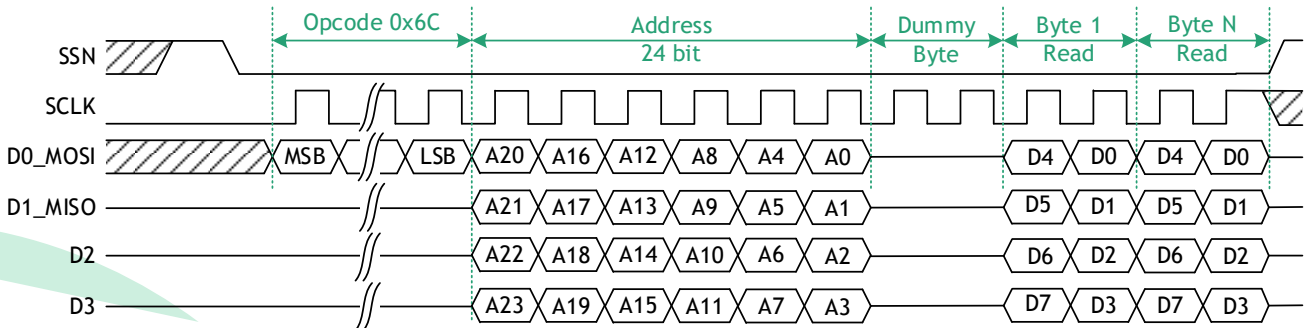


Figure 20: Quad read 24 bit address in SDR mode

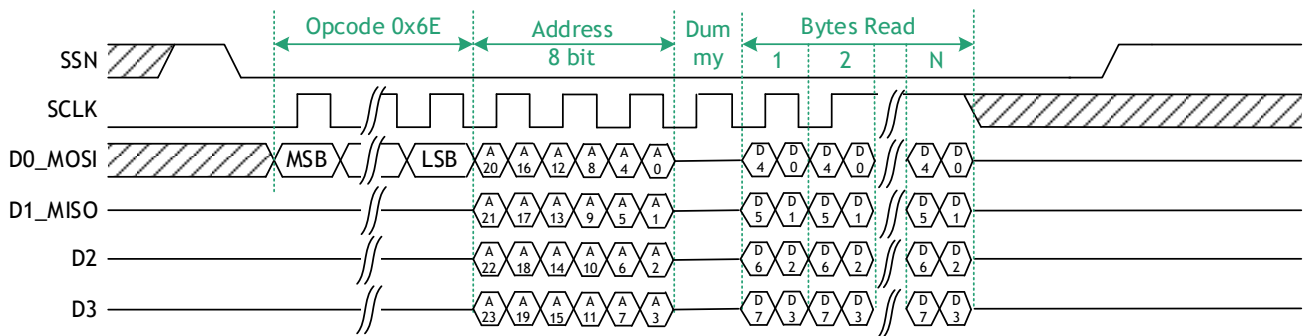


Figure 21: Quad read 24 bit address in DDR mode

## 7.5.8 Dual Read

The QSPI interface allows a dual mode in which address and data are transmitted via 2 data lines. This needs to be enabled by setting parameter EN\_DUAL = 1 in register COM\_SET (0x13). Otherwise, quad-mode-related opcodes are skipped.

The quad read access to the registers starts with setting SSN LOW and sending one of the opcodes

- dual\_read\_short\_sdr (0x6F) for an 8-bit address, reading in standard mode, or
- dual\_read\_24bit\_sdr (0x70) for a 24-bit address, reading in standard mode, or
- dual\_read\_short\_ddr (0x71) for an 8-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock, or
- dual\_read\_24bit\_ddr (0x72) for an 24-bit address, reading in double data read mode, reading with both, rising and falling edge of the clock.

The target register address just follows the opcode. Afterwards, the data are at the lines D0\_MOSI, and D1\_MISO. Incremental read access to the subsequent registers is possible by continuously sending clock cycles. Each register is suitable as start address for an incremental access.

Address bits A23 to A7 is discarded during the read decoding when short addressing is selected (8 bit address instead of 24 bit address).

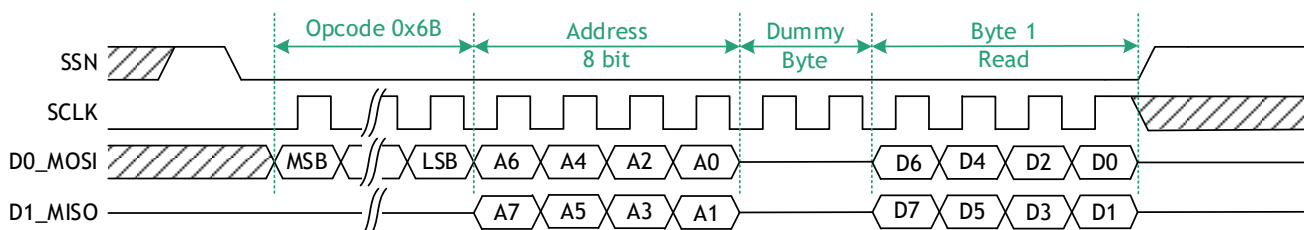


Figure 22: Dual read short address in SDR mode

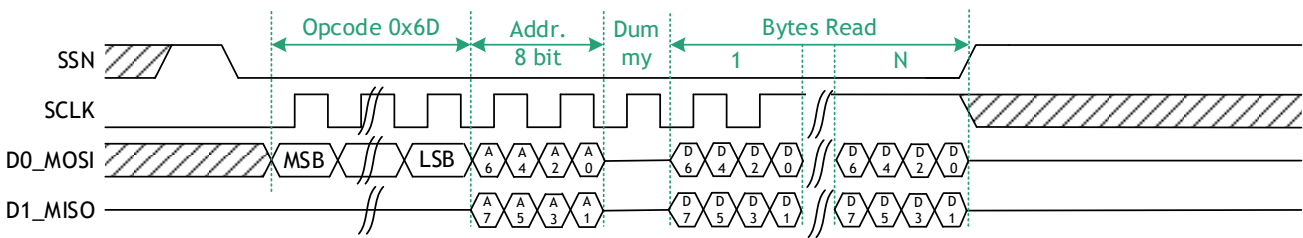


Figure 23: Dual read short address in DDR mode

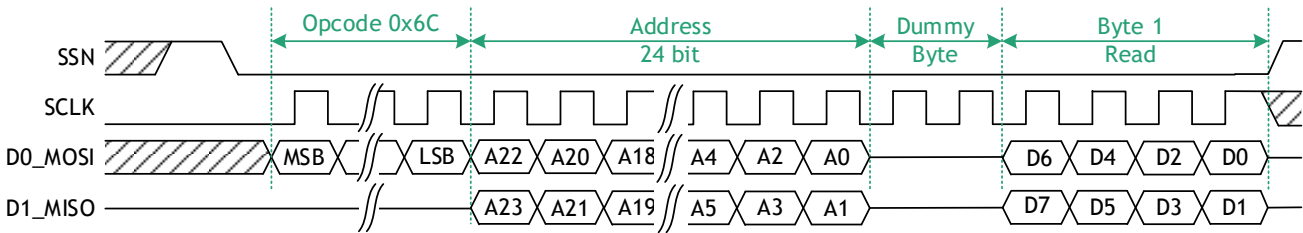


Figure 24: Dual read 24-bit address in SDR mode

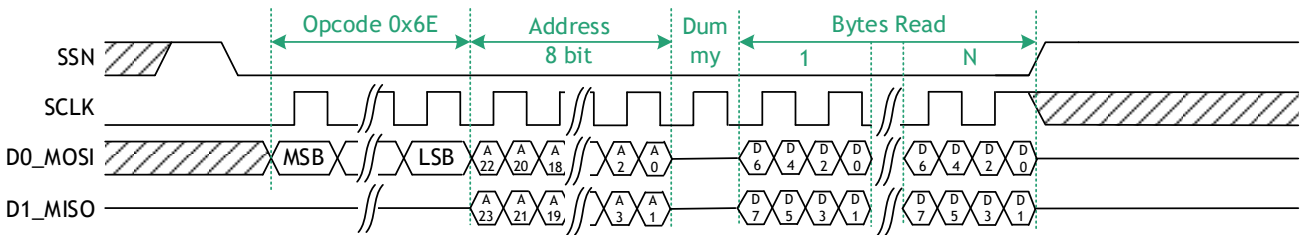


Figure 25: Dual read 24-bit address in DDR mode

### 7.5.9 QSPI Transfer & Measure Rates

The QSPI data rate depends on the SPI mode and read mode as well as the number of data read. The total measure rate is finally defined by the whole measure sequence and depends on multiple variables like

- Time-of-flight (maximum distance), Number of receive hits, Transfer mode (Read pulse width or not, read 2 or 3 bytes), Read status or not

The following table shows some possible scenarios. The maximum measure rate may vary from 100 kps to 500 kps.

*Table 55: QSPI transfer rates SDR, 5 MHz reference, 100m distance*

| S/D | #Dx    | Init ns | Dist m | ToF ns | INTN ns | fspi MHz | Transfer mode | Hits on Ch 1 | Hits on Ch 2 | Status | Measure rate kpsps |  |  |   |   |   |    |     |
|-----|--------|---------|--------|--------|---------|----------|---------------|--------------|--------------|--------|--------------------|--|--|---|---|---|----|-----|
| SDR | Single | 1000    | 100    | 660    | 100     | 50       | 0 (6 bytes)   | 1            | 0            | 0      | 329                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 1 (4 bytes)   |              |              |        | 368                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 2 (3 bytes)   |              |              |        | 391                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 0             |              | 1            |        | 250                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 1             |              |              |        | 298                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 2             |              |              |        | 329                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 0             | 0            | 0            |        | 455                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 1             |              |              |        | 472                |  |  |   |   |   |    |     |
|     |        |         |        |        |         |          | 2             |              |              |        | 481                |  |  |   |   |   |    |     |
|     | Quad   |         |        |        |         |          | Single        |              |              |        |                    |  |  | 4 | 4 | 1 | 95 |     |
|     |        |         |        |        |         |          |               |              |              |        |                    |  |  |   |   |   | 1  | 125 |
|     |        |         |        |        |         |          |               |              |              |        |                    |  |  |   |   |   | 2  | 149 |
|     |        |         |        |        |         |          | Quad          |              |              |        |                    |  |  |   |   |   | 0  | 219 |
|     |        |         |        |        |         |          |               |              |              |        |                    |  |  |   |   |   | 1  | 255 |
|     |        |         |        |        |         |          |               |              |              |        |                    |  |  |   |   |   | 2  | 278 |
|     |        |         |        |        |         |          |               |              |              |        |                    |  |  |   |   |   |    |     |

*Table 56: QSPI transfer rates SDR, 10 MHz reference, 10m distance*

| S/D | #Dx    | Init ns | Dist. m | ToF ns | INTN ns | fspi MHz | Transfer mode | Hits on Ch 1 | Hits on Ch 2 | Status | Measure rate kps |
|-----|--------|---------|---------|--------|---------|----------|---------------|--------------|--------------|--------|------------------|
| SDR | Single | 400     | 10      | 66     | 100     | 50       | 1 (4 bytes)   | 1            | 0            | 0      | 655              |
|     |        |         |         |        |         |          |               |              |              | 1      | 499              |
|     | Quad   |         |         |        |         |          |               |              |              | 0      | 1080             |
|     |        |         |         |        |         |          |               |              |              | 1      | 778              |

Table 57: QSPI transfer rates DDR, 5 MHz reference, 100m distance

| S/D | #Dx    | Init<br>ns | Dist.<br>m | ToF<br>ns | INTN<br>ns | fspi<br>MHz | Transfer<br>mode | Hits on<br>Ch 1 | Hits on<br>Ch 2 | Status | Measure<br>rate<br>ksp/s |
|-----|--------|------------|------------|-----------|------------|-------------|------------------|-----------------|-----------------|--------|--------------------------|
| DDR | Single | 1000       | 100        | 660       | 100        | 50          | 0 (6 bytes)      | 1               | 1               | 1      | 291                      |
|     |        |            |            |           |            |             |                  | 4               | 4               |        | 158                      |
|     |        |            |            |           |            |             | 2 (3 bytes)      |                 |                 |        | 227                      |
|     | Quad   |            |            |           |            |             | 1 (4 bytes)      | 1               | 1               | 0      | 495                      |
|     |        |            |            |           |            |             |                  | 4               | 4               | 1      | 410                      |
|     |        |            |            |           |            |             |                  |                 |                 |        | 410                      |

### 7.5.10 QSPI Configuration

The following parameters are relevant for the configuration of the quad SPI interface.

Table 58: QSPI configuration

| Register      | Bit | Parameter   | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|-----|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11 WRN_LOCK | 0   | WRN_LOCK    | Write no lock register                                                                                                                                                                                                                                                                                                                                                                                     |
| 0x13 COM_SET  | 0   | DUMMY_CYCLE | Sets the number of dummy cycles present in the Dual SPI and Quad SPI communication. Values can range from 0 to up to 15 clock cycles.                                                                                                                                                                                                                                                                      |
|               | 3:2 | TR_MODE     | Transfer mode for reading from hit buffer:<br>0: Default mode. The slave reads three bytes of TOF and three bytes of PWSTOP<br>1: In this mode, the least significant bytes of TOF and PWSTOP are discarded, this leads to an increase in transmission speed at the expense of measurement accuracy.<br>2: In this mode, only the TOF is read and the PWSTOP is discarded. It is the fastest reading mode. |
|               | 1   | EN_DUAL     | Enables dual mode for the QSPI interface                                                                                                                                                                                                                                                                                                                                                                   |
|               | 0   | EN_QUAD     | Enables quad mode for the QSPI interface                                                                                                                                                                                                                                                                                                                                                                   |
| 0x14 CH_CFG   | 6:3 | BUFF_SIZE   | TDC FIFO buffer size, define numbers of TOF and PWSTOP samples transmitted during the access: Samples = buff_size + 1 the default means no limitation                                                                                                                                                                                                                                                      |
|               | 2:1 | CH_CFG      | Channel read out configuration<br>0: OFF<br>1: read channel 1 only                                                                                                                                                                                                                                                                                                                                         |

|  |   |                |                                                                                                                                                                                                                                    |
|--|---|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |   |                | 2: read channel 2 only<br>3: read channel 1 & 2 alternately                                                                                                                                                                        |
|  | 0 | <b>ACCMODE</b> | Defines the access mode.<br>0: Single access. Each read is for one TOF and PWSTOP only.<br>1: Incremental access. In this mode, the QSPI slave refreshes the TDC data every time it has completed the reading of the previous one. |

## 7.6 QSPI Read Access during TDC Measurement

### 7.6.1 Read Sequence with `tr_mode[1:0] = 0x0`

In this mode the user reads 3 bytes time-of-flight and 3 bytes pulse width per hit.

#### 1) Single event access

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFFFFF.

Note: Access order to 0x15 and 0x1b might be mixed on channel 1 and channel2.

LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR +3Bytes +SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR +3Bytes)
- Read Width of pulse#1 of STOP-Channel1 (+3Bytes +SSN=1)
- Read TOF of pulse#2 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR +3Bytes)
- Read Width of pulse#2 of STOP-Channel1 (+3Bytes +SSN=1)
- Read TOF of pulse#1 of STOP-Channel2 on 0x1b (SSN=0 +OPCODE+ADDR +3Bytes)
- Read Width of pulse#1 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TOF of pulse#2 of STOP-Channel2 on 0x1b (SSN=0 +OPCODE+ADDR +3Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

#### 2) Incremental DMA access of Stop-CH1 and Ch2

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFFFFF

Note: In this example, HIT\_BUFFER\_SIZE is configured to 3, further readings are marked with 0xFFFFFFFF

LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR +3Bytes+SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR +3Bytes)
- Read Width of pulse#1 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#1 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#1 of STOP-Channel2 (+3Bytes)
- Read TOF of pulse#2 of STOP-Channel1 (+3Bytes)
- Read Width of pulse#2 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#2 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+3Bytes)
- Read TOF of pulse#3 of STOP-Channel1 (+3Bytes)
- Read Width of pulse#3 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#3 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#3 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

### 3) Incremental DMA access with combined stop-channels 1&2 with a single access

Reason: Stops at pin STOP1 are send alternating to stop-channel1 and stop-channel2 to get higher pulse-pair resolution

Note: In this example, HIT\_BUFFER\_SIZE is configured to 2.

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFF.

Note: To speed up read-out it shall be possible to omit reading of pulse width.

#### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR+3Bytes+SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+3Bytes)
- Read Width of pulse#1 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#2 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+3Bytes)
- Read TOF of pulse#3 of STOP-Channel1 (+3Bytes)
- Read Width of pulse#3 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#4 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#4 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

## 7.6.2 Read Sequence with tr\_mode[1:0] = 0x1

Read 2 bytes of TOF and pulse width only. Least significant bytes will be ignored.

### 1. Single event access

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFF.

Access order to 0x15 and 0x1b might mixed on channel 1 and channel2.

#### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR+3Bytes+SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+2Bytes+SSN=1)
- Read TOF of pulse#2 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+2Bytes+SSN=1)
- Read TOF of pulse#1 of STOP-Channel2 on 0x1b (SSN=0 +OPCODE+ADDR+2Bytes+SSN=1)
- Read TOF of pulse#2 of STOP-Channel2 on 0x1b (SSN=0 +OPCODE+ADDR+2Bytes+SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

### 2. Incremental DMA access of Stop-CH1 and Ch2 with separated SPI commands

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFF.

Note: In this example, HIT\_BUFFER\_SIZE is configured to 2.

#### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR+3Bytes +SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+2Bytes)
- Read TOF of pulse#1 of STOP-Channel2 (+2Byte)
- Read TOF of pulse#2 of STOP-Channel1 (+2Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+2Bytes +SSN=1)

- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

### 3. Incremental DMA access with combined stop-channels 1&2 with a single access

Reason: Stops at pin STOP1 are send alternating to stop-channel1 and stop-channel2 to get higher pulse resolution

Note: In this example, HIT\_BUFFER\_SIZE is configured to 2.

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFF.

#### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR +3Bytes +SSN=1)
- Read TOF of pulse#1 on STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR +2Bytes)
- Read TOF of pulse#2 on STOP-Channel2 (+2Bytes)
- Read TOF of pulse#3 on STOP-Channel1 (+2Bytes)
- Read TOF of pulse#4 on STOP-Channel2 (+2Bytes)
- Read TOF of pulse#5 on STOP-Channel1 (+2Bytes)
- Read TOF of pulse#6 on STOP-Channel2 (+2Bytes)
- Read TOF of pulse#7 on STOP-Channel1 (+2Bytes)
- Read TOF of pulse#8 on STOP-Channel2 (+2Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

### 7.6.3 Read Sequence with tr\_mode[1:0] = 0x2

Read 3 bytes of TOF, no pulse width data.

#### 1. Single event access

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFF.

Note: Access order to 0x15 and 0x1b might mixed (=two decoder).

#### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR +3Bytes +SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0+OPCODE+ADDR +3Bytes)
- Read Width of pulse#1 of STOP-Channel1 (+3Bytes +SSN=1)
- Read TOF of pulse#2 of STOP-Channel1 on 0x15 (SSN=0+OPCODE+ADDR+3Bytes)
- Read Width of pulse#2 of STOP-Channel1 (+3Bytes +SSN=1)
- Read TOF of pulse#1 of STOP-Channel2 on 0x1b (SSN=0+OPCODE+ADDR+3Bytes)
- Read Width of pulse#1 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TOF of pulse#2 of STOP-Channel2 on 0x1b (SSN=0+OPCODE+ADDR+3Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

## 2. Incremental DMA access of Stop-CH1 and Ch2 with separated SPI commands

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFFFFF.

Note: In this example, HIT\_BUFFER\_SIZE is configured to 2.

### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR+3Bytes+SSN=1)
- Read TOF of pulse#1 of STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+3Bytes)
- Read Width of pulse#1 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#1 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#1 of STOP-Channel2 (+3Bytes)
- Read TOF of pulse#2 of STOP-Channel1 (+3Bytes)
- Read Width of pulse#2 of STOP-Channel1 (+3Bytes)
- Read TOF of pulse#2 of STOP-Channel2 (+3Bytes)
- Read Width of pulse#2 of STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)

## 3. Incremental DMA access with combined stop-channel1&2 with a single access

Reason: Stops at pin STOP1 are send alternating to stop-channel1 and stop-channel2 to get higher pulse resolution

Note: In this example, HIT\_BUFFER\_SIZE is configured to 2.

Note: reading of status is optional, missing stop pulses are marked with 0xFFFFFFFF.

### LOOP:

- Wait for Interrupt
- Read Status (optional) (SSN=0 +OPCODE+ADDR+3Bytes +SSN=1)
- Read TOF of pulse#1 on STOP-Channel1 on 0x15 (SSN=0 +OPCODE+ADDR+2Bytes)
- Read Width of pulse#1 on STOP-Channel1 (+3Bytes)
- Read TOF of pulse#2 on STOP-Channel2 (+3Bytes)
- Read Width of pulse#2 on STOP-Channel2 (+3Bytes)
- Read TOF of pulse#3 on STOP-Channel1 (+3Bytes)
- Read Width of pulse#3 on STOP-Channel1 (+3Bytes)
- Read TOF of pulse#4 on STOP-Channel2 (+3Bytes)
- Read Width of pulse#4 on STOP-Channel2 (+3Bytes +SSN=1)
- Read TDC\_STAT\_REGF on 0x22 (SSN=0 +OPCODE+ADDR +4Bytes)
- REINIT done by REINIT pin or SPI REINIT command (ssn\_init\_ena=0)



## 9 Soldering information

The ENS160 uses an open LGA package. This package can be soldered using a standard reflow process in accordance with IPC/JEDEC J-STD-020D (Figure 26).

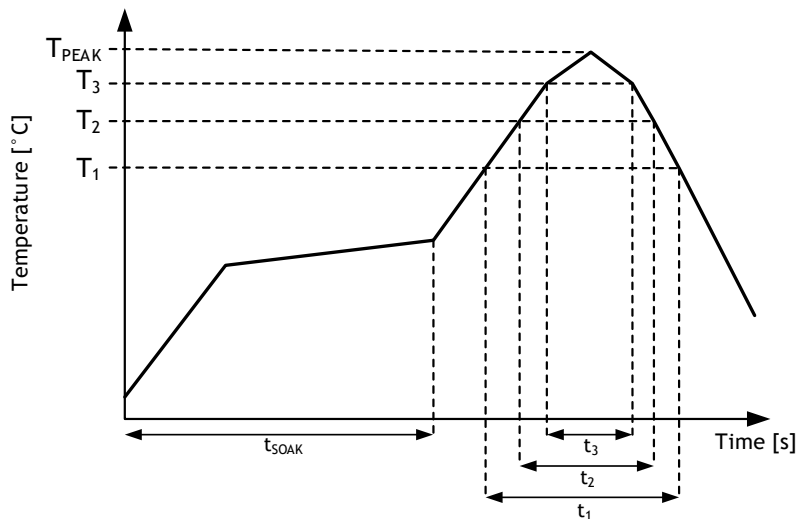


Figure 26: Solder reflow profile graph

The detailed settings for the reflow profile are shown in Table 59.

Table 59: Solder Reflow Profile

| Parameter                                  | Reference  | Rate / Unit |
|--------------------------------------------|------------|-------------|
| Average temperature gradient in preheating |            | 2.5 K/s     |
| Soak time                                  | $t_{SOAK}$ | 2..3 min    |
| Soak temp range                            | Ts max     | 200°C       |
|                                            | Ts min     | 150°C       |
| Time above 217°C (T1)                      | $t_1$      | Max. 60s    |
| Time above 230°C (T2)                      | $t_2$      | Max. 50s    |
| Time above TPEAK -10°C (T3)                | $t_3$      | Max. 10s    |
| Peak temperature in reflow                 | $T_{PEAK}$ | 260°C       |
| Temperature gradient in cooling            |            | Max. -5K/s  |

It is recommended to use a no-clean solder paste. There should not be any board wash processes, to prevent cleaning agents or other liquid materials contacting the sensor area.

10 Package drawings & markings

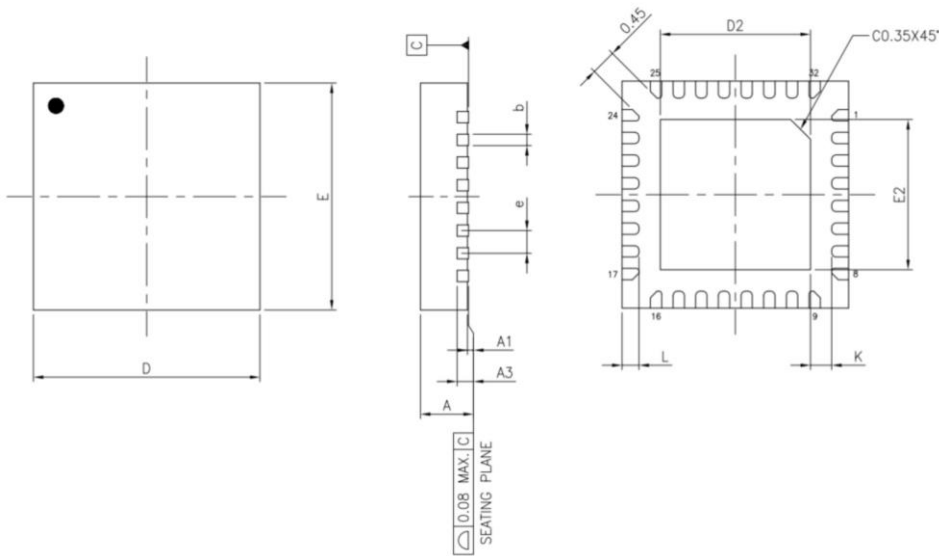


Figure 27: QFN32 package drawing

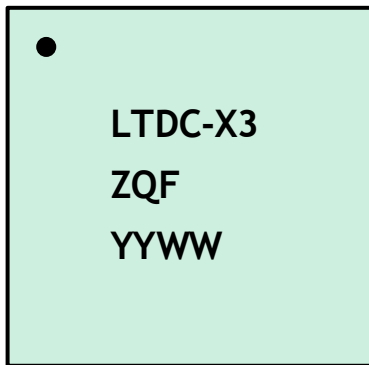
Table 60: QFN32 package dimensions

| Symbol                 | Dimensions |         |      |
|------------------------|------------|---------|------|
|                        | Min        | Nominal | Max  |
| A                      | 0.80       | 0.85    | 0.90 |
| A1                     | 0.00       | 0.02    | 0.05 |
| A3                     | 0.203 REF. |         |      |
| b                      | 0.15       | 0.20    | 0.25 |
| D                      | 3.90       | 4.00    | 4.10 |
| E                      | 3.90       | 4.00    | 4.10 |
| e                      | 0.40 BSC   |         |      |
| L                      | 0.35       | 0.40    | 0.45 |
| K                      | 0.20       | -       | -    |
| Pad size<br>118x11 MIL | 2.65       | 2.70    | 2.75 |

Figure 28: Recommend QFN32 Land Pattern

Note(s):

1. All dimensions are in millimeters.
2. PCB land pattern are shown as red dotted lines.
3. Add 0.05mm all around the nominal lead width and length for the PCB land pattern.



YY = Year, WW = Week

Figure 29: QFN32 package marking

Tape & Reel

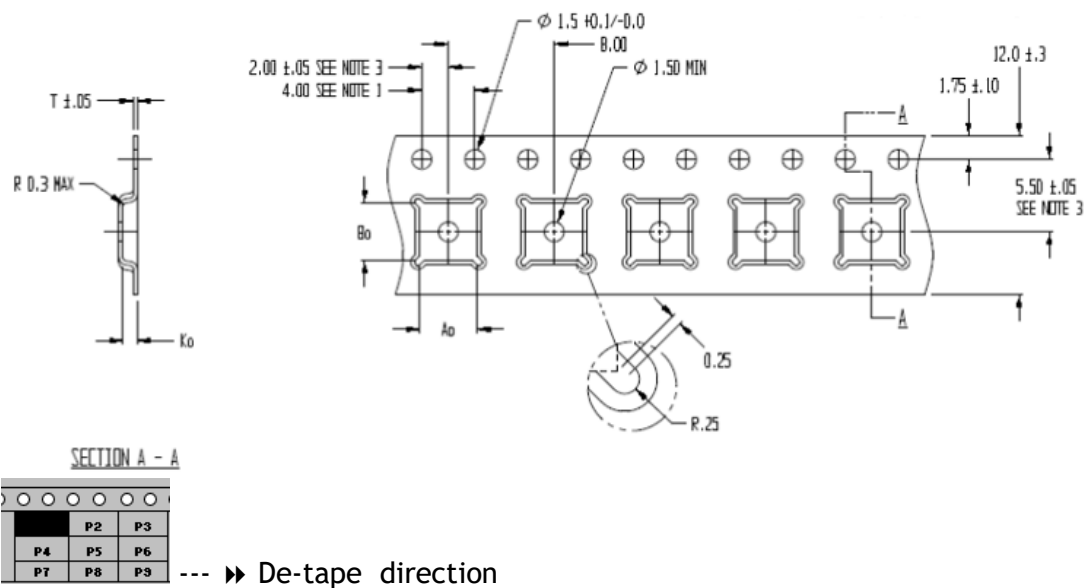


Figure 30: Tape drawing

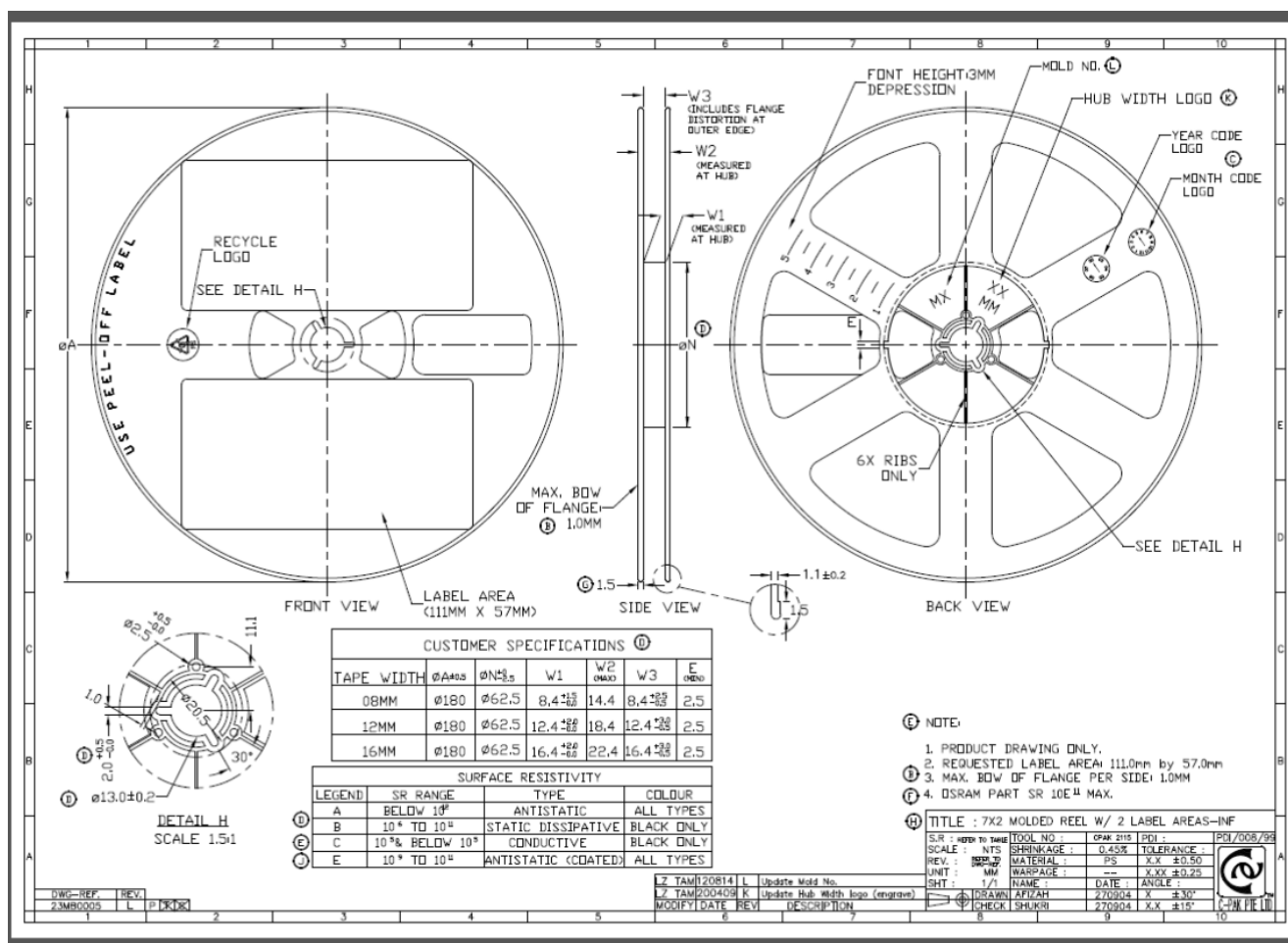


Figure 31: Reel drawing

## 11 Ordering information

Table 61: Ordering information

| Ordering Code | Material ID | Package | Delivery Form | Delivery Quantity |
|---------------|-------------|---------|---------------|-------------------|
| LTDC-X3       | 503710001   | QFN32   | Tape & reel   | 1000 pcs          |

## 12 RoHS Compliance & ScioSense Green Statement

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## 14 Document status

Table 62: Document status

| Document Status          | Product Status  | Definition                                                                                                                                                                                                                                                                  |
|--------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice.                                                                            |
| Preliminary Datasheet    | Pre-Production  | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice.                    |
| Datasheet                | Production      | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade.                                |
| Datasheet (Discontinued) | Discontinued    | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs. |

## 15 Revision information

Table 63: Revision history

| Revision | Date    | Comment              | Page                    |
|----------|---------|----------------------|-------------------------|
| F        | 2025-03 | Draft before release | All                     |
| 1        | 2025-04 | First release        | All, especially p41, 42 |
|          |         |                      |                         |

### Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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[ZSSC3123AA2R](#) [MAX31856MUD+](#) [MAX31856MUD+T](#) [ZSSC3240CI3W](#) [ZSSC3286BI3R](#) [ZSSC4132CE4W](#)