MODEL: DEVKIT-MEMS-006 | DESCRIPTION: MICROPHONE DEVELOPMENT KIT

FEATURES

- 4 detachable evaluation boards
- 1 analog & 1 digital MEMs
- duplicated digital MEMS for stereo configuration
- plated through hole I/O terminals for multiple testing options

RoHS

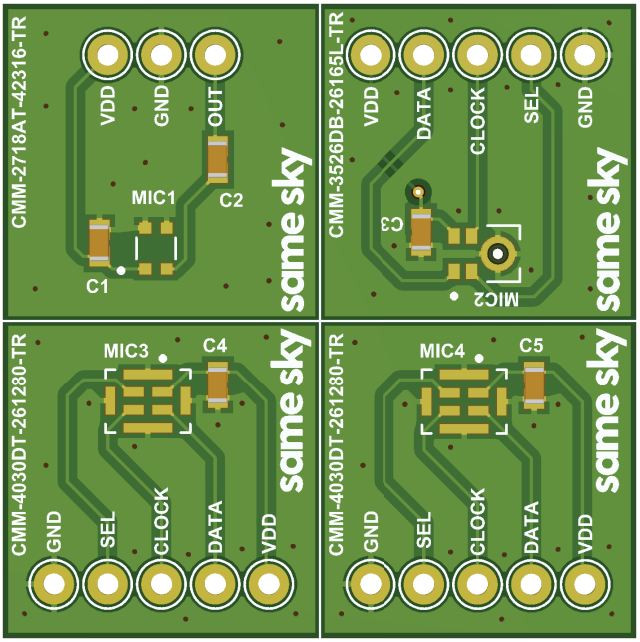
EVAL BOARD

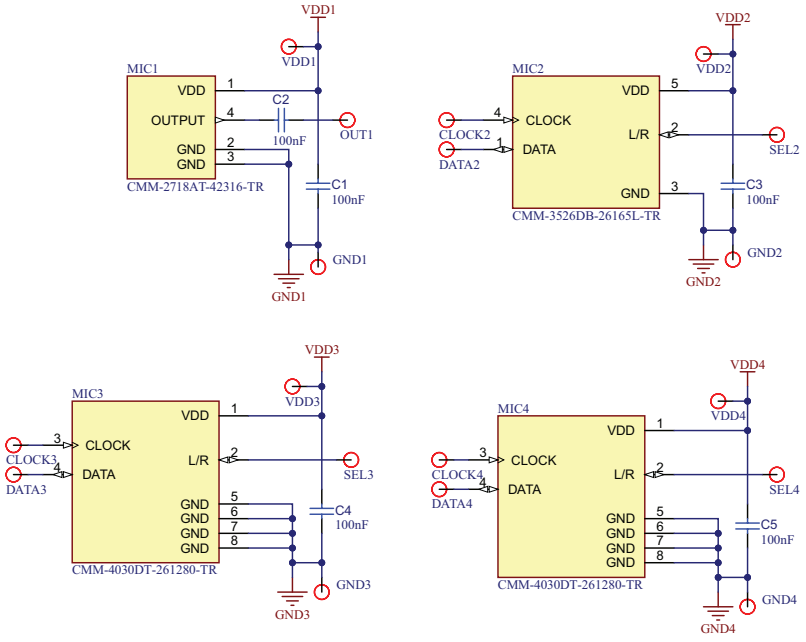
	circuit	technology	output	acoustic port	size (mm)	sensitivity typ (dB)	current max (µA)
CMM-2718AT-42316-TR	MIC1	MEMS	analog	top	2.75 x 1.85	-42	250
CMM-3526DB-26165L-TR	MIC2	MEMS	digital	bottom	3.50 x 2.65	-26	900
CMM-4030DT-261280-TR	MIC3	MEMS	digital	top	4.00 x 3.00	-26	900
CMM-4030DT-261280-TR	MIC4	MEMS	digital	top	4.00 x 3.00	-26	900

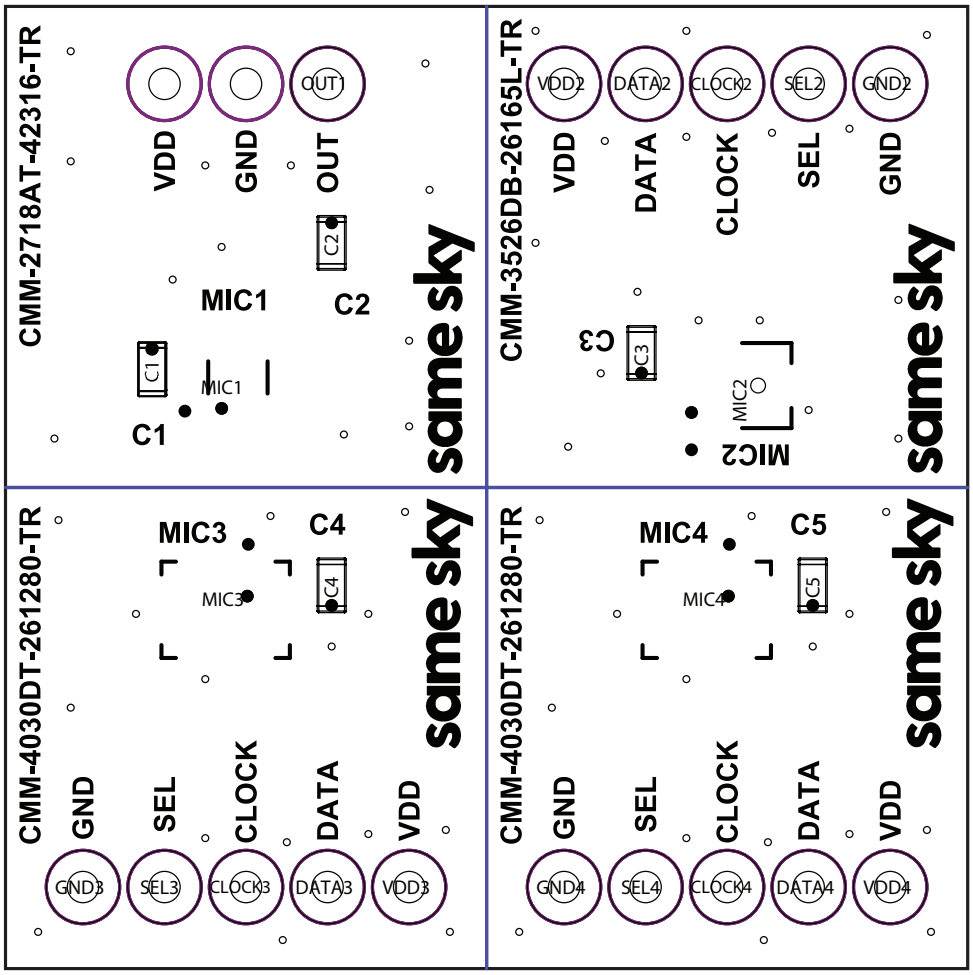
OPERATIONAL INSTRUCTIONS

This Same Sky MEMS microphone evaluation board consists of four independent microphone evaluation circuits. One microphone provides an analog output signal, while three microphones provide digital output signals. Top and bottom sound port options are provided for the digital output microphones, while the analog option is provided as a top port. Two identical circuits of one of the digital options are included, allowing evaluation in a stereo configuration. External bypass capacitors are included on the power supply rails of the evaluation boards, and a DC blocking capacitor is placed in the analog output signal path. A DC power supply of 1.65~3.60V should be connected between the VDD and GND pins of the board to be evaluated. Please refer to the respective data sheets for proper connections to the remaining signal pins.

CIRCUIT DIAGRAMS & BOARD LAYOUTS







CMM-2718AT-42316-TR

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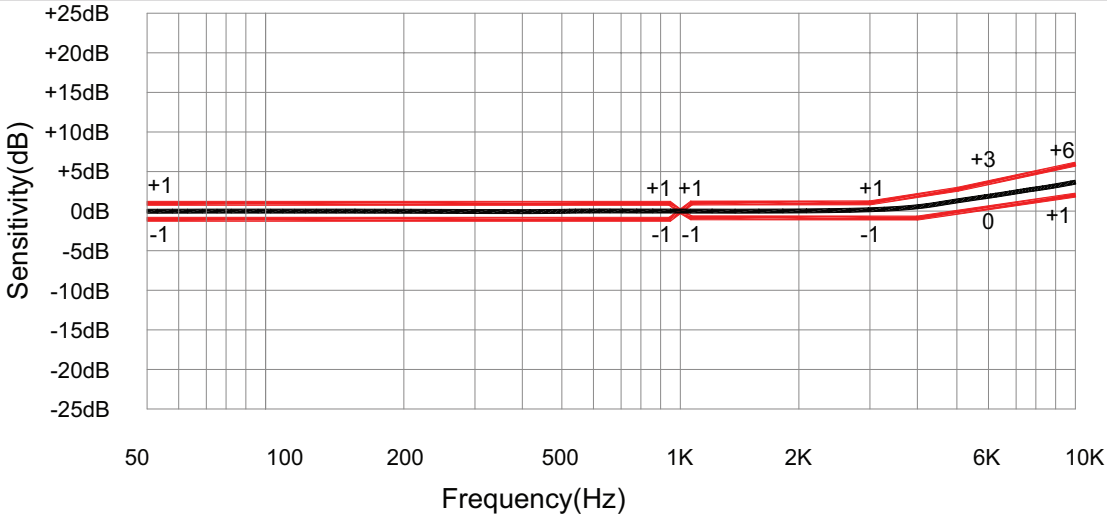
ELECTRICAL

parameter	conditions/description	min	typ	max	units
directivity	omnidirectional				
sensitivity (S)	at 94 dB SPL, 1 kHz	-45	-42	-39	dB
supply voltage (V_{DD})		1.6	2.0	3.6	V
current consumption (I_{DSS})	V_{DD} = 2.0 V			250	µA
frequency (f)		50		10,000	Hz
signal to noise ratio (S/N)	at 94 dB SPL, 1 kHz (A-weighted)		57		dBA
total harmonic distortion (THD)	at 94 dB SPL, 1 kHz		0.10		%
acoustic overload point (AOP)	at 10% THD, 1 kHz		130		dB SPL
output impedance (Zout)	at 1 kHz			300	Ω
power supply rejection ratio (PSRR)	200 mVp-p sine wave @ 1kHz, VDD = 2.0V		75		dB
power supply rejection (PSR)	100 mVp-p square wave @ 217 Hz, VDD = 2.0V, A-weighted		-102		dBV(A)

Notes: 1. All specifications measured at 23±2°C, humidity at 55±20%, unless otherwise noted.

FREQUENCY RESPONSE CURVE



CMM-3526DB-26165L-TR

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ELECTRICAL

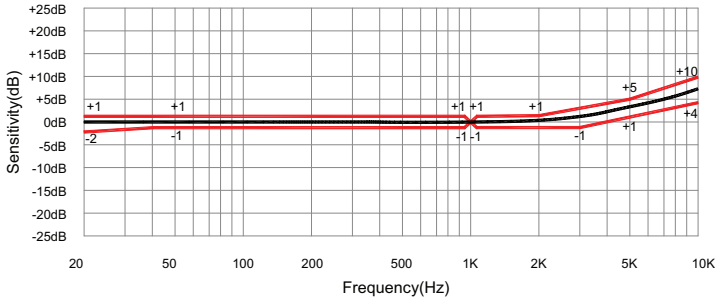
parameter	conditions/description	min	typ	max	units
directivity	omnidirectional				
sensitivity (S)	at 94 dB SPL, 1 kHz	-27	-26	-25	dB FS
supply voltage (V_{DD})		1.65		3.6	V
current consumption (I_{DD})	low-power mode normal mode		280 680	400 900	µA µA
frequency (f)		20		10,000	Hz
signal to noise ratio (S/N)	at 94 dB SPL, 1 kHz (A-weighted) low-power mode normal mode		 63 64		 dBA dBA
total harmonic distortion (THD)	at 94 dB SPL, 1 kHz		0.2		%
acoustic overload point (AOP)	at 10% THD, 1 kHz		120		dBSPL
power supply rejection (PSR)	100 mVp-p square wave @ 217 Hz (A-weighted) low-power mode normal mode		 -90 -80		 dB FS dB FS

DIGITAL INTERFACE

parameter	conditions/description	min	typ	max	units
clock frequency	sleep mode low-power mode normal mode	0 150 1.3		10 900 4.8	kHz kHz MHz
sleep current (I_{SLEEP})	F_{CLOCK} < 10 kHz		3		µA
DC output	full scale= ±100		4		%FS
data format	1/2 cycle PDM				
short circuit output current (I_{SC})	grounded data pin	1		20	mA
output load (C_{LOAD})				100	pF
fall-asleep time	F_{CLOCK} < 10 kHz			20	µs
wake-up time	F_{CLOCK} > 150 kHz			20	ms
startup time (T_{start})	time to start up in any mode after VDD and CLOCK are applied			20	ms
mode switch time	time to switch between modes, VDD remains on			20	ms
clock duty cycle		40		60	%
logic input high (V_{IH})	I_{OUT} = 1 mA	0.65XV_{DD}		V_{DD}+0.3	V
logic input low (V_{IL})	I_{OUT} = 1 mA	-0.3		0.35XV_{DD}	V
logic output high (V_{OH})	I_{OUT} = 1 mA	V_{DD}-0.45			V
logic output low (V_{OL})	I_{OUT} = 1 mA			0.45	V

Notes: 1. All specifications measured at 23±2°C, humidity at 55±20%, V_{DD} = 2.0 V, F_{CLOCK} = 2.4 MHz (normal mode), F_{CLOCK} = 768 kHz (low-power mode), L/R pin grounded, no load, unless otherwise noted.

FREQUENCY RESPONSE CURVE



CMM-4030DT-261280-TR

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ELECTRICAL

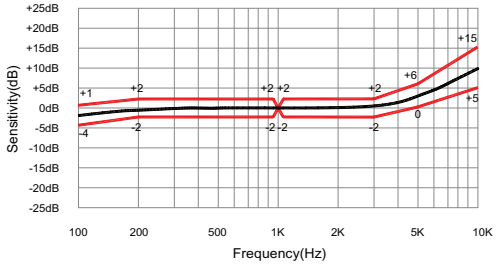
parameter	conditions/description	min	typ	max	units
directivity	omnidirectional				
sensitivity (S)	at 94 dB SPL, 1 kHz	-27	-26	-25	dB FS
supply voltage (V_{DD})		1.65		3.6	V
current consumption (I_{DD})	standard mode (F_{CLOCK} = 2.4 MHz) low-power mode (F_{CLOCK} = 768 kHz)		680 280		µA µA
signal to noise ratio (S/N)	at 94 dB SPL, 1 kHz (A-weighted)		58		dBA
total harmonic distortion (THD)	at 94 dB SPL, 1 kHz		0.1		%
acoustic overload point (AOP)	at 10% THD, 1 kHz		120		dBSPL
power supply rejection (PSR)	100 mVp-p square wave @ 217 Hz (A-weighted)		-80		dB FS
polarity	input higher voltage		increasing density of 1's		

DIGITAL INTERFACE

parameter	conditions/description	min	typ	max	units
clock frequency	sleep mode low-power mode standard mode	0 150 1.3		10 900 4.8	kHz kHz MHz
sleep current (I_{SLEEP})	F_{CLOCK} < 10 kHz		3		µA
dc output	full scale = ±100		4		%FS
fall-asleep time	F_{CLOCK} < 10 kHz			20	µs
wake-up time	F_{CLOCK} > 150 kHz			20	ms
startup time	time to start up in any mode after V_{DD} and CLOCK applied			20	ms
mode switch time	time to switch between modes, V_{DD} remains on			20	ms
data format	1/2 cycle PDM				
short circuit output current (I_{SC})	connect DATA to ground	1		20	mA
output load (C_{LOAD})				100	pF
logic input high (V_{IH})		0.65XV_{DD}		V_{DD}+0.3	V
logic input low (V_{IL})		-0.30		0.35XV_{DD}	V
logic output high (V_{OH})		V_{DD}-0.45			V
logic output low (V_{OL})				0.45	V
clock duty cycle		40		60	%
clock rise time (T_R)				15	ns
clock fall time (T_F)				15	ns
data into hi z time (t_{DZ})		5		20	ns
delay time for data driven (t_{DD})		25		50	ns
data valid time (t_{DV})		40		100	ns

Notes: 1. All specifications measured at 23±2°C, humidity at 55±20%, VDD = 2.0 V, FCLOCK = 2.4 MHz, unless otherwise noted.

FREQUENCY RESPONSE CURVE



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