# ML22594-xxxMB

**4-Channel Mixing Speech Synthesis LSI with Built-in MASK ROM for Automotive**

## GENERAL DESCRIPTION

The ML22594-xxx is 4-channel mixing speech synthesis LSIs with built-in MASK ROM for voice data. These LSIs incorporate into them an HQ-ADPCM decoder that enables high sound quality, 16-bit D/A converter, low-pass filter, 1.0 W monaural speaker amplifier for driving speakers , and over-current detectible function for Speaker Pins. And the high quality and a long time sound regeneration is possible by using the voice regeneration which the outside ROM was used for.
Since functions necessary for voice output are all integrated into a single chip, a system can be upgraded with audio features by only using one of these LSIs.

- Capacity of internal memory and the maximum voice production time (when HQ-ADPCM※1 method used)

| Product name | ROM capacity | Maximum voice production time (sec) | | |
|---|---|---|---|---|
| | | $f_{sam}$ = 8.0 kHz | $f_{sam}$ = 16.0 kHz | $f_{sam}$ = 32.0 kHz |
| ML22594- xxx | 6 Mbits(Internal) | 243 | 121 | 60 |
| | 128 Mbits(Exteranal) | 5240 | 2620 | 1310 |

## FEATURES

- ROM capacity: Internal 6Mbits, External 128Mbits (Max)
- Speech synthesis method: Can be specified for each phrase.
  HQ-ADPCM / 8-bit non-linear PCM / 8-bit PCM / 16-bit PCM
- Sampling frequency: Can be specified for each phrase.
  12.0/24.0/48.0 kHz, 8.0/16.0/32.0 kHz, 6.4/12.8/25.6 kHz
- Built-in low-pass filter and 16-bit D/A converter
- Built-in speaker driver amplifier: 1.0 W, 8Ω (at $DV_{DD}$ = 5 V)
  (with over-current detectible function for Speaker pins)
- External analog voice input (built-in analog mixing function)
- CPU command interface: Clock synchronous serial interface
- Maximum number of phrases: 1024 phrases, from 000h to 3FFh
- Edit ROM
- Volume control: CVOL command: Adjustable through 32 levels (including OFF)
  AVOL command: Adjustable through 50 levels (including OFF)
- Repeat function: LOOP command
- Channel mixing function: 4 channels
- Power supply voltage detection function: Can be controlled at six levels from 2.7 to 4.0 V (including the OFF setting)
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 4.5 to 5.5 V
- Operating temperature range: –40°C to +105°C※2
- Package: heat sink type 30-pin plastic SSOP(P-SSOP30-56-0.65-Z6K)
- Product name: ML22594-xxxMB (“xxx” denotes ROM code number)

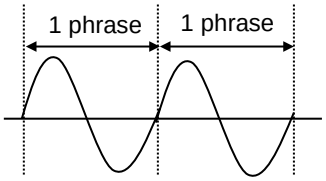
※1 Ky's Technology HQ-ADPCM is a high sound quality audio compression technology of "Ky's".
“Ky’s” is a Registered trademark of National Universities corporate Kyushu Institute of Technology

※2 The limitation on the operation time changes by the using condition.
(Refer to "LIMITATION ON THE OPERATION TIME (PLAY-BACK TIME)")

The table below summarizes the differences between the exsisting speech synthesis LSIs (ML225XG and ML22Q573) and the ML22594.

| Item | ML22Q573 | ML2257X | ML22Q553 | ML22594 |
|---|---|---|---|---|
| CPU interface | Serial | Serial | ← | ← |
| ROM type | FLASH | MASK | FLASH | MASK |
| ROM capacity | 4 Mbits | 2/4 Mbits | 4 Mbits | 6 Mbits |
| External ROM interface | No | ← | ← | Serial |
| Playback method | HQ-ADPCM<br>8-bit straight PCM<br>8-bit non-linear PCM<br>16-bit straight PCM | ← | ← | ← |
| Maximum number of phrases | 1024 | ← | ← | 1024<br>(Internal512 /<br>External512) |
| Sampling frequency (kHz) | 6.4/8.0/12.0/<br>12.8/16.0/24.0/<br>25.6/32.0/48.0 | ← | ← | ← |
| Clock frequency | 4.096 MHz (has a crystal oscillator circuit built-in) | ← | ← | ← |
| D/A converter | 16-bit voltage-type | ← | ← | ← |
| Low-pass filter | FIR interpolation filter<br>(High-pass interpolation) | ← | ← | ← |
| Speaker driving amplifier | Built-in<br>1.0 W<br>(8Ω, $DV_{DD}$ = 5 V) | ← | ← | ← |
| Over-current detectible function for Speaker Pins | No | ← | Yes | ← |
| Simultaneous sound production function (mixing function) | 4-channel | ← | ← | ← |
| Edit ROM | Yes | ← | ← | ← |
| Volume control | 32 levels | ← | ← | ← |
| Silence insertion | 20 to 1024 ms<br>(4 ms steps) | ← | ← | ← |
| Repeat function | Yes | ← | ← | ← |
| External analog input | Yes | ← | ← | ← |
| External speech data input | No | ← | ← | ← |
| Interval at which a seam is silent during continuous playback (*1) | No | ← | ← | ← |
| Power supply voltage | 2.7 V to 5.5 V | ← | 4.5 V to 5.5 V | ← |
| Ambient temperature | -40°C to 105°C | ← | ← | ← |
| Package | 30-pin SSOP | ← | ← | ← |

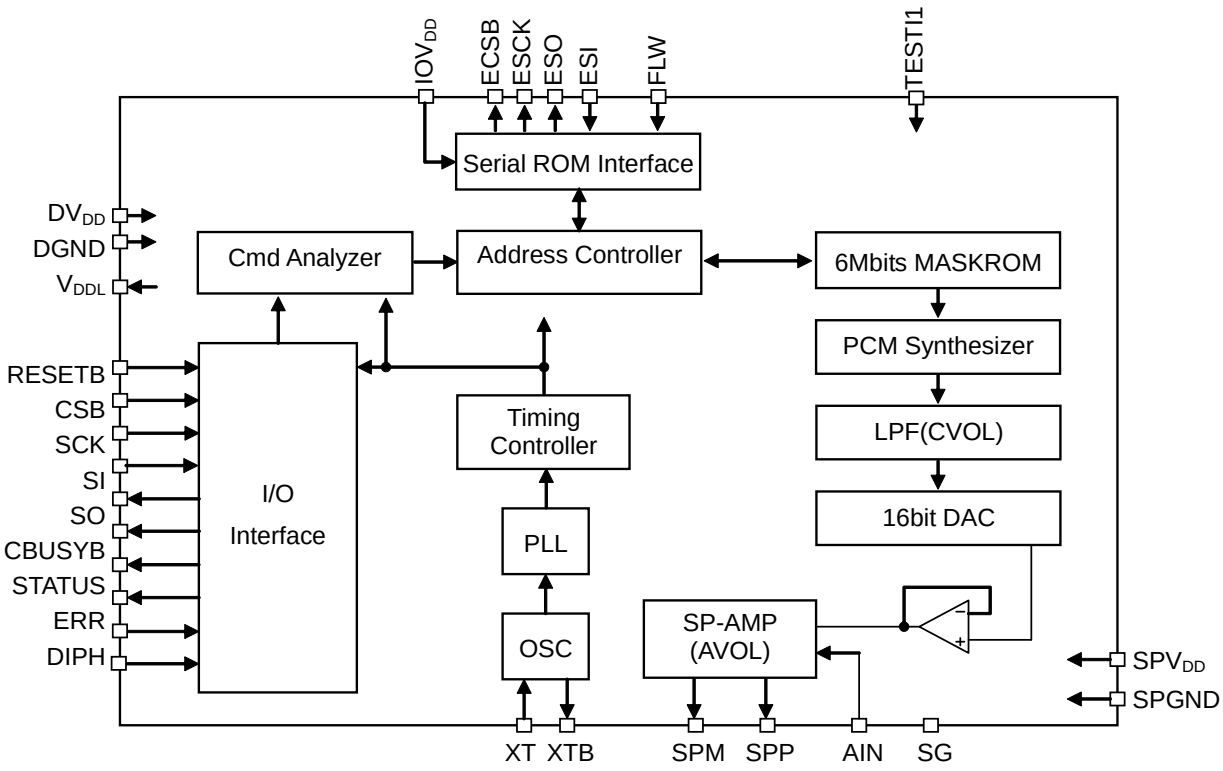
*1: Continuous playback as shown below is possible.
(Playback method: 8-bit straight PCM, 8-bit non-linear PCM, 16-bit straight PCM)




No silence interval

## BLOCK DIAGRAM

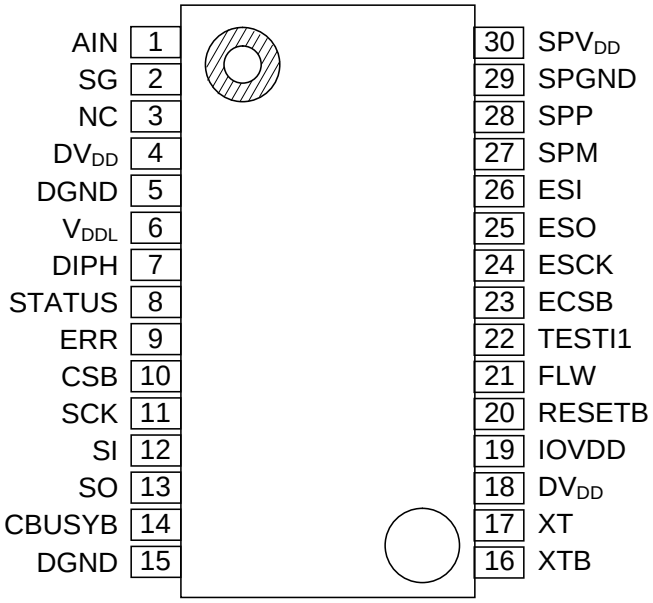
The block diagrams of the ML22594-xxx are shown below.




**Block Diagram of ML22594-xxx**

## PIN CONFIGURATION (TOP VIEW)

● ML22594-xxx




NC : Unused pin

**30-Pin Plastic SSOP**

## PIN DESCRIPTION (1)

| Pin | Symbol | I/O | Attribute | Description | Attribute | Initial value (*1) |
|---|---|---|---|---|---|---|
| 1 | AIN | I | — | Speaker amplifier input pin. | analog | 0 |
| 2 | SG | O | — | Built-in speaker amplifier's reference voltage output pin.<br>Connect a capacitor of 0.1 μF or more between this pin and DGND. | analog | 0 |
| 3 | NC | — | — | NC(Unused) pin | analog | 0 |
| 4,18 | $DV_{DD}$ | — | — | Digital power supply pin.<br>Connect a bypass capacitor of 10μF or more between this pin and DGND. | power | — |
| 5,15 | DGND | — | — | Digital ground pin | gnd | — |
| 6 | $V_{DDL}$ | O | — | 2.5 V regulator output pin.<br>Acts as an internal power supply (for logic). Connect a capacitor of 10 μF or more between this pin and DGND. | power | 0 |
| 7 | DIPH | I | Positive | Serial interface switching pin.<br>Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the SI pin into the inside of the LSI.<br>When this pin is at a "L" level, SI input data is shifted into the LSI on the rising edges of the SCK clock pulses and a status signal is output from the SO pin on the falling edges of the SCK clock pulses.<br>When this pin is at a "H" level, SI input data is shifted into the LSI on the falling edges of the SCK clock pulses and a status signal is output from the SO pin on the rising edges of the SCK clock pulses. | digital | 0 |
| 8 | STATUS | O | Positive | Channel status output pin.<br>Outputs the BUSYB or NCR signal for each channel by inputting the OUTSTAT command. | digital | 1 |
| 9 | ERR | O | Positive | Error output pin.<br>Outputs a "H" level if an error occurs. | digital | 0 |
| 10 | CSB | I | Negative | Chip select pin.<br>A "L" level on this pin accepts the SCK or SI inputs. When this pin is at a "H" level, neither the SCK nor SI signal is input to the LSI. | digital | 1 |
| 11 | SCK | I | Positive | Synchronous serial clock input pin. | clk | 0 |
| 12 | SI | I | — | Synchronous serial data input pin.<br>When the DIPH pin is at a "L" level, data is shifted in on the rising edges of the SCK clock pulses.<br>When the DIPH pin is at a "H" level, data is shifted in on the falling edges of the SCK clock pulses. | digital | 0 |
| 13 | SO | O | Positive | Channel status serial output pin.<br>Outputs a status signal on the falling edges of the SCK clock pulses when the DIPH pin is at a "L" level; outputs a status signal on the rising edges of the SCK clock pulses when the DIPH pin is at a "H" level.<br>When the CSB pin is at a "L" level, the status of each channel is output serially in sync with the SCK clock. When the CSB pin is at a "H" level, this pin goes into a high impedance state. | digital | Hi-Z |

## PIN DESCRIPTION (2)

| Pin | Symbol | I/O | Attribute | Description | Attribute | Initial value(*1) |
|---|---|---|---|---|---|---|
| 14 | CBUSYB | O | Negative | Command processing status signal output pin.<br>This pin outputs a “L” level during command processing.<br>Be sure to enter commands with the CBUSYB pin driven at a “H” level. | digital | (*2) |
| 16 | XTB | O | Negative | Connects to a crystal or a ceramic resonator.<br>When using an external clock, leave this pin open.<br>If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible. | clk | 1 |
| 17 | XT | I | Positive | Connects to a crystal or a ceramic resonator.<br>A feedback resistor of around 1 MΩ is built in between this XT pin and the XTB pin. When using an external clock, input the clock from this pin.<br>If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible. | clk | 0 |
| 19 | $IO_{VDD}$ | I | — | External ROM interface power supply pin.<br>Use the power supply which is the same as the external ROM.<br>Connect a bypass capacitor of 0.1μF or more between this pin and DGND. | analog | 0 |
| 20 | RESETB | I | Negative | Reset input pin.<br>At “L” level input, the LSI enters the initial state. After a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a “L” level to this pin. After the power supply voltage is stabilized, drive this pin at a “H” level.<br>This pin has a pull-up resistor built in. | digital | 0 |
| 21 | FLW | I | Positive | External ROM interface disenable pin.<br>When a “H” level is inputted, the external ROM interface is disenable. “L” level is inputted, the external ROM interface is enable. Has a pull-down resistor built in. | digital | 0 |
| 22 | TESTI1 | I | Negative | Used as either an input pin for testing or a reset input pin for Flash rewriting. Has a pull-down resistor built in. | digital | 0 |
| 23 | ECSB | O | Negative | External ROM interface chip select pin.<br>A “L” level is external ROM access. | digital | 1 |
| 24 | ESCK | O | Positive | External ROM interface serial clock output pin. | digital | 1 |
| 25 | ESO | O | Positive | External ROM interface serial data output pin. | digital | 1 |
| 26 | ESI | I | Positive | External ROM interface serial data input pin.<br>Has a pull-down resistor built in. | digital | 0 |
| 27 | SPM | O | — | Output pin of the built-in speaker amplifier. | analog | Hi-Z |
| 28 | SPP | O | — | Output pin of the built-in speaker amplifier.<br>Can be configured as an AOUT amplifier output by command setting. | analog | 0 |
| 29 | SPGND | — | — | Speaker amplifier ground pin. | gnd | — |
| 30 | $SPV_{DD}$ | — | — | Speaker amplifier power supply pin.<br>Connect a bypass capacitor of 10μF or more between this pin and SPGND. | power | — |

*1: Indicates the initial value at reset input or during power down.

*2: When ML22594 is reset, this pin is "L" level, when ML22594 is power-down, this pin is "H" level.

## ABSOLUTE MAXIMUM RATINGS

DGND = SPGND = 0 V, Ta = 25°C

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $DV_{DD}$<br>$SPV_{DD}$ | — | −0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | — | −0.3 to $DV_{DD}$+0.3 | V |
| Power dissipation | $P_D$ | When the LSI is mounted on JEDEC 4-layer board. When $SPV_{DD}$ = 5V | 1000 | mW |
| Output short-circuit current | $I_{OS}$ | Applies to all pins except SPM, SPP, $V_{DDL}$, and $V_{DDR}$. | 10 | mA |
| | | Applies to SPM and SPP pins. | 500 | mA |
| | | Applies to $V_{DDL}$ and $V_{DDR}$ pins. | 50 | mA |
| Storage temperature | $T_{STG}$ | — | −55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

DGND = SPGND = 0 V

| Parameter | Symbol | Condition | Range | | | Unit |
|---|---|---|---|---|---|---|
| $DV_{DD}$, $SPV_{DD}$ Power supply voltage | $DV_{DD}$<br>$SPV_{DD}$ | — | 4.5 to 5.5 | | | V |
| $IO_{VDD}$ Power supply voltage | $IO_{VDD}$ | — | 2.7 to 5.5 *1 | | | V |
| Operating temperature | Top | — | −40 to +105 | | | °C |
| Master clock frequency | $f_{OSC}$ | — | Min. | Typ. | Max. | MHz |
| | | | 3.5 | 4.096 | 4.5 | |

*1 : When External ROM interface does not be used, $IO_{VDD}$ can be set in 0V.

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

$DV_{DD}$ = $SPV_{DD}$ = 4.5 to 5.5 V, $IOV_{DD}$ = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +105°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| "H" input voltage1(*1) | $V_{IH1}$ | — | 0.8×$DV_{DD}$ | — | $DV_{DD}$ | V |
| "H" input voltage2(*2) | $V_{IH2}$ | — | 0.8×$IOV_{DD}$ | — | $IOV_{DD}$ | V |
| "L" input voltage1(*1) | $V_{IL1}$ | — | 0 | — | 0.2×$DV_{DD}$ | V |
| "L" input voltage2(*2) | $V_{IL2}$ | — | 0 | — | 0.2×$IOV_{DD}$ | V |
| "H" output voltage 1 (*3) | $V_{OH1}$ | $I_{OH}$ = –1 mA | $DV_{DD}$–0.4 | — | — | V |
| "H" output voltage 2 (*4) | $V_{OH2}$ | $I_{OH}$ = –50 µA | $DV_{DD}$–0.4 | — | — | V |
| "H" output voltage 3 (*5) | $V_{OH3}$ | $I_{OH}$ = –1 mA | $IOV_{DD}$–0.4 | — | — | V |
| "L" output voltage 1 (*3) | $V_{OL1}$ | $I_{OL}$ = 2 mA | — | — | 0.4 | V |
| "L" output voltage 2 (*4) | $V_{OL2}$ | $I_{OL}$ = 50 µA | — | — | 0.4 | V |
| "L" output voltage 3 (*5) | $V_{OL3}$ | $I_{OL}$ = 2 mA | — | — | 0.4 | V |
| Output leakage current1 (*6) | $I_{OOH}$ | VOH = $DV_{DD}$ (CSB="H") | — | — | 10 | µA |
| | $I_{OOL}$ | VOL = DGND (CSB="H") | –10 | — | — | µA |
| Output leakage current2 (*7) | $I_{OOH}$ | VOH = $IOV_{DD}$ (FLW="H") | — | — | 10 | µA |
| | $I_{OOL}$ | VOL = DGND (FLW="H") | –10 | — | — | µA |
| "H" input current 1 (*8) | $I_{IH1}$ | $V_{IH}$ = $DV_{DD}$ | — | — | 10 | µA |
| "H" input current 2 (*9) | $I_{IH2}$ | $V_{IH}$ = $DV_{DD}$ | 0.8 | 5.0 | 20 | µA |
| "H" input current 3 (*10) | $I_{IH3}$ | $V_{IH}$ = $DV_{DD}$ | 20 | 100 | 400 | µA |
| "H" input current 4 (*11) | $I_{IH4}$ | $V_{IH}$ = $IOV_{DD}$ | 2 | 100 | 400 | µA |
| "L" input current 1 (*12) | $I_{IL1}$ | $V_{IL}$ = DGND | –10 | — | — | µA |
| "L" input current 2 (*9) | $I_{IL2}$ | $V_{IL}$ = DGND | –20 | –5.0 | –0.8 | µA |
| "L" input current 3 (*13) | $I_{IL3}$ | $V_{IL}$ = DGND | –400 | –100 | –20 | µA |
| Supply current during playback 1 | $I_{DD1}$ | $f_{OSC}$ = 4.096 MHz fs=48kHz, f=1kHz, When 16bitPCM Playback No output load | — | — | 54(*15) | mA |
| | | | — | — | 1(*16) | |
| Supply current during playback 2 (*14) | $I_{DD2}$ | $f_{OSC}$ = 4.096 MHz fs=48kHz, f=1kHz, When 16bitPCM Playback using External ROM No output load | — | — | 50(*15) | mA |
| | | | — | — | 5(*16) | |
| Supply current during playback 3 | $I_{DD3}$ | $f_{OSC}$ = 4.096 MHz During silence playback No output load | — | — | 47(*15) | mA |
| | | | — | — | 1(*16) | |
| Power-down supply current | $I_{DDS1}$ | Ta = –40 to +55°C | — | — | 10(*17) | µA |
| | | Ta = –40 to +105°C | — | — | 20(*17) | µA |

(*1) Applies to the DIPH, CSB, SCK, SI, RESETB, TESTI1 and XT pins.
(*2) Applies to the FLW, ESI pins.
(*3) Applies to the STATUS, ERR, SO and CBUSYB pins.
(*4) Applies to the XTB pin.
(*5) Applies to the ECSB, ESCK and ESO pins.
(*6) Applies to the SO pin.
(*7) Applies to the ECSB, ESCK and ESO pins
(*8) Applies to the DIPH, CSB, SCK, SI and RESETB pins.
(*9) Applies to the XT pin.
(*10) Applies to the TESTI1 pin.
(*11) Applies to the FLW and ESI pins. (Typ. Is 5.0V condition)
(*12) Applies to the DIPH, CSB, SCK, SI, TESTI1, FLW and ESI pins.
(*13) Applies to the RESETB pin.
(*14) ECSB, ESCK and ESO pins load capacitance = 45pF(max)
(*15) Supply current which added $DV_{DD}$ and $SPV_{DD}$.
(*16) Supply current which applies $IOV_{DD}$.
(*17) Supply current which added $DV_{DD}$, $SPV_{DD}$ and $IOV_{DD}$.

### Analog Section Characteristics

DVDD = SPVDD = 4.5 to 5.5 V, IOVDD = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = −40 to +105°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| AIN input resistance | $R_{AIN}$ | Input gain: 0 dB | 10 | 20 | 30 | kΩ |
| AIN input voltage range | $V_{AIN}$ | | — | — | $SPV_{DD}$ × 2/3 | Vp-p |
| Line output resistance | $R_{LA}$ | At 1/2$SPV_{DD}$ output | — | — | 100 | Ω |
| LINE output load resistance | $R_{LA}$ | At SPGND10kΩ load | 10 | — | — | kΩ |
| LINE output voltage range | $V_{A0}$ | At SPGND10kΩ load | $SPV_{DD}$ /6 | — | $SPV_{DD}$ × 5/6 | V |
| SG output voltage | $V_{SG}$ | – | 0.95x $SPV_{DD}$ /2 | $SPV_{DD}$ /2 | 1.05x $SPV_{DD}$ /2 | V |
| SG output resistance | $R_{SG}$ | — | 57 | 96 | 135 | kΩ |
| SPM, SPP output load resistance | $R_{LSP}$ | — | 6 | 8 | — | Ω |
| Speaker amplifier output power | $P_{SPO}$ | $SPV_{DD}$ = 5.0V, f = 1 kHz $R_{SPO}$ = 8Ω, THD≦ 10% | 800 | 1000 | — | mW |
| Output offset voltage between SPM and SPP with no signal present | $V_{OF}$ | SPIN–SPM gain = 0 dB With a load of 8Ω | −50 | — | +50 | mV |
| Regulator output voltage | $V_{DDL}$ $V_{DDR}$ | Output load current = −35 mA | 2.25 | 2.5 | 2.75 | V |

**AC Characteristics (1)**

$DV_{DD}$ = $SPV_{DD}$ = 4.5 to 5.5 V, $IOV_{DD}$ = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +105°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Master clock duty cycle | $f_{duty}$ | — | 40 | 50 | 60 | % |
| RESETB input pulse width | $t_{RST}$ | — | 10 | — | — | µs |
| Reset noise rejection pulse width | $t_{NRST}$ | RESETB pin | — | — | 0.1 | µs |
| Noise rejection pulse width | $t_{NINP}$ | CSB, SCK, and SI pins | — | — | 5 | ns |
| Command input interval time1 | $t_{INT}$ | $f_{OSC}$ = 4.096 MHz<br>At STOP/SLOOP/CLOOP/<br>VOL command input<br>After status read | 10 | — | — | µs |
| Command input interval time2 | $t_{INTC}$ | $f_{OSC}$ = 4.096 MHz<br>After input first command at<br>two-time command input<br>mode | 0 | — | — | µs |
| Command input enable time | $t_{cm}$ | $f_{OSC}$ = 4.096 MHz<br>During continuous playback<br>At SLOOP input | — | — | 10 | ms |
| At PUP command input<br>CBUSYB “L” level output time | $t_{PUP}$ | 4.096 MHz<br>At external clock input | — | — | 4 | ms |
| At AMODE command input<br>CBUSYB “L” level output time(*3) | $t_{PUPA1}$ | 4.096 MHz<br>At external clock input<br>POP = “0”<br>DAEN = “0”→”1”<br>or SPEN = “0”→”1” | 39 | 41 | 43 | ms |
| At AMODE command input<br>CBUSYB “L” level output time | $t_{PUPA2}$ | 4.096 MHz<br>At external clock input<br>POP = “1”<br>DAEN = “0”→”1”<br>(SPEN = “0”) | 72 | 74 | 76 | ms |
| At AMODE command input<br>CBUSYB “L” level output time | $t_{PUPA3}$ | 4.096 MHz<br>At external clock input<br>POP = “0”<br>DAEN = “0”→”1”<br>(SPEN = “0”) | 32 | 34 | 36 | ms |
| At PDWN command input<br>CBUSYB “L” level output time | $t_{PD}$ | $f_{OSC}$ = 4.096 MHz | — | — | 10 | µs |
| At AMODE command input<br>CBUSYB “L” level output time(*3) | $t_{PDA1}$ | 4.096 MHz<br>At external clock input<br>POP = “0”<br>DAEN = “1”→”0”<br>or SPEN = “1”→”0” | 106 | 108 | 110 | ms |
| At AMODE command input<br>CBUSYB “L” level output time | $t_{PDA2}$ | 4.096 MHz<br>At external clock input<br>POP = “1”<br>DAEN = “1”→”0”<br>(SPEN = “0”) | 143 | 145 | 147 | ms |
| At AMODE command input<br>CBUSYB “L” level output time | $t_{PDA3}$ | 4.096 MHz<br>At external clock input<br>POP = “0”<br>DAEN = “1”→”0”<br>(SPEN = “0”) | 103 | 105 | 107 | ms |

| | | | | | | |
|---|---|---|---|---|---|---|
| CBUSYB "L" level output time 1 (*1) | $t_{CB1}$ | $f_{OSC}$ = 4.096 MHz | — | — | 10 | μs |
| CBUSYB "L" level output time 2 (*2) | $t_{CB2}$ | $f_{OSC}$ = 4.096 MHz | — | — | 3 | ms |
| CBUSYB "L" level output time 3 (*4) | $t_{CB3}$ | $f_{OSC}$ = 4.096 MHz | — | — | 200 | μs |

Note: Output pin load capacitance = 45 pF (Max.)

*1: Applies to cases where a command is input, except after the PUP, PDWN, PLAY, START or AMODE command input.

*2: Applies to cases where the PLAY or START command is input.

*3: When FAD3-0 is initial value (8h)

*4: Applies to cases where the STOP command is input

**AC Characteristics (2) CPU serial interface**

$DV_{DD}$ = $SPV_{DD}$ = 4.5 to 5.5 V, $IOV_{DD}$ = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +105°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCK input enable time from CSB fall | $t_{ESCK}$ | — | 100 | — | — | ns |
| SCK hold time from CSB rise | $t_{CSH}$ | — | 100 | — | — | ns |
| Data floating time from CSB rise | $t_{DOZ}$ | $R_L$ = 3 kΩ | — | — | 100 | ns |
| Data setup time from SCK rise | $t_{DIS1}$ | DIPH = “L” | 50 | — | — | ns |
| Data hold time from SCK rise | $t_{DIH1}$ | DIPH = “L” | 50 | — | — | ns |
| Data output delay time from SCK fall | $t_{DOD1}$ | DIPH = “L” | — | — | 90 | ns |
| Data setup time from SCK fall | $t_{DIS2}$ | DIPH = “H” | 50 | — | — | ns |
| Data hold time from SCK fall | $t_{DIH2}$ | DIPH = “H” | 50 | — | — | ns |
| Data output delay time from SCK rise | $t_{DOD2}$ | DIPH = “H” | — | — | 90 | ns |
| SCK “H” level pulse width | $t_{SCKH}$ | — | 100 | — | — | ns |
| SCK “L” level pulse width | $t_{SCKL}$ | — | 100 | — | — | ns |
| CBUSYB output delay time from SCK rise | $t_{DBSY1}$ | DIPH = “L” | — | — | 90 | ns |
| CBUSYB output delay time from SCK fall | $t_{DBSY2}$ | DIPH = “H” | — | — | 90 | ns |

Note: Output pin load capacitance = 45 pF (Max.)

**AC Characteristics (3) External ROM serial interface**

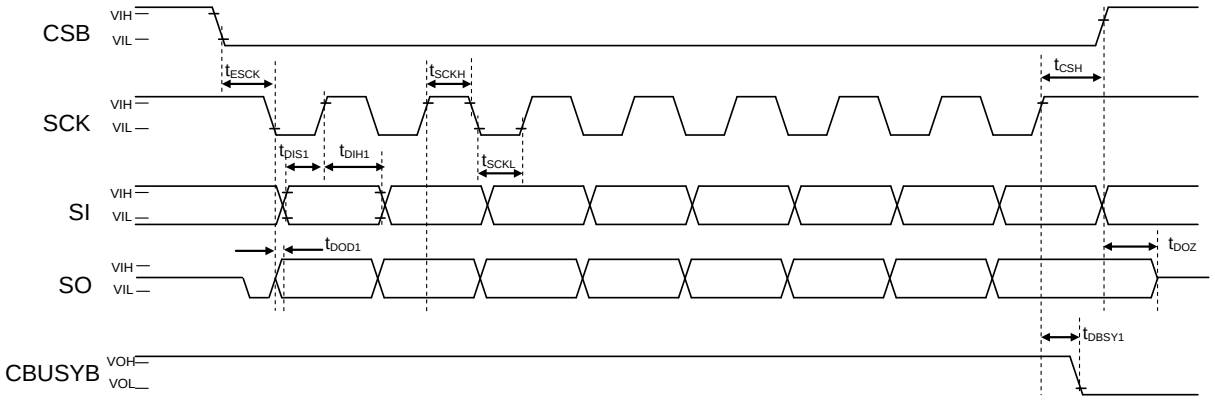
$DV_{DD}$ = $SPV_{DD}$ = 4.5 to 5.5 V, $IOV_{DD}$ = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +105°C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ESCK input enable time from ECSB fall edge | $t_{ECSS}$ | $f_{OSC}$ = 4.096 MHz | 50 | — | — | ns |
| ESCK input hold time from ECSB rise edge | $t_{ECSH}$ | $f_{OSC}$ = 4.096 MHz | 50 | — | — | ns |
| Data setup time from ESCK rise edge | $t_{EDIS}$ | $f_{OSC}$ = 4.096 MHz | 10 | — | — | ns |
| Data hold time from ESCK rise edge | $t_{EDIH}$ | $f_{OSC}$ = 4.096 MHz | 10 | — | — | ns |
| Data output delay time from ESCK rise edge | $t_{EDOD}$ | $f_{OSC}$ = 4.096 MHz | — | — | 5 | ns |
| ESCK clock frequency | $t_{ESCKF}$ | $f_{OSC}$ = 4.096 MHz | 16.0 | 16.384 | 16.5 | MHz |
| ESCK “H” level pulse width | $t_{ESCKH}$ | $f_{OSC}$ = 4.096 MHz | 26 | — | — | ns |
| ESCK “L” level pulse width | $t_{ESCKL}$ | $f_{OSC}$ = 4.096 MHz | 26 | — | — | ns |
| Data output delay time from FLW rise edge. | $t_{EFLH}$ | — | — | — | 1 | ms |
| Data output delay time from FLW fall edge. | $t_{EFHL}$ | — | — | — | 1 | ms |

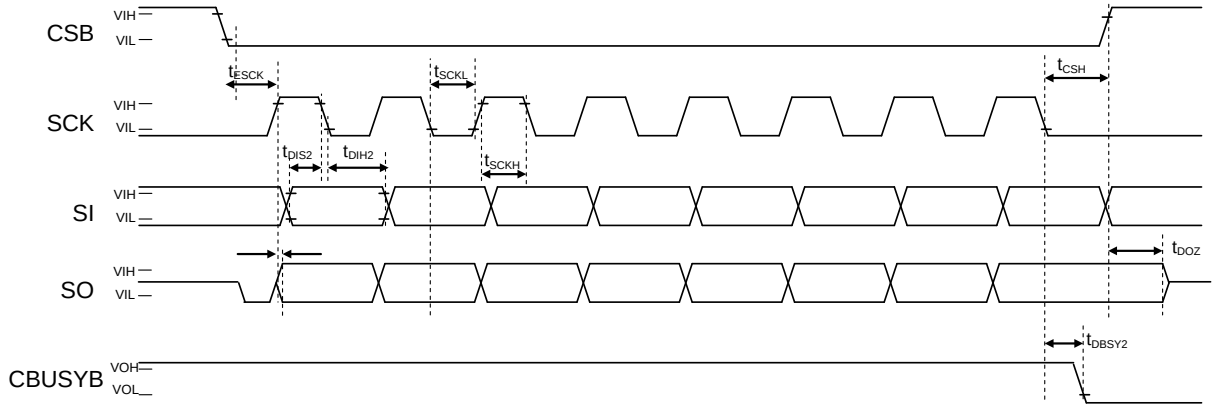
Note: Output pin load capacitance = 45 pF (Max.)

## TIMING DIAGRAMS

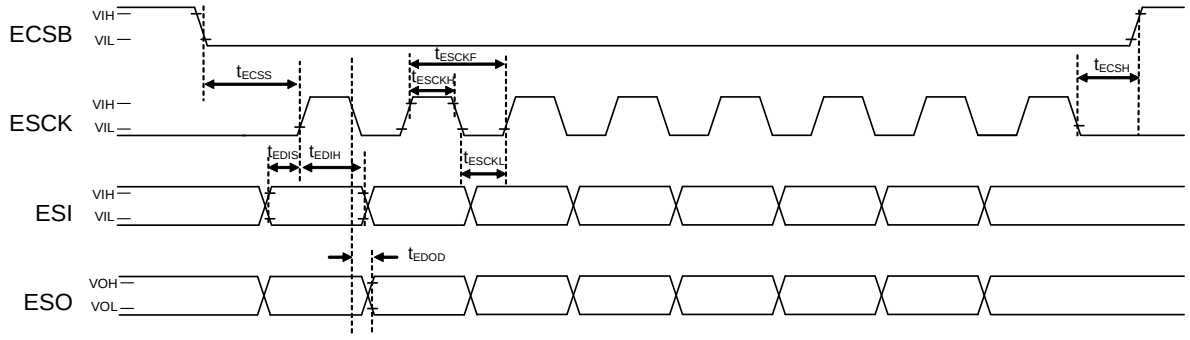
### CPU Serial Interface Data Timing (When DIPH = "L")



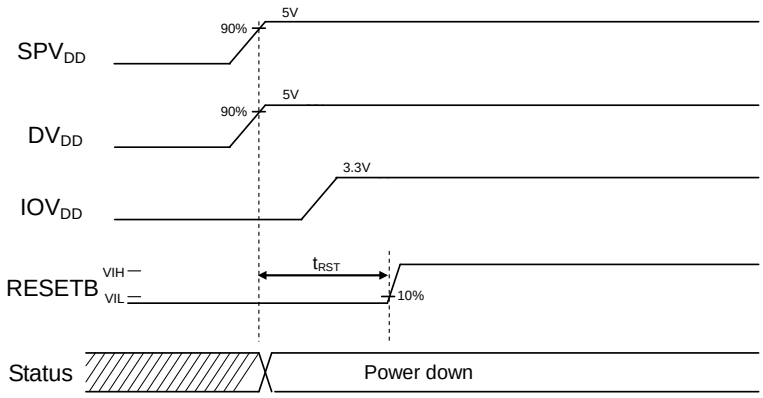

### CPU Serial Interface Data Timing (When DIPH = "H")




### External ROM Serial Interface Data Timing



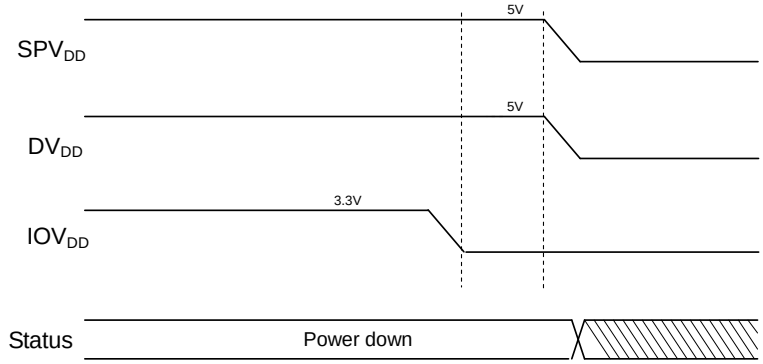
**Power-On Timing**




Oscillation is stopped after power-on.
Be sure to power-on IOVDD after DVDD/SPVDD.
When IOVDD isn't used, it is possible that it is fixed in 0V.

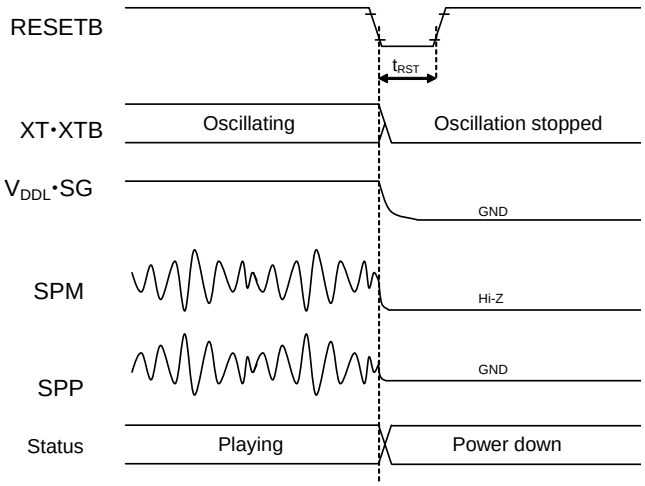
Be sure to set “L”level the RESETB pin before the first command input.

**Power Shut-down Timing**



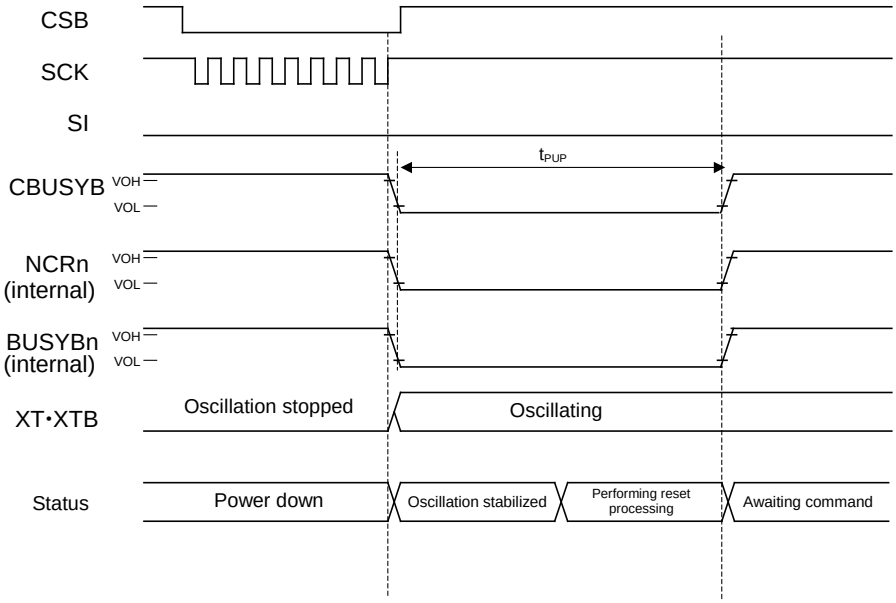

Be sure to power shut-down DVDD/SPVDD after IOVDD.
When IOVDD isn't used, it is possible that it is fixed in 0V.

**Reset Input Timing**

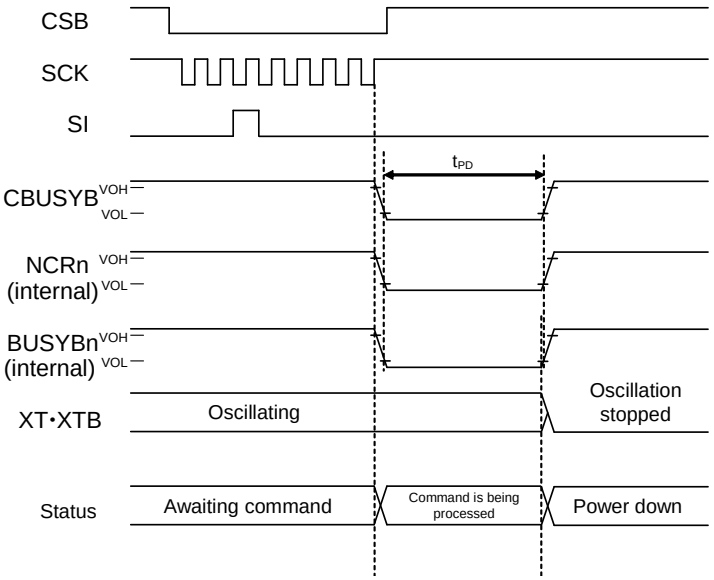



Note: The same timing applies in cases where the Reset signal is input during waiting for command.

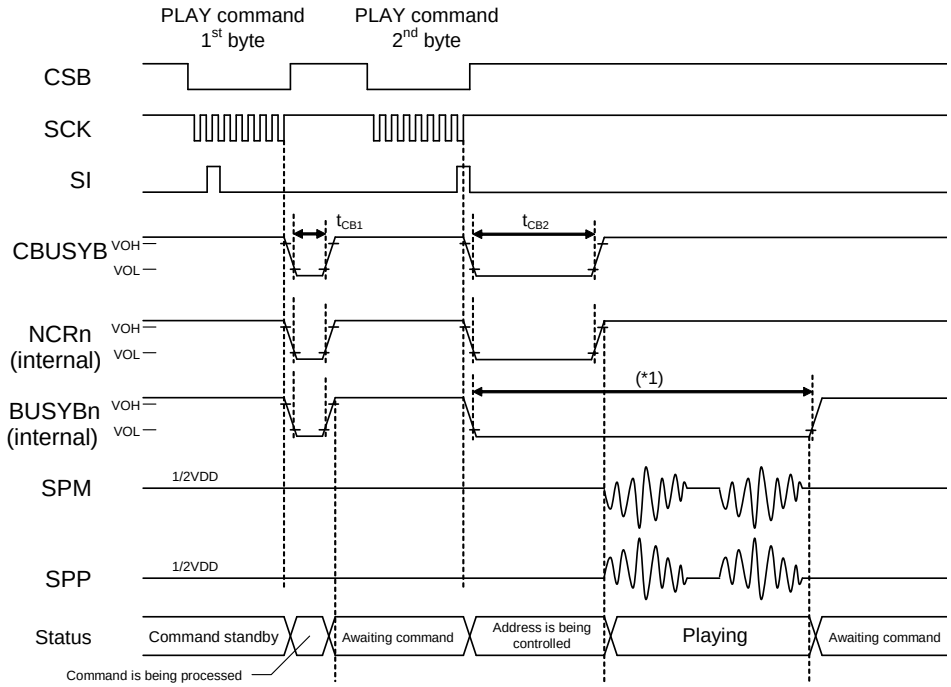
**Power-Up Timing**




**Power-Down Timing**

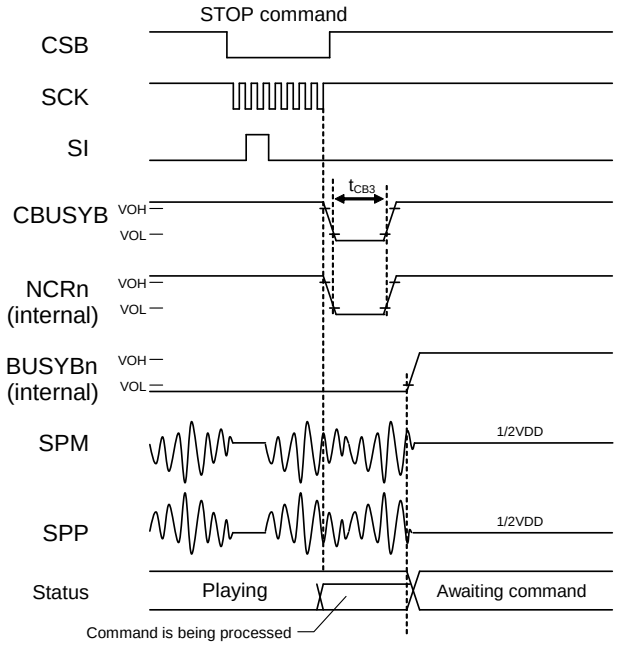


**Playback Start Timing by the PLAY Command**

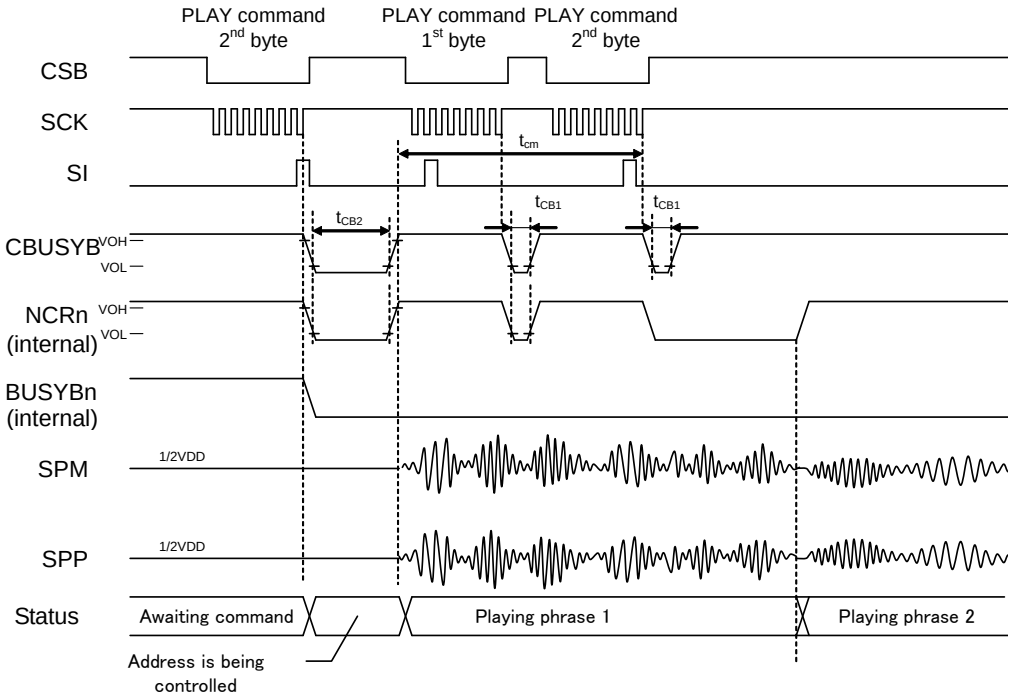



*1: Length of the "L" interval of BUSYBn is = $t_{CB2}$ + voice production time length.

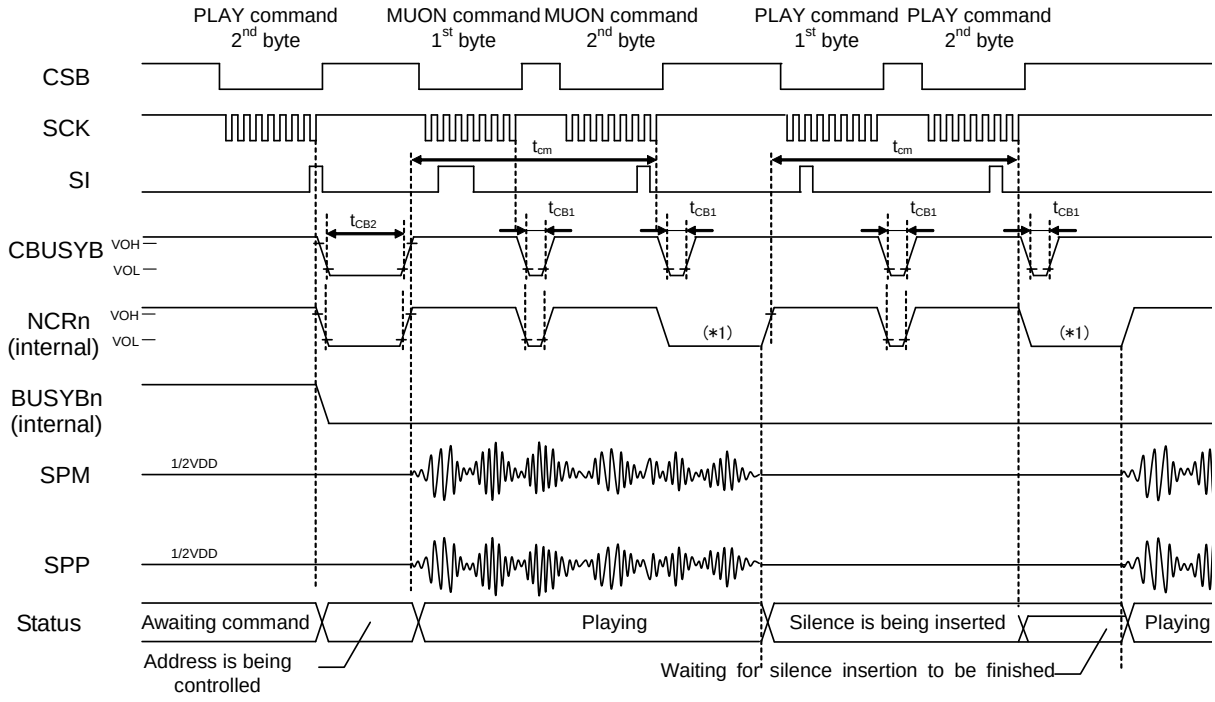
**Playback Stop Timing**



**Continuous Playback Timing by the PLAY Command**

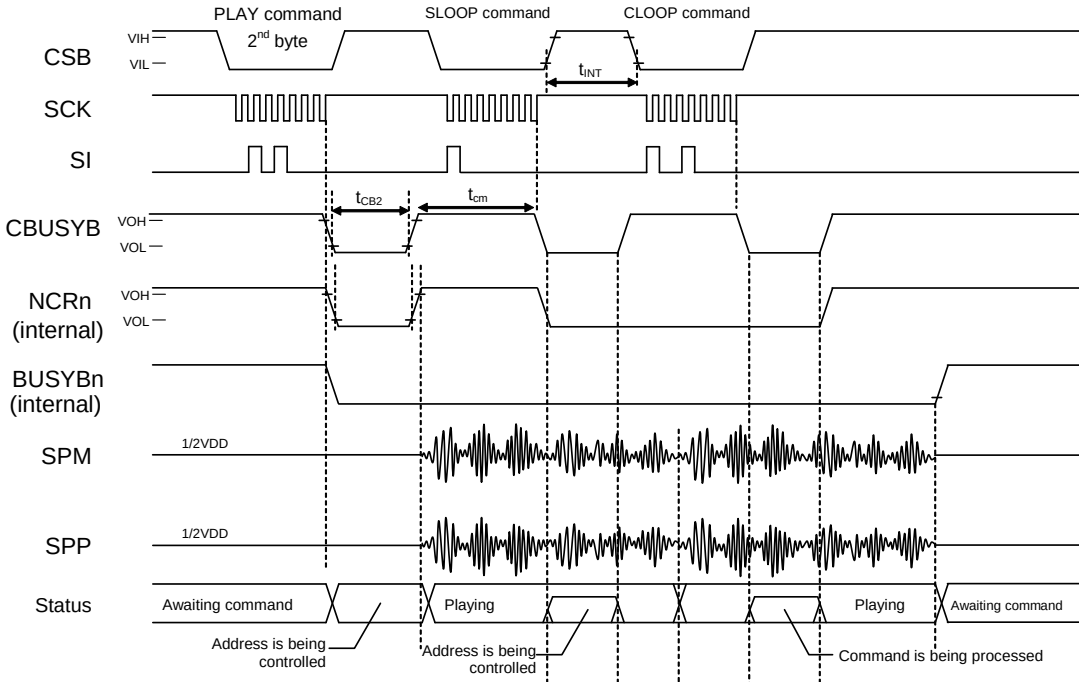



**Silence Insertion Timing by the MUON Command**

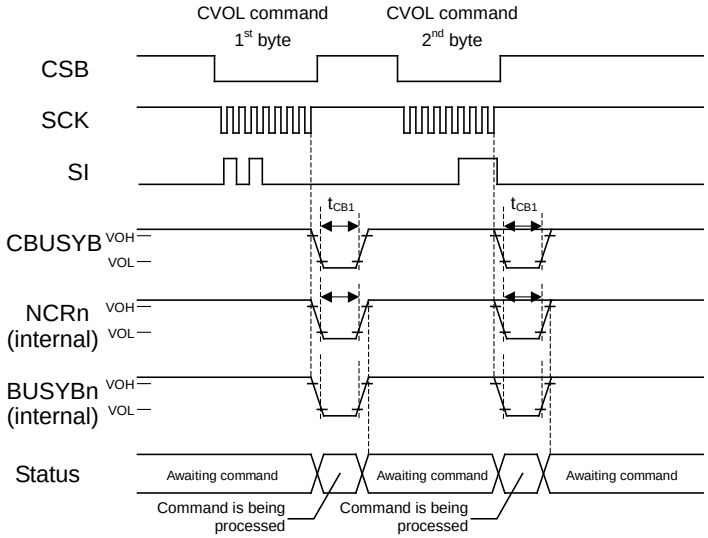



*1: The “L” level period of the NCR pin during playback or silence insertion operation varies depending on the timing at which the MUON command is input.

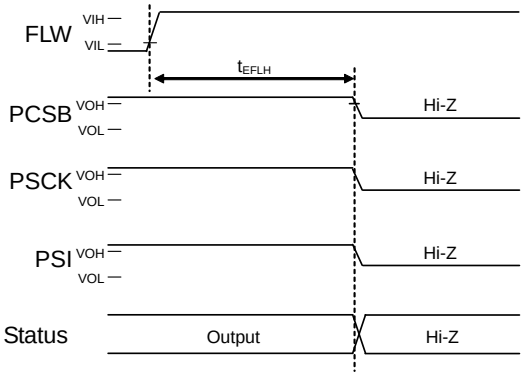
### Repeat Playback Set/Release Timing by the SLOOP and CLOOP Commands



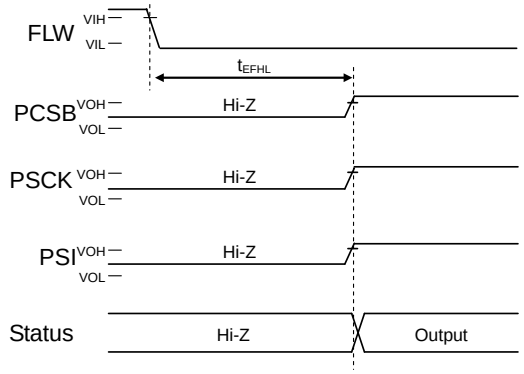

### Timing of Volume Change by the CVOL Command



**External ROM interface at FLW rise**




**External ROM interface at FLW fall**

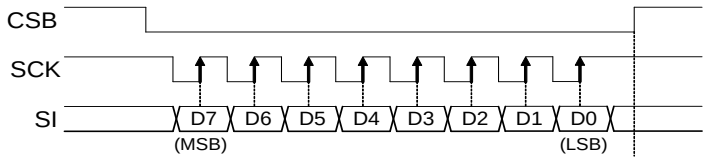


## FUNCTIONAL DESCRIPTION

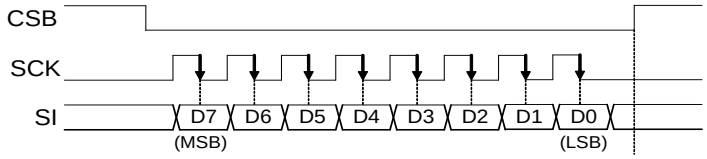
### Synchronous Serial Interface

The CSB, SCK, SI, and SO pins are used to input various commands or read the status of the device.
For command input, after inputting a “L” level to the CSB pin, input data through the SI pin with MSB first in sync with the SCK clock signal. The data input through the SI pin is shifted into the LSI in sync with the SCK clock signal, then the command is executed at the eighth pulse of the rising or falling edge of the SCK clock.
For status reading, after a “L” level is input to the CSB pin, stauts is output from the SO pin in sync with the SCK clock signal.
Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:
- When the DIPH pin is at a “L” level, the data input through the SI pin is shifted into the LSI on the rising edges of the SCK clock pulses and a status signal is output from the SO pin on the falling edges of the SCK clock pulses.
- When the DIPH pin is at a “H” level, the data input through the SI pin is shifted into the LSI on the falling edges of the SCK clock pulses and a status signal is output from the SO pin on the rising edges of the SCK clock pulses.
It is possible to input commands even with the CSB pin tied to a “L” level. However, if unexpected pulses caused by noise etc. are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal input of command. In addition, the serial interface can be brought back to its initial state by driving the CSB pin at a “H” level.
When the CSB pin is at ta “L” level, the status of each channel is output serially in sync with the SCK clock. When the CSB pin is at a ”H” level, the SO pin goes into a high impedance state.

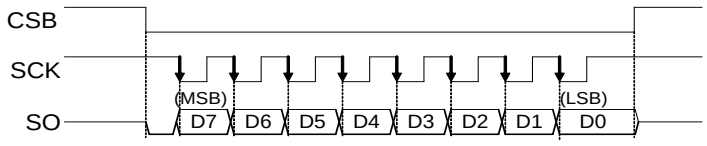
- Command Input Timing: SCK rising edge operation (when DIPH pin = “L” level)



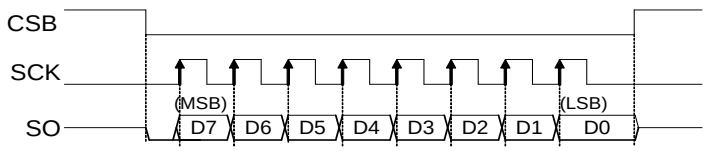

- Command Input Timing: SCK falling edge operation (when DIPH pin = “H” level)




- Command Output Timing: SCK falling edge operation (when DIPH pin = “L” level)

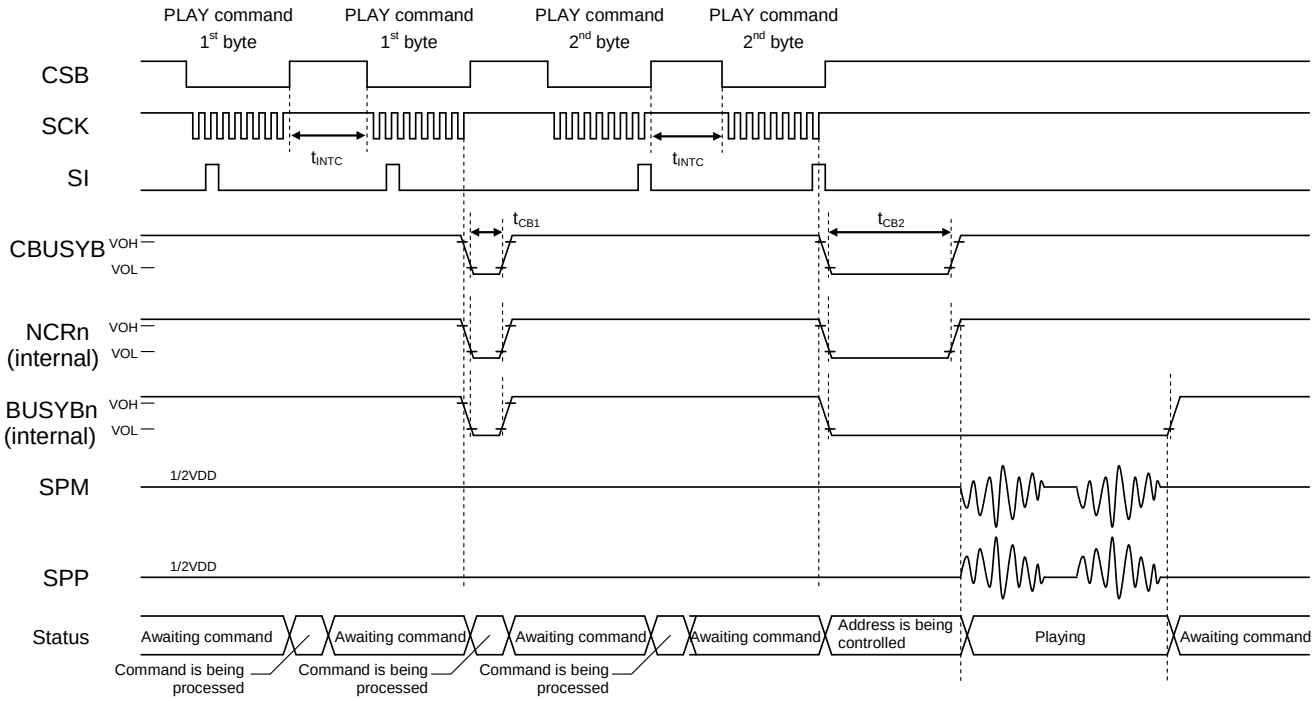



Command Output Timing: SCK rising edge operation (when DIPH pin = “H” level)



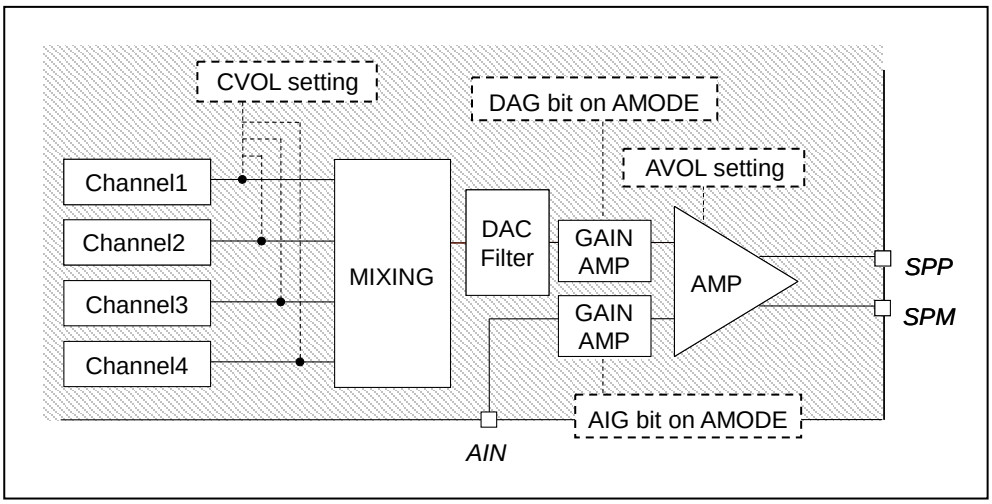
To prevent malfunction caused by serial interface pin noise, the ML22594 is provided with the two-time command input mode, where the user inputs one command two times. Use the PUP command to set the two-time command input mode. For the method of setting the two-time command input mode, see the the section on “1. PUP command” described later.

In two-time command input mode, input one command two times in succession. Then, the command becomes valid only when the data input first matches the data input second. After the first data input, if a data mismatch occurs when the second data is input, a ”H” level is output from the ERR pin. An error, if occurred, can be cleared by the ERCL command.



**To know the volume controls more**

Three commands (: CVOL, AVOL and AMODE) can control volume.
CVOL sets volume of each channel. AVOL sets volume of signal after mixing.
And AMODE sets input gain of amplifier.




**Voice Synthesis Algorithm**

The ML22594 contains four algorithm types to match the characteristic of playback voice: HQ-ADPCM algorithm, 8-bit straight PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.
Key feature of each algorithm is described in the table below.

| Voice synthesis algorithm | Feature |
|---|---|
| HQ-ADPCM | Algorithm that enables high sound quality and high compression, which have been achieved by the improved 4-bit ADPCM that uses variable bit-length coding. |
| 8-bit Nonlinear PCM | Algorithm that plays back mid-range of waveform as 10-bit equivalent voice quality. |
| 8-bit PCM | Normal 8-bit PCM algorithm |
| 16-bit PCM | Normal 16-bit PCM algorithm |

**Memory Allocation and Creating Voice Data**

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the ROM's voice data. It contains data for controlling the start/stop addresses of voice data for 1024 phrases(512phrases for internal ROM, 512phases for external ROM), use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data. For the details, refer to the section on "Edit ROM Function."
No edit ROM area is available unless the edit ROM is used.

The ROM data is created using a dedicated tool.

Configuration of Internal ROM data(6Mbit)

| | |
|---|---|
| 0x00000<br>0x01FFF | Voice control area<br>(Fixed 64Kbits) |
| 0x02000<br>0x0206F | Test area |
| 0x02070<br>0x021AF | Filter area |
| 0x021B0 | Voice area |
| 0xBFFFF | Edit ROM area<br>Depends on creation of ROM data |

Configuration of External ROM data(128Mbit)

| | |
|---|---|
| 0x000000<br>0x001FFF | Voice control area<br>(Fixed 64Kbits) |
| 0x002000<br>0x00206F | Test area |
| 0x002070<br>0x0021AF | Filter area |
| 0x0021B0 | Voice area |
| 0xFFFFFF | Edit ROM area<br>Depends on creation of ROM data |

**Playback Time and Memory Capacity**

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.
The equation below gives the playback time when the edit ROM function is not used.

$$\text{Playback time} = \frac{1.024 \times (\text{Memory capacity} - 64)\ (\text{Kbits})}{\text{Sampling frequency (kHz)} \times \text{Bit length}}\ (\text{sec})$$

Example: Let the sampling frequency be 16 kHz and HQ-ADPCM algorithm. Then the playback time is approx. 121 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (6144 - 64)\ (\text{Kbits})}{16\ (\text{kHz}) \times 3.2\ (\text{bits})\ (\text{average})} \cong 121\ (\text{sec})$$

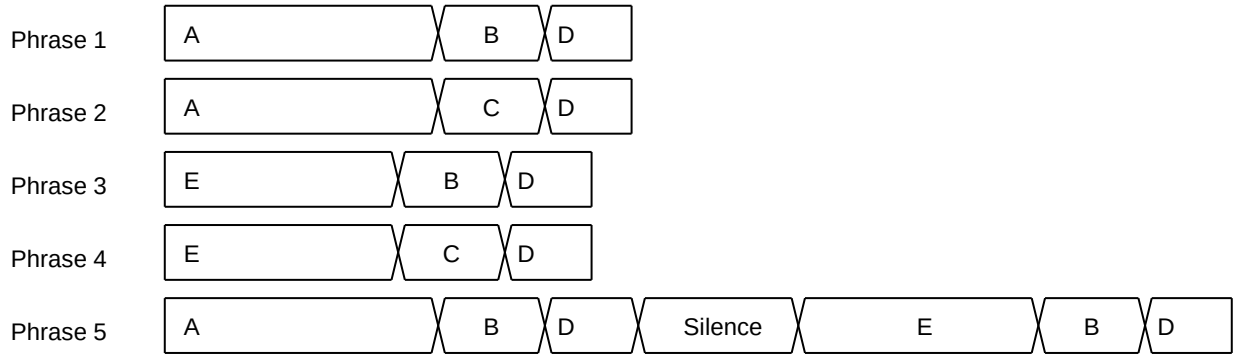
**Edit ROM Function**

With the edit ROM function, multiple phrases can be played in succession. The following functions can be configured using the edit ROM function:

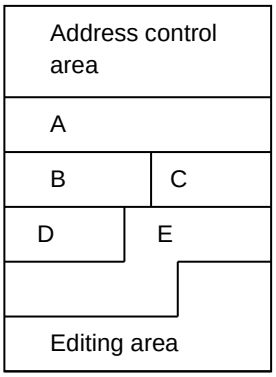
・Continuous playback: There is no limit to the continuous playback count that can be specified. It depends on the memory capacity only.
・Silence insertion: 20 to 1024 ms

Using the edit ROM function enables an effective use of the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the edit ROM function.

Examples of Phrases Using the Edit ROM Function




Example of ROM Data Where the Contents Above Are Stored in ROM



**Mixing Function**

The ML22594 can perform simultaneous mixing of four channels. It is possible to specify FADR, PLAY, STOP, and CVOL for each channel separately.

• Precautions for Waveform Clamp at the Time of Channel Mixing
If channel mixing is done, the possibility of an occurrence of a clamp increases from the mixing calculation point of view. If it is known beforehand that a clamp will occur, then adjust the sound volume of each channel using the VOL command.

• Mixing of Different Sampling Frequency
It is not possible to perform channel mixing by a different sampling frequency group.
When performing channel mixing, the sampling frequency group of the first playback channel is selected. Therefore, note that if channel mixing is performed by a sampling frequency group other than the selected sampling frequency group, then the playback will not be of constant speed: some times faster and at other times slower.
The available sampling groups for channel mixing by a different sampling frequency are listed below.
8.0 kHz, 16.0 Hz, 32.0 kHz … (Group 1)
12.0 kHz, 24.0 kHz, 48 kHz … (Group 2)
6.4 kHz, 12.8 kHz, 25.6 kHz … (Group 3)

Figures below show cases where a phrase is played at a sampling frequency belonging to a different sampling frequency group.

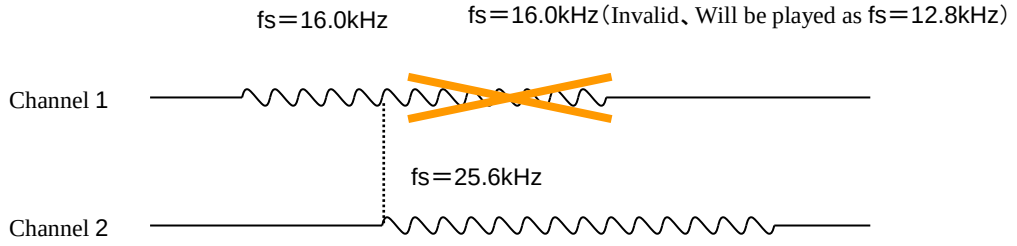



Figure 1 Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group during playback on channels 1 and 2

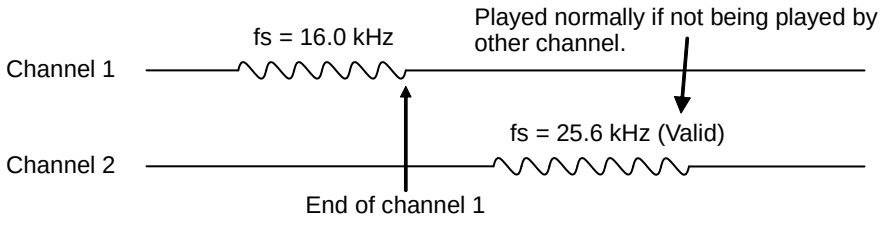
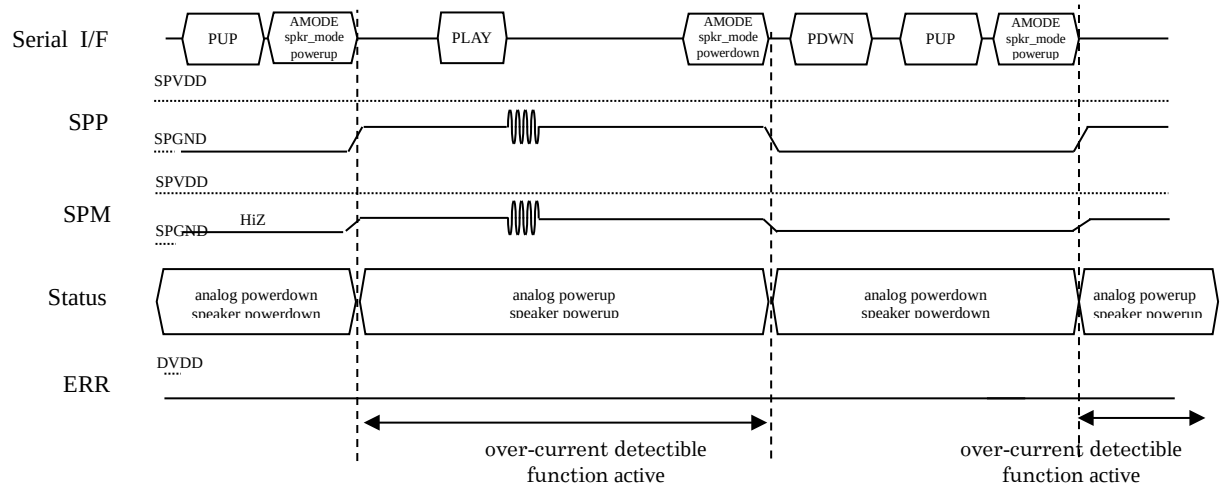



Figure 2 Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group after playback is finished at the other channel

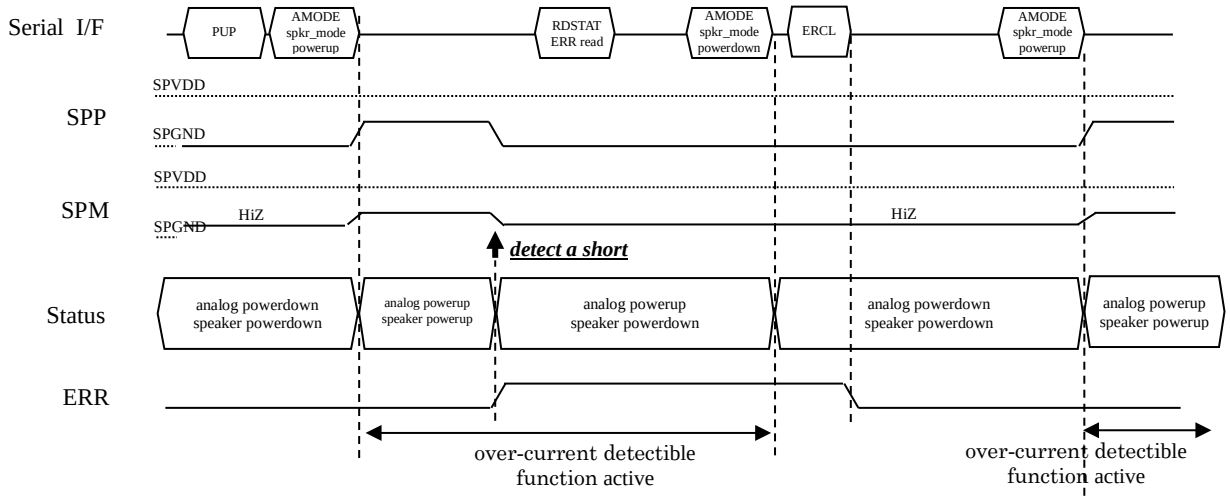
**Over-current detectible function at Speaker pins**

The over-current detectible function for the Speaker pins detect a short between SPP and SPM, and a short between SPP/SPM and GND.
The over-current detectible function is effective on speaker power-up by the AMODE command.




over-current detectible function for Speaker pins

When the over-current is detected, the speaker amplifier output pin(SPP/SPM) go to power-down forcibly, and a short error is informed by the ERR pin “H”.
In the case of error outbreak, please confirm a status of error by the RDSTAT command, stop playback, and set the speaker power-down by the AMODE command. Afterwards, please clear an error by the ERCL command.
If performing playback again, set the speaker power-up by the AMODE command, and next set the PLAY command.
However, when shorting to GND is going on, even if the following operation is done, the speaker amplifier output pin(SPP/SPM) go to power-down forcibly, and the ERR pin becomes “H”.
(1)After setting power-down by the AMODE command , do power-up by the AMODE command
(2)After detect a short error, when input ERCL command without power-down operation of speaker amplifier by the AMODE command




over-current detectible function Operation Flow
(Example)

**Command List**

Each command is configured in 1-byte (8-bit) units. Each of the AMODE, AVOL FADR, PLAY, MUON, and CVOL commands forms one command by two bytes.Be sure to input the following commands only.
Input each command with CBUSYB set to a ”H” level.

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description |
|---|---|---|---|---|---|---|---|---|---|
| PUP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WCM | Shifts the device currently powered down to a command wait state. Also the two-time command input mode is set by this command. |
| AMODE | 0 | 0 | 0 | 0 | 0 | 1 | HPF1 | HPF0 | Analog section control command.<br>Configures settings for power-up operation and analog input/output.<br>Selects the type of HPF. |
| | 0 | DAG1 | DAG0 | AIG1 | AIG0 | DAEN | SPEN | POP | |
| AVOL | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Analog mixing signal volume setting command. Use the data of the 2nd byte to specify volume. |
| | — | — | AV5 | AV4 | AV3 | AV2 | AV1 | AV0 | |
| FAD | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Sets the fade-in time in cases where the speaker amplifier is enabled by the AMODE command. |
| | 0 | 0 | 0 | 0 | FAD3 | FAD2 | FAD1 | FAD0 | |
| PDWN | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Shifts the device from a command wait state to a power-down state. |
| FADR | 0 | 0 | 1 | 1 | C1 | C0 | F9 | F8 | Playback phrase specification command.<br>Can be specified for each channel. |
| | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | |
| PLAY | 0 | 1 | 0 | 0 | C1 | C0 | F9 | F8 | Playback start command.<br>Use the data of the 2nd byte to specify a phrase number.<br>Can be specified for each channel. |
| | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | |
| START | 0 | 1 | 0 | 1 | CH3 | CH2 | CH1 | CH0 | Playback start command without phrase specification. Used to start playback on multiple channels at the same time after phrases are specified with the FADR command. After a phrase is played with the PLAY command, the same phrase can be played with this command. |
| STOP | 0 | 1 | 1 | 0 | CH3 | CH2 | CH1 | CH0 | Playback stop command.<br>Can be specified for each channel. |

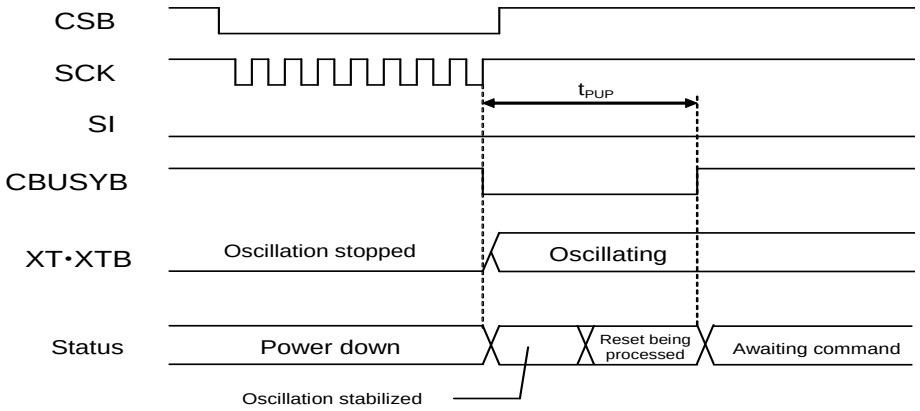
| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description |
|---|---|---|---|---|---|---|---|---|---|
| MUON | 0 | 1 | 1 | 1 | CH3 | CH2 | CH1 | CH0 | Silence insertion command. Use the data of the 2nd byte to specify the length of silence. Can be specified for each channel. |
| | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | |
| SLOOP | 1 | 0 | 0 | 0 | CH3 | CH2 | CH1 | CH0 | Repeat playback mode setting command. The setting is enabled during playback. Can be specified for each channel. |
| CLOOP | 1 | 0 | 0 | 1 | CH3 | CH2 | CH1 | CH0 | Repeat playback mode release command. When the STOP command is input, repeat playback mode is released automatically. Can be specified for each channel. |
| CVOL | 1 | 0 | 1 | 0 | CH3 | CH2 | CH1 | CH0 | Volume setting command. Use the data of the 2nd byte to specify volume. Can be specified for each channel. |
| | — | — | — | CV4 | CV3 | CV2 | CV1 | CV0 | |
| RDSTAT | 1 | 0 | 1 | 1 | 0 | 0 | 0 | ERR | Status serial read command. This command reads the command status and the status of the fail safe function for each channel. |
| OUTSTAT | 1 | 1 | 0 | 0 | 0 | BUSY/NCR | C1 | C0 | Status output command. This command outputs the command status of each channel from the STATUS pin. |
| SAFE | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Fail safe setting command. Sets settings for power supply voltage detection, temperature detection, and monitoring time. |
| | TM2 | TM1 | TM0 | TSD1 | TSD0 | BLD2 | BLD1 | BLD0 | |
| ERCL | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | This command clears error while the fail safe function is operating. |

**Description of Command Functions**

1. PUP command

| ・command | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WCM |
|---|---|---|---|---|---|---|---|---|

The PUP command is used to shift the ML22594 from a power down state to a command waiting state.
The ML22594 can only accept the PUP command while it is in a power down state. Therefore, in a power down state, the device will ignore any other command if entered.
The ML22594 enters a power down state under any of the following conditions:
1) When power is turned on
2) At RESETB input
3) When CBUSYB go to a “H” level after inputting the power down command




The WCM bit is used to set the two-time command input mode. When set to ”1”, the command input thereafter will be processed in two-time command input mode and becomes valid only when the first data input matches the second one.

| WCM | Two-time command input mode |
|---|---|
| 0 | No (initial value) |
| 1 | Yes |

The regulator starts operating after the PUP command is entered. Any command will be ignored if entered while oscillation is stabilized. However, if a “L” level is input to the RESETB pin, the LSI enters a power down state immediately.

Neither line output nor speaker output is enabled by the PUP command. Power up the analog section by the AMODE command.

2. AMODE command

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | HPF1 | HPF0 | 1st byte |
| 0 | DAG1 | DAG0 | AIG1 | AIG0 | DAEN | SPEN | POP | 2nd byte |

The AMODE command is used to configure various settings for the analog section.
If the PDWN command is input while the analog section is in the power-up state, the analog section enters a power down state under the setting conditions that were in effect when the analog section was powered up by the AMODE command. To perform a power-down operation using different conditions from those used at analog section power-up, set settings by the AMODE command.
To change the setting of DAEN/SPEN while the analog section is in the power-up state, first put the analog section into the power-down state and then put the analog section into the power-up state again by the AMODE command.
The detailed command settings are shown below.
Each setting is initialized upon reset release or by the PUP command.
Don't input the STOP command during the AMODE command is being proccessed (CBUSYB="L").
Input the AMODE command for analog section into the power-down state before the PDWN command is input.

The HPF1/HPF0 bits set the cut-off frequency of the HPF.

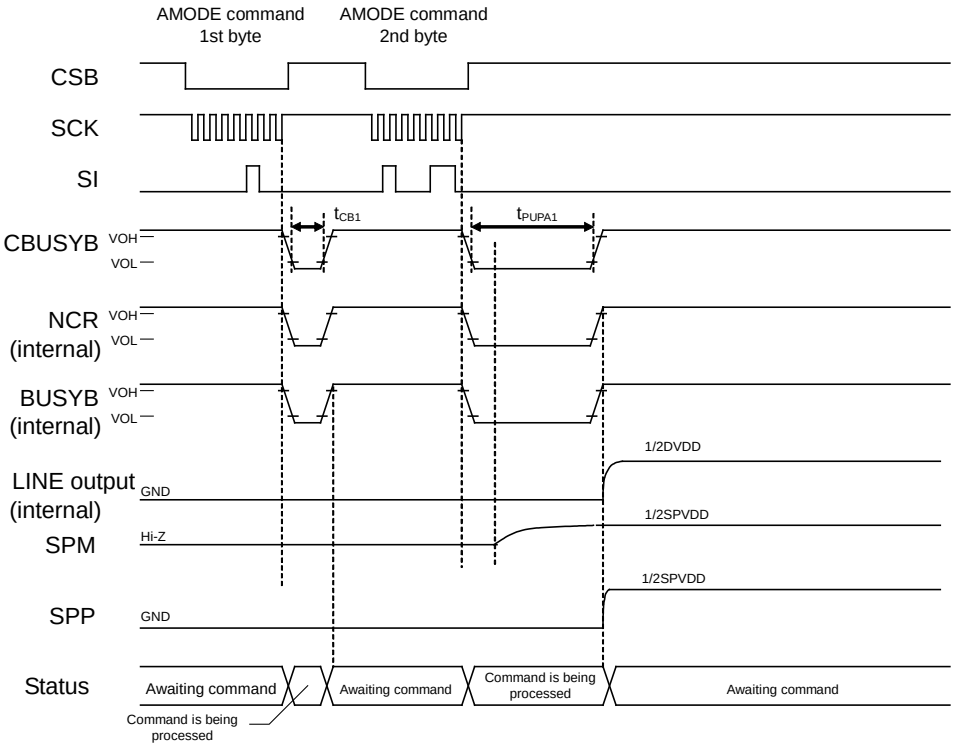
| HPF1 | HPF0 | Cut-off frequency |
|---|---|---|
| 0 | 0 | Off (initial value) |
| 0 | 1 | 200 Hz |
| 1 | 0 | 300 Hz |
| 1 | 1 | 400 Hz |

The POP bit specifies whether to suppress generation of "pop" noise.

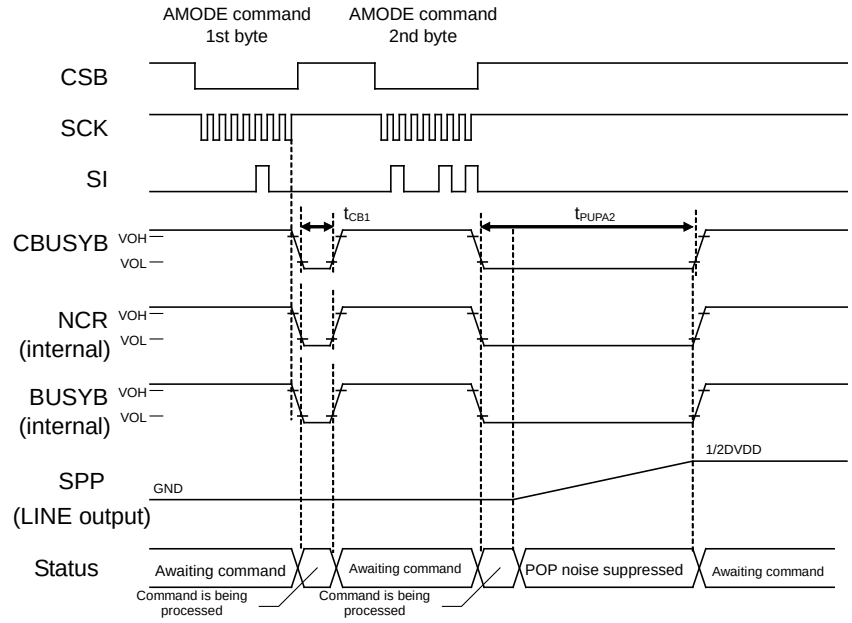
- If the bit is "0" (no pop noise suppression) and the DAEN bit is "1", the LINE output rises from the DGND level to the SG level in about 35 ms, at which time the analog section enters the power-up state. If the DAEN bit is "0", the LINE output falls from the SG level to the DGND level in about 110 ms, at which time the analog section enters the power down state.
- If the bit is "1" (with pop noise suppression) and the DAEN bit is "1", the LINE output rises from the DGND level to the SG level in about 90 ms, at which time the analog section enters the power-up state. If the DAEN bit is "0", the LINE output falls from the SG level to the DGND level in about 140 ms, at which time the analog section enters the power down state.

| POP | Pop noise suppression |
|---|---|
| 0 | No (initial value) |
| 1 | Yes |

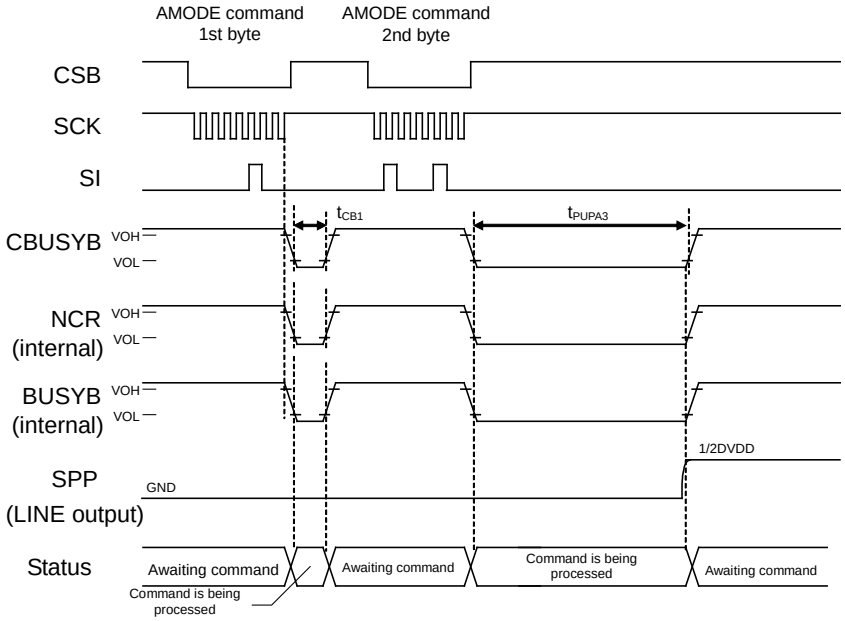
・ When powering up the speaker amplifier
Setting values: POP bit = “0”, DAEN and SPEN bits = “0” → “1”



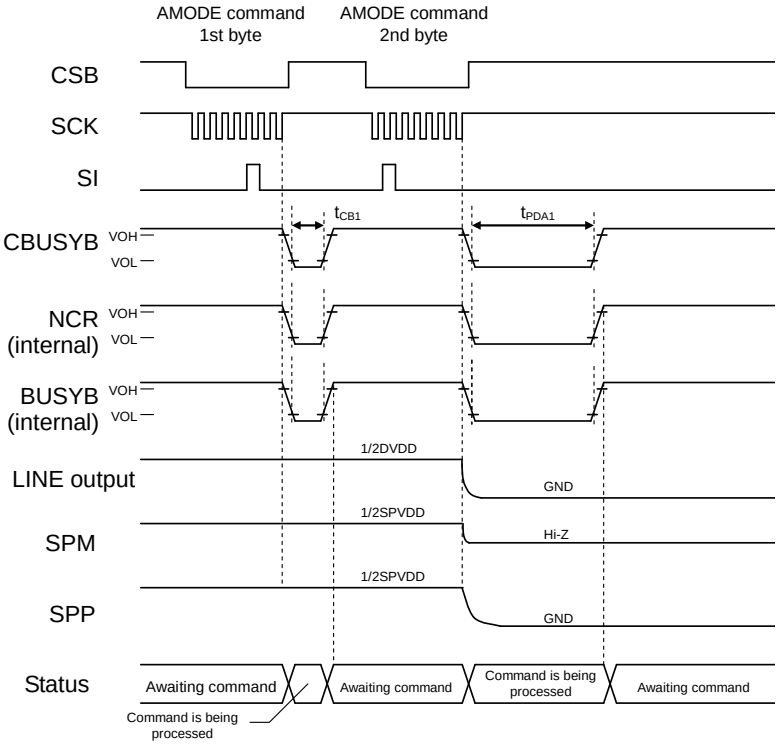

・ When powering up the line amplifier (with pop noise suppression)
Setting values: POP bit = “1”, DAEN bit = “0” → “1” (SPEN bit = “0”)



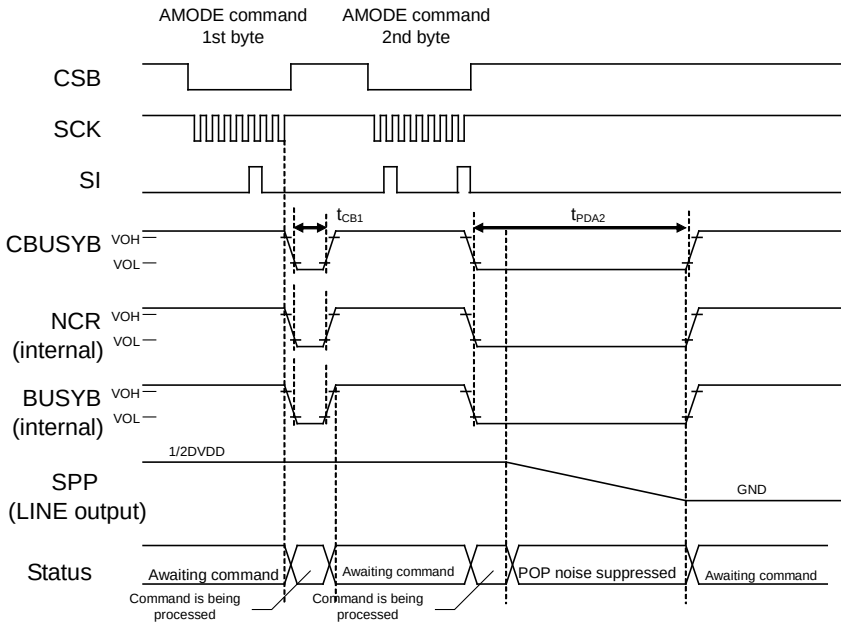
・ When powering up the line amplifier (without pop noise suppression)
Setting values: POP bit = “0”, DAEN bit = “0” → “1” (SPEN bit = “0”)



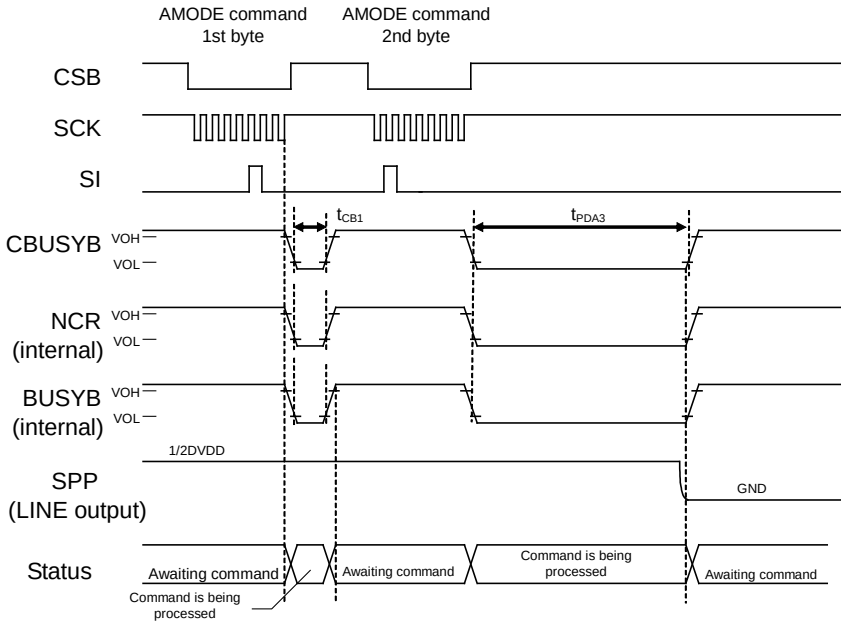

・ When putting the speaker amplifier into the power down state
Setting values: POP bit = “0”, DAEN and SPEN bits = “1” → “0”



・ When putting the line amplifier into the power down state (with pop noise suppression)
Setting values: POP bit = “1”, DAEN bit = “1” → “0” (SPEN bit = “0”)




・ When putting the line amplifier into the power down state (without pop noise suppression)
Setting values: POP bit = “0”, DAEN bit = “1” → “0” (SPEN bit = “0”)



The DAG1,0 bits are used to set the gain of the internal DAC signal. The AIG1,0 bits are used to set the gain of an analog signal from the AIN pin. DAG1,0 and AIG1,0 are only enabled when the speaker amplifier is used.

| DAG1 | DAG0 | Volume |
|---|---|---|
| 0 | 0 | Input OFF |
| 0 | 1 | Input ON (–6 dB) |
| 1 | 0 | Input ON (0 dB) (initial value) |
| 1 | 1 | Input ON (0 dB) (Setting prohibited) |

| AIG1 | AIG0 | Volume |
|---|---|---|
| 0 | 0 | Input OFF (initial value) |
| 0 | 1 | Input ON (–6 dB) |
| 1 | 0 | Input ON (0 dB) |
| 1 | 1 | Input ON (0 dB) (Setting prohibited) |

Input the analog signal from the AIN pin after the AMODE command (CBUSYB="H").

The DAEN bit takes power-up and power-down control of the DAC section.

| DAEN | Status of the DAC section |
|---|---|
| 0 | Power-down state (initial value) |
| 1 | Power-up state |

The SPEN bit takes power-up and power-down control of the speaker section.
When the SPEN bit = "0", the SPP pin is configured as a LINE output.

| SPEN | Status of the speaker section |
|---|---|
| 0 | Power-down state (initial value) |
| 1 | Power-up state |

Relationship between DAEN, SPEN, and POP signals and the analog section

| DAEN | SPEN | POP | Mode | Status |
|---|---|---|---|---|
| 0 | 0 | 0 | At speaker output | Power-down (initial value) |
| | | | At LINE output | Power-down (without pop noise suppression) |
| 0 | 0 | 1 | At speaker output | Power-down |
| | | | At LINE output | Power-down (with pop noise suppression) |
| — | 1 | — | Speaker output | DAC/speaker power-up |
| 1 | 0 | 0 | LINE output | DAC power-up (without pop noise suppression) |
| 1 | 0 | 1 | LINE output | DAC power-up (with pop noise suppression) |

Pin status during power down

The status of each output pin during power down by the AMODE command is shown below.

| Analog output pin | State |
|---|---|
| $V_{DDL}$ | DGND |
| $V_{DDR}$ | DGND |
| SG | DGND |
| SPM | Hi-Z |
| SPP | DGND |

3. AVOL commnd

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1st byte |
| 0 | 0 | AV5 | AV4 | AV3 | AV2 | AV1 | AV0 | 2nd byte |

The AVOL command is used to adjust the volume of the speaker amplifier. It is possible to input the AVOL command regardless of the status of the NCR signal.
The command enables 50-level adjustment of volume, as shown in the table below. When the PUP or AMODE command is input, the value set by the AVOL command is initialized (0 dB).

| AV5–0 | Volume | AV5–0 | Volume |
|---|---|---|---|
| 3F | +12dB | 1F | –8.0 |
| 3E | +11.5 | 1E | –9.0 |
| 3D | +11.0 | 1D | –10.0 |
| 3C | +10.5 | 1C | –11.0 |
| 3B | +10.0 | 1B | –12.0 |
| 3A | +9.5 | 1A | –13.0 |
| 39 | +9.0 | 19 | –14.0 |
| 38 | +8.5 | 18 | –16.0 |
| 37 | +8.0 | 17 | –18.0 |
| 36 | +7.5 | 16 | –20.0 |
| 35 | +7.0 | 15 | –22.0 |
| 34 | +6.5 | 14 | –24.0 |
| 33 | +6.0 | 11 | –26.0 |
| 32 | +5.5 | 12 | –28.0 |
| 31 | +5.0 | 11 | –30.0 |
| 30 | +4.5 | 10 | –32.0 |
| 2F | +4.0 | 0F | –34.0 |
| 2E | +3.5 | 0E | OFF |
| 2D | +3.0 | 0D | OFF |
| 2C | +2.5 | 0C | OFF |
| 2B | +2.0 | 0B | OFF |
| 2A | +1.5 | 0A | OFF |
| 29 | +1.0 | 09 | OFF |
| 28 | +0.5 | 08 | OFF |
| 27 | +0.0 (initial value) | 07 | OFF |
| 26 | –1.0 | 06 | OFF |
| 25 | –2.0 | 05 | OFF |
| 24 | –3.0 | 04 | OFF |
| 23 | –4.0 | 03 | OFF |
| 22 | –5.0 | 00 | OFF |
| 21 | –6.0 | 01 | OFF |
| 20 | –7.0 | 00 | OFF |

4. FAD command

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1st byte |
| 0 | 0 | 0 | 0 | FAD3 | FAD2 | FAD1 | FAD0 | 2nd byte |

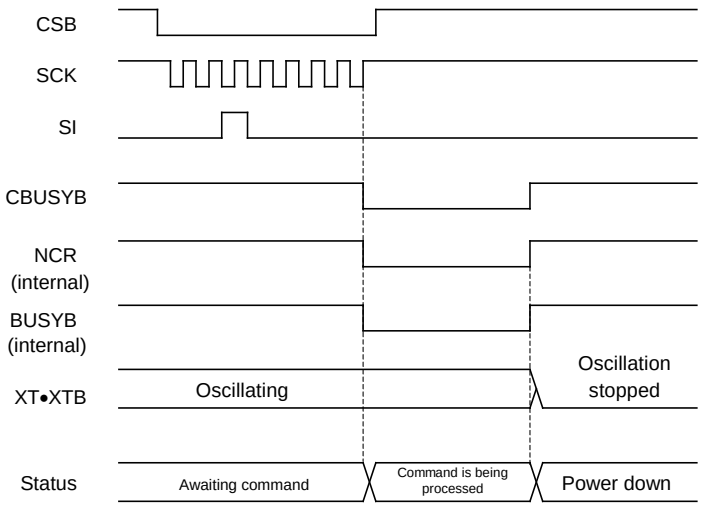
The FAD command is used to set the fade-in time for the speaker amplifier.
The fade-in time cna be adjusted through 16 levels, as shown in the table below. The initial value after reset is 298 μs. When the PUP command is input, the value set by the FAD command is initialized (298 μs).

| FAD3–0 | Fade-in time (μs) |
|---|---|
| F | 442 |
| E | 422 |
| D | 401 |
| C | 381 |
| B | 360 |
| A | 340 |
| 9 | 319 |
| 8 | 298 (initial value) |
| 7 | 278 |
| 6 | 257 |
| 5 | 237 |
| 4 | 216 |
| 3 | 195 |
| 2 | 175 |
| 1 | 154 |
| 0 | 134 |

5. PDWN command

| ・command | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

The PDWN command is used to shift the ML22594 from a command waiting state to the power down state. However, since every setting will be initialized after entering the power down state, initial settings need to be set after power-up. This command is invalid during playback.
To resume playback after the ML22594 has shifted to the power down state, first input the PUP and AMODE commands and then input the PLAY command.




Oscillation stops after a lapse of command processing time after the PDWN command is input. The regulator stops operation after a lapse of command processing time after the PDWN command is input. At this time, the SPM output of the speaker amplifier goes into a Hi-Z state to prevent generation of pop noise.

Initial stauts at reset input and status during power down
The status of each output pin is as follows:

| Analog output pin | State |
|---|---|
| $V_{DDL}$ | DGND |
| $V_{DDR}$ | DGND |
| SG | DGND |
| SPM | Hi-Z |
| SPP | DGND |

6. FADR command

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | C1 | C0 | F9 | F8 | 1st byte |
| F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 2nd byte |

The FADR command is used to specify a phrase to be played. A playback channel and a playback phrase are set by this command. The FADR command can be set for each channel; however, the command cannot be input for multiple channels simultaneously. Input the FADR command with each NCR set to a "H" level.
When a playback phrase is specified for each channel, use the START command to start playback.
Since it is possible to specify a playback phrase (F9–F0) at the time of creating a ROM that stores voice data, specify the phrase that was specified when the ROM was created.

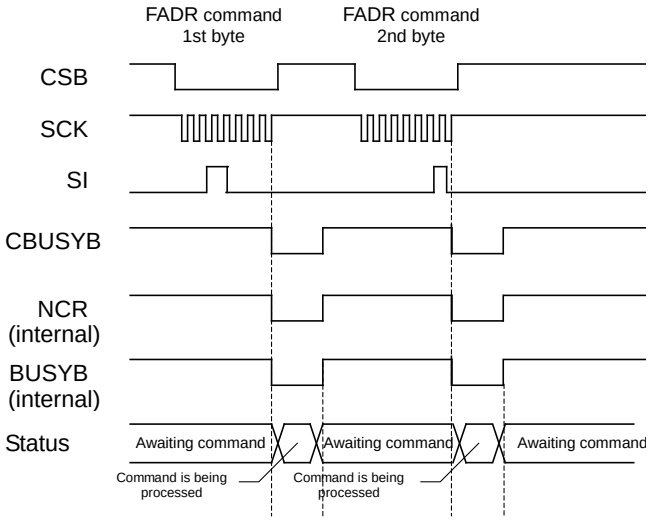
Number of phrase ( Internal ROM and External ROM )

| | Number of phrase | F9-F0 |
|---|---|---|
| Internal ROM | 512 | 000h – 1FFh |
| External ROM | 512 | 200h – 3FFh |

Channel settings

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | Channel 0 |
| 0 | 1 | Channel 1 |
| 1 | 0 | Channel 2 |
| 1 | 1 | Channel 3 |

The diagram below shows the timing for specifying (F9–F0) = 02H as the phrase to play on channel 1.

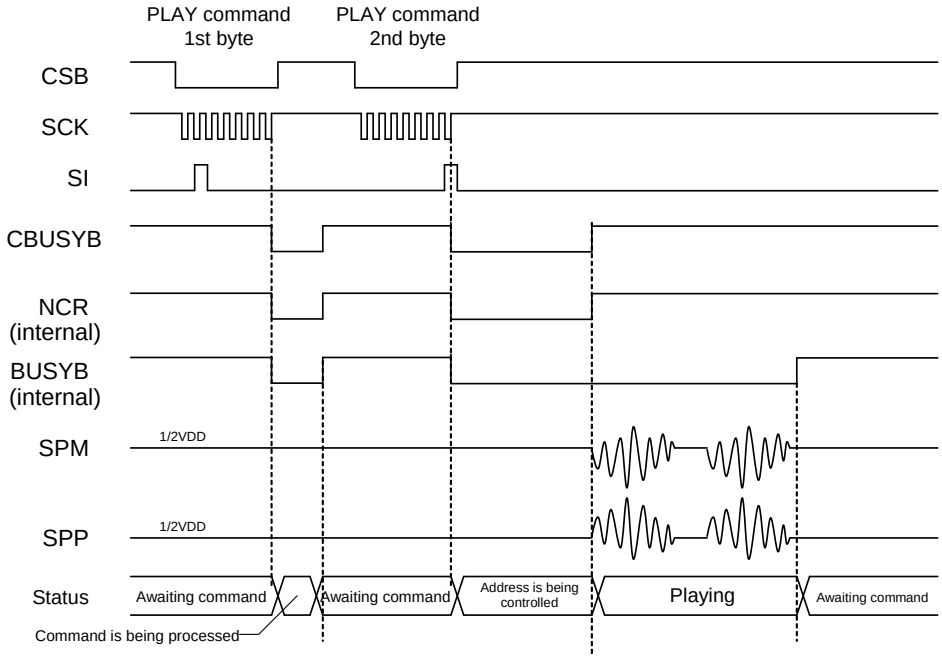


7. PLAY command

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | C1 | C0 | F9 | F8 | 1st byte |
| F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 2nd byte |

The PLAY command is used to start playback with phrase specified. This command can be input when the NCR signal on the target channel is at a "H" level.
Since it is possible to specify a playback phrase (F9–F0) at the time of creating a ROM that stores voice data, specify the phrase that was specified when the ROM was created.
The figure below shows the timing of phrase (F9–F0 = 01H) playback.




When the 1st byte of the PLAY command is input, the device enters a state awaiting input of the 2nd byte of the PLAY command after a lapse of command processing time. When the 2nd byte of PLAY command is input, after a lapse of command processing time, the device starts reading from the ROM the address information of the phrase to be played. Thereafter, playback operation starts, the playback is performed up to the specified ROM address, and then the playback terminates automatically.
The NCR signal is at a "L" level during address control, and goes "H" when the address control is finished and playback starts. When the NCR signal on the target channel goes "H", it is possible to input the PLAY command for the next playback phrase.
During address control, the BUSYB signal is at a "L" level during playback and goes "H" when playback is finished. Whether the playback is going on can be known by the BUSYB signal.

Number of phrase ( Internal ROM and External ROM )

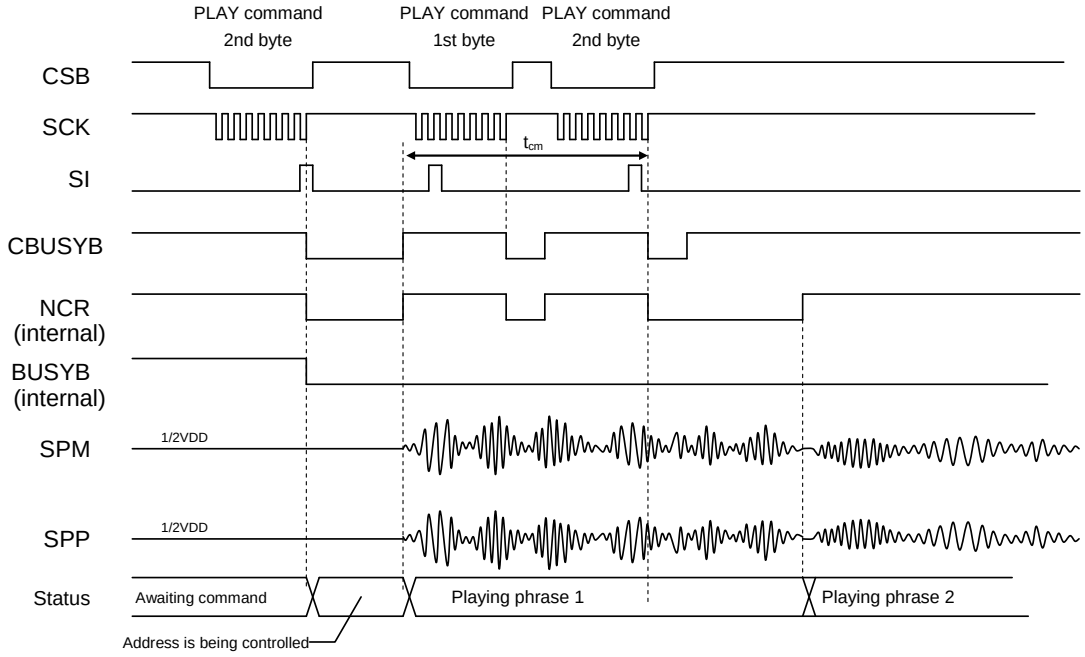
| | Number of phrase | F9-F0 |
|---|---|---|
| Internal ROM | 512 | 000h – 1FFh |
| External ROM | 512 | 200h – 3FFh |

Channel settings

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | Channel 0 |
| 0 | 1 | Channel 1 |
| 1 | 0 | Channel 2 |
| 1 | 1 | Channel 3 |

PLAY Command Input Timing for Continuous Playback

The diagram below shows the PLAY command input timing in cases where one phrase is played and then the next phrase is played in succession.




As shown in the diagram above, if performing continuous playback, input the PLAY command for the second phrase within 10 ms ($t_{cm}$) after the NCR signal on the target channel goes “H”. Input the following PLAY command after checking that playback is completed by the RDSTAT command, when it is not continuous playback.

8. START command

・command

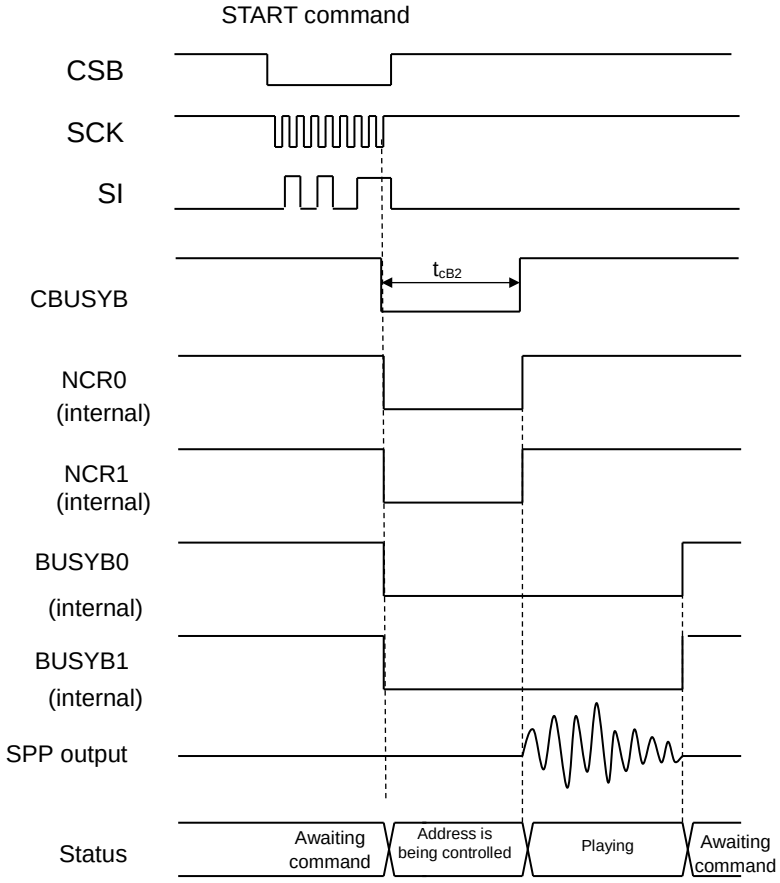
| 0 | 1 | 0 | 1 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|

The START command is a channel synchronization start (i.e., starts phrase playback on multiple channels simultaenously) command. It is necessary to specify playback phrases using the FADR command before inputting the START command. Setting any bit(s) from CH0 to CH3 to "1" starts playback on the corresponding channel(s). Input the START command with each NCR set to a "H" level.
The figure below shows the timing when starting playback on channel 00 and channel 1 simultaneously.

Channel settings

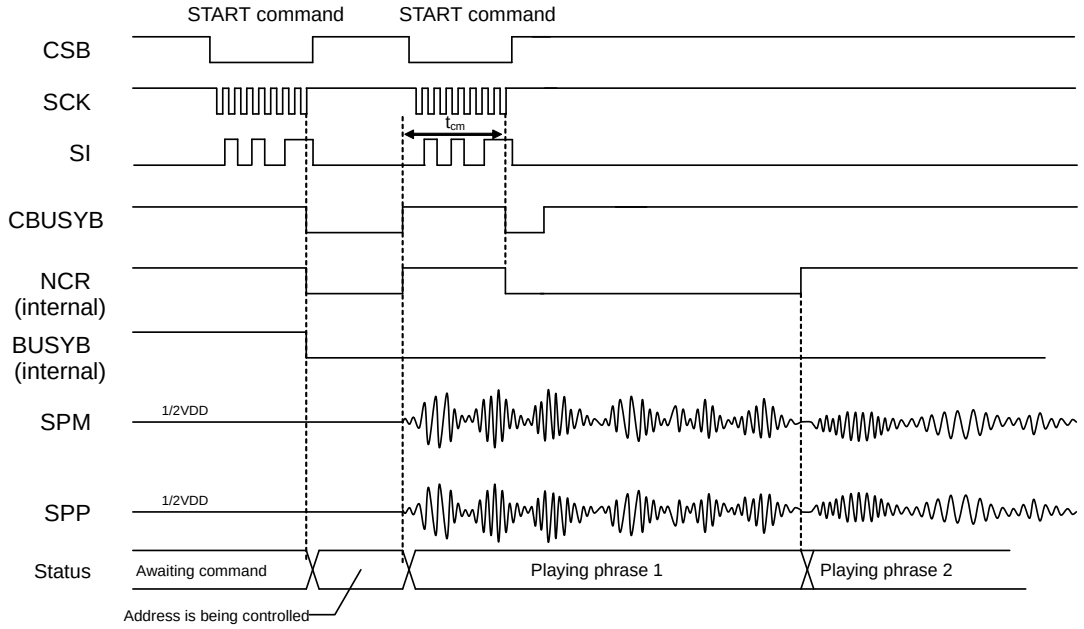
| | Channel |
|---|---|
| CH0 | Setting this bit to "1" starts playback on channel 0. |
| CH1 | Setting this bit to "1" starts playback on channel 1. |
| CH2 | Setting this bit to "1" starts playback on channel 2. |
| CH3 | Setting this bit to "1" starts playback on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).



START Command Input Timing for Continuous Playback

The diagram below shows the START command input timing in cases where one phrase is played and then the next phrase is played in succession.



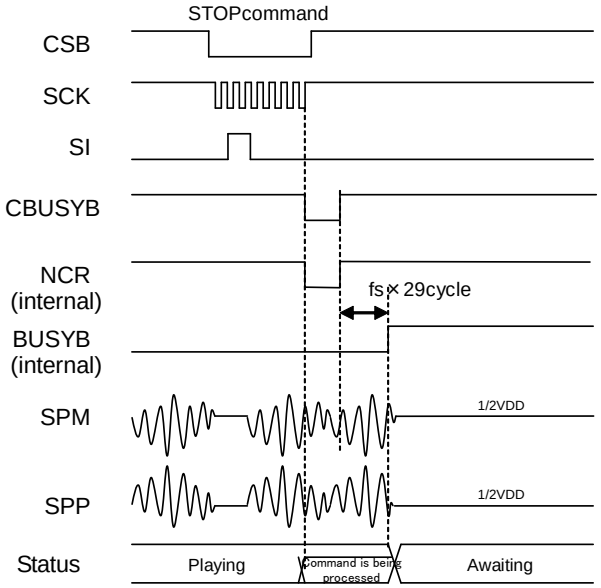

As shown in the diagram above, if performing continuous playback, input the START command for the second phrase within 10 ms ($t_{cm}$) after the NCR signal on the target channel goes “H”. Input the following START command after checking that playback is completed by the RDSTAT command, when it is not continuous playback.

9. STOP command

・command

| 0 | 1 | 1 | 0 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|

The STOP command is used to stop playback. It can be set for each channel. Setting any bit(s) from CH0 to CH3 to "1" stops playback on the corresponding channel(s). If the speech synthesis processing for all channels stops, the AOUT output goes to the $V_{SG}$ level and the NCR and BUSYB signals go to a "H" level.
Although it is possible to input the STOP command regardless of the status of NCR during playback, a prescribed command interval time needs taking.




Channel settings

| | Channel |
|---|---|
| CH0 | Setting this bit to "1" stops playback on channel 0. |
| CH1 | Setting this bit to "1" stops playback on channel 1. |
| CH2 | Setting this bit to "1" stops playback on channel 2. |
| CH3 | Setting this bit to "1" stops playback on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).

The STOP command allows specifying multiple channels at one time.

10. MUON command

・command

| 0 | 1 | 1 | 1 | CH3 | CH2 | CH1 | CH0 | 1st byte |
|---|---|---|---|---|---|---|---|---|
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | 2nd byte |

The MUON command allows inserting a silence between two playback phrases. The command can be input when the NCR signal on the target channel is at a "H" level.
Set the silence time length after inputting this command. It can be set for each channel. The MUON command allows specifying multiple channels at one time. Setting any bit(s) from CH0 to CH3 to "1" plays silence on the corresponding channel(s).

Channel settings

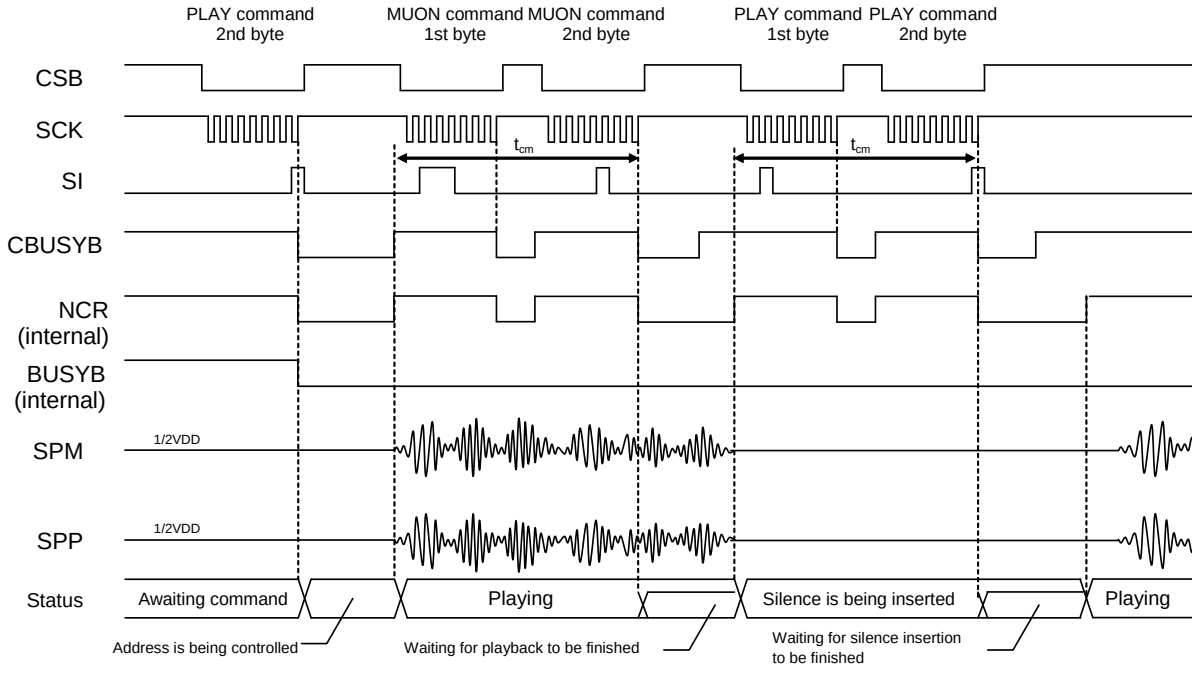
| | Channel |
|---|---|
| CH0 | Setting this bit to "1" inserts a silence on channel 0. |
| CH1 | Setting this bit to "1" inserts a silence on channel 1. |
| CH2 | Setting this bit to "1" inserts a silence on channel 2. |
| CH3 | Setting this bit to "1" inserts a silence on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).

As the silence length (M7–M0), a value between 20 ms and 1024 ms can be set at 4 ms intervals (252 steps in total).
The equation to set the silence time length is shown below.
The silence length (M7–M0) must be set to 04h or higher.

$$t_{mu}=(2^7\times(M7)+2^6\times(M6)+2^5\times(M5)+2^4\times(M4)+2^3\times(M3)+2^2\times(M2)+2^1\times(M1)+2^0\times(M0)+1)\times 4ms$$

The figure below shows the timing of inserting a silence of 20 ms between the repetitions of a phrase of (F7–F0) = 01h.



When the PLAY command is input, the address control over phrase 1 ends, the phrase playback starts, and the CBUSYB and NCR signals go to a “H” level. Input the MUON command after this CBUSYB signal changes to a “H” level. After the MUON command input, the NCR signal remains “L” until the end of phrase 1 playback, and the device enters a state waiting for the phrase 1 playback to terminate.
When the phrase 1 playback is terminated, the silence playback starts and the NCR signal goes to a “H” level. After the NCR signal has gone to a “H” level, re-input the PLAY command in order to play phrase 1.
After the PLAY command input, the NCR signal once again goes to a “L” level and the device enters a state waiting for the termination of silence playback.
When the silence playback is terminated and then the phrase 1 playback starts, the NCR signal goes “H”, and the device enters a state where it is possible to input the next PLAY or MUON command.
The BUSYB signal remains “L” until the end of a series of playback.

As shown in the diagram above, if performing continuous playback, input the MUON/PLAY/START command for the second phrase within 10 ms ($t_{cm}$) after the NCR signal on the target channel goes “H”. Input the following MUON/PLAY/START command after checking that playback is completed by the RDSTAT command, when it is not continuous playback.

11. SLOOP command

・command

| 1 | 0 | 0 | 0 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|

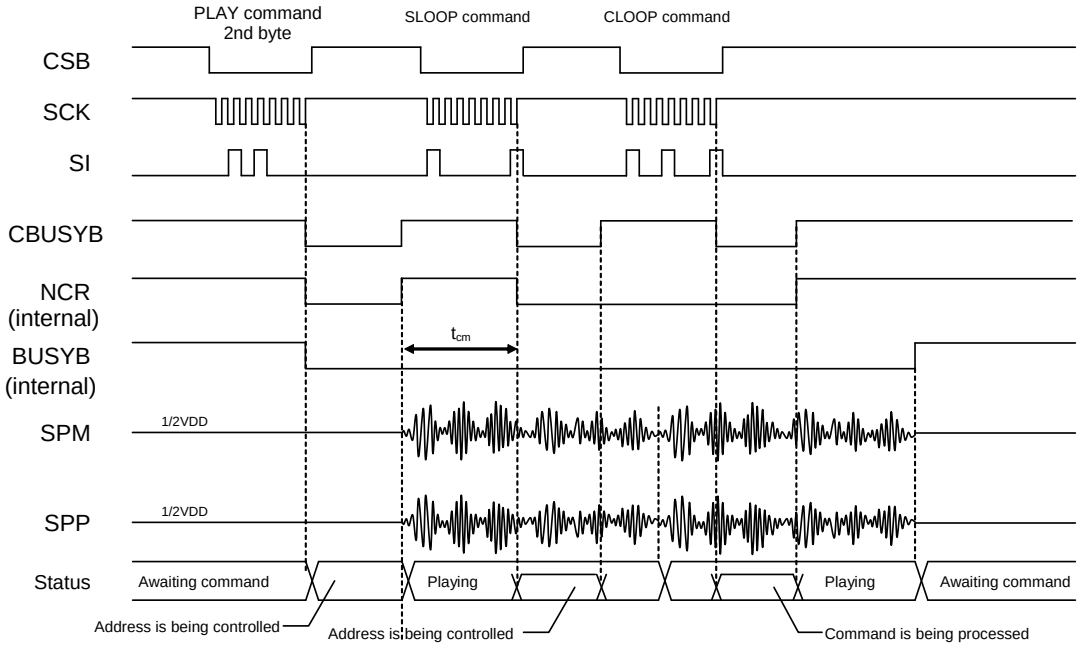
The SLOOP command is used to set repeat playback mode. The command can be input for each channel. The SLOOP command allows specifying multiple channels at one time. Setting any bit(s) from CH0 to CH3 to "1" repeats playback on the corresponding channel(s). Input the SLOOP command with each NCR set to a "H" level.

Channel settings

| | Channel |
|---|---|
| CH0 | Setting this bit to "1" repeats playback on channel 0. |
| CH1 | Setting this bit to "1" repeats playback on channel 1. |
| CH2 | Setting this bit to "1" repeats playback on channel 2. |
| CH3 | Setting this bit to "1" repeats playback on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).

Once repeat playback mode is set, the current phrase is repeatedly played until the repeat playback setting is released by the SLOOP command or until playback is stopped by the STOP command. In the case of a phrase that was edited using the edit function, the edited phrase is repeatedly played. Following shows the SLOOP command input timing.




Effective Range of SLOOP Command Input

The SLOOP command is only enabled during playback. After the PLAY command is input, input the SLOOP command within 10 ms ($t_{cm}$) after the NCR signal on the target channel goes "H". This will enable the SLOOP command, so that repeat playback will be carried out. The NCR signal remains "L" during repeat playback mode.

12. CLOOP command

・command

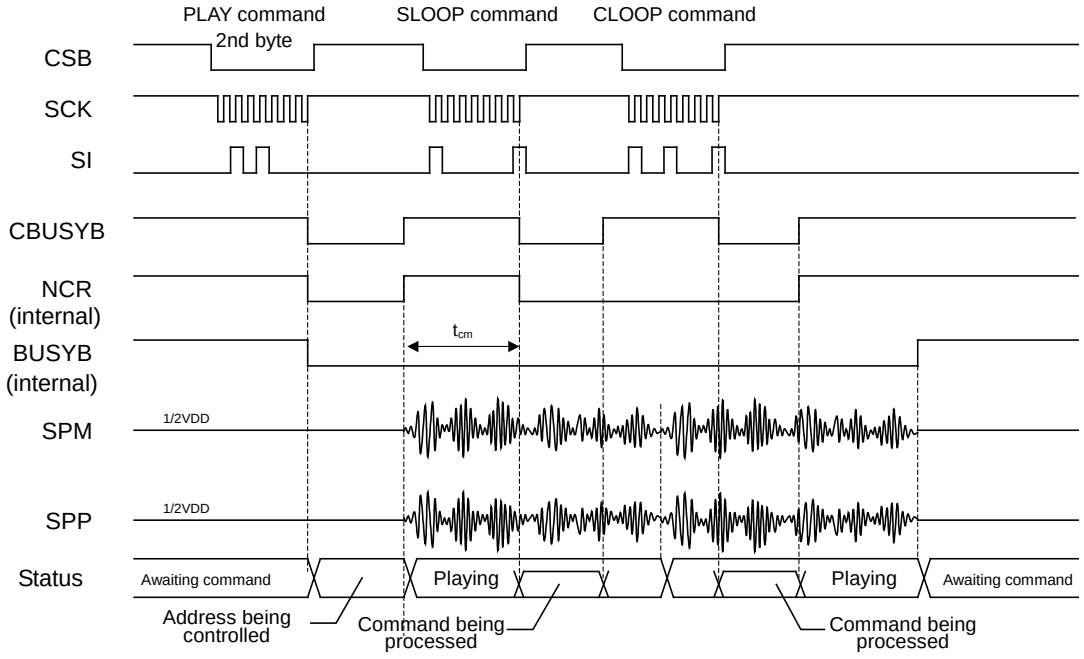
| 1 | 0 | 0 | 1 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|

The CLOOP command releases repeat playback mode. The command can be input for each channel. The CLOOP command allows specifying multiple channels at one time. Setting any bit(s) from CH0 to CH3 to "1" releases repeat playback on the corresponding channel(s). When repeat playback mode is released, the NCR signal goes "H".
It is possible to input the CLOOP command regardless of the status of the NCR signal during playback, but a prescribed command interval needs taking.

Channel settings

| | Channel |
|---|---|
| CH0 | Setting this bit to "1" releases repeat playback on channel 0. |
| CH1 | Setting this bit to "1" releases repeat playback on channel 1. |
| CH2 | Setting this bit to "1" releases repeat playback on channel 2. |
| CH3 | Setting this bit to "1" releases repeat playback on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).



13. CVOL command

・command

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | CH3 | CH2 | CH1 | CH0 | 1st byte |
| 0 | 0 | 0 | CV4 | CV 3 | CV 2 | CV 1 | CV 0 | 2nd byte |

The CVOL command is used to adjust the playback volume on each channel. It is possible to input the VOL command regardless of the status of the NCR signal.
The CVOL command can be set for each channel. The CVOL command allows specifying multiple channels at one time. Setting any bit(s) from CH0 to CH3 to "1" sets the playback volume on the corresponding channel(s). The volume setting is initialized by the AMODE command.

Channel settings

| | Channel |
|---|---|
| CH0 | Setting this bit to "1" sets the volume on channel 0. |
| CH1 | Setting this bit to "1" sets the volume on channel 1. |
| CH2 | Setting this bit to "1" sets the volume on channel 2. |
| CH3 | Setting this bit to "1" sets the volume on channel 3. |

Be sure to set the channel setting bits( CH0-CH3).

The command enables 32-level adjustment of volume, as shown in the table below. The initial value after reset release is set to 0 dB. Upon reset release or when the PUP command is input, the values set by the CVOL command are initialized.

| CV4–0 | Volume | CV4–0 | Volume |
|---|---|---|---|
| 1F | 0 dB (initial value) | 0F | –6.31 |
| 1E | –0.28 | 0E | –6.90 |
| 1D | –0.58 | 0D | –7.55 |
| 1C | –0.88 | 0C | –8.24 |
| 1B | –1.20 | 0B | –9.00 |
| 1A | –1.53 | 0A | –9.83 |
| 19 | –1.87 | 09 | –10.74 |
| 18 | –2.22 | 08 | –11.77 |
| 17 | –2.59 | 07 | –12.93 |
| 16 | –2.98 | 06 | –14.26 |
| 15 | –3.38 | 05 | –15.85 |
| 14 | –3.81 | 04 | –17.79 |
| 13 | –4.25 | 03 | –20.28 |
| 12 | –4.72 | 02 | –23.81 |
| 11 | –5.22 | 01 | –29.83 |
| 10 | –5.74 | 00 | OFF |

14. RDSTAT command

・command

| 1 | 0 | 1 | 1 | 0 | 0 | 0 | ERR |
|---|---|---|---|---|---|---|---|

The RDSTAT command enables reading the status of internal operation. It is possible to input the CLOOP command regardless of the status of the NCR signal during playback, but a prescribed command interval needs taking.
The ERR bit selects reading the playback status for each channel or reading the status of the fail-safe function.
Keep the SI pin to “L” when read the status.

| ERR | Content of data to read |
|---|---|
| 0 | NCR and BUSYB signals for each channel (Initial value) |
| 1 | Status of the fail-safe function |

If the ERR bit is set to ”0”, the following status will be read:

| Output bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Output data | BUSYB3 | BUSYB2 | BUSYB1 | BUSYB0 | NCR3 | NCR2 | NCR1 | NCR0 |

When the ERR bit = ”0”, the NCR and BUSYB signals of each channel are read. The NCR signal outputs a “L” level while this LSI is performing command processing and goes to a “H” level when the LSI enters a command waiting state. The BUSY signal outputs a “L” level during voice playback.
The table below shows the contents of each data output at a status read.

| | Output status signal |
|---|---|
| BUSY3 | Channel 3 BUSYB output |
| BUSY2 | Channel 2 BUSYB output |
| BUSY1 | Channel 1 BUSYB output |
| BUSY0 | Channel 0 BUSYB output |
| NCR3 | Channel 3 NCR output |
| NCR2 | Channel 2 NCR output |
| NCR1 | Channel 1 NCR output |
| NCR0 | Channel 0 NCR output |

If the ERR bit is set to “1”, the following status will be read

| Output bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| OutPut data | 0 | 0 | EXR ERR | SPM ERR | SPP ERR | TSD ERR | BLD ERR | WCM ERR |

When the ERR bit=”1”, the state of six fail-safe Function is read.
If any of fail-safe function is activated,the ERR pin is set to a “H” level and the corresponding error bit is set to “1”. If the ERR pins set to a “H” level,
check the error contents using the RDSTAT command and take appropriate measures.
ERR bit is cleared by ERCL command

| Error signal | Error contents |
|---|---|
| EXRERR | External ROM read err bit.<br>This bit is set to “1” if the voice control area data of External ROM is “00h”.<br>It becomes an error when it accesses the External ROM under the condition that the External ROM isn't connected. |
| SPMERR | SPM pin short error bit.<br>This bit is set to “1” if the SPM pin is short to SPP pin or GND |
| SPPERR | SPP pin short error bit<br>This bit is set to “1” if the SPP pin is short to SPM pin or GND |
| TSDERR | High temperature error bit.<br>This bit is set to “1” if the temperature of the LSI reaches or exceeds the temperature set by the SAFE command. For details see the section on the SAFE command. |
| BLDERR | Power supply voltage error bit.<br>This bit is set to “1” if the power supply voltage level reaches or falls below the voltage set by the SAFE command. For details see the section on the SAFE command. |
| WCMERR | Command tansfer errro bit.<br>This bit is set to “1” if a transfer error occurs in two-time command input mode. |

15. OUTSTAT command

・command

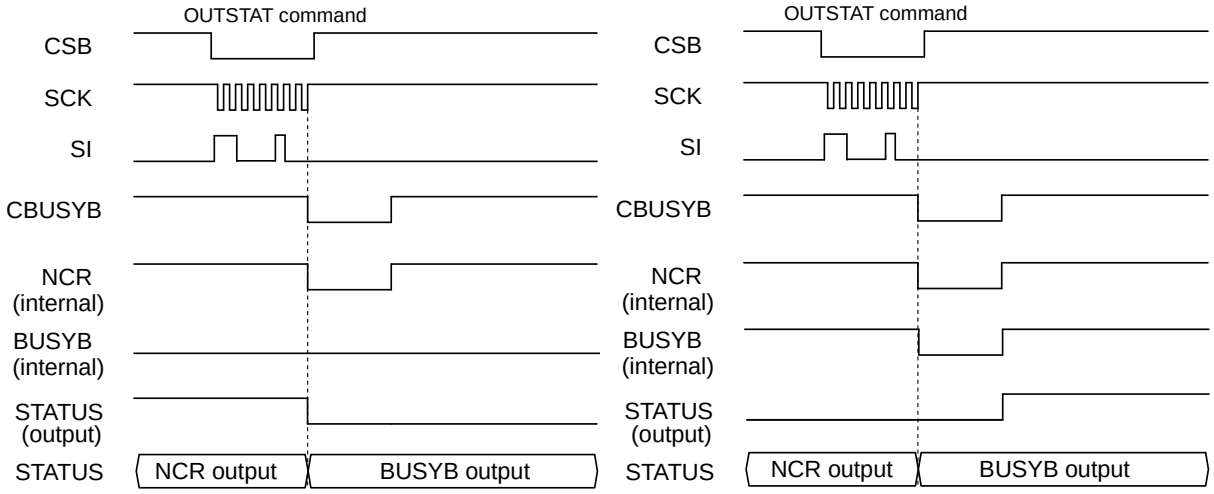
| 1 | 1 | 0 | 0 | 0 | BUSY/NCR | C1 | C0 |
|---|---|---|---|---|---|---|---|

The OUTSTAT command is used to output the BUSYB or NCR signal on the specified channel from the STATUS pin. It is possible to input the CLOOP command regardless of the status of the NCR signal during playback, but a prescribed command interval needs taking.

| BUSY/NCR | STATUS pin status |
|---|---|
| 0 | Outputs the NCR signal on the specified channel. |
| 1 | Outputs the BUSYB signal on the specified channel. |

Channel settings

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | Channel 0 (initial value) |
| 0 | 1 | Channel 1 |
| 1 | 0 | Channel 2 |
| 1 | 1 | Channel 3 |



16. SAFE command

・command

| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|
| TM2 | TM1 | TM0 | TSD1 | TSD0 | BLD2 | BLD1 | BLD0 |

The SAFE command is sets the settings for the low-voltage detection and temperature detection functions.
The BLD2–0 bits are used to set the power supply voltage detection level. The judgment voltage can be selected from among six levels from 2.7 to 4.0 V. The power supply voltage is monitored each time it reaches the value set by TM2–0, and if the power supply voltage reaches or falls below the set detection voltage two times or more, the ERR pin outputs a ”H” level and the RDSTAT command’s BLDERR bit is set to ”1”.
If the ERR pin is set to a ”H” level, check the error contents using the RDSTAT command. If the BLDERR bit is at ”1”, it is possibly a power supply related failure.

| BLD2 | BLD1 | BLD0 | Judgment power supply voltage |
|---|---|---|---|
| 0 | 0 | 0 | OFF |
| 0 | 0 | 1 | 2.7V±5% (initial value) |
| 0 | 1 | 0 | 3.0V±5% |
| 0 | 1 | 1 | 3.3V±5% |
| 1 | 0 | 0 | 3.6V±5% |
| 1 | 0 | 1 | 4.0V±5% |
| 1 | 1 | 0 | (4.0V±5%) |
| 1 | 1 | 1 | (4.0V±5%) |

The TSD1–0 bits are used to set the temperature detection level. Tj=140°C or OFF can be selected as the judgment temperature. The temperature is monitored each time it reaches the value set by TM2–0, and if the temperature reaches or exceeds the set value two times or more, the ERR pin outputs a ”H” level and the RDSTAT command’s TSDERR bit is set to ”1”.
If the ERR pin is set to a ”H” level, check the error contents using the RDSTAT command. If the TSDERR bit is at ”1”, reduce the volume using the AVOL command or put the analog section into the power down state using the AMODE command.

| TSD1 | TSD0 | Judgment temperature (Tj) |
|---|---|---|
| 0 | 0 | OFF |
| 0 | 1 | Setting prohibited |
| 1 | 0 | Setting prohibited |
| 1 | 1 | 140±10°C (initial valle,) |

The judgment temperature(Tj) is 140±10°C. This LSI is beyond Tj=130°C in the operating temperature(-40°C - +150°C) depending on a operating condition and occurs by a high temperature error. The ambient temperature at that case is as follows.

| Power supply($D^{VDD}$=$SP^{VDD}$) | Power dissipation($P_D$) | Amient temperature(Ta) |
|---|---|---|
| 4.5V | 0.686W | Not detect in the operating temperature |
| 5.0V | 0.861W | detect more than 104°C |
| 5.5V | 1.055W | detect more than 98°C |

* $\theta$ ja＝31.2[°C/W](JEDEC 2layers(refer to 67pages)), 1W/8ohm-Speaker

$\theta$ ja changes by an implementation condition. The maximum ambient temperature(Tamax) that this LSI does not detect the high temperature error is calculated in the following expressions in using the power dissipation.

$$Tamax = 130[°C] - \theta ja[°C/W] \times P_D[W]$$

The maximum ambient temperature(Tamax) in power supply voltage 5.0V and $\theta$ ja=36[°C/W] is as follows.

$$Tamax = 130[°C] - 36 \times 0.861 \fallingdotseq 99[°C]$$

The TM2–0 bits are used to set the monitor interval to detect a low voltage or temperature.

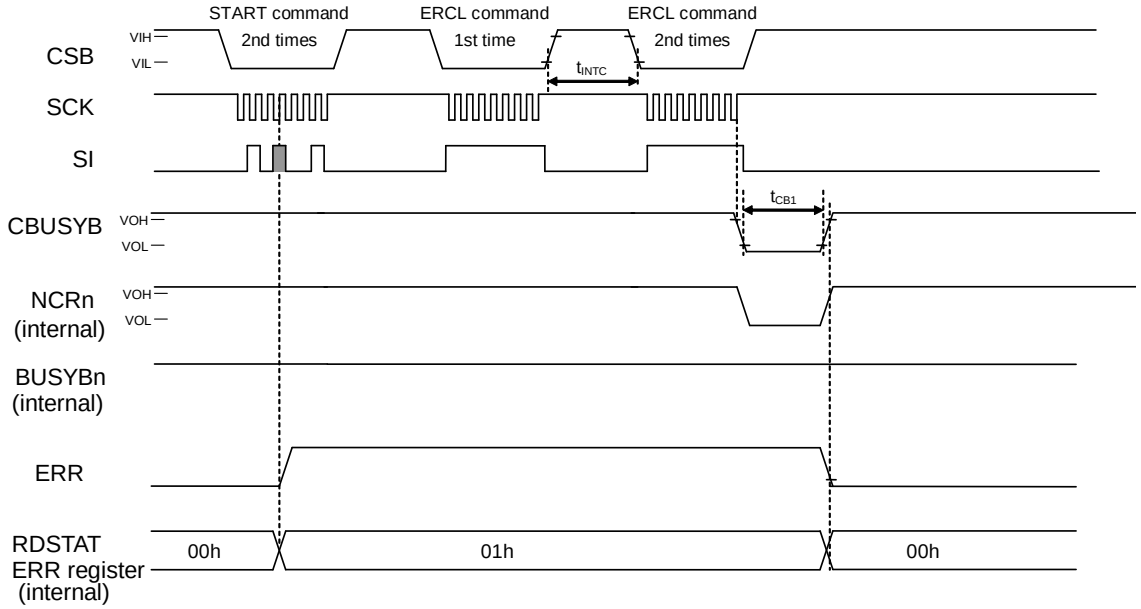
| TM2 | TM1 | TM0 | Monitor interval |
|---|---|---|---|
| 0 | 0 | 0 | Constantly monitors |
| 0 | 0 | 1 | 2 ms (initial value) |
| 0 | 1 | 0 | 4 ms |
| 0 | 1 | 1 | 8 ms |
| 1 | 0 | 0 | 16 ms |
| 1 | 0 | 1 | 32 ms |
| 1 | 1 | 0 | 64 ms |
| 1 | 1 | 1 | 128 ms |

17. ERCL command

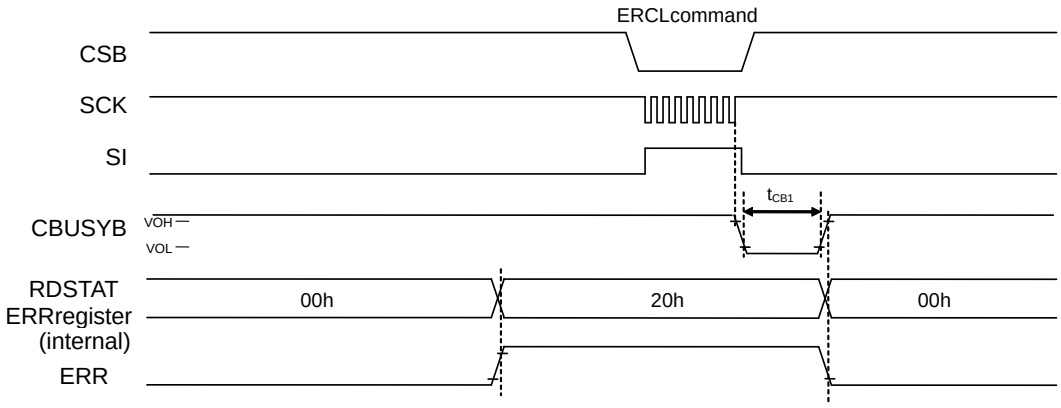
| ・command | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|

The ERCL command is used to clear an error if it occurs.
If an error occurs, a “H” level is outputted from the ERR pin. When the ERCL command is inputted, the ERR pin outputs a ”L” level.
However, when the high temperature error and the power-supply voltage error continue, TSDERR of the RDSTAT command , BLDERR of the RDSTAT command and the ERR pin keep outputting "H" even if the ERCL command is inputted.

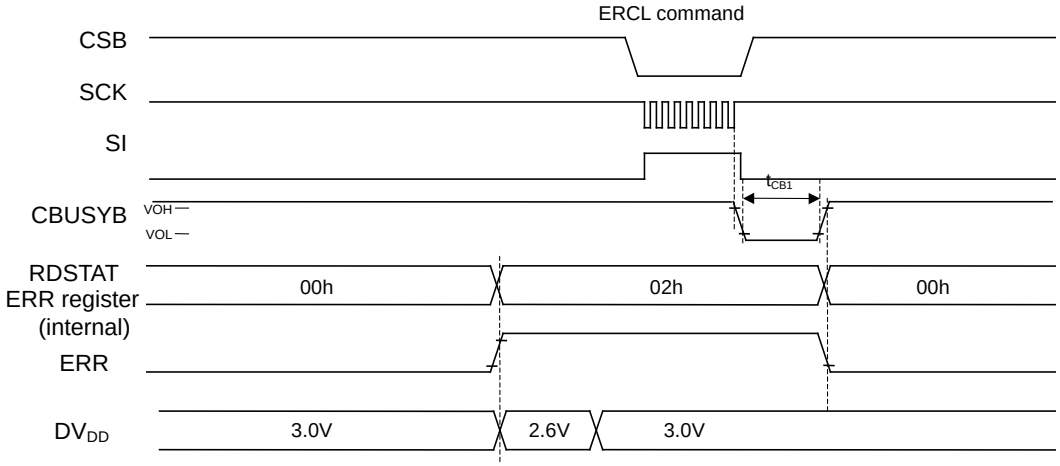
Timing diagram for when an error occurs at the time of setting the two-time command input mode



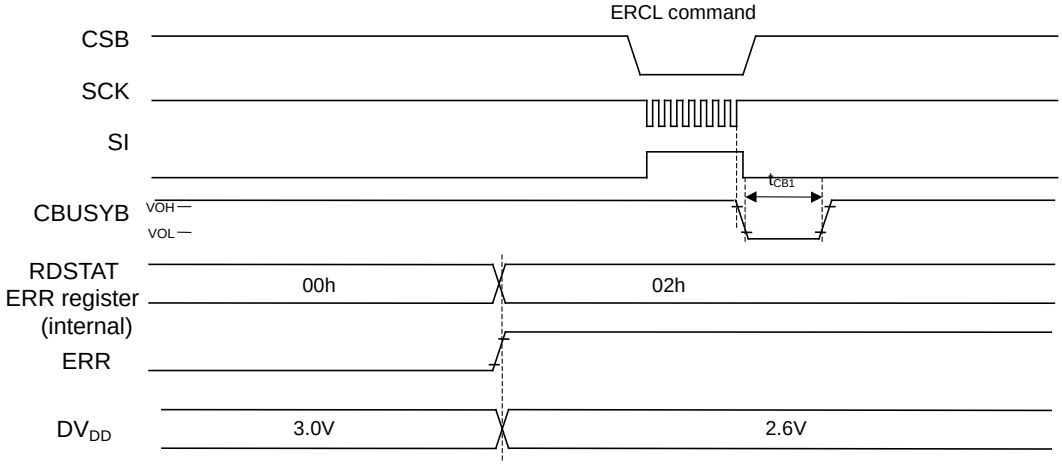

Timing diagram for when an error occurs at the External ROM



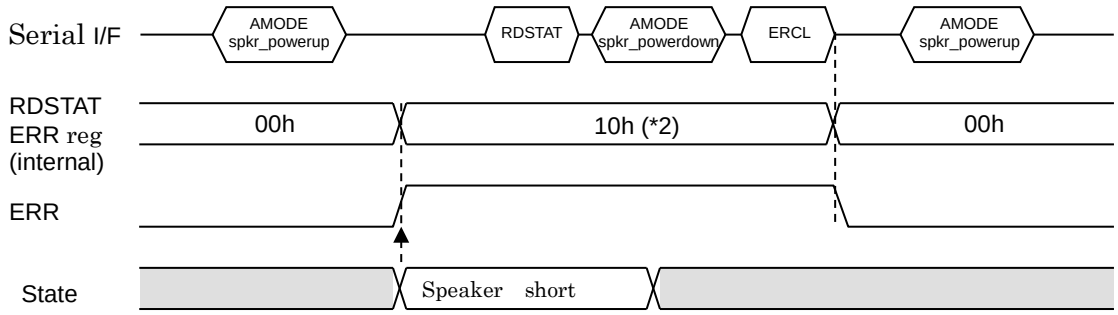
If a power supply voltage error occurs and then the power supply voltage is returned (when the SAFE command's BLD2–0 bits = 001h)



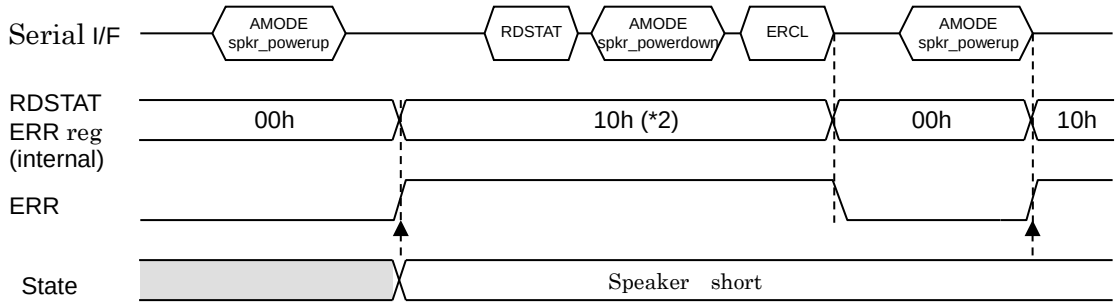

If a power supply voltage error occurs but the power supply voltage is not returned



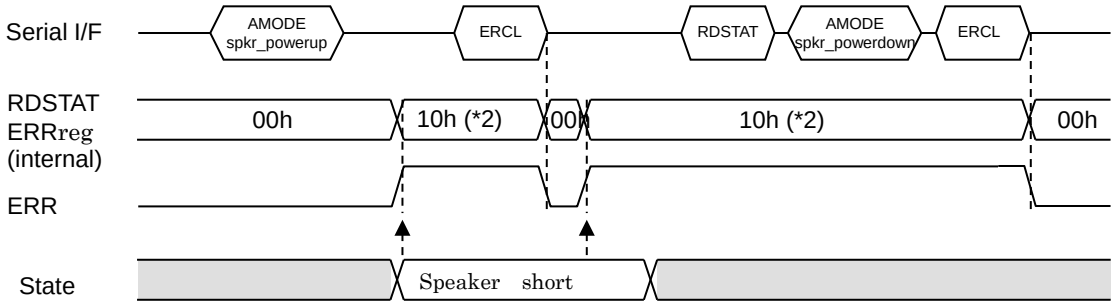
When Speaker-short situation is released before Error Clear Flow(*1)




When Speaker-short situation is continued after Error Clear Flow(*1).



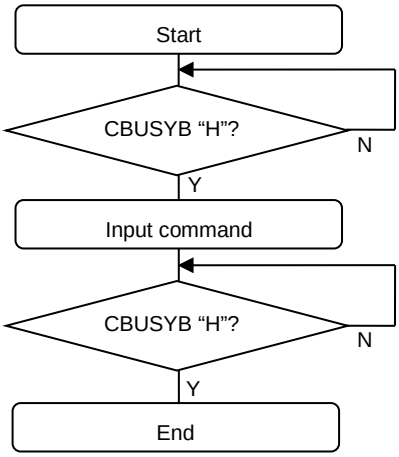

When ERCL is inputed before Error Clear Flow(*1).



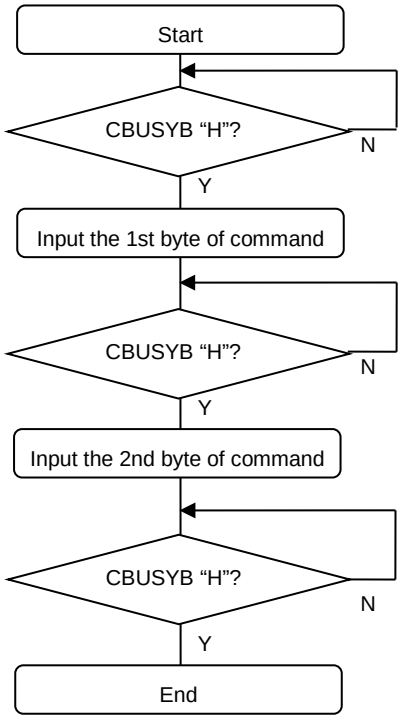

*1:Error Clear Flow:RDSTAT=>AMODE(Speaker Power-down) => ERCL
*2: SPM pin short error

**Command Flow Charts**

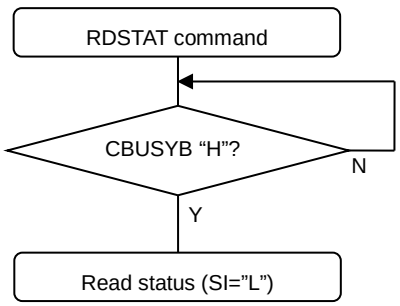
1-Byte Command Input Flow (applied to the PUP, PDWN, START, STOP, SLOOP, CLOOP, OUTSTAT, and ERCL commands)



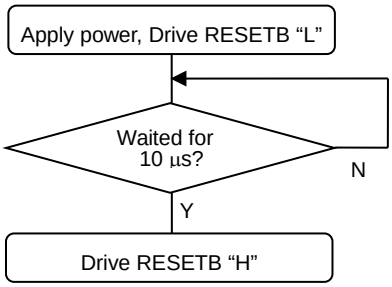

2-Byte Command Input Flow (applied to the AMODE, AVOL, FAD, FADR, PLAY, MUON, CVOL, and SAFE commands)



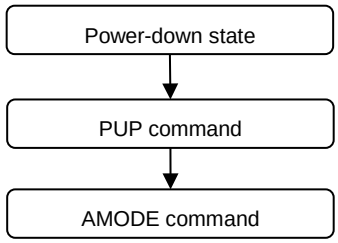

Status Read Flow



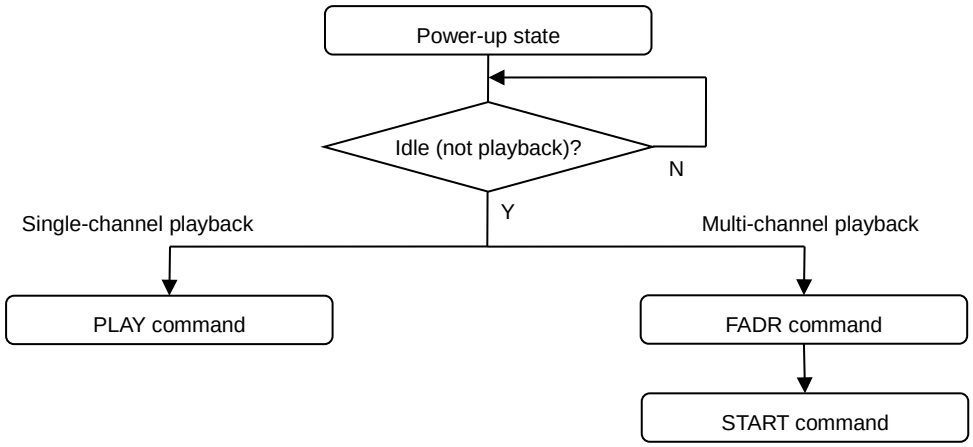
Power-On Flow



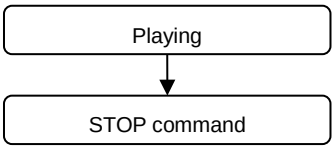

Example of Power-Up Flow



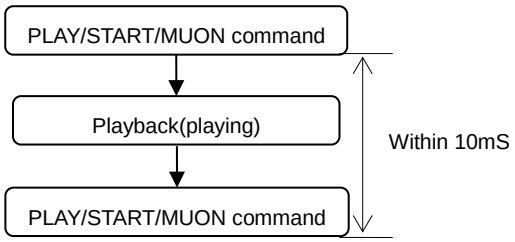

Example of Playback Start Flow



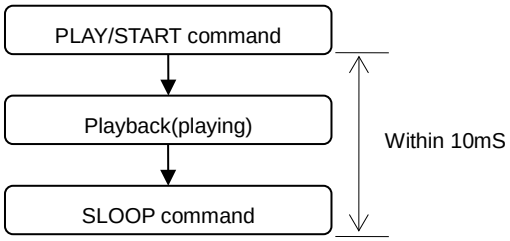

Example of Playback Stop Flow



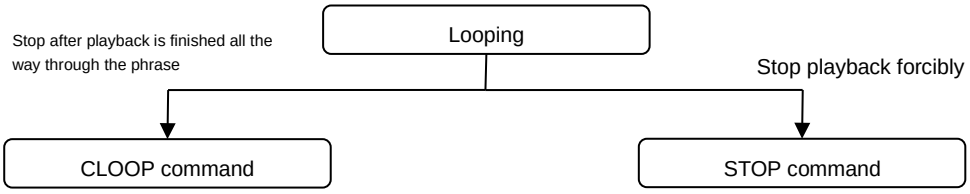
Continuous Playback Start Flow



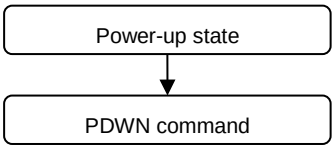

Loop Start Flow



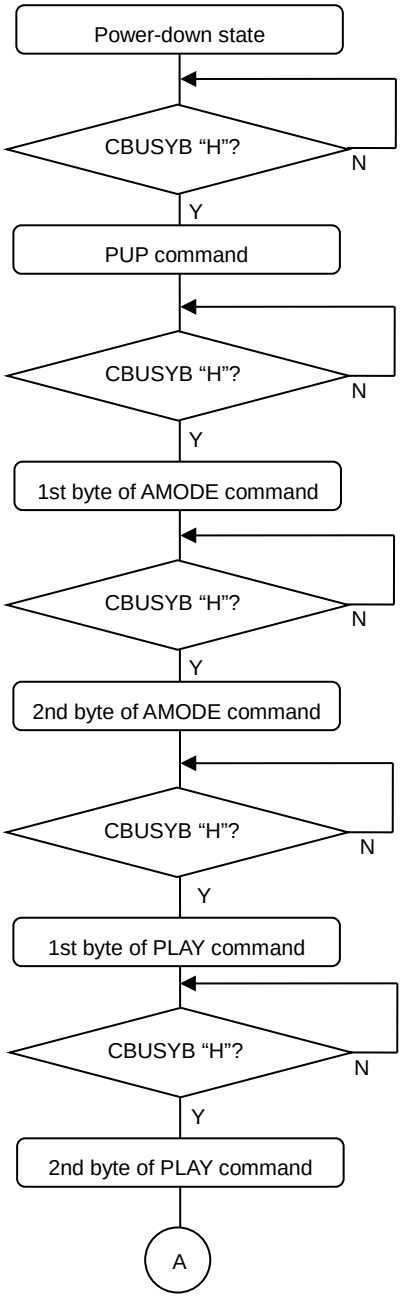

Loop Stop Flow

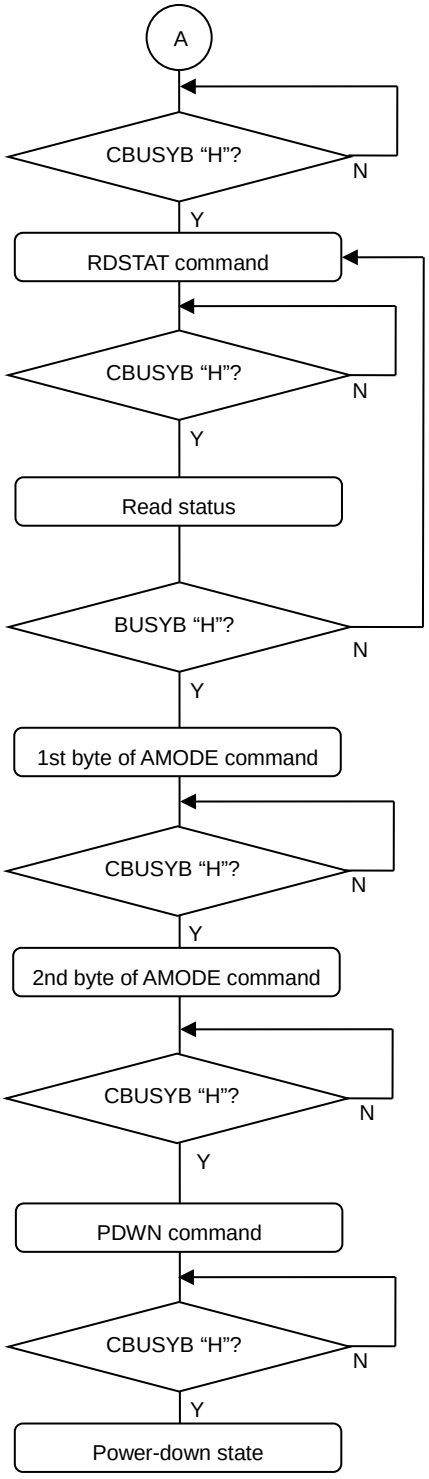



Power-Down Flow

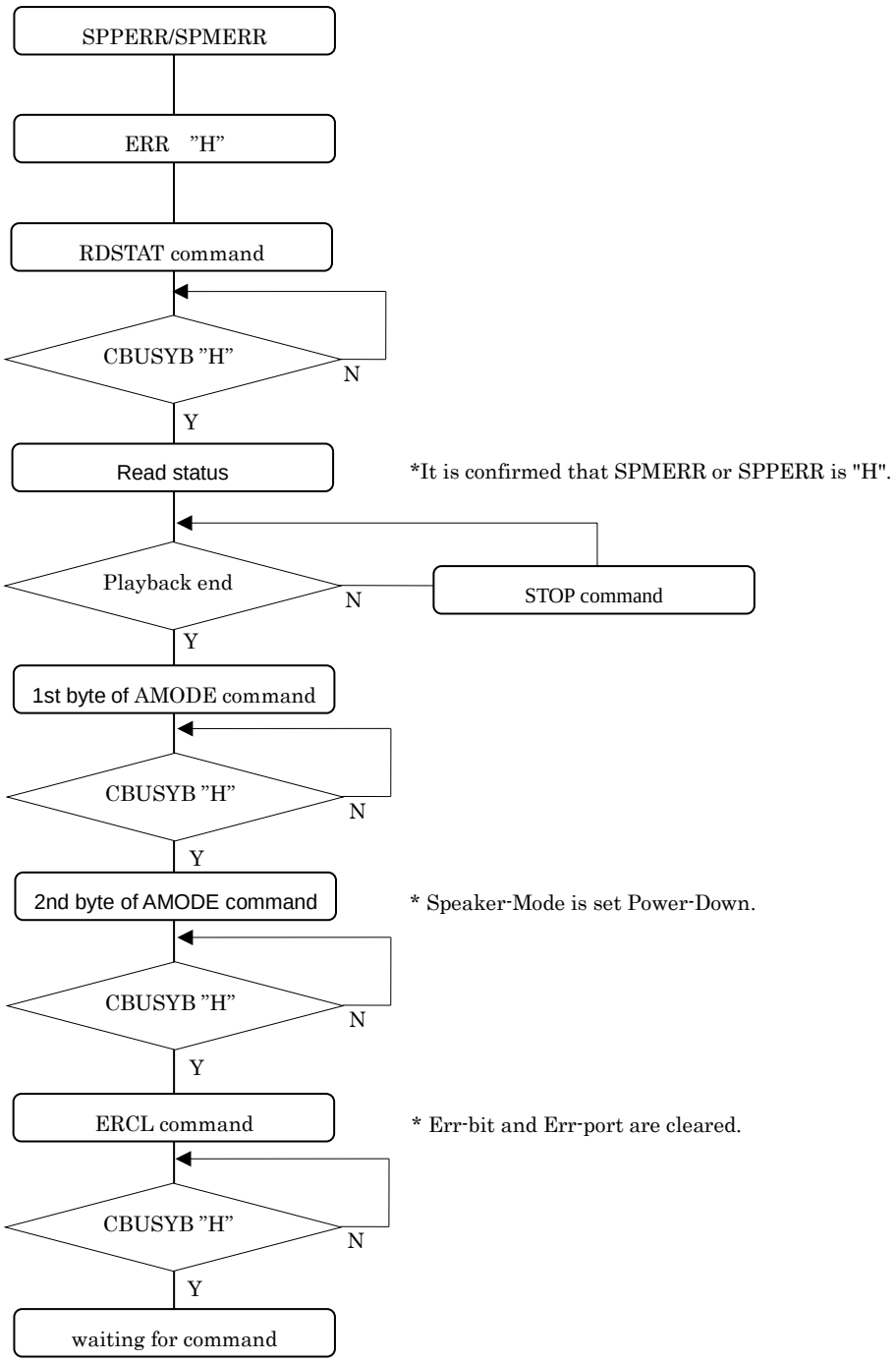


Detailed Flow of “Power-Up ⇒ Playback ⇒ Power-Down”

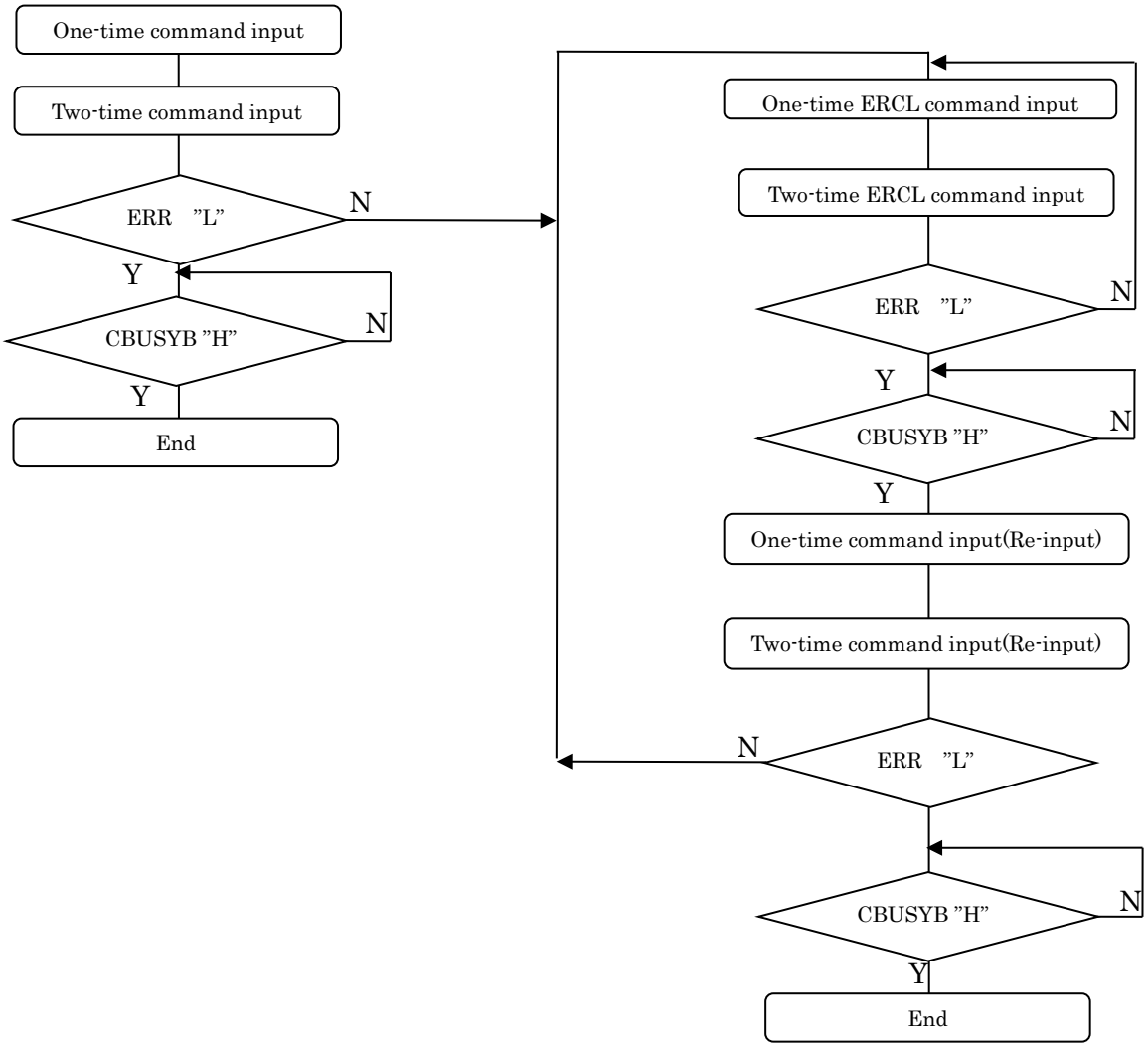


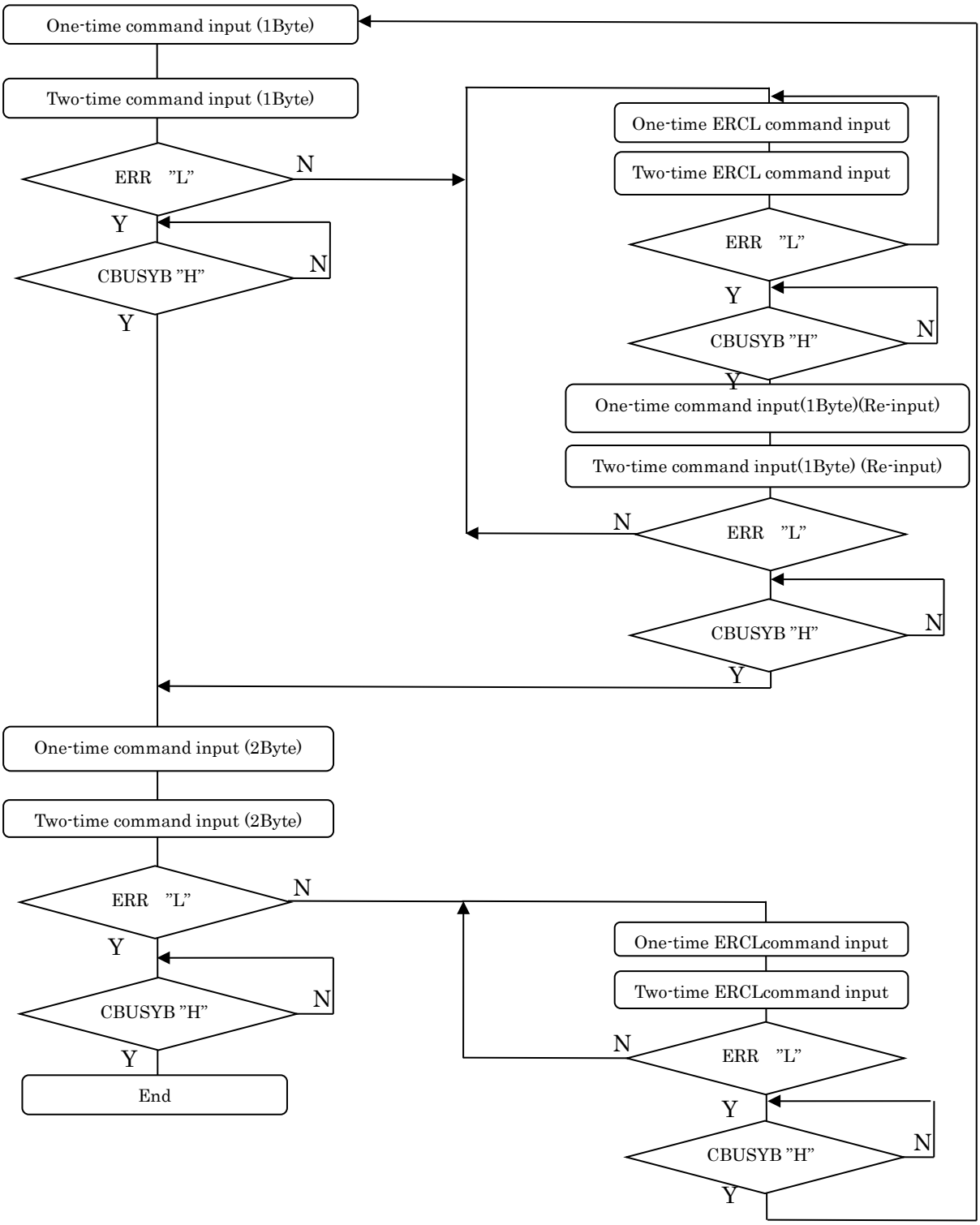
Detailed flow of “SPP/SPM Short detecting”



1-Byte Command input flow of two-time command input mode
（applied to the PDWN, STOP, SLOOP, CLOOP, RDSTAT, OUTSTAT, and ERCL commands）



2-Byte Command input flow of two-time command input mode
（applied to the AMODE, AVOL, FAD, FADR, PLAY, MUON, CVOL, and SAFE commands）



**Handling of the SG Pin**

The SG pin is the signal ground pin for the built-in speaker amplifier. Connect a capacitor between this pin and the analog ground so that this pin will not carry noise.
The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.
Always start playback after each output voltage is stabilized.

| Pin | Recommended capacitance value | Remarks |
|---|---|---|
| SG | 0.1 μF ±20% | The larger the connection capacitance, the longer the speaker amplifier output pin (SPM and SPP) voltage stabilization time. |

**Handling of the $V_{DDL}$ Pins**

The $V_{DDL}$ pin is the power supply pins for the internal circuits. Connect a capacitor between each of these pins and the ground in order to prevent noise generation and power fluctuation.
The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.
Always start the next operation after each output voltage is stabilized.

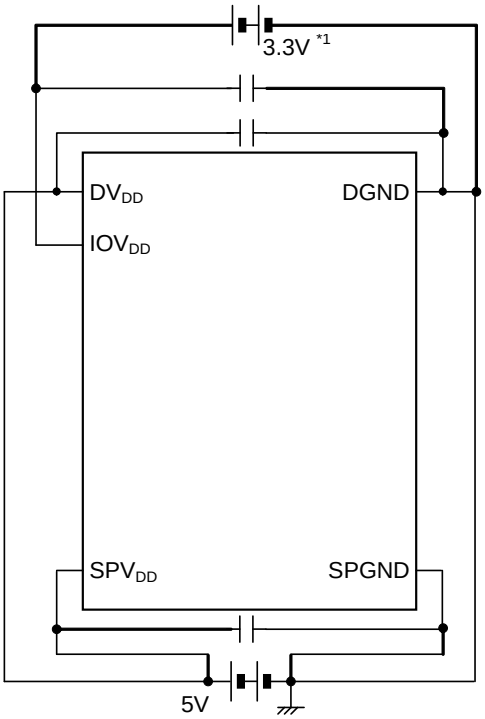
| Pin | Recommended capacitance value | Remarks |
|---|---|---|
| $V_{DDL}$ | 10 μF ±20% | The larger the connection capacitance, the longer the stabilization time. |

**Power Supply Wiring**

The power supplies of this LSI are divided into the following three:

- Digital power supply ($DV_{DD}$) and Digital ground(DGND)
- Speaker amplifier power supply ($SPV_{DD}$) and Speaker amplifier ground(SPGND)
- External ROM interface power supply(IO $V_{DD}$)

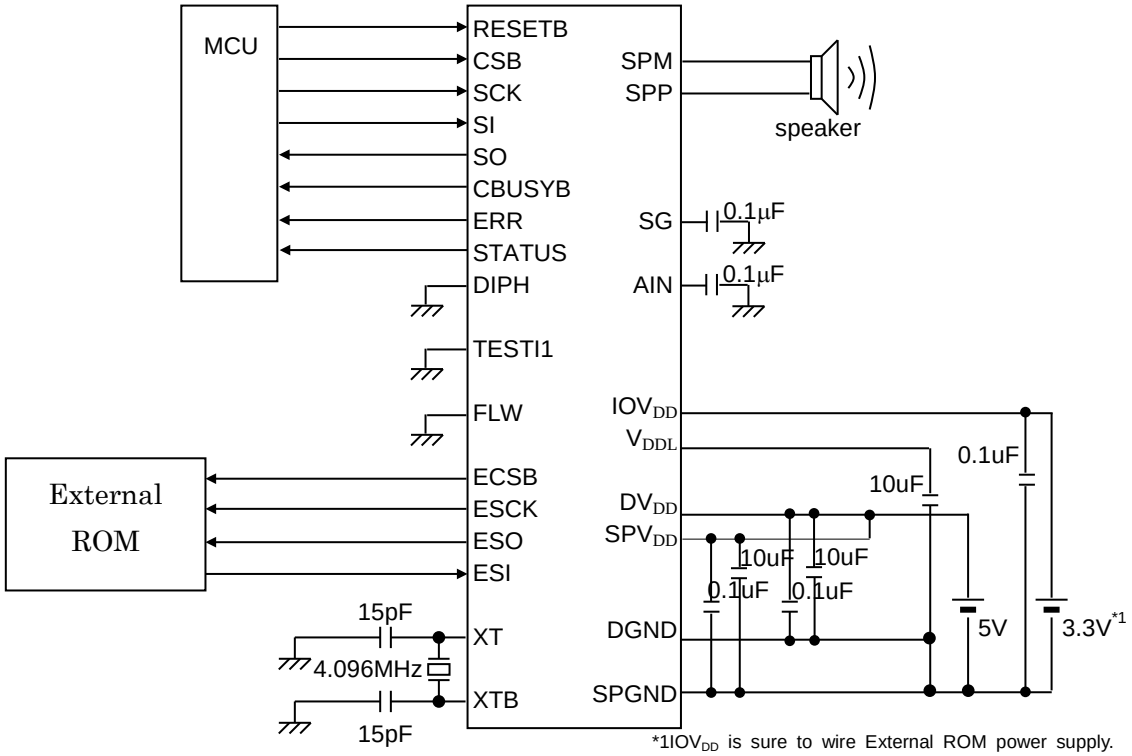
As shown in the figure below, be sure to diverge the wiring of $DV_{DD}$ and $SPV_{DD}$ from the root of the same power supply. DGND/SPGND is similar, too.
$IOV_{DD}$ is sure to wire External ROM power supply.




*1 : $IOV_{DD}$ is sure to wire External ROM power supply.

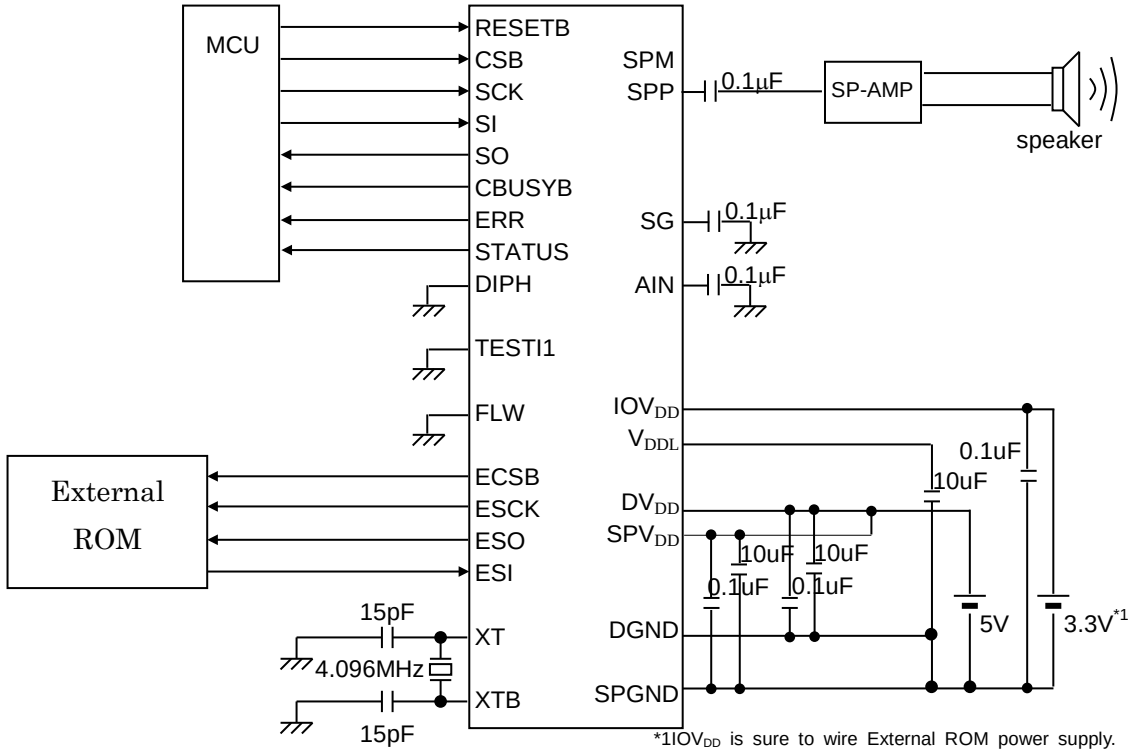
## APPLICATION CIRCUIT

At using internal speaker amplifier (speaker output)




*1$IOV_{DD}$ is sure to wire External ROM power supply.

At using external speaker amplifier (line output)




*1$IOV_{DD}$ is sure to wire External ROM power supply.

## RECOMMENDED CERAMIC OSCILLATION

Recommended ceramic resonators for oscillation and conditions are shown below for reference.

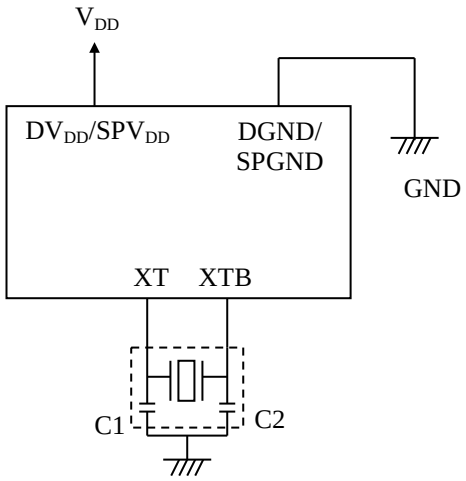
### KYOCERA Corporation

| Freq [Hz] | Type | Optimal load capacity | | | | | |
|---|---|---|---|---|---|---|---|
| | | C1 [pF] | C2 [pF] | Rf [Ohm] | Rd [Ohm] | Supply voltage Range [V] | Operating Temperature Range [°C] |
| 4.096M | PBRV4.096MR50Y000 | 15(internal) | | --- | -- | 4.5 to 5.5 | -40 to +125 |

### MURATA Corporation

| Freq [Hz] | Type | Optimal load capacity | | | | | |
|---|---|---|---|---|---|---|---|
| | | C1 [pF] | C2 [pF] | Rf [Ohm] | Rd [Ohm] | Supply voltage Range [V] | Operating Temperature Range [°C] |
| 4M | CSTCR4M00G55B-R0 | 39(internal) | | --- | -- | 4.5 to 5.5 | -40 to +125 |
| 4.096M | CSTCR4M09G55B-R0 | | | | | | |

#### Circuit diagram



## LIMITATION ON THE OPERATION TIME (PLAY-BACK TIME)

ML22594's operating temperature is 105°C. But the average ambient temperature at 1W play-back (8ohm drive) during 10 years in the reliability design is Ta=70°C. (max ( the package heat resistance $\theta$ ja=24.6[°C/W]) )

When ML22594 operates 1W play-back(8ohm drive) consecutively, the product life changes by the package temperature rise by the consumption. This limitation does not matter in the state that a speaker amplifier does not play.

The factor to decide the operation time ( play-back time ) is the average ambient temperature( Ta ), play-back Watts( at the speaker drive mode), the soldering area ratio*1, and so on. In addition, the limitation on the operation time changes by the heat designs of the board.

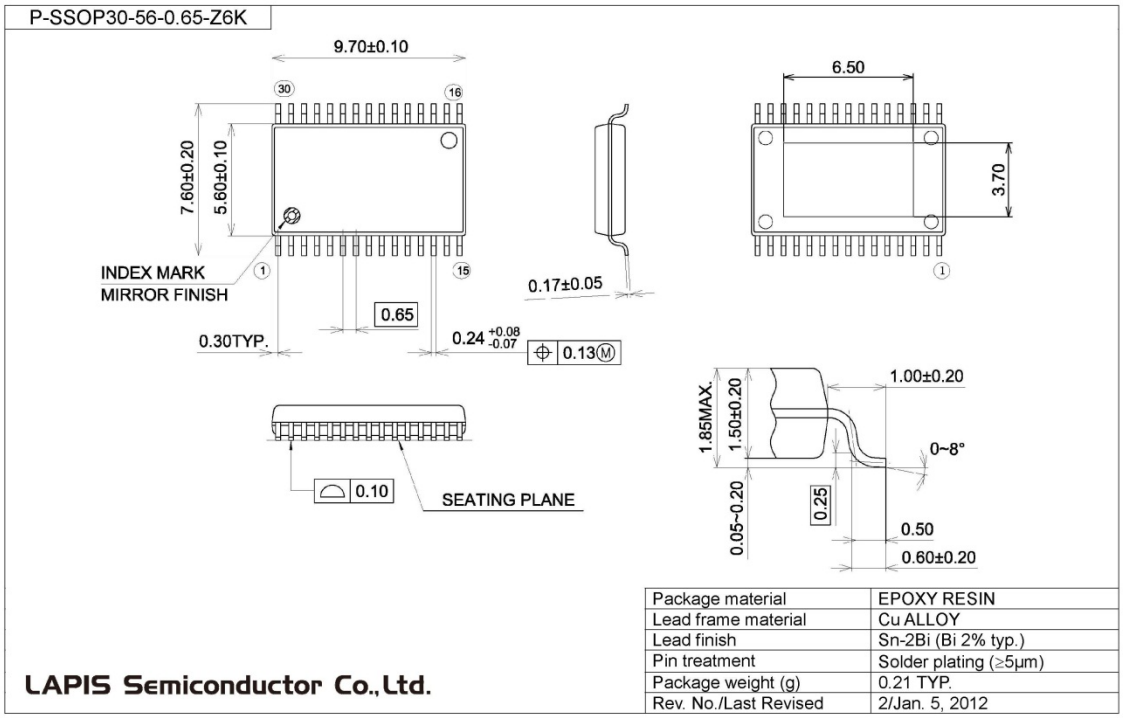
## PACKAGE HEAT RESISTANCE VALUE (REFERENCE VALUE)

The following table is the package heat resistance value $\theta$ ja (reference value).
This value changes the condition of the board (size, layer number, and so on)

| The board | $\theta$ ja | The condition |
|---|---|---|
| JEDEC 4layers*1 (W/L/t=76.2/114.5/1.6(mm)) | 24.6[°C /W] | No wind (0m/s) the soldering area ratio*3:100% |
| JEDEC 2layers*2 (W/L/t=76.2/114.5/1.6(mm)) | 31.2[°C /W] | |

*1 : The wiring density : 1st layer(Top) 60% / 2nd layer 100% / 3rd layer 100% / 4th layer(Bottom) 60%.
*2 : The wiring density : 1st layer(Top) 60% / 2nd layer(Bottom) 100%.
*3 : The soldering area ratio is the ratio that the heat sink area of ML22594 and a land pattern on the board are soldered. 100% mean that the heat sink area of ML22594 is completely soldered to the land pattern on the board. About the land pattern on the board, be sure to refer to the next clause (PACKAGE DIMENSIONS).

## PACKAGE DIMENSIONS




| | |
|---|---|
| Package material | EPOXY RESIN |
| Lead frame material | Cu ALLOY |
| Lead finish | Sn-2Bi (Bi 2% typ.) |
| Pin treatment | Solder plating (≥5μm) |
| Package weight (g) | 0.21 TYP. |
| Rev. No./Last Revised | 2/Jan. 5, 2012 |

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Notes for heat sink type Package

This LSI adopts a heat sink type package to raise a radiation of heat characteristic. Be sure to design the land pattern corresponding to the heat sink area of the LSI on a board, and solder each other. The heat sink area of the LSI solder open or GND on the board.

## REVISION HISTORY

| Document No. | Date | Page | | Description |
|---|---|---|---|---|
| | | Previous Edition | Current Edition | |
| FEDL22594FULL-01 | Sep. 19, 2012 | – | – | Final edition 1. |
| FEDL22594FULL-02 | Nov. 20, 2012 | 51 | 51 | Add EXRERR. |
| | | 55 | 55 | Add External ROM error timing diagram. |
| FEDL22594-03 | Apr. 24, 2013 | 11 | 11 | Add tCB3. |
| | | 18 | 18 | Change Playback Stop Timing. |
| FEDL22594-04 | Dec. 9, 2014 | - | 34 | Add tPUPA3 timing diagram. |
| | | - | 35 | Add tPDA3 timing diagram. |
| FEDL22594-05 | Mar. 8, 2015 | 68 | 68 | Change Application Circuit. |
| FEDL22594-06 | Oct. 16, 2017 | 2 | 2 | Differences table correction. |
| | | - | 3 | Add Playback method. |
| | | 5,6 | 6,7 | Add instructions. |
| | | 8 | 9 | Add instructions to ”DC Characteristics". |
| | | 12 | 13 | Add instructions to “AC Characteristics". |
| | | 13 | 14 | Modify CPU Serial Interface Data Timing. |
| | | 15 | 15 | Modify Power-On Timing. |
| | | 15 | 15 | Modify Power Shut-down Timing. |
| | | 23 | 23 | Add $t_{INTC.}$ |
| | | - | 24 | Add “To know the volume controls more”. |
| | | 25 | 25 | Modify “Playback Time and Memory Capacity”. |
| | | 34 | 34 | Modify “When putting the speaker amplifier into the power down state”. |
| | | 42 | 42 | Modify “PLAY Command Input Timing for Continuous Playback”. |
| | | 53 | 53 | STATUS of OUTSTAT command is added. |
| | | 70 | 70 | Unit correction |

Notes

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