RICHTEK®

RTQ2833A

3A, 18V, High-Efficiency Step-Down Converter with Internally-Compensated Fast Current-Mode Control

1 General Description

The RTQ2833A is a high-performance, synchronous step-down converter that can deliver up to 3A output current with an input supply voltage range of 4V to 18V. The device integrates low $R_{DS(ON)}$ power MOSFETs, an accurate 0.5V reference, and an integrated diode for the bootstrap circuit to offer a very compact solution.

The RTQ2833A adopts internally-compensated fast current-mode (FCM) control architecture that provides fast transient response and further reduces the external-component count. The FCM operates at a truly fixed switching frequency over the line, load, and output voltage range and makes the EMI filter design easier.

The device offers a variety of functions for more design flexibility. The selectable switching frequency allows the RTQ2833A to meet various application requirements. An independent enable control input pin and a power-good indicator are provided for easy sequence control. The built-in spread-spectrum frequency modulation further helps system designers with better EMI management.

Full protection features are also integrated in the device for increased reliability, including input UVLO, cycle-by-cycle current limit, OVP, UVP, OTP, and selectable soft-start time to control the inrush current during the startup. The RTQ2833A is available in a thermally enhanced WQFN-14L 3x2.5 (FC) package. The recommended junction temperature range is from –40°C to 150°C.

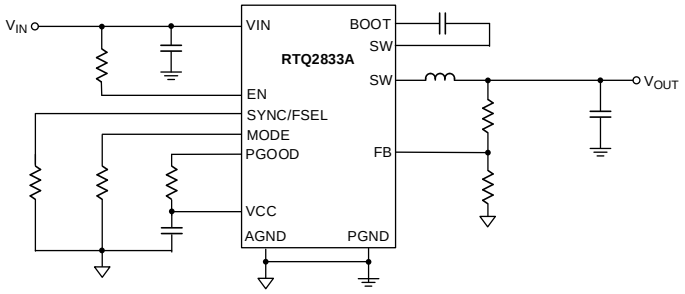
2 Features

- **4V to 18V Input Voltage Range**
- **0.5V to 7V Output Voltage**
- **Internally-Compensated FCM control**
- **Integrated 25mΩ/13.9mΩ MOSFETs**
- **0.5V ±0.5% Voltage Reference Accuracy Over Full Temperature Range**
- **Synchronizable to an External Clock**
- **Selectable Spread Spectrum Reducing EMI Emission**
- **Adjustable Switching Frequency (500kHz/750kHz/1MHz/1.5MHz/2.2MHz)**
- **Selectable Current Limit Level**
- **Selectable Soft-Start Tim (0.5ms/1ms/2ms/4ms)**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **Power-Good Indicator**
- **Output Overvoltage, Output Undervoltage, Input Undervoltage, Overcurrent, and Over-Temperature Protection**
- **–40°C to 150°C Operating Junction Temperature**

3 Applications

- Wireless Infrastructure and Wired Communication Equipment
- Optical and Fiber Network Equipment
- Testing and Measurement Instruments
- Healthcare Equipment

4 Simplified Application Circuit



5 Ordering Information

RTQ2833A □-□□

Packing
B: Pin 1 Orientation
(Quadrant 2, Follow EIA-481)

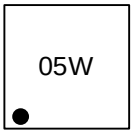
Product Grade
T: Industrial

Package Type(1)
N: WQFN-14L 3x2.5 (FC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

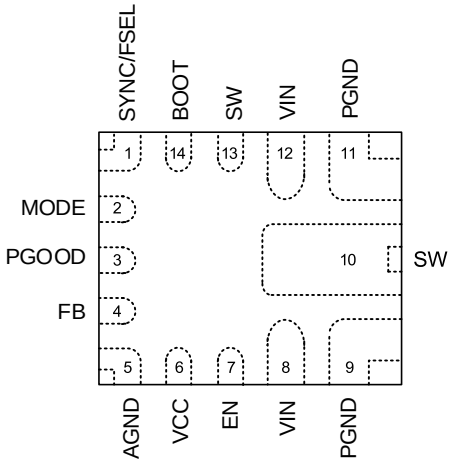


05: Product Code
W: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



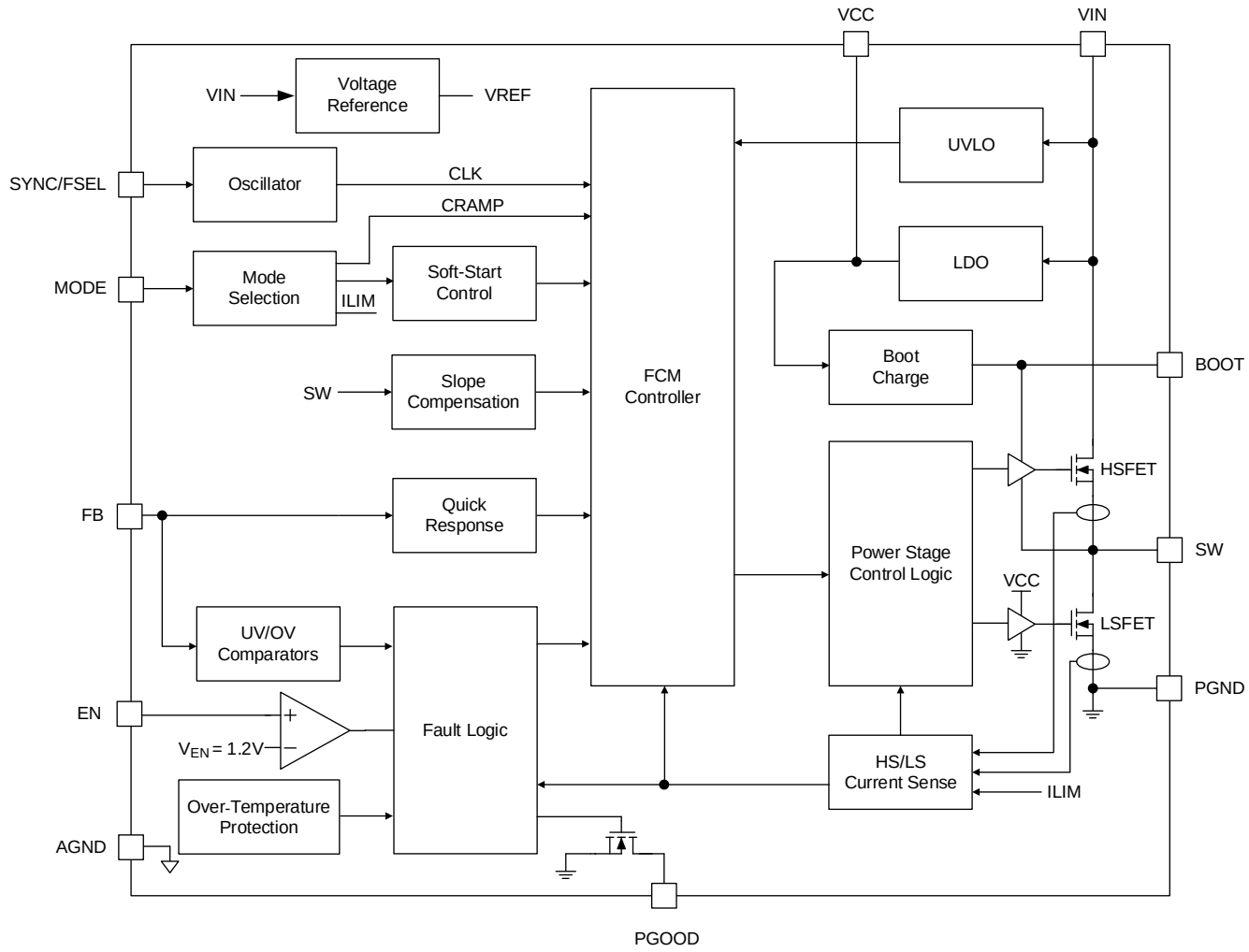
WQFN-14L 3x2.5 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SYNC/FSEL	Multi-function configuration pin. Frequency selection, spread spectrum modulation enable, and external clock synchronization. A resistor to ground sets the switching frequency of the device and enables/disables spread spectrum modulation. An external clock can also be applied to this pin to synchronize the switching frequency.
2	MODE	Current limit and soft-start time selection pin. Connect this pin to ground through a resistor.
3	PGOOD	Open-drain, power-good indication output. The power-good indication output is pulled low when the feedback voltage is outside the PGOOD threshold, the IC shuts down due to OTP, EN goes low, or before the soft-start has finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
4	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. It is suggested to place the FB resistor divider as close to the FB pin and AGND as possible.
5	AGND	Analog GND. AGND and PGND are connected by a short trace and at only one point to reduce circulating currents.
6	VCC	3V internal LDO output. Requires a 2.2μF, at least 6.3V rating ceramic capacitor from the VCC pin to AGND pins as the decoupling capacitor. The placement is required to be as close as possible. It is not recommended to connect VCC to supply other rails.
7	EN	Enable control input. Leave this pin floating to enable. Enable/disable with an external signal, or adjust the input undervoltage-lockout with a resistor divider.
8, 12	VIN	Input voltage. Support 4V to 18V input voltage. It is suggested to place equal-value input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
9, 11	PGND	Ground return for the power stage. Use wide PCB traces to make the connections. AGND and PGND are connected by a short trace and at only one point to reduce circulating currents.
10	SW	Switch node. Connect to the power inductor.

Pin No.	Pin Name	Pin Function
13	SW	Return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin. Pin 10 and pin 13 are connected internally.
14	BOOT	Bootstrap, supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BOOT and SW pins.

9 Function Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- −0.3V to 20V
- VIN to SW ---------- −0.3V to 20V

  VIN to SW (t ≤ 20ns) ---------- −6V to 25V
- Switch Voltage, SW ---------- −0.3V to 20V

  SW (t ≤ 20ns) ---------- −5V to 22V
- Boot Voltage, BOOT ---------- −0.3V to 24V
- BOOT to SW (VBOOT-VSW) ---------- −0.3V to 4V
- All Other Pins ---------- −0.3V to 4V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- −65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Voltage, VIN ---------- 4V to 18V
- Junction Temperature Range ---------- −40°C to 150°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WQFN-14L 3x2.5 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	59.5	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	38.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	33.7	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board, which is in size of 76mm x 76mm; furthermore, all layers with 2 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 4V to 18V, T_J = -40°C to 150°C, unless otherwise specified.)

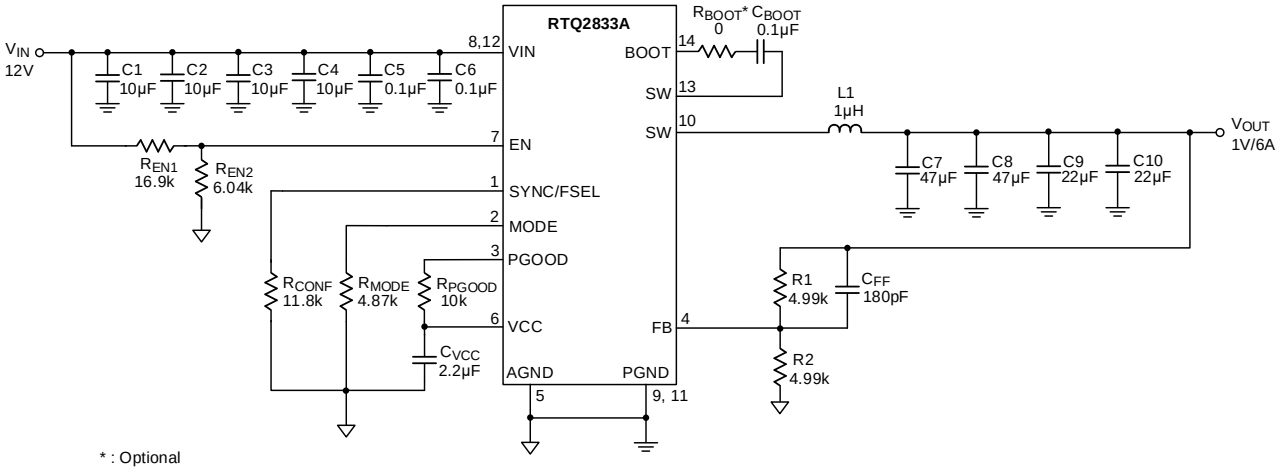
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VIN Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V	--	15	25	μA
VIN Supply Current (Quiescent)	I_Q	V_{EN} = 1.3V, V_{FB} = 550mV, V_{IN} = 12V, 1MHz	--	1700	2000	μA
UVLO						
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	3.9	4	4.1	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} hysteresis	--	0.15	--	V
Logic Threshold						
EN Input Voltage Rising Threshold	V_{EN_R}		--	1.2	1.25	V
EN Input Voltage Falling Threshold	V_{EN_F}		1.05	1.1	--	V
EN Threshold Hysteresis	V_{EN_HYS}		--	0.1	--	V
EN Pull-Up Current	I_{ENP1}	V_{EN} = 1.1V	0.4	1.5	--	μA
	I_{ENP2}	V_{EN} = 1.3V	--	11.6	--	
LDO Output						
LDO Output Voltage	V_{CC}	V_{IN} = 12V	--	3	--	V
LDO Output Current Limit	I_{LIM_LDO}	V_{IN} = 12V	--	75	--	mA
Reference Voltage						
Reference Voltage	V_{REF}		497.5	500	502.5	mV
Input Leakage Current into FB Pin	I_{FB}	V_{IN} = 12V, V_{EN} = 0V V_{FB} = 500mV, non-switching mode	--	1	--	nA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency						
Switching Frequency	f_{SW1}	R_{CONF} = 24.3kΩ	450	500	550	kHz
	f_{SW2}	R_{CONF} = 17.4kΩ	675	750	825	
	f_{SW3}	R_{CONF} = 11.8kΩ	900	1000	1100	
	f_{SW4}	R_{CONF} = 8.06kΩ	1350	1500	1650	
	f_{SW5}	R_{CONF} = 4.99kΩ	1980	2200	2420	
Synchronization						
SYNC Threshold Voltage	V_{SYNC_IH}	high level	1.8	--	--	V
	V_{SYNC_IL}	low level	--	--	0.8	V
Spread Spectrum						
Spread-Spectrum Range	SSP		--	+10	--	%
On-Time Timer Control						
Minimum On Time	$t_{ON,MIN}$	I_{OUT} > 0.5 x I_{L_PK-PK}	--	30	--	ns
Minimum Off Time	$t_{OFF,MIN}$		--	115	--	ns
BOOT-LX UVLO	$V_{BOOT\_UVLO\_H}$	Rising	--	2.35	--	V
	$V_{BOOT\_UVLO\_L}$	Falling	--	2.17	--	V
$R_{DS(ON)}$						
On-Resistance of High-Side MOSFET	R_{DSON_H}	T_J = 25°C, V_{IN} = 12V, V_{BOOT}–V_{SW} = 3V	--	25	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	T_J = 25°C, V_{CC} = 3V,	--	13.9	--	
Soft-Start						
Soft-Start Time	t_{SS1}	R_{MODE} = 1.78kΩ	--	0.5	--	ms
	t_{SS2}	R_{MODE} = 2.21kΩ	--	1	--	
	t_{SS3}	R_{MODE} = 2.74kΩ	--	2	--	
	t_{SS4}	R_{MODE} = 3.32kΩ	--	4	--	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H1}	R_{MODE} = 1.78kΩ	4.3	4.9	5.4	A
	I_{LIM_H2}	R_{MODE} = 22.1kΩ	2.8	3.3	3.6	
Low-Side Switch Sourcing Current Limit	I_{LIM_L1}	R_{MODE} = 1.78kΩ	3.4	4.2	4.65	A
	I_{LIM_L2}	R_{MODE} = 22.1kΩ	2.4	3	3.4	
Low-Side Switch Sinking Current Limit	I_{L_SNK}		1.9	--	--	A
Hiccup Time	T_{HICCUP}		--	7 x t_{SS}	--	ms
Output Undervoltage and Overvoltage Protections						
Output OVP Threshold	V_{OVP}	V_{FB} rising threshold	--	120	--	%V_{REF}
Output UVP Threshold	V_{UVP}	V_{FB} falling threshold	--	80	--	%V_{REF}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good Function						
Power-Good Threshold	V_{TH_PGLH1}	V_{FB} rising threshold, PGOOD from low to high	89	92	95	%V_{REF}
	V_{TH_PGHL1}	V_{FB} rising threshold, PGOOD from high to low	113	116	119	
	V_{TH_PGLH2}	V_{FB} falling threshold, PGOOD from low to high	105	108	111	
	V_{TH_PGHL2}	V_{FB} falling threshold, PGOOD from high to low	81	84	87	
Power-Good Sink Current Capability	I_{PGOOD_SK}	I_{PGOOD} = 2mA, V_{IN} = 12V	--	--	0.5	V
Power-Good Leakage Current	I_{PGOOD_LK}	V_{PGOOD} = 4.7V	--	--	5	μA
Minimum VIN for Valid PGOOD Output			--	0.9	1.05	V
OTP						
Over-Temperature Protection Threshold	T_{OTP}	(Note 7)	--	165	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	(Note 7)	--	12	--	°C
Output Discharge						
Output Discharge Resistor	R_{DIS}	V_{IN} = 12V, V_{SW} = 0.5V, power conversion disabled.	--	100	--	Ω

Note 7. Specifications are guaranteed by design, not production test.

15 Typical Application Circuit



Note 8. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

Table 1. Suggested Component Selections for the Application of 500kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_Min} (µF)	$C_{OUT\_Typical}$ (µF)	C_{OUT_Max} (µF)	C_{FF} (pF)
0.75	4.99	10	1.5	188	210	470	180
1	4.99	4.99	2.2	116	188	470	390
3.3	28	4.99	4.7	94	141	470	47
5	28	3.09	6.8	47	94	470	47

Table 2. Suggested Component Selections for the Application of 750kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_Min} (µF)	$C_{OUT\_Typical}$ (µF)	C_{OUT_Max} (µF)	C_{FF} (pF)
0.75	4.99	10	1	141	160	470	270
1	4.99	4.99	1.5	94	141	470	270
3.3	28	4.99	3.3	94	141	470	33
5	28	3.09	4.7	47	94	470	33

Table 3. Suggested Component Selections for the Application of 1000kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_Min} (µF)	$C_{OUT\_Typical}$ (µF)	C_{OUT_Max} (µF)	C_{FF} (pF)
0.75	4.99	10	0.82	138	160	470	180
1	4.99	4.99	1	88	138	470	180
3.3	28	4.99	3.3	44	66	470	22
5	28	3.09	3.3	44	66	470	22

Table 4. Suggested Component Selections for the Application of 1500kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_Min} (µF)	$C_{OUT\_Typical}$ (µF)	C_{OUT_Max} (µF)	C_{FF} (pF)
0.75	1	2	0.68	94	116	470	470
1	1	1	0.82	47	94	470	470
3.3	28	4.99	2.2	22	66	470	15
5	28	3.09	2.2	66	88	470	15

Table 5. Suggested Component Selections for the Application of 2200kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_Min} (µF)	$C_{OUT\_Typical}$ (µF)	C_{OUT_Max} (µF)	C_{FF} (pF)
0.75	1	2	0.47	88	110	470	330
1	1	1	0.68	47	88	470	330
3.3	28	4.99	1.5	22	44	470	15
5	28	3.09	1.5	22	44	470	10

Table 6. Suggested Inductors for Typical Application Circuit

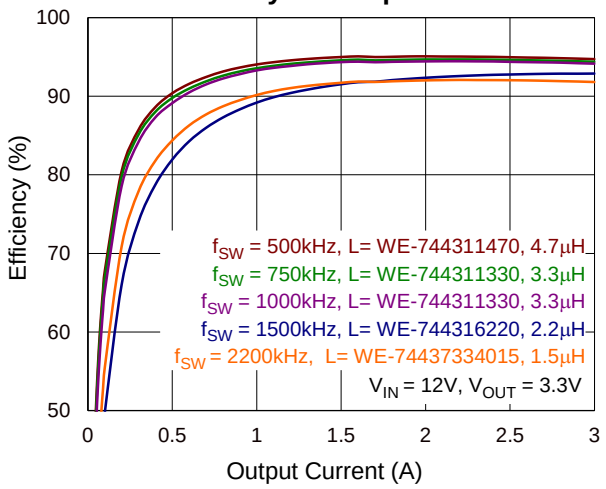
Inductance (µH)	Part No.	I_{SAT} (A)	DCR (mΩ)	Dimensions (mm)	Supplier
0.47	744316047	16	2.75	5.5 x 5.5 x 4	WE-HCI
0.68	744373340068	14.5	11	5.5 x 5.5 x 2	WE-HCI
0.82	744383350082	7	30	3.0 x 3.0 x 1.5	WE-HCI
1	744316100	11.5	4.75	5.5 x 5.5 x 4	WE-HCI
1.2	74437334012	11.3	23	5.5 x 5.5 x 2	WE-HCI
1.5	74437334015	10	26.5	5.5 x 5.5 x 2	WE-HCI
2.2	744316220	7.5	11.3	5.5 x 5.5 x 4	WE-HCI
3.3	744311330	11	17.2	7.0 x 7.0 x 4	WE-HCI
4.7	744311470	7	19.5	7.0 x 7.0 x 4	WE-HCI
6.8	74437349068	9.5	46	7.3 x 6.6 x 4.8	WE-HCI

Table 7. Suggested Capacitor for Typical Application Circuit

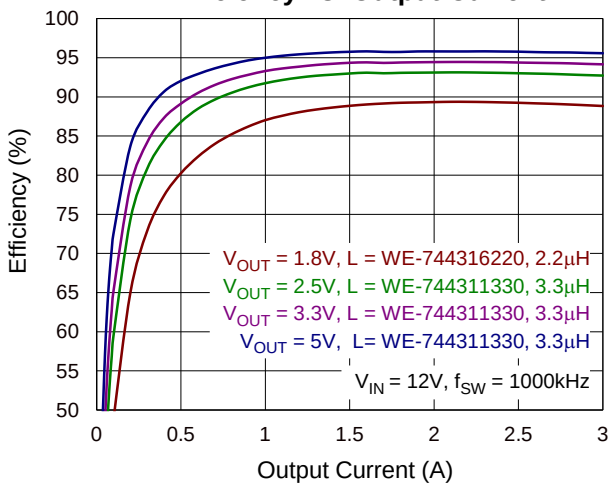
Capacitance (µF)	Part No.	Case Size	Supplier
0.1	GRM188R71H104KA93	0603	Murata
10	GRM21BZ71E106KE15	0805	Murata
22	GRM188R61A226ME15	0603	Murata
47	GRM21BR61A476ME15L	0805	Murata

16 Typical Operating Characteristics

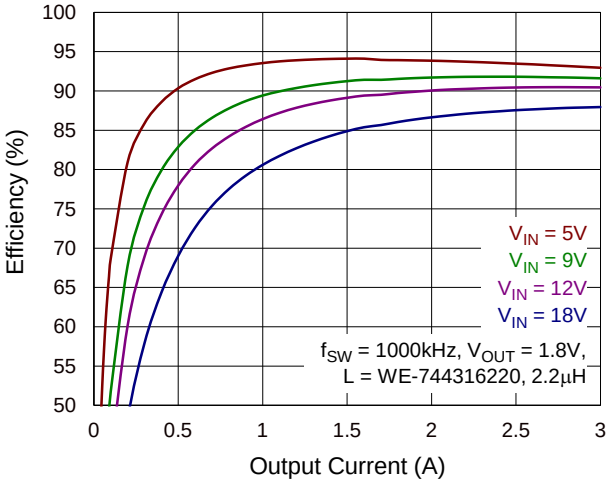
Efficiency vs. Output Current



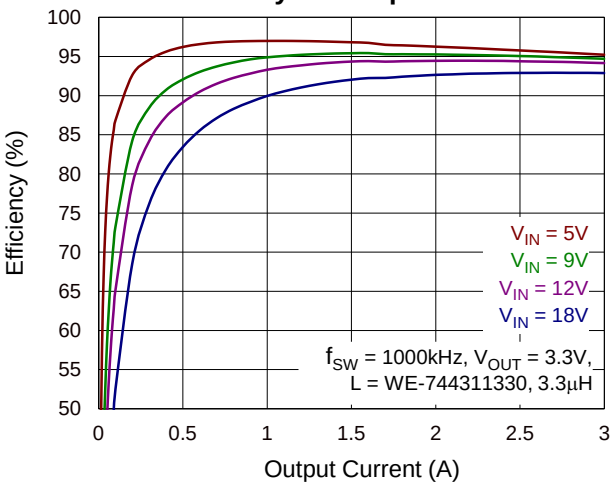
Efficiency vs. Output Current



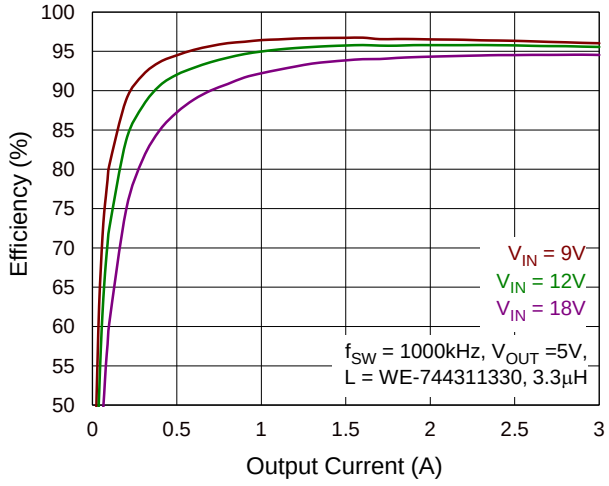
Efficiency vs. Output Current



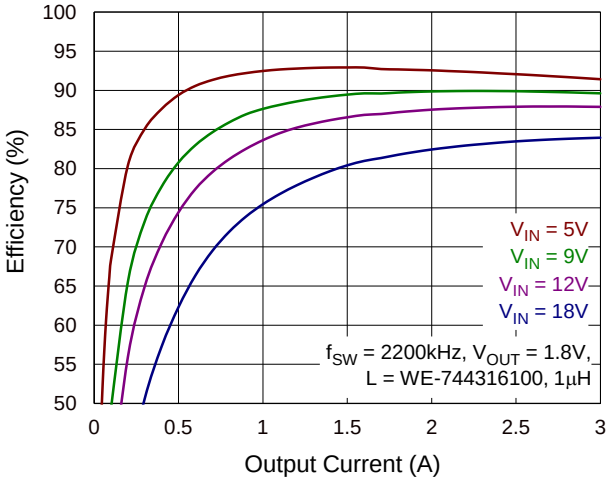
Efficiency vs. Output Current

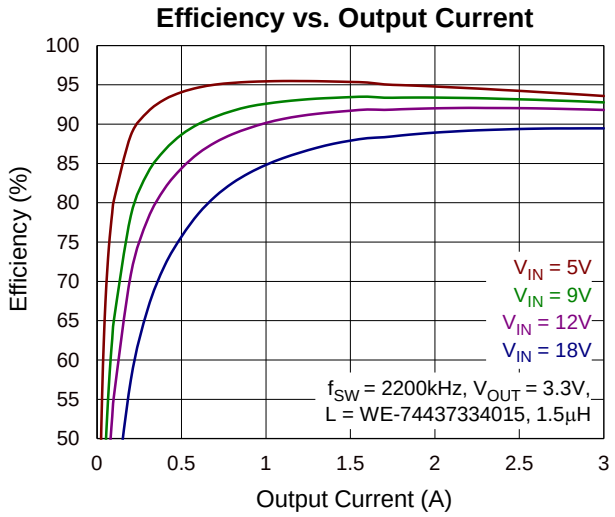


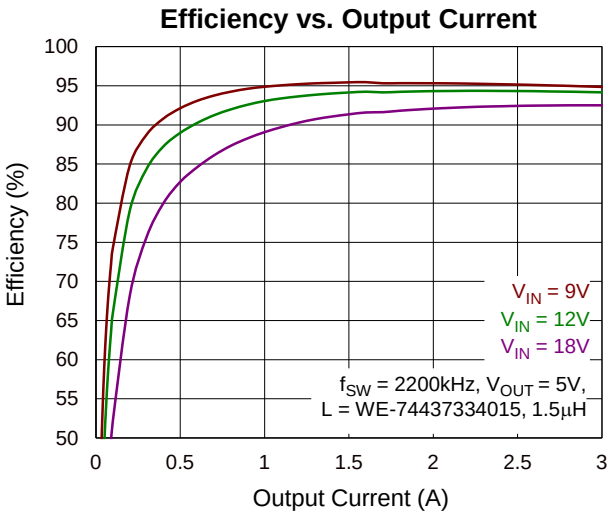
Efficiency vs. Output Current

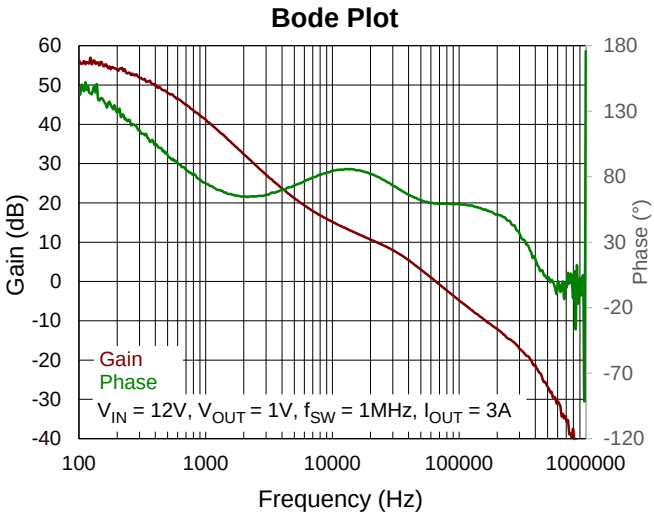


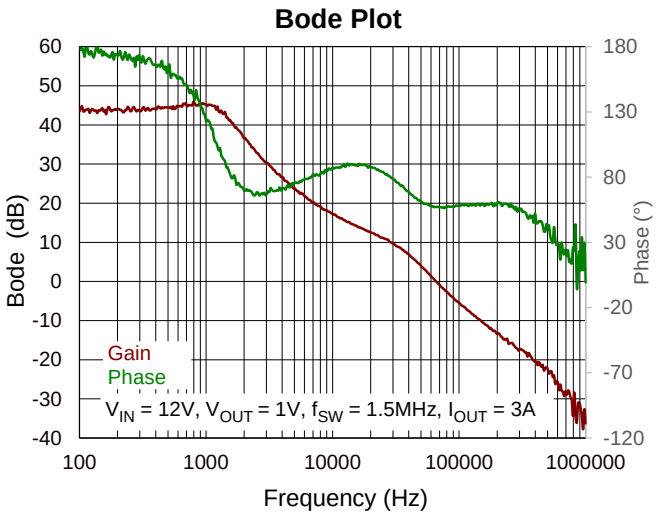
Efficiency vs. Output Current

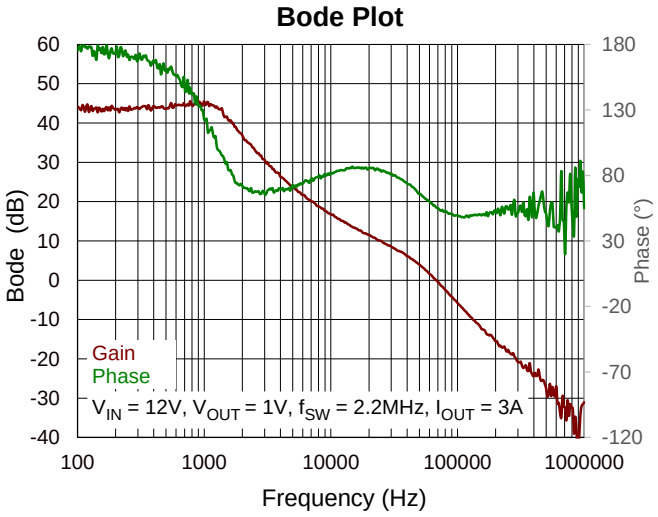


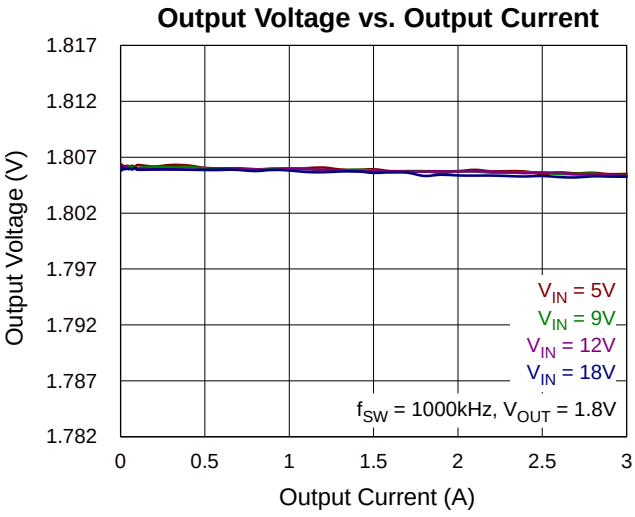




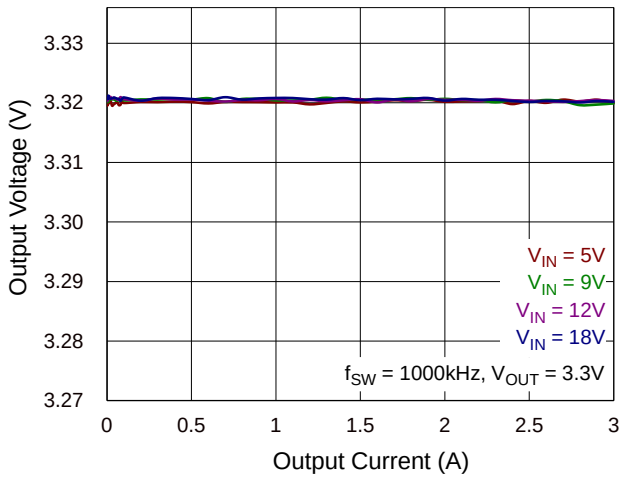




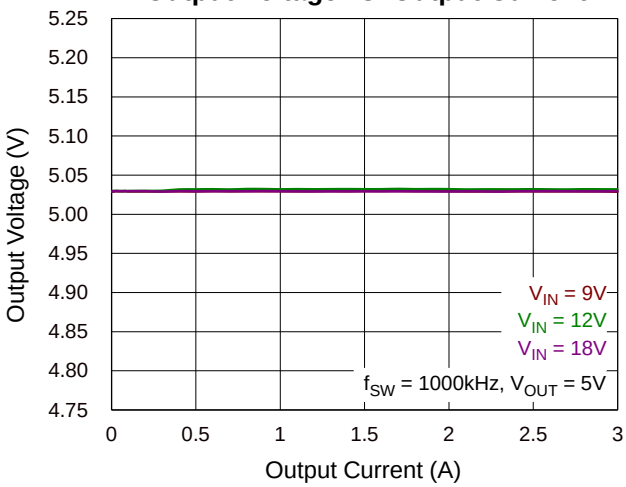




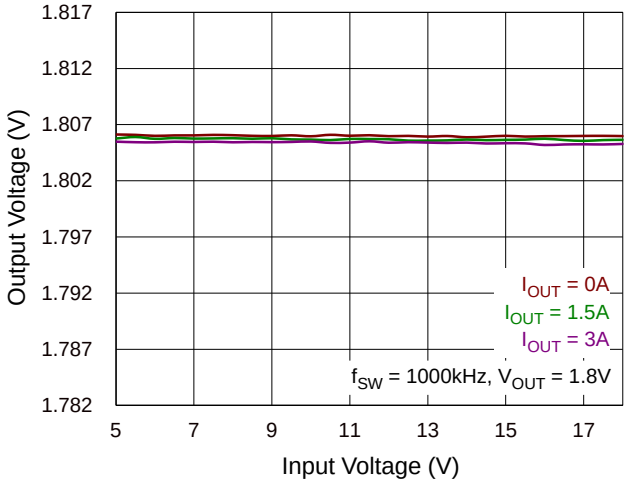
Output Voltage vs. Output Current



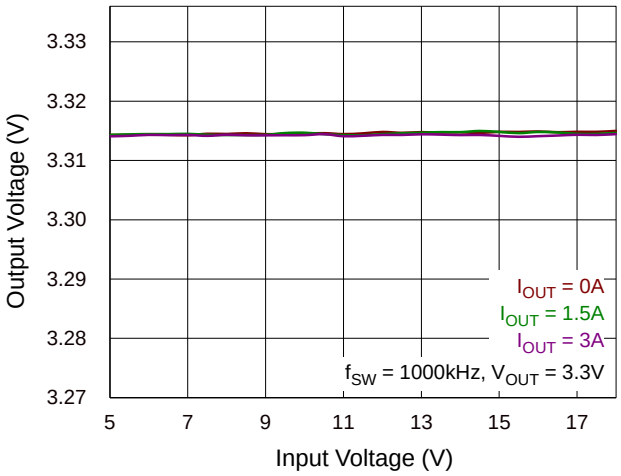
Output Voltage vs. Output Current



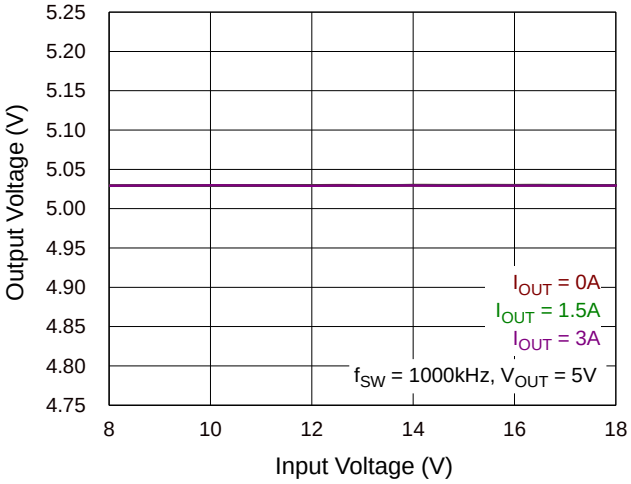
Output Voltage vs. Input Voltage



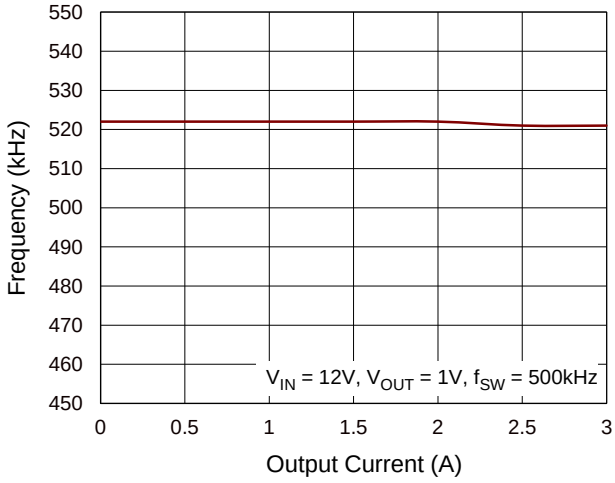
Output Voltage vs. Input Voltage



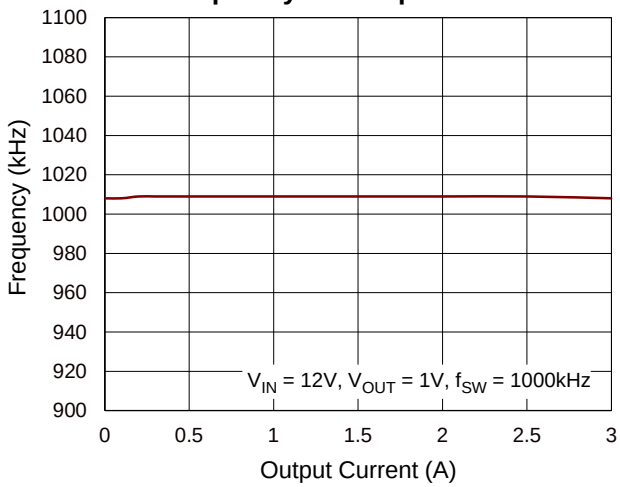
Output Voltage vs. Input Voltage



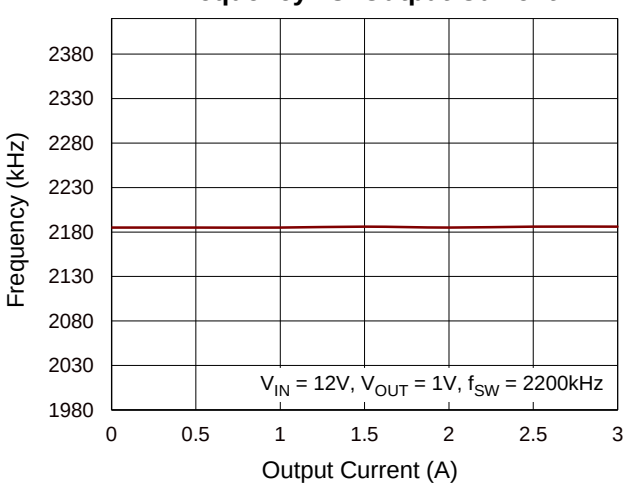
Frequency vs. Output Current



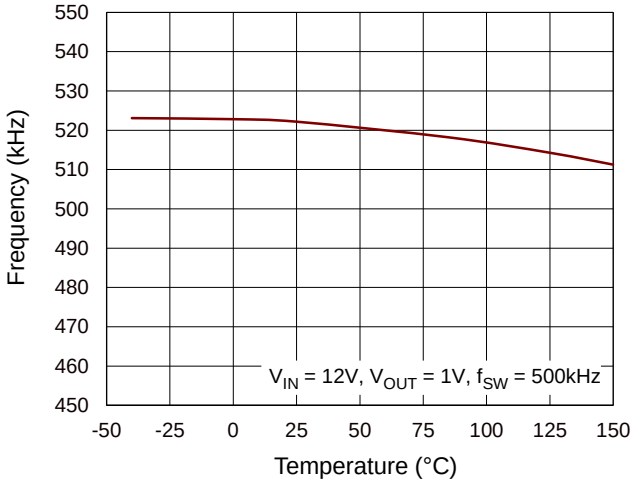
Frequency vs. Output Current



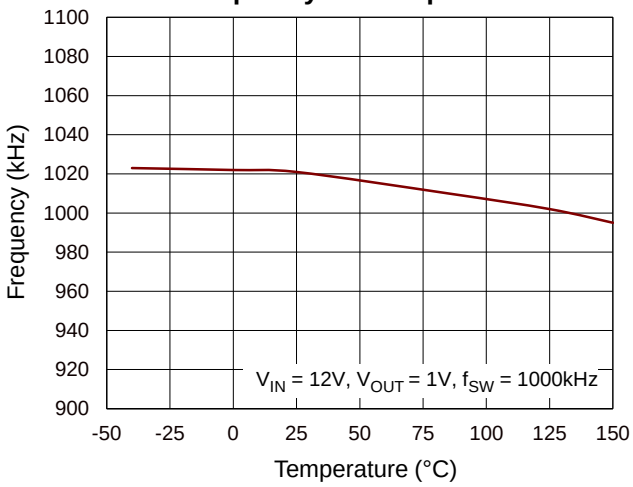
Frequency vs. Output Current



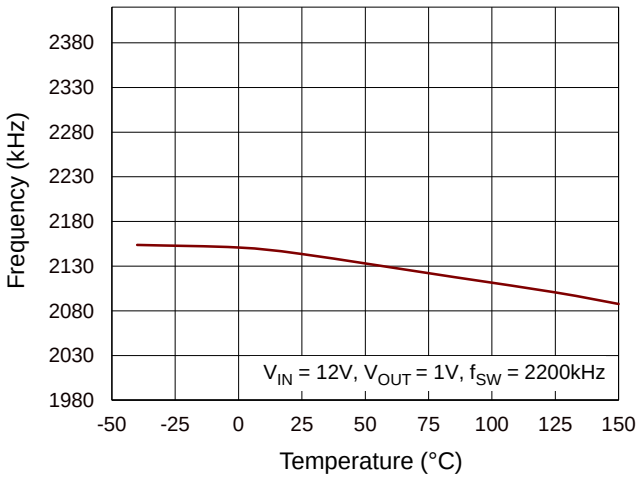
Frequency vs. Temperature



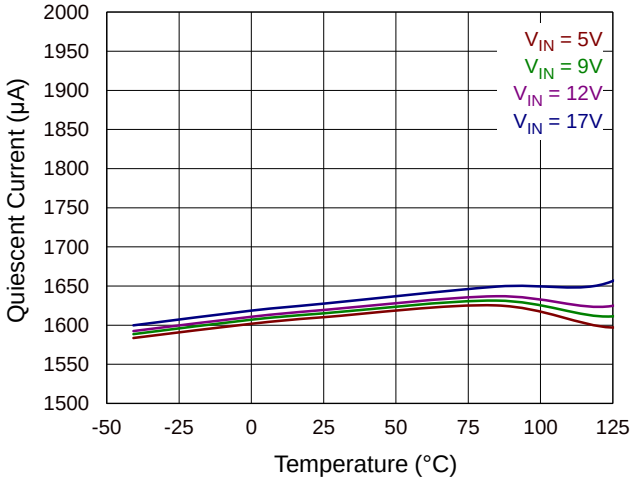
Frequency vs. Temperature



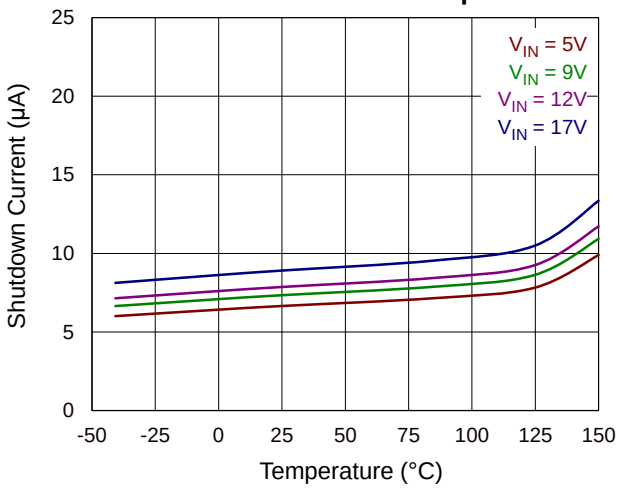
Frequency vs. Temperature



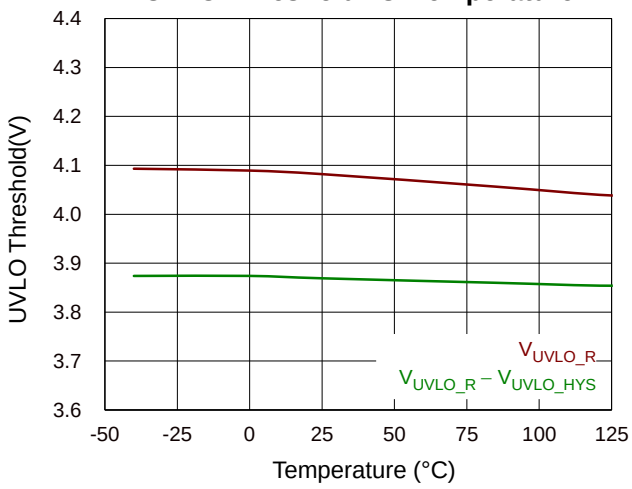
Quiescent Current vs. Temperature



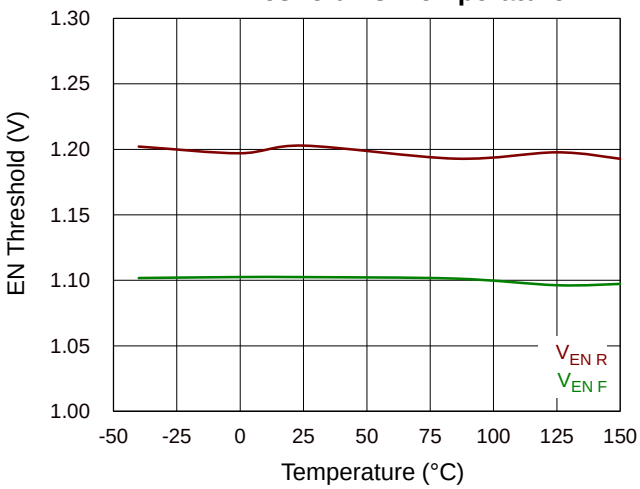
Shutdown Current vs. Temperature



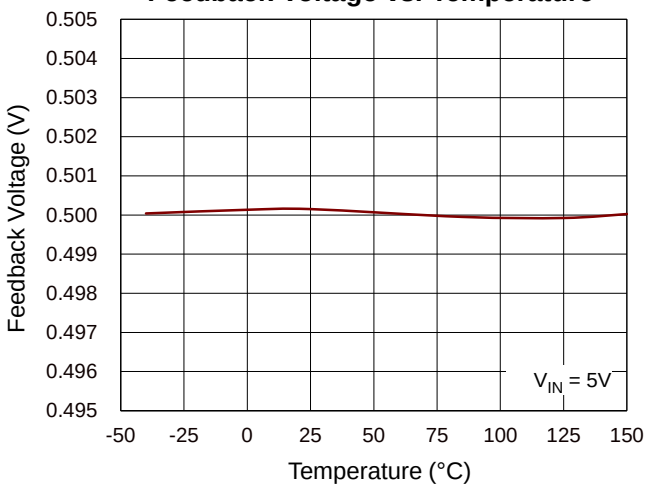
UVLO Threshold vs. Temperature



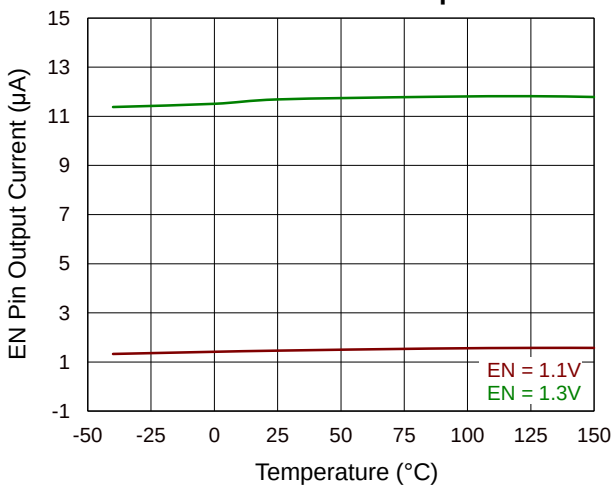
EN Threshold vs. Temperature



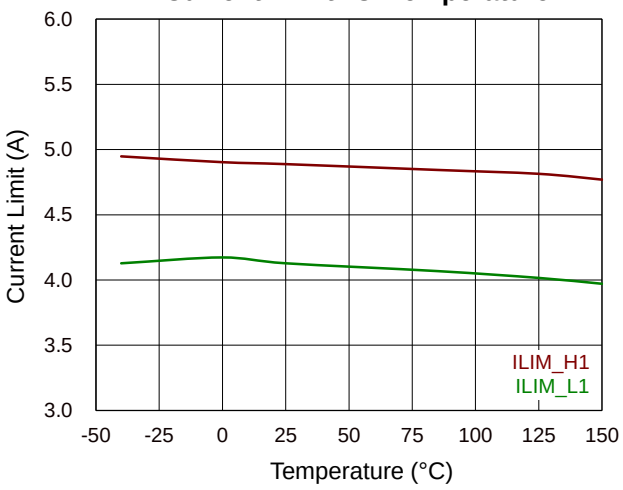
Feedback Voltage vs. Temperature



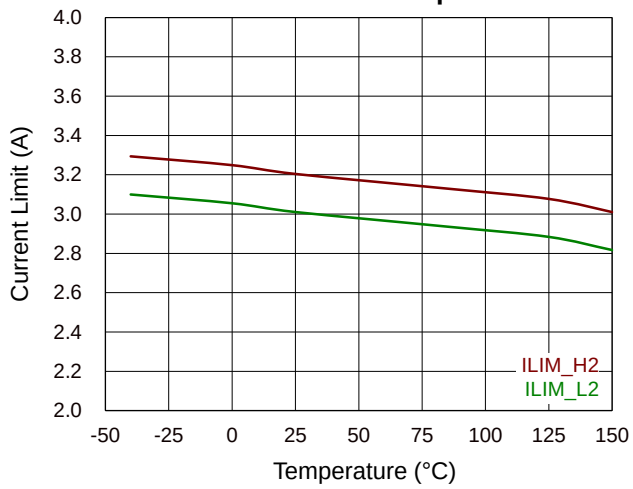
Enable Current vs. Temperature



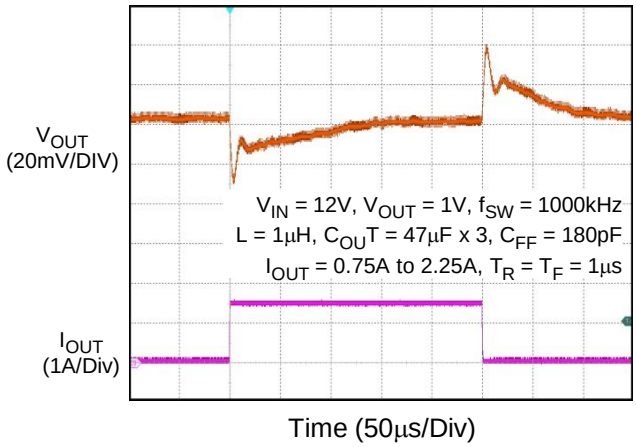
Current Limit vs. Temperature



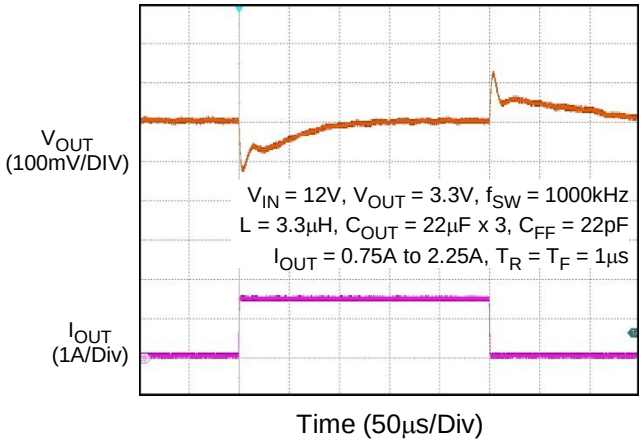
Current Limit vs. Temperature



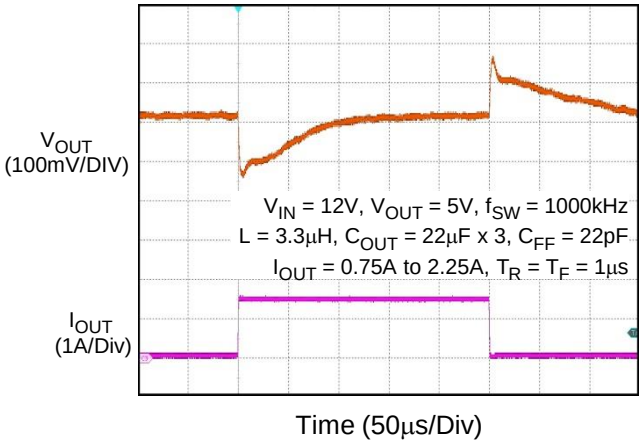
Transient Response



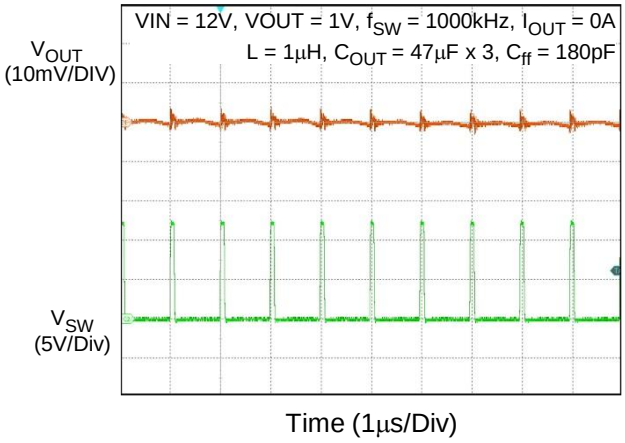
Transient Response



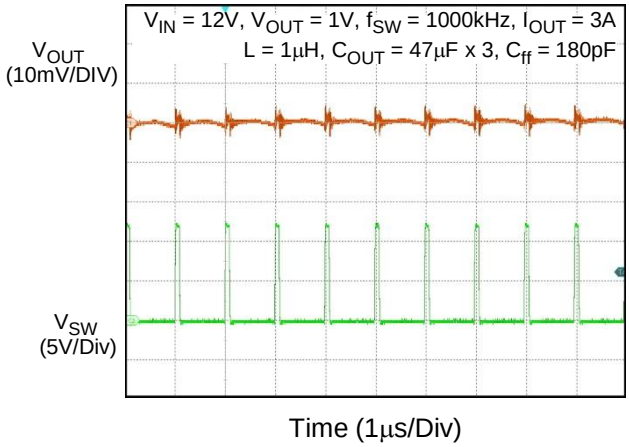
Transient Response



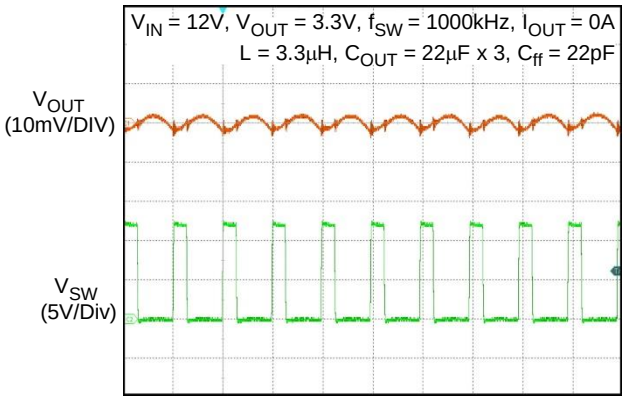
Output Ripple Voltage



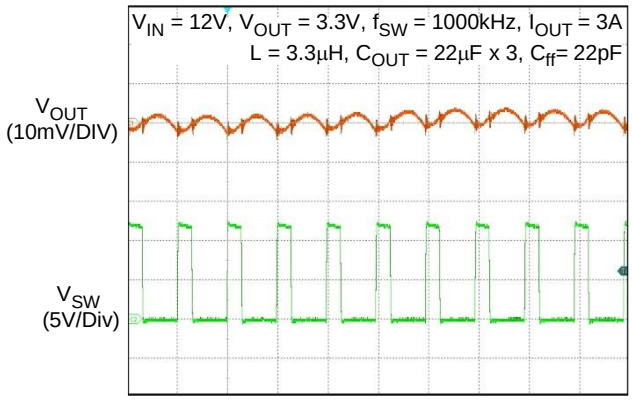
Output Ripple Voltage



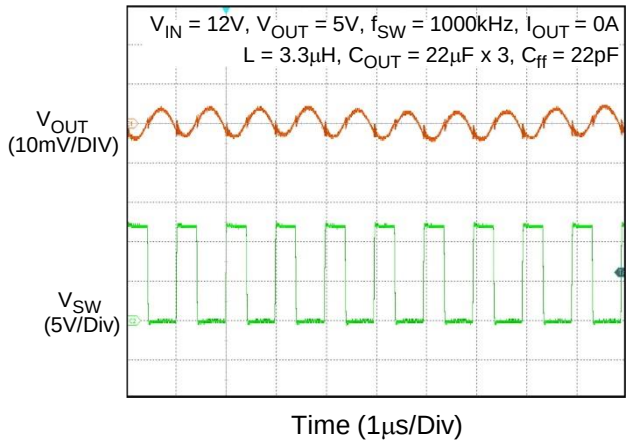
Output Ripple Voltage



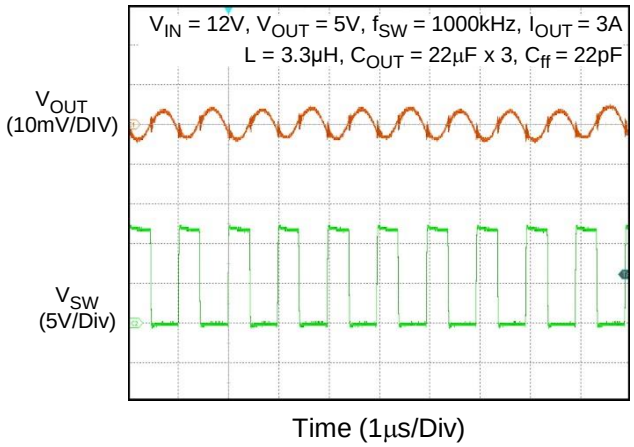
Output Ripple Voltage



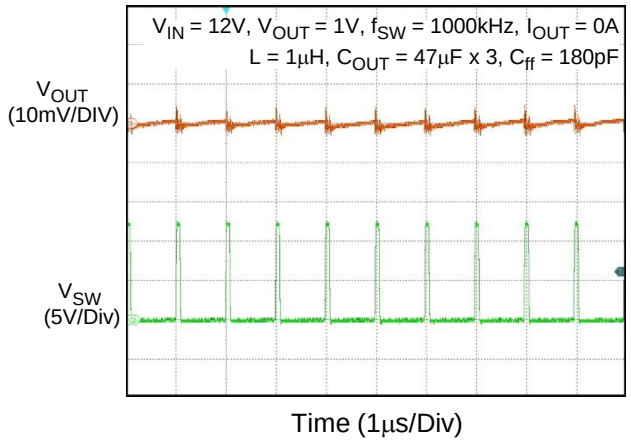
Output Ripple Voltage



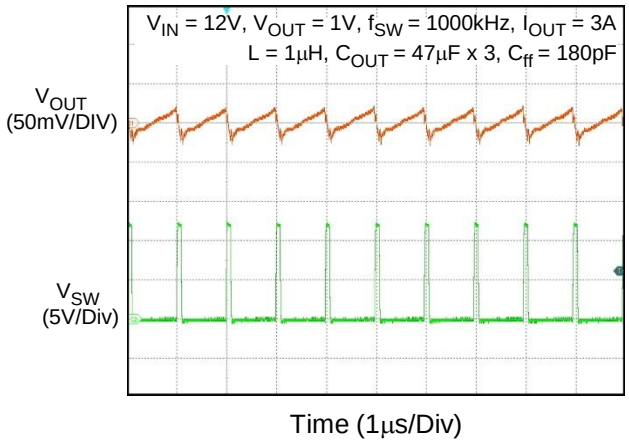
Output Ripple Voltage



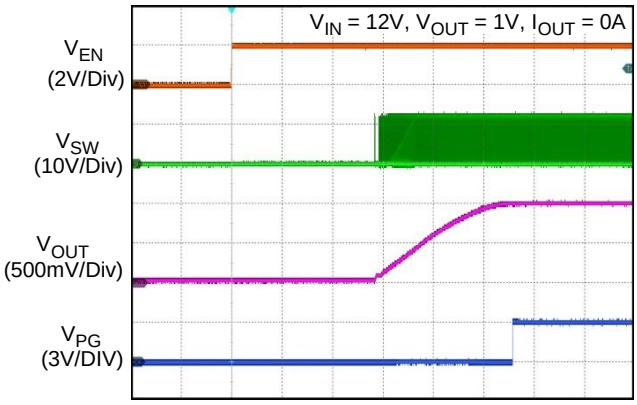
Input Ripple Voltage



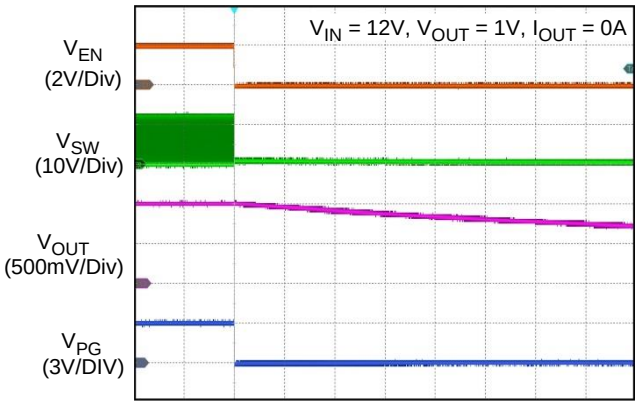
Input Ripple Voltage



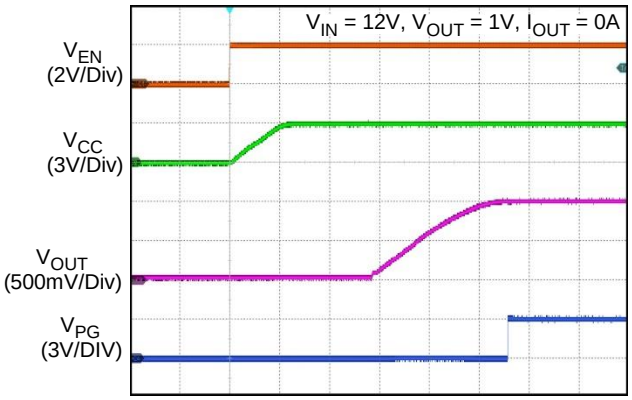
Power On from EN



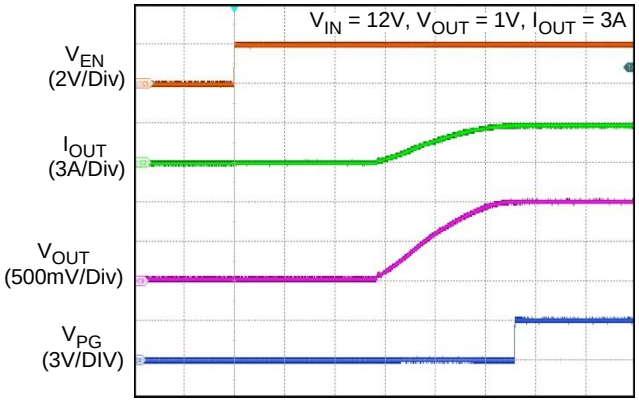
Power Off from EN



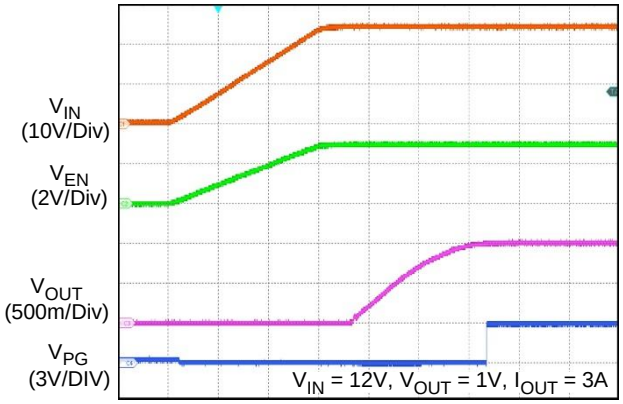
Power On from EN



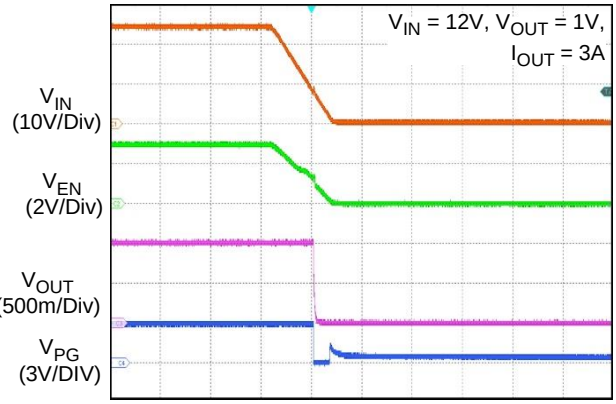
Power On from EN



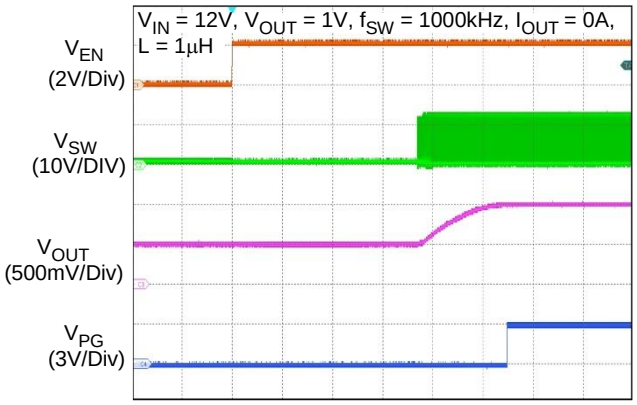
Power On from VIN



Power Off from VIN

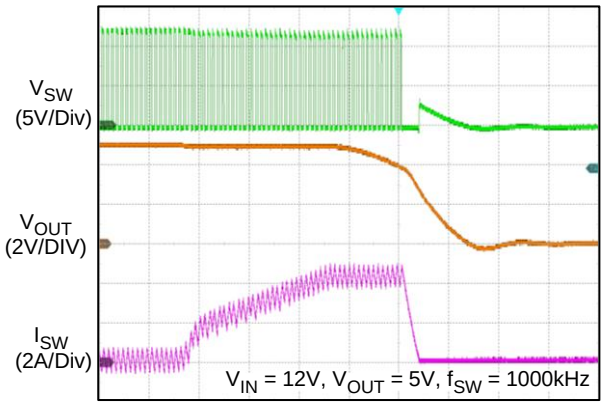


Pre-Bias Start-Up



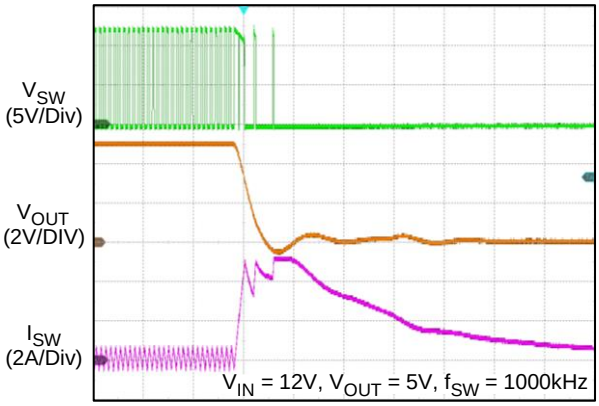
Time (1ms/Div)

Over-Current Protection - Overload



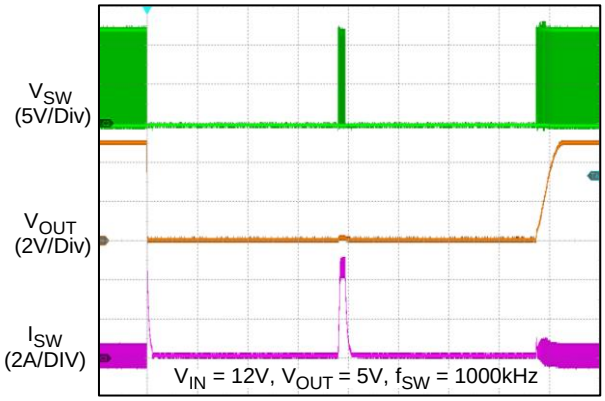
Time (20µs/Div)

Over-Current Protection - Short



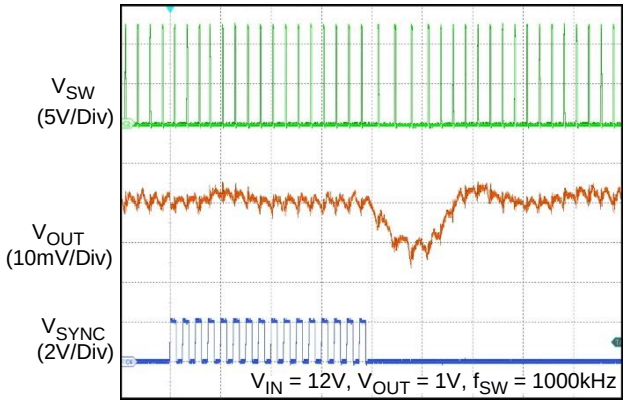
Time (20µs/Div)

Short-Circuit Protection and Recovery



Time (2ms/Div)

Clock Synchronization Transitions



Time (4µs/Div)

17 Operation

17.1 Control Loop

The RTQ2833A is a high-efficiency step-down converter that utilizes fast current-mode (FCM) control, offering excellent noise immunity and fast load transient response without the need for complex external compensators. FCM is an enhanced current control architecture that incorporates an internal oscillator to provide a fixed-frequency clock signal for maintaining constant frequency operation. The ramp generation circuit simulates the information of the inductor current, enhancing the noise immunity of the loop and allowing the use of low equivalent series resistance (ESR) output capacitors, such as Multi-Layer Ceramic Capacitors (MLCC).

Furthermore, the control loop integrates slope compensation to improve stability under various operating conditions. The quick response circuit enhances transient response by adjusting the offset of the virtual ramp. It monitors the feedback voltage (V_{FB}) and supports an extension of the on-time duration when the output voltage decreases, while reducing the on-time duration when the output voltage exceeds the desired level.

17.2 Power and Bias Supply

The VIN pins on the RTQ2833A supply voltage to the drain terminal of the internal HSFET and serve as a bias voltage source for the internal regulator, generating a 3V to VCC voltage. The VCC pin voltage is used for internal chip bias and gate drive for the LSFET, while the gate drive for the HSFET is provided by a floating supply (C_{BOOT}) located between the BOOT and SW pins. This floating supply is charged by an internal synchronous diode from the VCC. Additionally, another internal charge pump ensures that the C_{BOOT} voltage is sufficient to activate the HSFET.

17.3 Enable, Start-Up, Shutdown, and UVLO

The RTQ2833A implements Undervoltage-Lockout (UVLO) protection to prevent operation without fully turn-on the internal power MOSFETs. The UVLO monitors the VIN voltage. When the VIN voltage is lower than the Undervoltage-Lockout Rising threshold (V_{UVLO_R}), the device stops switching. UVLO is non-latching protection mechanism.

The EN pin is provided to control the device turn-on and turn-off states. When the EN pin voltage is above the EN Input Voltage Rising Threshold (V_{EN_R}), the device starts switching and when the EN pin voltage falls below the EN Input Voltage Falling Threshold (V_{EN_F}), it stops switching. The RTQ2833A internally weak pulls-up the EN pin. When appropriate voltages are present on the VIN, VCC, and EN pins, the RTQ2833A will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp will limit the ramp rate of the output voltage to prevent excessive input current during start-up. The soft-start ramp is selectable through a setting resistor to the MODE pin. Figure 1 below shows the typical power-up sequence of the device when the EN pin voltage crosses the EN Input Rising Threshold.

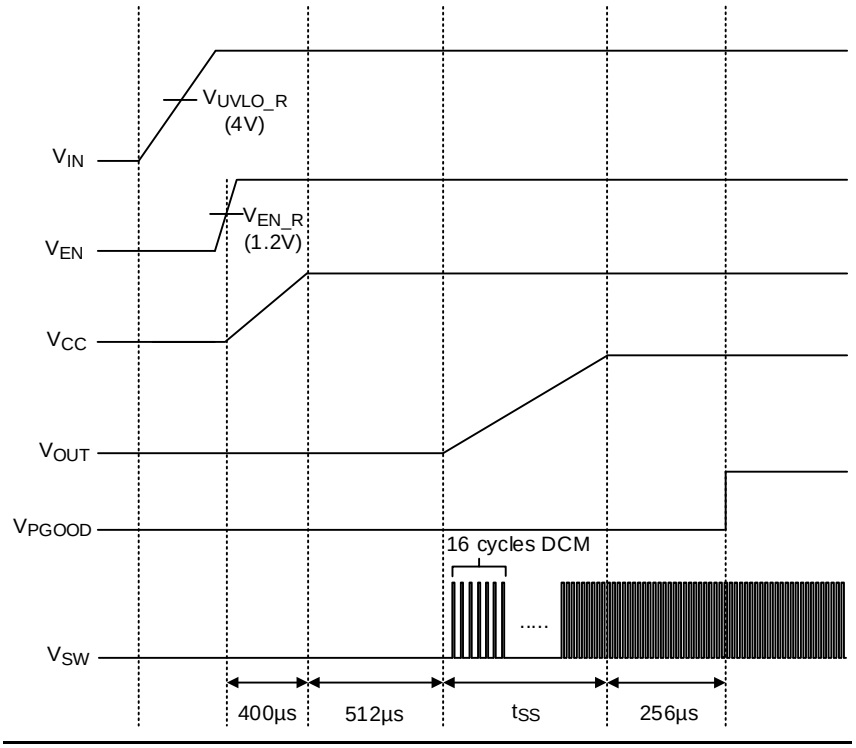


Figure 1. Power Up Sequence

17.4 Pre-Bias

If there is a residual voltage on the output voltage before start-up, both the internal HSFET and LSFET are prohibited from switching until the internal V_{REF} ramps up higher than feedback voltage. When the soft-start ramp exceeds the feedback voltage, switching will begin, and the output voltage will smoothly rise from the pre-biased level to its regulated target. During start up, the device operates in discontinuous conduction mode (DCM).

17.5 Mode Selection for Soft-Start Time and Current Limit

The MODE pin offers 24 different states of operation as a combination of current Limit and soft-start time. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 8. The MODE pin setting can be reset by cycling the VIN power or EN ON/OFF. The R_{MODE} is required to use a 1% tolerance resistor.

17.6 Quick Response Loop and Transient Response

The RTQ2833A features a built-in dynamic adjustment loop that automatically activates to enhance dynamic response when the FB voltage drops or rises by 1%. The dynamic adjustment is categorized into three levels: normal, fast, and fastest, to align with the response speed of the transient loop. Selecting the "fastest" level typically provides the optimal transient response. However, it may lead to minor ringing in the output voltage, which does not impact the stability of the loop during steady state operation.

Table 8. MODE Pin Setting

R_{MODE} (kΩ)	Current Limit	Transient Response	Soft-Start Time (ms)
1.78	High	Normal	0.5
2.21	High	Normal	1
2.74	High	Normal	2
3.32	High	Normal	4
4.02	High	Fast	0.5
4.87	High	Fast	1
5.9	High	Fast	2
7.32	High	Fast	4
9.09	High	Fastest	0.5
11.3	High	Fastest	1
14.3	High	Fastest	2
18.2	High	Fastest	4
22.1	Low	Normal	0.5
26.7	Low	Normal	1
33.2	Low	Normal	2
40.2	Low	Normal	4
49.9	Low	Fast	0.5
60.4	Low	Fast	1
76.8	Low	Fast	2
102	Low	Fast	4
137	Low	Fastest	0.5
174	Low	Fastest	1
243	Low	Fastest	2
412	Low	Fastest	4

17.7 Switching Frequency, Minimum On-Time, and Minimum Off-Time

The RTQ2833A offers five different switching frequencies of 500kHz, 750kHz, 1000kHz, 1500kHz, and 2200kHz by setting a resistor R_{CONF} from the SYNC/FSEL pin to GND. The frequency options are listed in Table 9. The selection of the operating frequency is a trade-off between efficiency and component size. High-frequency operation allows the use of smaller inductors and capacitors. Operating at lower frequencies improves efficiency by reducing internal gate charge and transition losses but requires larger inductance and/or capacitance values to maintain low output ripple voltage. An additional constraint on operating frequency is the minimum controllable on-time and off-time. The minimum on-time is the shortest duration in which the high-side power MOSFET (HSFET) can be in its “on” state, typically 30ns. In steady-state operation, the minimum duty cycle can be estimated by ignoring component losses as follows:

$$D_{MIN} = f_{SW} \times t_{ON\_MIN}$$

where t_{ON_MIN} is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. The minimum off-time, t_{OFF_MIN}, is the shortest duration that the RTQ2833A can turn on the low-side power MOSFET (LSFET), trip the current comparator, and turn the power MOSFET back off. This time is 140ns (maximum). The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF\_MIN})$.

Table 9. Switching Frequency and Spread Spectrum Selection

f_{SW} (kHz)	Spread Spectrum	Recommended E96 Standard Value (1%) (kΩ)	Recommended E12 Standard Value (10%) (kΩ)	R_{CONF} Normal Range (kΩ)
500	ON	243	270	243 - 270
750	ON	174	180	174 - 180
1000	ON	118	120	118 - 121
1500	ON	80.6	82	80.6 - 82.5
2200	ON	49.9	47	47.0 - 51.1
500	OFF	24.3	27	24.3 - 27
750	OFF	17.4	18	17.4 - 18.0
1000	OFF	11.8	12	11.8 - 12.1
1500	OFF	8.06	8.2	8.06 - 8.25
2200	OFF	4.99	4.7	<5.11

17.8 Spread-Spectrum Operation

The periodic switching signals can cause energy to concentrate at one frequency and its harmonics, which may lead to radiated energy and potential electromagnetic interference (EMI) issues. The RTQ2833A features an optional spread spectrum function, which can be enabled/disabled by connecting a resistor from SYNC/FSEL to ground, further simplifying compliance with CISPR and automotive EMI requirements. The spread-spectrum function activates after the soft-start process is completed. It operates using a pseudo-random sequence with a +10% spread of the switching frequency. For example, when the RTQ2833A is set to 2.2MHz, the frequency varies from 2.2MHz to 2.42MHz. Therefore, the RTQ2833A still ensures that the 2.2MHz switching frequency setting does not drop to the AM band limit of 1.8MHz. Note that the spread spectrum function cannot be activated when the device is synchronized with an external clock via the SYNC/FSEL pin.

17.9 Synchronization to an External Clock

The RTQ2833A can be synchronized with an external clock suppling to the SYNC/FSEL pin.

The external clock can be supplied at any time. When the external clock is supplied before the device starts up, the switching frequency follows the external clock and the setting resistor R_{CONF} can be floating.

If the external clock is supplied after the device has started up, the PWM cycle will switch to synchronize with the external clock by counting 4 switching cycles. If the external clock is lost during normal operation, the PWM will switch to the corresponding internal clock, as shown in Table 10.

Table 10. External Clock Corresponding to Internal Clock

External Synchronized Clock F_{SW} (kHz)	Corresponding Internal Clock F_{SW} (kHz)
400 - 600	500
600 - 857	750
857 - 1200	1000
1200 - 1810	1500
1810 - 2640	2200

The threshold of the external SYNC clock frequency range has an approximate tolerance of ±5%. Table 11 shows the decoding range of the external clock.

Table 11. Frequency Decode Thresholds

MINIMUM (kHz)	TYPICAL (kHz)	MAXIMUM (kHz)
570	600	630
814	857	900
1140	1200	1260
1736	1810	1884

17.10 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure enough voltage in the bootstrap capacitor for turning on the high-side MOSFET switch under any condition. The BOOT UVLO feature is typically activated when the converter operates at an extremely high conversion ratio, or when the higher VOUT application runs at a very light load. For extremely high conversion ratios after soft-start is finished, the low-side MOSFET switch may not have enough turn-on time to charge the bootstrap capacitor. The device monitors the voltage of the bootstrap capacitor and forces to turn on the low-side MOSFET switch when the voltage of the bootstrap capacitor falls below $V_{BOOT\_UVLO\_L}$ (typically, 2.17V). The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.35V).

17.11 Internal Regulator

The device integrates a 3V linear regulator (VCC) that is supplied by VIN and provides power to the internal circuitry. The VCC can be used as the PGOOD pull-up supply, but it is “NOT” allowed to power other devices or circuitry. The VCC pin must be bypassed to ground with a minimum effective capacitance of 1μF. In many applications, a 2.2μF, X7R is recommended, and it should be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

17.12 Power-Good Output

The RTQ2833A features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of the comparator prevents false flag operations for short excursions in the output voltage, such as during line and load transients. Pull up PGOOD with a resistor to VCC or an external voltage below 5.5V. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above the power-good high threshold V_{TH_PGLH1} (typically 92% V_{REF}), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapses. When V_{FB} exceeds V_{TH_PGHL1} (typically 116% V_{REF}), the PGOOD pin will be pulled low. The V_{PGOOD} can be pulled high again if V_{FB} drops back to the power-good high threshold V_{TH_PGLH2} (typically 108% V_{REF}). When V_{FB} is below the power-good low threshold V_{TH_PGHL2} (typically 84% V_{REF}), the PGOOD pin will be pulled low. Once started up, if any internal protection is triggered, PGOOD will be pulled low to ground. The internal open-drain pull-down device (10Ω, typically) will pull the PGOOD pin low. The power-good indication profile is shown in Figure 2.

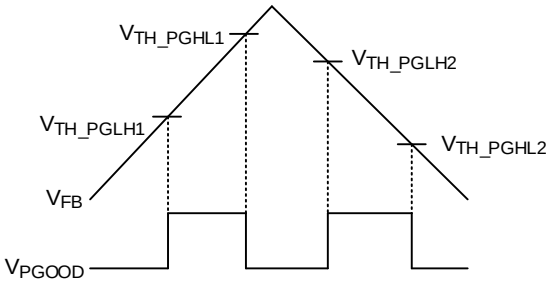


Figure 2. The Logic of PGOOD

17.13 Current Protection

The RTQ2833A provides two levels of current protection, which are adjustable according to the recommended mode pin-to-ground resistance in Table 8. When selecting the high current level, both the high-side current limit and the low-side current limit are set to the high level. Similarly, when selecting the low current level, both the high-side current limit and the low-side current limit are set to the low level. For reverse overcurrent scenarios, the RTQ2833A also provides the low-side switch sinking current limit function to restrict the reverse current.

17.14 High-Side Switch Peak Current-Limit Protection

The RTQ2833A integrates cycle-by-cycle high-side switch peak current-limit protection to prevent abnormal increases in inductor current, which could exceed the rated saturation current of the inductor, effectively avoiding device overheating or damage in cases of output overload or short circuit.

In the event of an overcurrent condition, the converter promptly shuts off the high-side MOSFET switch and activates the low-side MOSFET switch. The high-side MOSFET will not be reactivated until the current falls below the low-side current limit, preventing the inductor current from exceeding the high-side MOSFET switch peak current limit.

When the high-side current limit is continuously triggered for 15 cycles, the RTQ2833A enters Hiccup mode.

The current level specifications in the electrical specifications are obtained through measurements in open-loop conditions. In practical applications, the inductor current through the high-side MOSFET switch is measured after a certain delay when the high-side MOSFET switch is turned on. This may result in slight discrepancies between actual and specified values due to varying inductor current slopes.

17.15 Low-Side Switch Current-Limit Protection and Output Undervoltage Protection

The RTQ2833A not only implements the high-side switch peak current limit but also provides the sourcing current and sinking current limits for the low-side MOSFET switch. With these current protections, the IC can easily control inductor current on both sides of the switch and avoid current runaway for short-circuit conditions. For the low-side MOSFET switch sourcing current limit, there is a specific comparator in the internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit, the new switching cycle is not initiated until the inductor current drops below the low-side MOSFET switch sourcing current limit. For the low-side MOSFET switch sinking current-limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side MOSFET switch sinking current exceeds the low-side MOSFET switch sinking current limit I_{L_SNK} (minimum, 1.9A), the device immediately turns off both the low-side and high-side MOSFET switches.

When the current is limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below the output UVP threshold (V_{UVP}), the UVP comparator detects it and shuts down the device to avoid the excessive heat. If the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated. When the overcurrent condition is removed, the output voltage returns to the regulated value.

17.16 Output Overvoltage Protection (OVP)

The RTQ2833A supports output overvoltage protection (OVP) by constantly monitoring the feedback voltage V_{FB}. If V_{FB} exceeds above the overvoltage protection trip threshold (typically 120% of the internal reference voltage), HSFET turns off and LSFET turns on until the low-side switch sinking current limit is reached. After the output voltage is lower than the overvoltage protection recovery threshold (typically 108% of the internal reference voltage), the RTQ2833A restarts and executes a soft-start sequence.

17.17 Over-Temperature Protection (OTP)

The RTQ2833A includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operations when the junction temperature exceeds the Over-Temperature Protection Threshold (T_{OTP}). Once the junction temperature cools down by the Over-Temperature Protection Hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

17.18 Output Voltage Discharge

An internal 100Ω discharge switch discharges the VOUT through the SW node during any fault events such as UVP, OTP, OCP, or when the VIN voltage falls below UVLO.

17.19 Discontinuous Conduction Mode (DCM) during Soft Start

During the soft start period, the converter operates in discontinuous conduction mode in the first 16 switching cycles to prevent the discharge of residual bias on the output voltage. After 16 cycles of DCM, the zero-current detection level gradually shifts towards the negative current direction to mitigate the drop in VOUT during the transition. When the soft start is completed, the converter enters FCCM mode.

17.20 Forced Continuous-Conduction Mode (FCCM)

The RTQ2833A operates in forced continuous-conduction mode during normal operation.

18 Application Information

(Note 9)

A general RTQ2833A application circuit is shown in the typical application circuit section. External component selection is largely driven by the load requirements. First, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT}, can be selected. Next, feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as the EN and UVLO threshold.

18.1 Switching Frequency and Spread Spectrum Selection

The switching frequency and spread spectrum function are configured by connecting a resistor from the SYNC/FSEL pin to ground. The selection of the switching frequency is a trade-off between efficiency and system component size. High-frequency operation allows the use of smaller inductor and capacitor values. Operating at lower frequencies improves efficiency by reducing internal gate charge and transition losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for a smaller case size, but the increased ripple lowers the effective current-limit threshold and increases the AC losses in the inductor. To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines the ripple current and the load-transient performance.

The selected inductor must have a sufficient saturation current rating above the peak inductor current before saturation. The peak inductor current (I_{L_PEAK}) is estimated as below.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

The reverse inductor current should be considered. The design of the inductor valley current should be higher than I_{L_SNK} to prevent triggering the low-side switch sinking current limit during no-load operation.

18.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. The C_{IN} should be sized appropriately to prevent large input ripple. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 3 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors.

The equivalent series resistance (ESR) is very low for ceramic capacitors. The ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} = 200mV for typical applications.

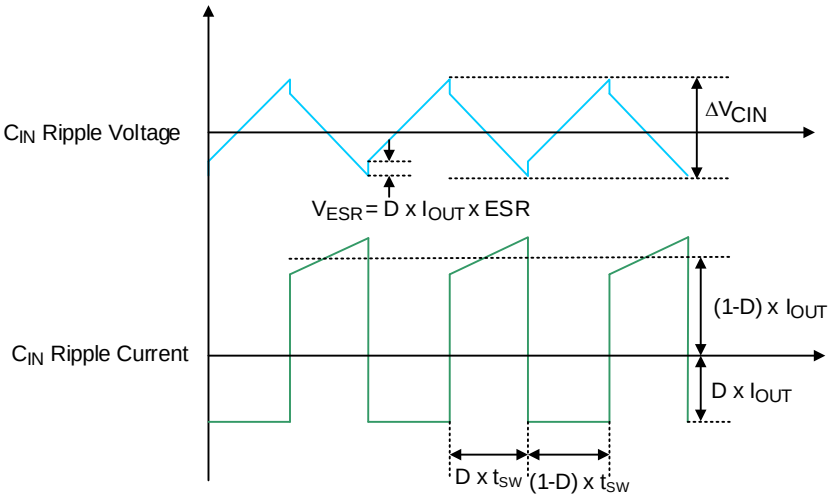


Figure 3. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the converter can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) using the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which should be considered when evaluating the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worst-case $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for the design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (under-damped) tank circuit. If the RTQ2833A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, one small ceramic capacitor of 0.1μF should be placed close to the part. The capacitors should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.4 Output Capacitor Selection

The selection of C_{OUT} is determined by considering the voltage ripple, transient loads, and control loop stability. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components: the ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, and can be expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The highest output ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration when choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined using the following equation:

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated using the following equation:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.5 Internal VCC Regulator

Good bypassing at the VCC pin is necessary to supply the high transient currents required by the power MOSFET gate drivers. Place a low ESR MLCC capacitor with capacitance ≥ 2.2μF (or effective capacitance ≥ 1μF) as close as possible to the VCC pin. The rated voltage of C_{VCC} is at least 6.3V or higher to minimize DC bias derating. A 0603 or 0805 size capacitor is recommended.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect VCC to provide power to other devices or loads, or to supply VCC voltage through an external power source.

18.6 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage approximately equal to V_{VCC} each time the LS-FET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is from 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications, a 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

EMI issues are worse when the switch is turned on rapidly due to high di/dt noises. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (<10Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 4, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor connection.

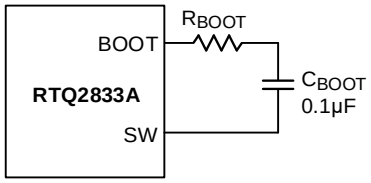


Figure 4. External Bootstrap Resistor at the BOOT Pin

18.7 Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 5. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage V_{REF}, is typically 0.5V

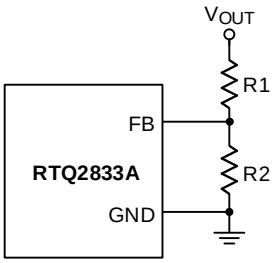


Figure 5. Output Voltage Setting

The selection of voltage divider resistors can refer to suggested component selections. The recommended resistance for R2 is in the range of 1kΩ to 10kΩ to ensure good noise immunity. The resistance of R1 can then be obtained as follows:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used. The placement of the resistive divider should be very close to the FB pin to minimize PCB trace length and noise immunity considerations. Furthermore, great care should be taken to route the feedback trace away from noise sources, such as the inductor or the SW trace.

18.8 Feedforward Capacitor (C_{FF})

Using a feedforward capacitor (C_{FF}) to improve stability and extend bandwidth is a common practice, and in the stability of the RTQ2833A loop, C_{FF} plays a crucial role. Adding capacitor C_{FF} between the upper feedback divider resistor, as shown in Figure 6.

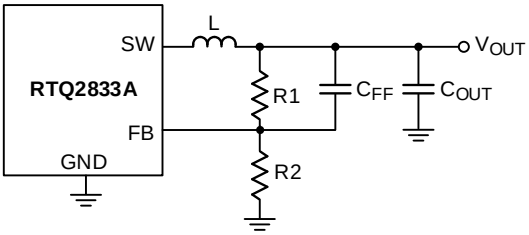


Figure 6. Feedback Loop with Feedforward Capacitor

The capacitor adds a dependent zero to the pole in the control loop, which can be strategically placed to improve phase margin and bandwidth. This improvement can be measured in both the transient response and the Bode plot, as shown in Figure 7. The pole frequency is higher than the zero frequency ($f_Z < f_P$), so once the zero location is determined, the pole location is also fixed. The recommended position for the zero is at 1/4 of the switching frequency, as indicated by the following formula, which can be used to quickly calculate the value of C_{FF}.

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}}$$

$$f_P = \frac{1}{2\pi (R1//R2) \times C_{FF}}$$

$$C_{FF} = \frac{2}{\pi \times R1 \times f_{SW}}$$

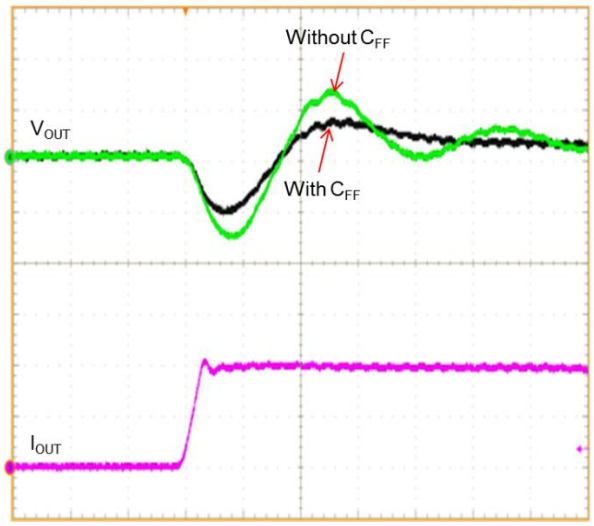


Figure 7. Load Transient Response with and without Feedforward Capacitor

18.9 Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the EN Input Voltage Rising Threshold (V_{EN_R}), the device starts switching. It stops switching when the EN pin voltage falls below the EN Input Voltage Falling Threshold (V_{EN_F}). The RTQ2833A internally weekly pull-down the EN pin. For automatic start-up, the EN pin can be connected to the input supply VIN directly through a pull-up resistor R_{EN}. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to VIN by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 8, to have an additional delay.

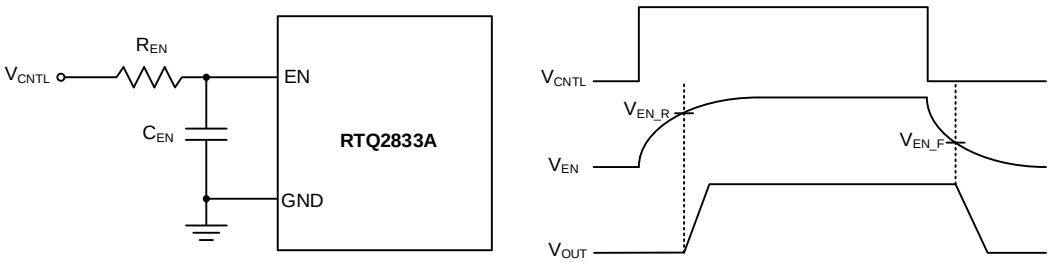


Figure 8. Enable Timing Control

An external MOSFET can be added for the EN pin for logic control, as shown in Figure 9. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be controlled by logic to pull down the EN pin.

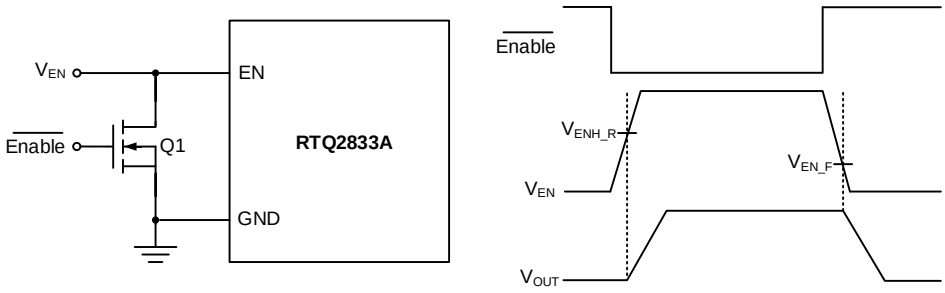


Figure 9. Logic Control for the EN Pin

Figure 10 shows the internal block diagram of the RTQ2833A EN pin. A resistor divider between VIN and EN can set a different turn-on (V_{START}) and turn-off thresholds (V_{STOP}) respectively. The EN pin has a pull-up current I_{ENP1} that sets the default state of the pin when it is floating. This current increases to I_{ENP2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set as follows:

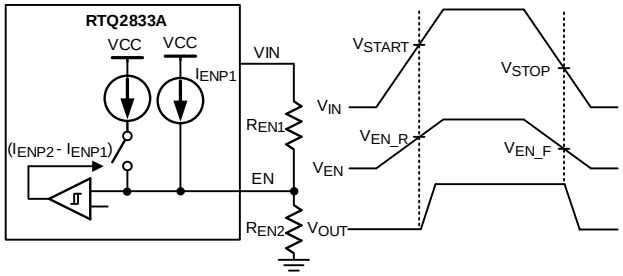


Figure 10. Adjustable VIN UVLO

$$R_{EN1} = \frac{V_{START} \times \frac{V_{EN\_F}}{V_{EN\_R}} - V_{STOP}}{I_{ENP1}\left(1 - \frac{V_{EN\_F}}{V_{EN\_R}}\right) + (I_{ENP2} - I_{ENP1})}$$

$$R_{EN2} = \frac{R_{EN1} \times V_{EN\_R}}{V_{START} + (R_{EN1} \times I_{ENP1}) - V_{EN\_R}}$$

where

I_{ENP1} = 1.5μA

I_{ENP2} = 11.6μA

V_{ENL} = 1.1V

V_{ENH} = 1.2V

18.10 Thermal Considerations

Thermal Considerations in many applications, the RTQ2833A does not generate much heat due to its high efficiency and low thermal resistance of its thermally enhanced WQFN-14L 3x2.5 (FC) package. However, in applications where the RTQ2833A is running at a high ambient temperature, high input voltage, and high switching frequency, the generated heat may exceed the maximum junction temperature of the part. To avoid permanent damage to the device, the junction temperature should never exceed the maximum junction temperature listed under Absolute Maximum Ratings. If the junction temperature reaches approximately 165°C, the RTQ2833A will stop switching the power MOSFETs until the temperature drops by about 12°C cooler. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA(EFFECTIVE)}$

Where

- $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C.
- T_A is the ambient operating temperature.
- $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. The temperature of the inductor also affects the θ_{JA}. A rule of thumb is to use $\theta_{JA(EFFECTIVE)} = \theta_{JA}$ x 120% for system design. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be enhanced by incorporating a copper ground heat sink. Additionally, including backside copper with thermal vias, stiffeners, and other enhancements can help reduce thermal resistance.

Table 12 shows the simulated thermal resistance of the RTQ2833A when mounted on PCBs with varying stack-up and copper thickness. The thermal model layout is based on the RTQ2833A evaluation board.

Table 12. Simulated Thermal Resistance with Difference Tack-Up and Copper Thickness

Simulated θ_{JA}	θ_{JA} (°C/W)
4 Layer with 2oz copper	33.7
4 Layer with 1oz copper	45
2 Layer with 1oz copper	61.5

As an example, consider the case when the RTQ2833A is used in applications where V_{IN} = 12V, I_{OUT} = 3A, V_{OUT} = 1V.

The efficiency at 1V, 3A is 85.4% by using WE-744316100 (1μH, 4.75mΩ DCR) as the inductor and measured at room temperature. The core loss 0.213W can be obtained from its website. In this case, the power dissipation of the RTQ2833A is

$$P_D = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I^2_{OUT} \times DCR + P_{CORE}\right) = 0.407W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 40.4°C/W by using the RTQ2833A evaluation board with a 4-layer PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

T_J = 0.407W x 40.4°C/W + 25°C = 41.4°C

18.11 Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2833A:

- Use a four-layer or six-layer PCB with a maximum ground plane for optimal thermal performance.
- VIN pins should have equal input capacitors on each side of the IC. Place these input capacitors as close to VIN pins as possible.
- Maximize the width and shorten the main current path, such as the VIN, SW, VOUT, and PGND copper plane, to minimize parasitic impedance.
- Place the decoupling capacitor, C_{VCC}, as close to VCC pin as possible.

- The ground connection between analog ground and power ground should be close to the IC to minimum the ground current loops. If there is only one ground plane, it should keep enough isolation between analog return signals and high power signals.
- Place the bootstrap capacitor, C_{BOOT}, as close to the IC as possible. Route the trace with a width of 20mil or wider. A 0.1μF to 1μF with 10V rating is recommended for the bootstrap capacitor.
- Place multiple vias under the device near VIN and PGND, and place near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2833A to additional ground planes within the circuit board and on the bottom side.
- The high-frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Connect the feedback sense network behind the via of the output capacitor rather than the inductor output node.
- Place the feedback components R1, R2, and C_{FF} near the device to minimize the FB trace distance, regardless of single-end or remote sensing.

Figure 11 is the layout example, which uses (70mm x80mm), four-layer PCB with 2oz copper.

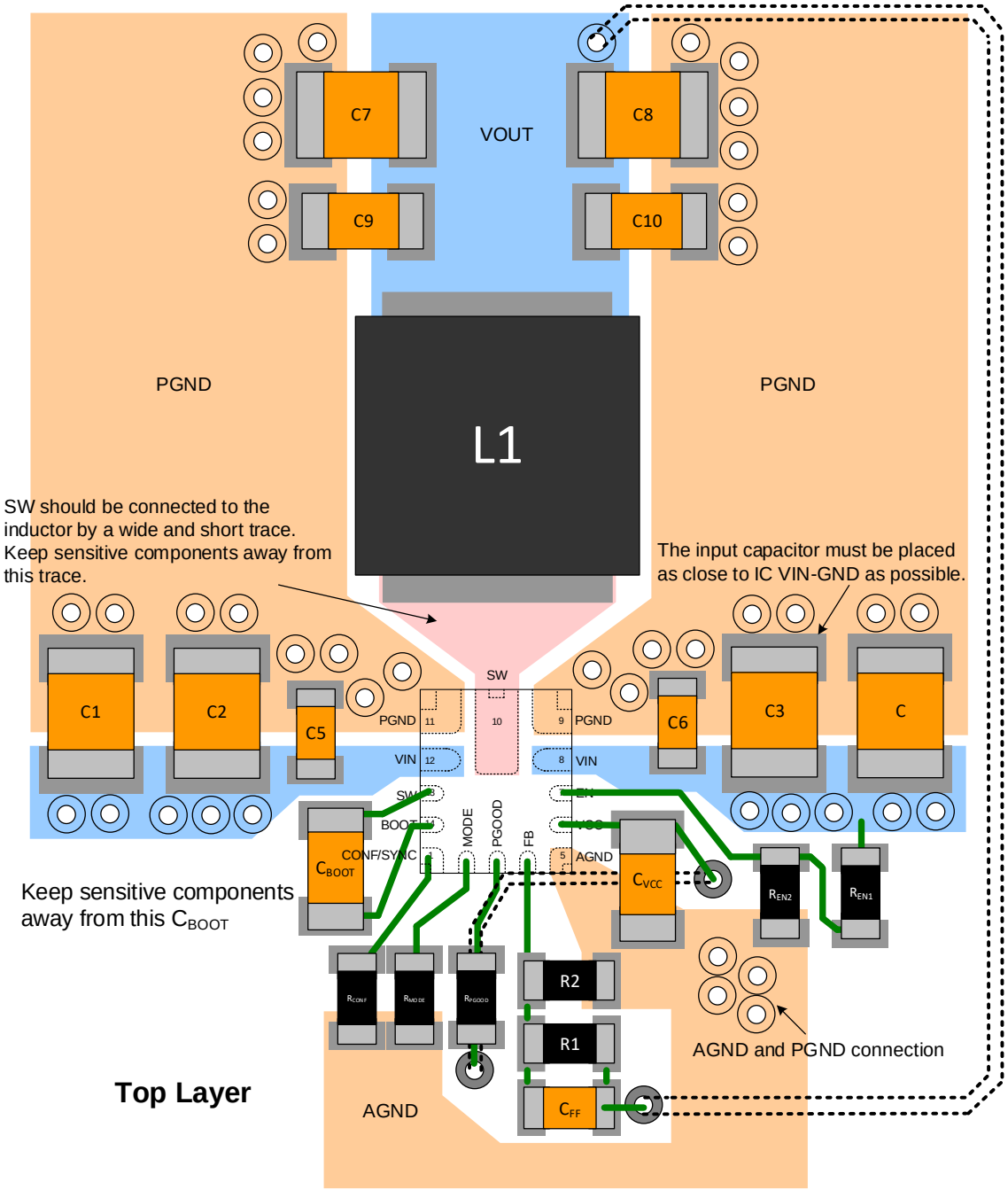
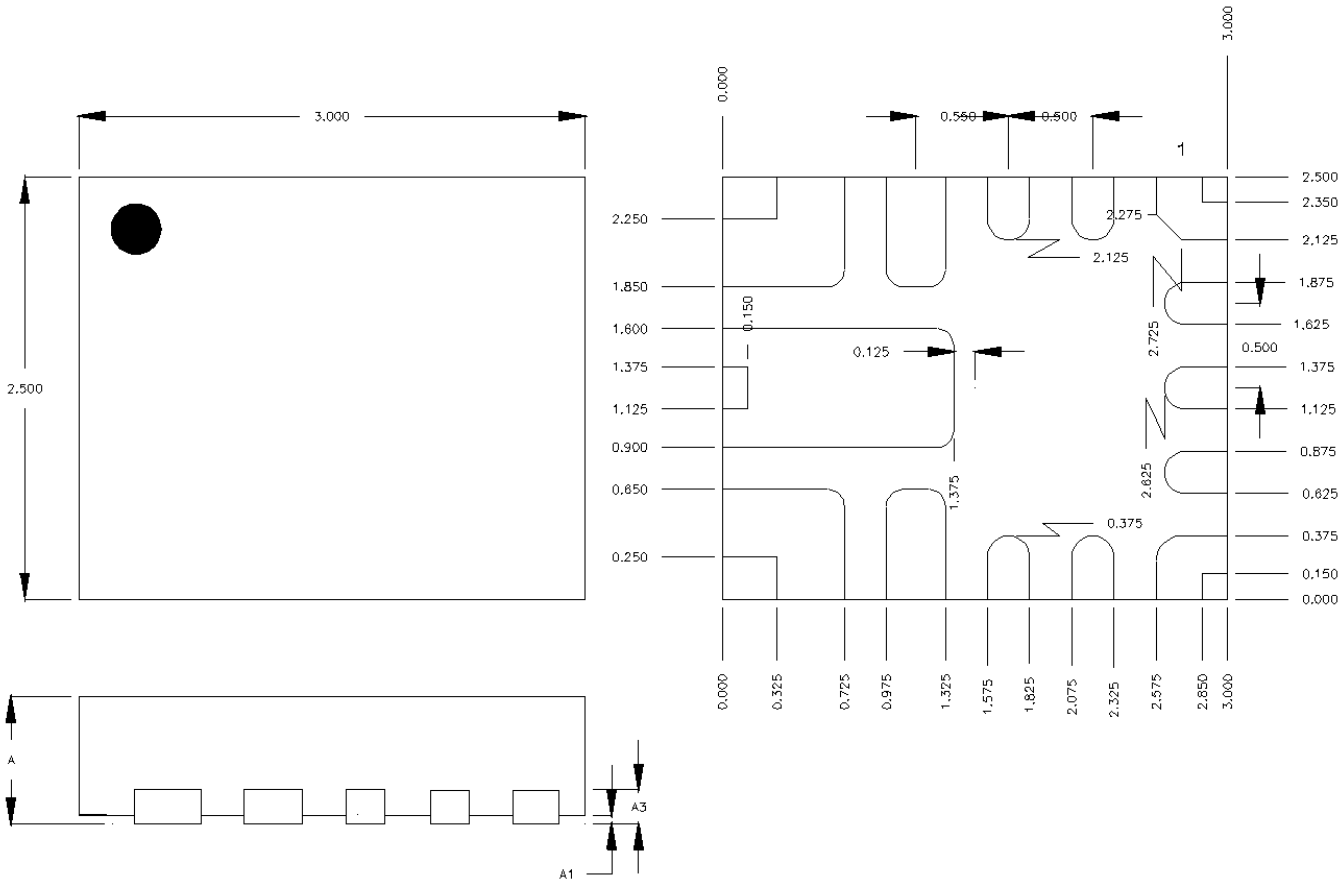


Figure 11. Layout Guide (Top Layer)

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

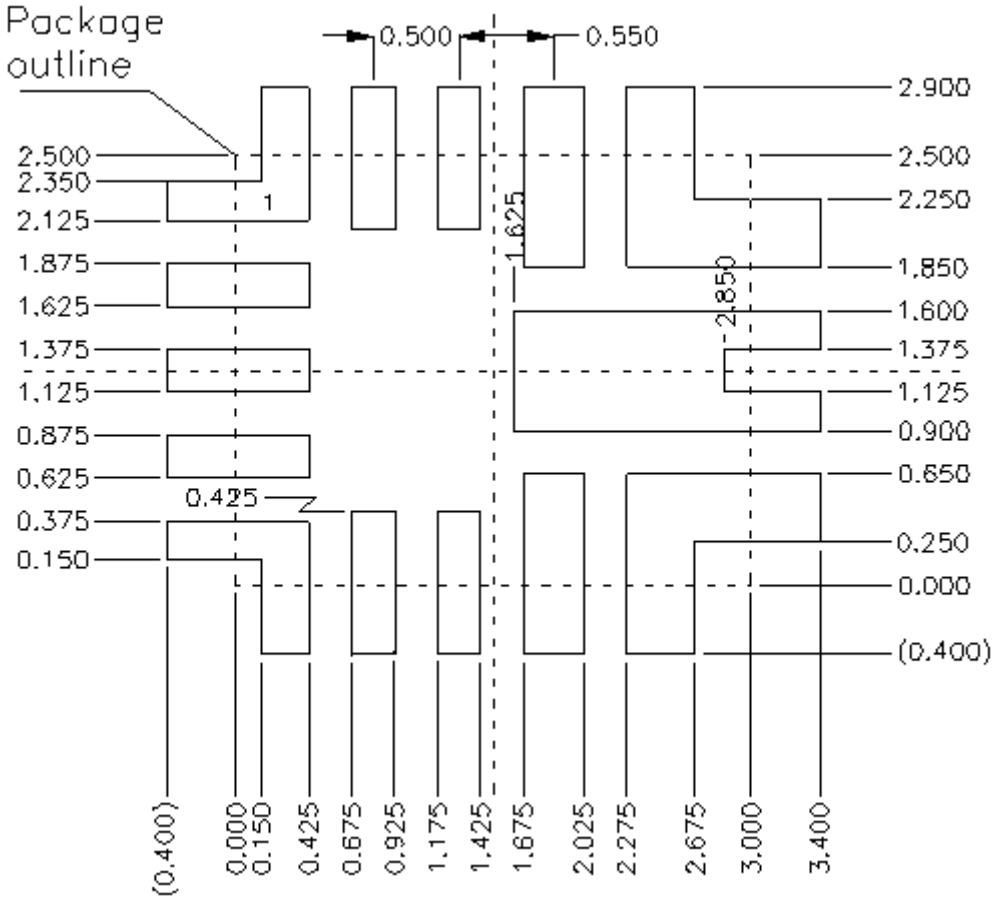


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

W-Type 14L QFN 3x2.5 Package (FC)

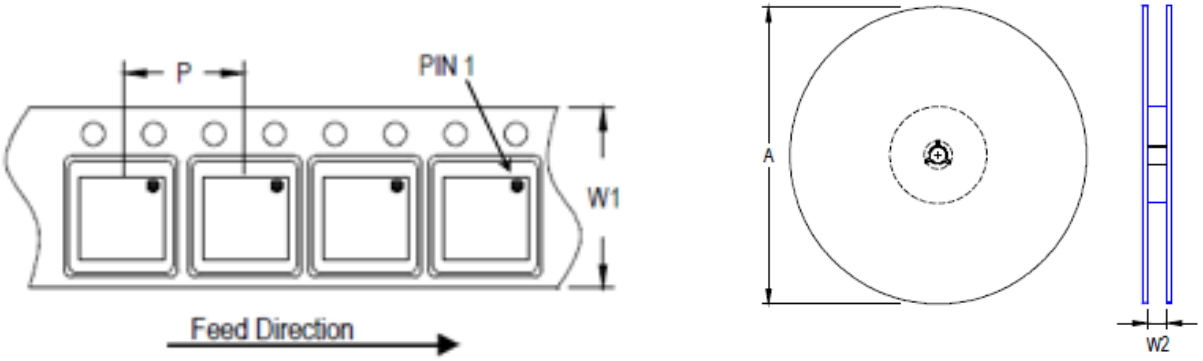
20 Footprint Information



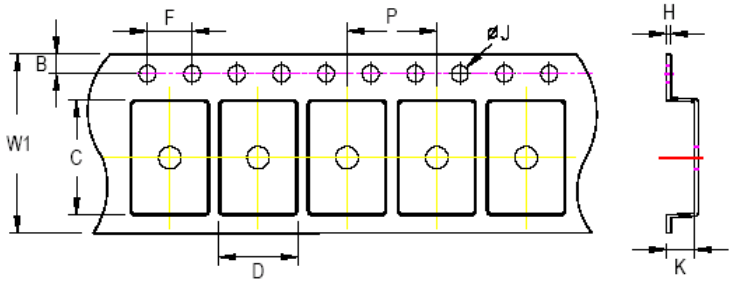
Package	Number of Pins	Tolerance
V/W/U/XQFN3x2.5-14(FC)	14	±0.05 mm

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x2.5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x2.5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

22 Datasheet Revision History

Version	Date	Description	Item
00	2024/9/19	Final	

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Switching Voltage Regulators ***category:***

Click to view products by Richtek ***manufacturer:***

Other Similar products are found below :

LV5695P-E FAN53610AUC33X NCP81108MNTXG NCP81109BMNTXG NCV891234MW50R2G AST1S31PUR NCP81203PMNTXG NCP81208MNTXG NCP81109GMNTXG NCP3235MNTXG NCP81109JMNTXG MP2161AGJ-Z NCP81241MNTXG RT8290ZSP S-8550AA-M5T1G NTE7223 NTE7222 NTE7224 L6986FTR MPQ4481GU-AEC1-P MPQ2171GJ-P MPQ2171GJ-AEC1-P NJW4153U2-A-TE2 MP28160GC-Z MPM3509GQVE-AEC1-P XDPE132G5CG000XUMA1 LT8653SEV#PBF MP5461GC-P MPQ4409GQBE-AEC1-P XC9141A50CMR-G XCL206F083CR-G FAN251015MNTXG SY7066QMC TPS53312RGTR SY5020AFVP SDH8654B IR3899AMTRPBF IR3889MTRPBF ME8123AD8G FM869C TC3776BA. FM869B LM61435AASQRJRRQ1 SQ33065WAQ JW15158DHSOPC#TR TPS62870Y1QWRXSRQ1 JW15158BHSOPC#TR SG3526DTR(XBLW) SG3526N(XBLW) UC2842BN(LX)