RICHTEK® **RT6585C**

Dual-Channel Synchronous DC-DC Step-Down Controller with 5V/3.3V LDOs

1 General Description

The RT6585C is a dual-channel step-down, controller generating supply voltages for battery-powered systems. It includes two Pulse-Width Modulation (PWM) controllers adjustable from 2V to 5.5V, and two fixed 5V/3.3V linear regulators. Each linear regulator provides up to 100mA output current and 3.3V linear regulator provides 1% accuracy under 35mA. The RT6585C provides a mode selection pin, SKIPSEL, to select Diode-Emulation Mode (DEM) or Audio Skipping Mode (ASM). Other features include on-board power-up sequencing, a power-good output, internal soft-start, and soft-discharge output that prevents negative voltage during shutdown.

A constant current ripple PWM control scheme operates without sense resistors and provides 100ns response to load transient. For maximizing power efficiency, the RT6585C automatically switches to the diode-emulation mode in light load applications. The RT6585C is available in the WQFN-20L 3x3 package. The recommended junction temperature range is –40°C to 125°C.

2 Ordering Information

RT6585C □□

- Package Type[(1)]
  QW: WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant[(2)]

Note 1.

- Marked with [(1)] indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with [(2)] indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Support Connected Standby Mode for Ultrabook**
- **CCRCOT Control with 100ns Load Step Response**
- **PWM Maximum Duty Ratio > 98%**
- **5V to 25V Input Voltage Range**
- **Dual Adjustable Output:**
  - **CH1: 2V to 5.5V**
  - **CH2: 2V to 4V**
- **5V/3.3V LDOs with 100mA Output Current**
- **1% Accuracy on 3.3V LDO Output**
- **Internal Frequency Setting**
  - **500kHz/600kHz (CH1/CH2)**
- **Internal Soft-Start and Soft-Discharge**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Independent Switcher Enable Control**
- **Built in OVP/UVP/OCP/OTP**
- **Non-latch UVLO**
- **Power-Good Indicator**
- **20-Lead WQFN Package**

4 Applications

- Notebook and Sub-Notebook Computers
- System Power Supplies
- 3-Cell and 4-Cell Li+ Battery-Powered Device

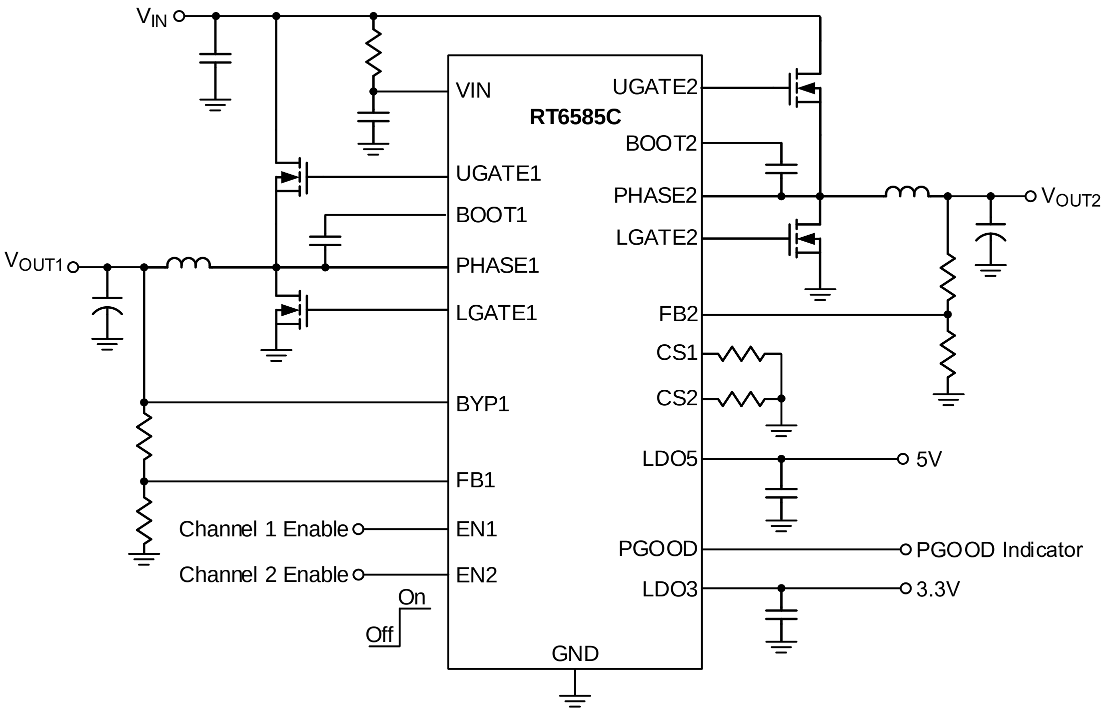
5 Marking Information

RE=YM
DNN

RE= : Product Code

YMDNN : Date Code

6 Simplified Application Circuit



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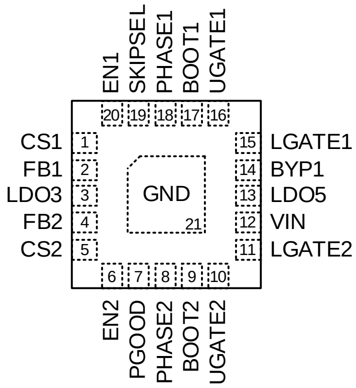
7 Pin Configuration

(TOP VIEW)



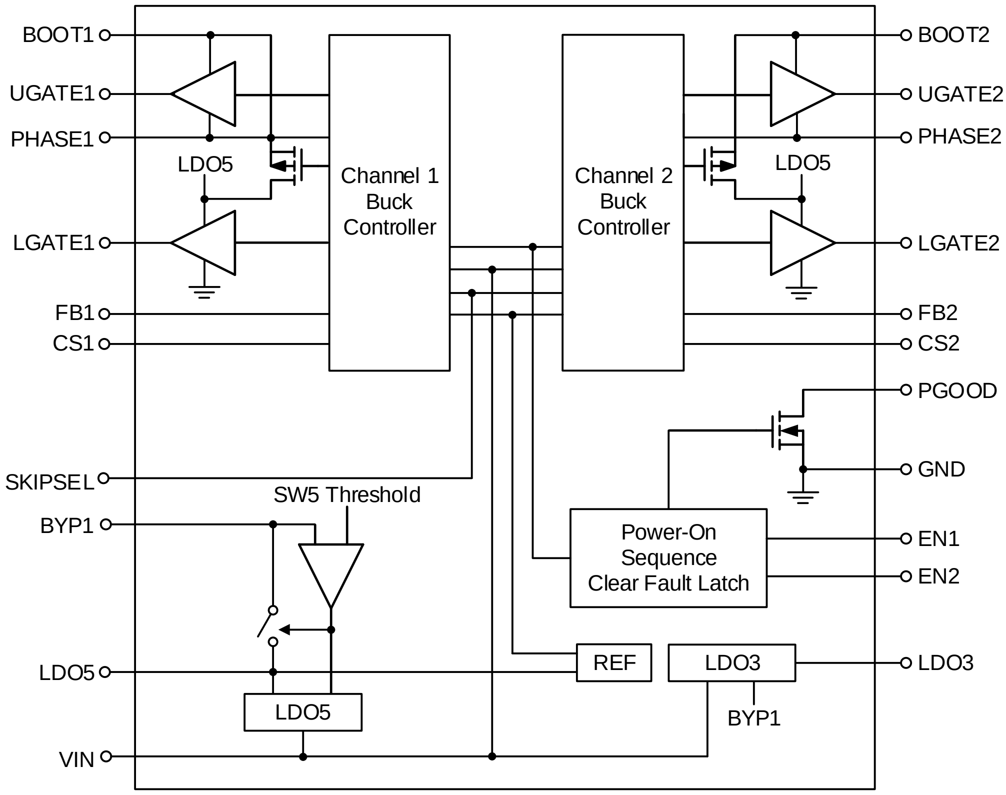
WQFN-20L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CS1	Current limit setting. Connect a resistor to GND to set the threshold for channel 1 synchronous $R_{DS(ON)}$ sense. The GND - PHASE1 current-limit threshold is 1/8th the voltage seen at CS1 over a 0.2V to 2V range. There is an internal 50μA current source from LDO5 to CS1.
2	FB1	Feedback voltage input for channel 1. Connect FB1 to a resistive voltage divider from VOUT1 to GND to adjust output from 2V to 5.5V.
3	LDO3	3.3V linear regulator output. It is always on when VIN is higher than VINPOR threshold.
4	FB2	Feedback voltage input for channel 2. Connect FB2 to a resistive voltage divider from VOUT2 to GND to adjust output from 2V to 4V.
5	CS2	Current limit setting. Connect a resistor to GND to set the threshold for channel 2 synchronous $R_{DS(ON)}$ sense. The GND - PHASE2 current-limit threshold is 1/8th the voltage seen at CS2 over a 0.2V to 2V range. There is an internal 50μA current source from LDO5 to CS2.
6	EN2	Enable control input for channel 2.
7	PGOOD	Power-Good indicator output for channel 1 and channel 2. (Logical AND)
8	PHASE2	Switch node of channel 2 MOSFETs. PHASE2 is the internal lower supply rail for the UGATE2 high-side gate driver. PHASE2 is also the current-sense input for the channel 2.
9	BOOT2	Bootstrap supply for channel 2 high-side gate driver. Connect to an external capacitor according to the typical application circuits.
10	UGATE2	High-side gate driver output for channel 2. UGATE2 swings between PHASE2 and BOOT2.
11	LGATE2	Low-side gate driver output for channel 2. LGATE2 swings between GND and LDO5.
12	VIN	Power input for 5V and 3.3V LDO regulators and buck controllers.
13	LDO5	5V linear regulator output. LDO5 is also the supply voltage for the low-side MOSFET and analog supply voltage for the device.
14	BYP1	Switch-over source voltage input for LDO5.
15	LGATE1	Low-side gate driver output for channel 1. LGATE1 swings between GND and LDO5.

Pin No.	Pin Name	Pin Function
16	UGATE1	High-side gate driver output for channel 1. UGATE1 swings between PHASE1 and BOOT1.
17	BOOT1	Bootstrap supply for channel 1 high-side gate driver. Connect to an external capacitor according to the typical application circuits.
18	PHASE1	Switch node of channel 1 MOSFETs. PHASE1 is the internal lower supply rail for the UGATE1 high-side gate driver. PHASE1 is also the current sense input for the Channel 1.
19	SKIPSEL	PWM operating mode selection. Diode-emulation mode: connect to LDO5 Audio skipping mode: short to GND
20	EN1	Enable control input for channel 1.
21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN to GND ---------- –0.3V to 30V
- BOOTx to GND
  DC ---------- –0.3V to 36V
  <100ns ---------- –5V to 42V
- BOOTx to PHASEx
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- PHASEx to GND
  DC ---------- –5V to 30V
  <100ns ---------- –10V to 42V
- UGATEx to GND
  DC ---------- –5V to 36V
  <100ns ---------- –10V to 42V
- UGATEx to PHASEx
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- LGATEx to GND
  DC ---------- –0.3V to 6V
  <100ns ---------- –5V to 7.5V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 3)
  WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VIN ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

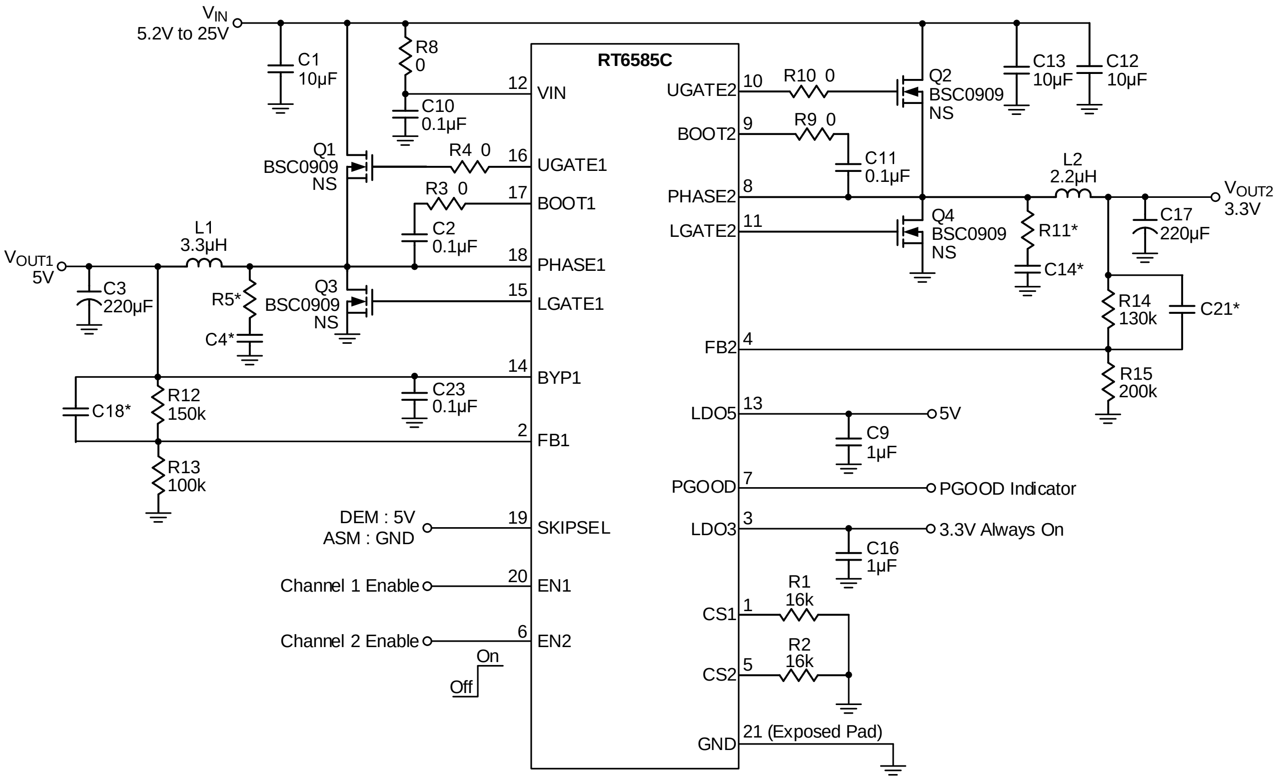
(V_{IN} = 12V, V_{EN1} = V_{EN2} = 3.3V, V_{CS1} = V_{CS2} = 2V, No Load, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Power On Reset	V_{IN_POR}	Rising threshold	--	4.6	4.9	V
		Falling threshold	3.2	3.7	--	
VIN Standby Supply Current	I_{VIN_SBY}	Both buck controllers off, V_{EN1} = V_{EN2} = GND	--	35	55	μA
VIN Quiescent Current	I_{VIN_nosw}	Both buck controllers on, V_{FBx} = 2.05V, V_{BYP1} = 5.05V	--	15	25	μA
BYP1 Supply Current	I_{BYP1_nosw}	Both buck controllers on, V_{FBx} = 2.05V, V_{BYP1} = 5.05V	--	120	180	μA
VIN Power On Reset	V_{IN_POR}	Rising threshold	--	4.6	4.9	V
Soft-Start						
Soft-Start Time	t_{SSx}	V_{OUT} ramp-up time	--	0.9	--	ms
Buck Controllers Output and FB Voltage						
FBx Valley Trip Voltage	V_{FBx}	CCM operation	1.98	2	2.02	V
BYP1 Discharge Current	I_{DCHG_BYP1}	V_{BYP1} = 0.5V	10	45	--	mA
PHASEx Discharge Current	I_{DCHG_LX}	V_{PHASEx} = 0.5V	5	8	--	mA
Switching Frequency						
Switching Frequency	f_{SWx}	V_{IN} = 20V, V_{OUT1} = 5V	400	500	600	kHz
	I_{LED_MAX}	V_{IN} = 20V, V_{OUT2} = 3.33V	480	600	720	
Minimum Off-Time	$t_{OFF(MIN)}$	V_{FBx} = 1.9V	--	200	275	ns
Current Sense						
CSx Source Current	I_{CSx}	V_{CSx} = 1V	47	50	53	μA
CSx Current Temperature Coefficient	TCI_{CSx}	In comparison with 25°C	--	4700	--	ppm/°C
Zero-Current Threshold 1	V_{ZC1_TH}	V_{FBx} = 2.05V, PHASE1 - GND	–8	–1	2	mV
Zero-Current Threshold 2	V_{ZC2_TH}	V_{FBx} = 2.05V, PHASE2 - GND	–8	–1	3.5	mV
Internal Regulator						
LDO5 Output Voltage	V_{LDO5}	V_{IN} = 12V, no load	4.9	5	5.1	V
		V_{IN} > 7V, I_{LDO5} < 100mA	4.8	5	5.1	
		V_{IN} > 5.5V, I_{LDO5} < 35mA	4.8	5	5.1	
		V_{IN} > 5V, I_{LDO5} < 20mA	4.5	4.75	5.1	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO3 Output Voltage	V_{LDO3}	V_{IN} = 12V, no load	3.267	3.3	3.333	V
		V_{IN} > 7V, I_{LDO3} < 100mA	3.217	3.3	3.383	
		V_{IN} > 5.5V, I_{LDO3} < 35mA	3.267	3.3	3.333	
		V_{IN} > 5V, I_{LDO3} < 20mA	3.217	3.3	3.383	
LDO5 Output Current	I_{LDO5}	V_{LDO5} = 4.5V, V_{BYP1} = GND, V_{IN} = 7.4V	100	175	--	mA
LDO3 Output Current	I_{LDO3}	V_{LDO3} = 3V, V_{IN} = 7.4V	100	175	--	mA
LDO5 Switch-over Threshold to BYP1	V_{SWTH}	Rising edge at BYP1 regulation point	--	4.66	--	V
LDO5 Switch-over Equivalent Resistance	R_{SW}	LDO5 to BYP1, 10mA	--	1.5	3	Ω
SKIP Mode Selection						
SKIPSEL Input Voltage	$V_{SKIPSEL}$	ASM operation	--	--	0.8	V
		DEM operation	1.2	--	--	
UVLO						
LDO5 UVLO Threshold	V_{UVLO5}	Rising edge	--	4.3	4.6	V
		Falling edge	3.7	3.9	4.1	
LDO3 UVLO Threshold	V_{UVLO3}	Channel x off	--	2.5	--	V
Power-Good						
PGOOD Threshold	V_{PGxTH}	PGOOD detect, V_{FBx} rising edge	84	88	92	%
		Hysteresis	--	8	--	
PGOOD Leakage Current		High state, V_{PGOOD} = 5.5V	--	--	1	μA
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Fault Detection						
OVP Trip Threshold	V_{OVP}	FBx with respect to internal reference	109	113	117	%
OVP Propagation Delay			--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP detect, FBx falling edge	47	52	57	%
UVP Shutdown Blanking Time	t_{SHDN_UVP}	From ENx enable	--	1.3	--	ms
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Logic Inputs						
ENx Threshold Voltage	V_{ENx_H}	SMPS on	1.6	--	--	V
	V_{ENx_L}	SMPS off	--	--	0.4	

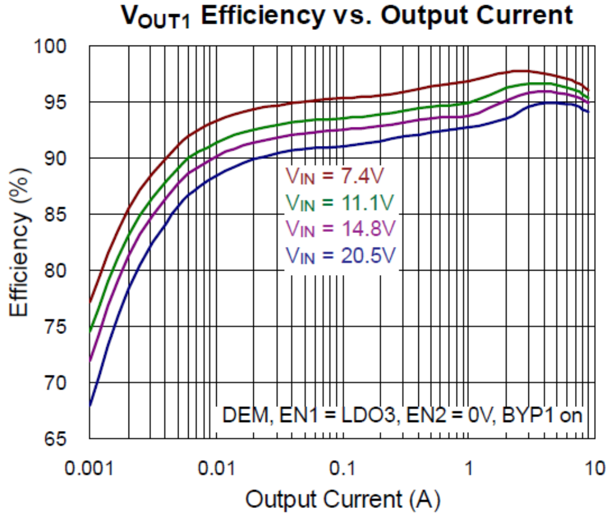
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Boost Switch						
Internal Boost Switch On-Resistance	R_{BST}	LDO5 to BOOTx	--	80	--	Ω
Power MOSFET Drivers						
Internal Boost Switch On-Resistance	RBST	LDO5 to BOOTx	--	80	--	Ω
UGATEx On-Resistance	RUG	High state, $V_{BOOTx} - V_{UGATEx}$ = 0.25V, $V_{BOOTx} - V_{PHASEx}$ = 5V	--	3	--	Ω
		Low state, $V_{UGATEx} - V_{PAHSEx}$ = 0.25V, $V_{BOOTx} - V_{PHASEx}$ = 5V	--	2	--	
LGATEx On-Resistance	RLG	High state, $V_{LDO5} - V_{LGATEx}$ = 0.25V, V_{LDO5} = 5V	--	3	--	Ω
		Low state, V_{LGATEx} – GND = 0.25V	--	1	--	
Dead-Time	td	LGATEx rising	--	20	--	ns
		UGATEx rising	--	30	--	

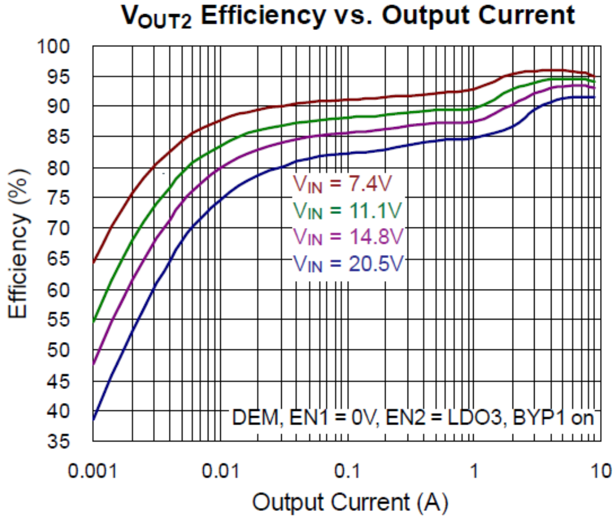
13 Typical Application Circuit

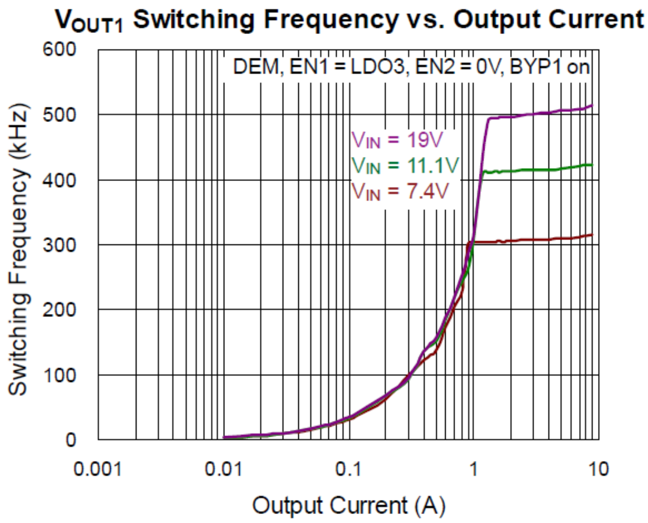


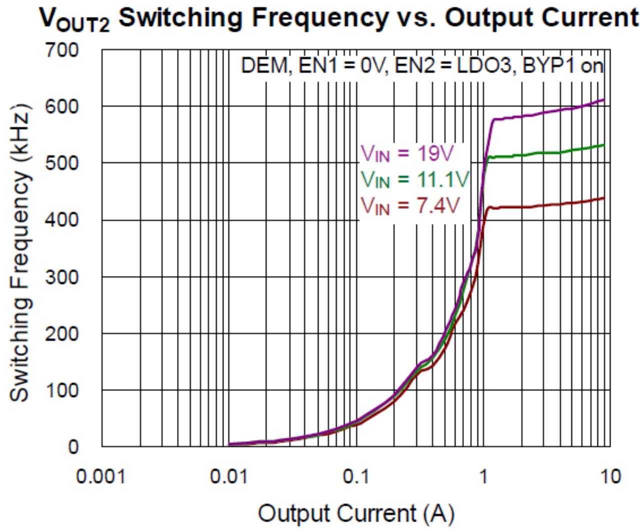
* : Optional

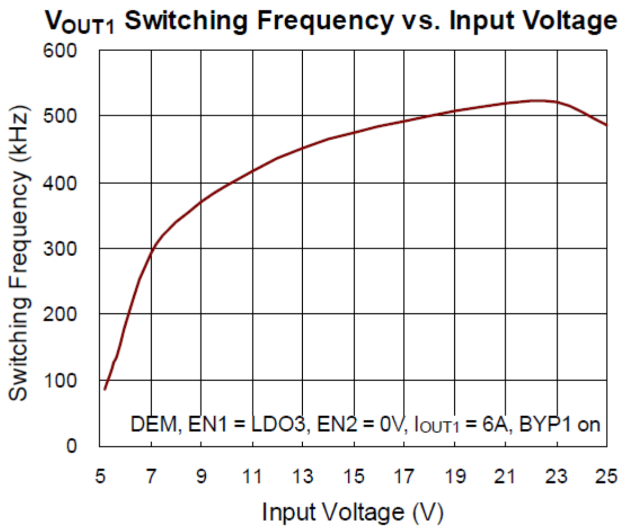
14 Typical Operating Characteristics

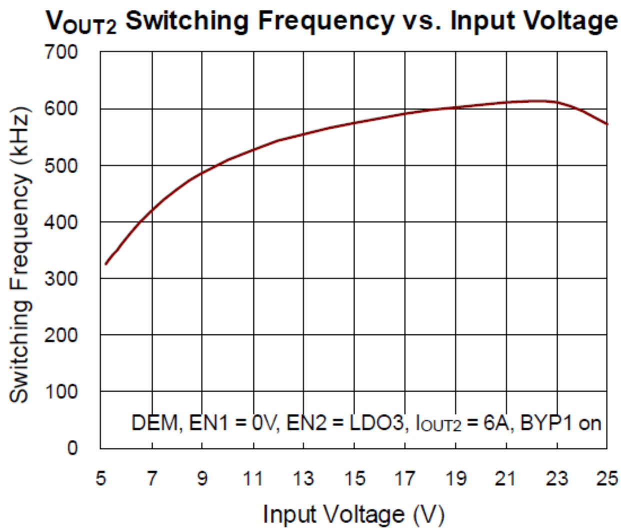




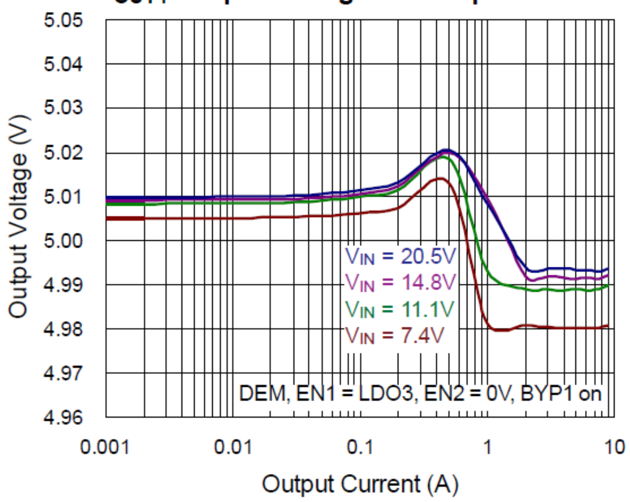




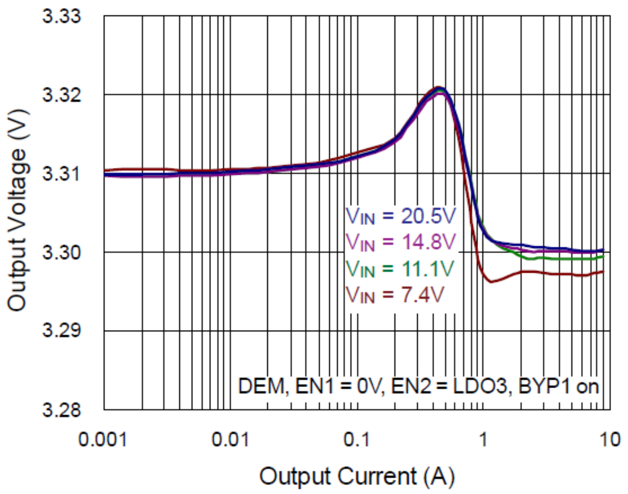




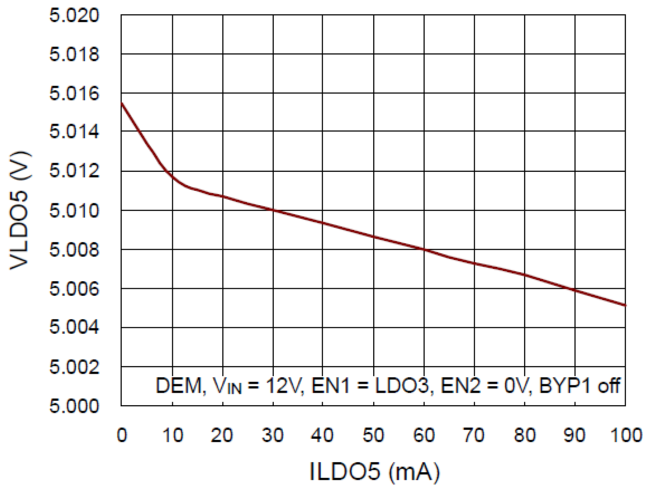
V_{OUT1} Output Voltage vs. Output Current



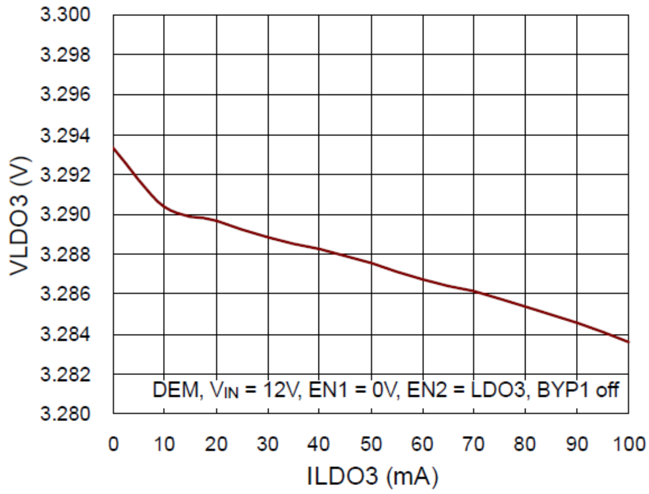
V_{OUT2} Output Voltage vs. Output Current



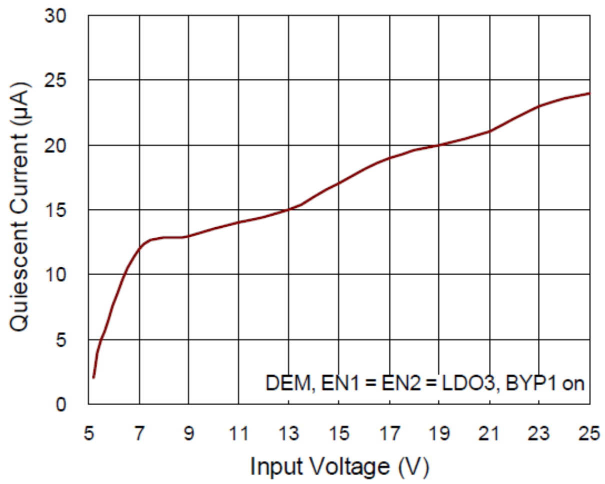
VLDO5 vs. ILDO5



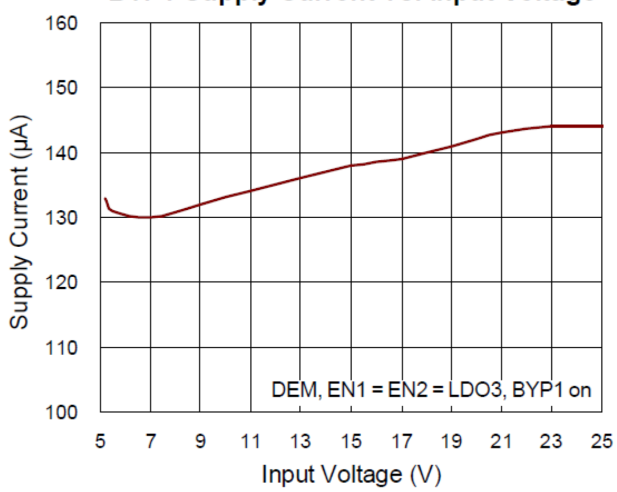
VLDO3 vs. ILDO3



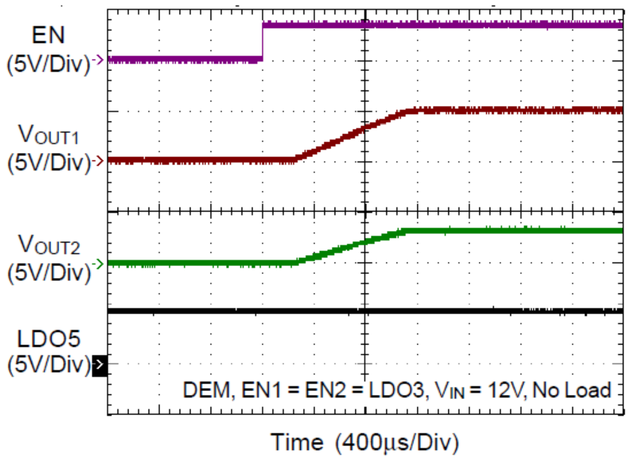
Quiescent Current vs. Input Voltage



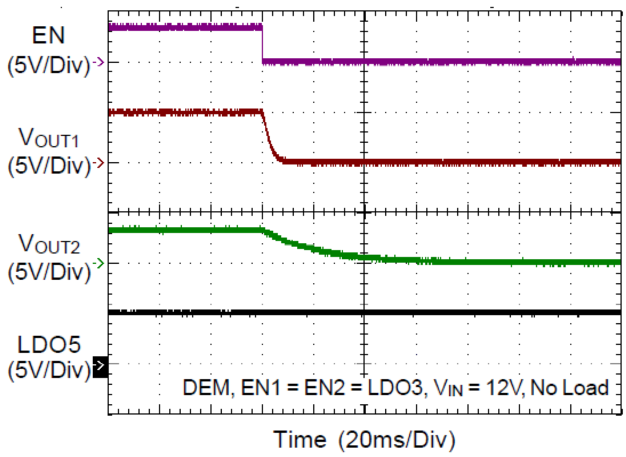
BYP1 Supply Current vs. Input Voltage



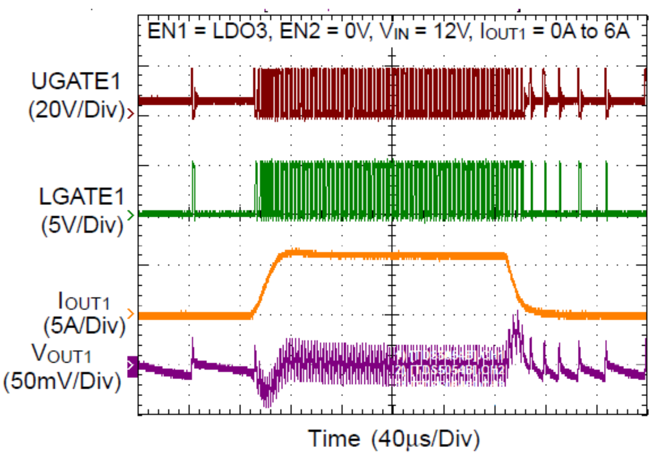
Power On from EN



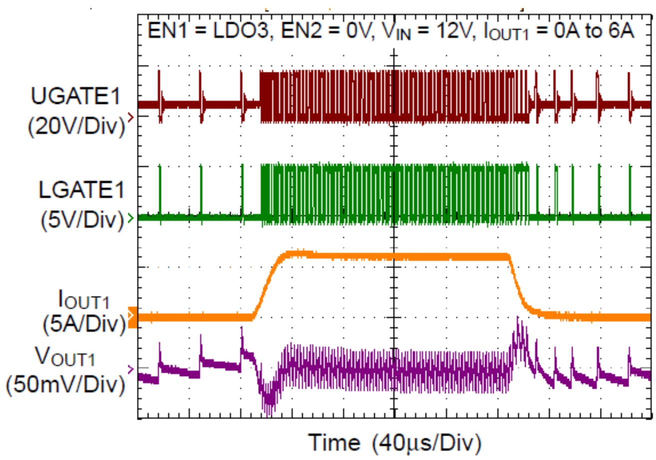
Power Off from EN



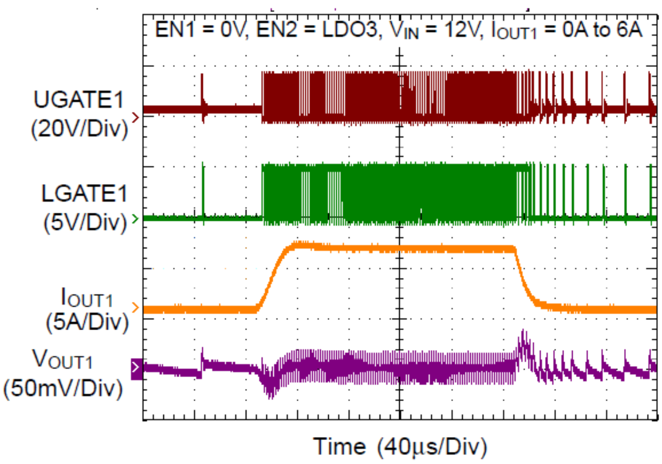
V_{OUT1} Load Transient Response at DEM



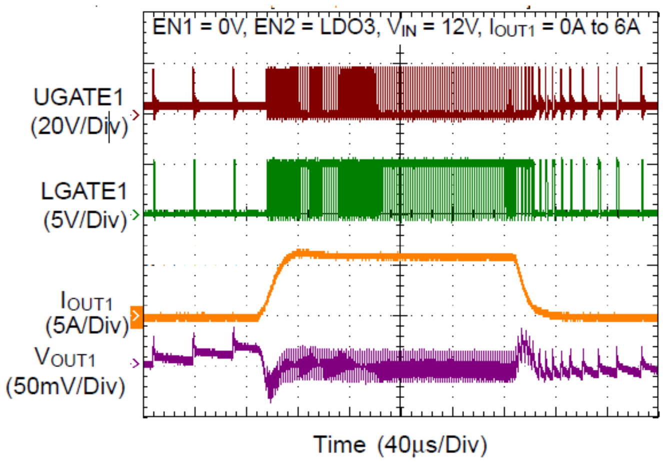
V_{OUT1} Load Transient Response at ASM

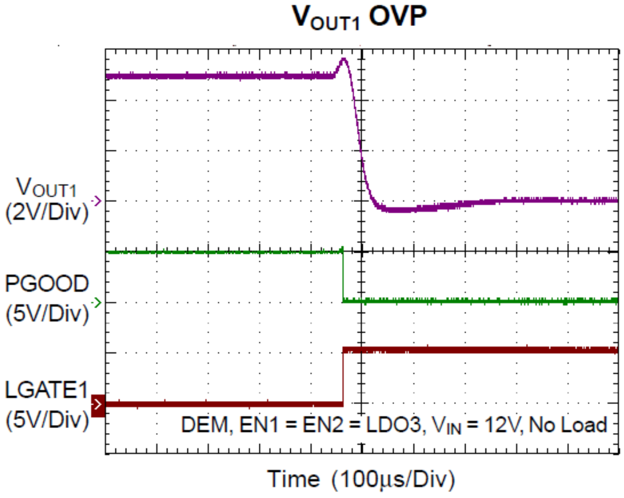


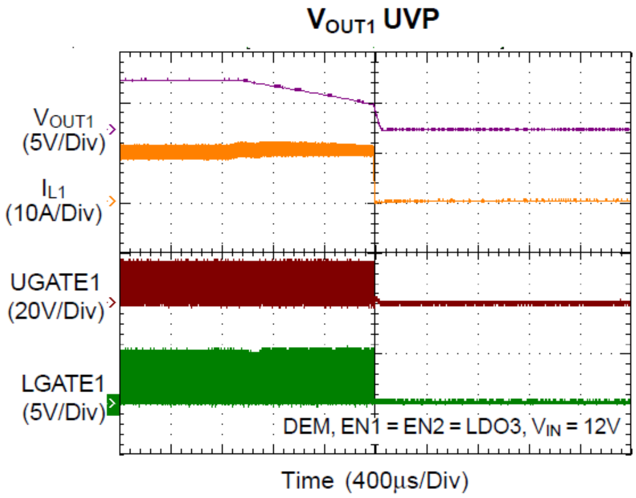
V_{OUT2} Load Transient Response at DEM



V_{OUT2} Load Transient Response at ASM




VOUT1 OVP
VOUT1 (2V/Div)
PGOOD (5V/Div)
LGATE1 (5V/Div)
DEM, EN1 = EN2 = LDO3, VIN = 12V, No Load
Time (100μs/Div)


VOUT1 UVP
VOUT1 (5V/Div)
IL1 (10A/Div)
UGATE1 (20V/Div)
LGATE1 (5V/Div)
DEM, EN1 = EN2 = LDO3, VIN = 12V
Time (400μs/Div)

15 Operation

The RT6585C includes two constant on-time synchronous step-down controllers and two linear regulators.

15.1 Buck Controller

In normal operation, the high-side N-MOSFET is turned on when the output is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

15.2 Soft-Start

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

15.3 PGOOD

The Power-Good output is an open-drain architecture. When the two channels soft-start are both finished, the PGOOD open-drain output will be high impedance.

15.4 Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

15.5 Overvoltage Protection (OVP) & Undervoltage Protection (UVP)

The two channel output voltages are continuously monitored for overvoltage and undervoltage conditions. When the output voltage exceeds overvoltage threshold (113% of VOUT), UGATE goes low and LGATE is forced high. When it is less than 52% of reference voltage, undervoltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until ENx is reset or LDO5 is re-supplied.

15.6 LDO5 and LDO3

When the VIN voltage exceeds the POR rising threshold, LDO3 and LDO5 will default turn-on. The linear regulator LDO5 and LDO3 provide 5V and 3.3V regulated output.

15.7 Switching Over

The BYP1 is connected to the Channel 1 output. After the Channel 1 output voltage exceeds the set threshold (4.66V), the output will be bypassed to the LDO5 output to maximize the efficiency.

16 Application Information

(Note 6)

The RT6585C is a dual-channel, low quiescent, Mach Response^{TM} DRVTM mode synchronous Buck controller targeted for Ultrabook system power supply solutions. Richtek's Mach ResponseTM technology provides fast response to load steps. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs, and avoids the problems caused by widely varying switching frequencies in CCR (constant current ripple) constant on-time and constant off-time PWM schemes. A special adaptive on-time control trades off the performance and efficiency over wide input voltage range. The RT6585C includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The LDO5 linear regulator steps down the battery voltage to supply both internal circuitry and gate drivers. The synchronous switch gate drivers are directly powered by LDO5. When VOUT1 rises above 4.66V, an automatic circuit disconnects the linear regulator and allows the device to be powered by VOUT1 via the BYP1 pin.

16.1 PWM Operation

The Mach Response^{TM} DRVTM mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so that the output ripple voltage provides the PWM ramp signal. Referring to the RT6585C's Function Block Diagram, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this oneshot is determined by the converter's input output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (200ns typ.). The on-time one-shot will be triggered if the error comparator is high, the low-side switch current is below the **current-limit threshold**, and the minimum offtime one-shot has timed out.

16.2 PWM Frequency and On-time Control

For each specific input voltage range, the Mach Response^{TM} control architecture runs with pseudo constant frequency by feed forwarding the input and output voltage into the on-time one-shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by VIN and proportional to the output voltage. The inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The frequency of 3V output controller is set higher than the frequency of 5V output controller. This is done to prevent audio frequency “beating” between the two sides, which switch asynchronously for each side.

The RT6585C adaptively changes the operation frequency according to the input voltage. Higher input voltage usually comes from an external adapter, so the RT6585C operates with higher frequency to have better performance. Lower input voltage usually comes from a battery, so the RT6585C operates with lower switching frequency for lower switching losses. For a specific input voltage range, the switching cycle period is given by:

For 5V VOUT,

$$\text{Period } (\mu\text{sec.}) = \frac{V_{IN} \times 1.62}{V_{IN} - 3.79}$$

For 3V VOUT,

$$\text{Period (μsec.)} = \frac{V_{IN} \times 1.45}{V_{IN} - 2.59}$$

where the VIN is in volt.

The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high-side power MOSFET.

16.3 Operation Mode Selection

The RT6585C supports two operation modes: diode emulation mode (DEM) and ultrasonic mode (ASM). The operation mode can be set via the SKIPSEL pin. When the SKIPSEL pin voltage is higher than 1.2V, the RT6585C operates in DEM. When the SKIPSEL pin Voltage is lower than 0.8V, the RT6585C operates in ASM.

16.4 Diode Emulation Mode

In diode emulation mode, the RT6585C automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next “ON” cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 1. and can be calculated as follows:

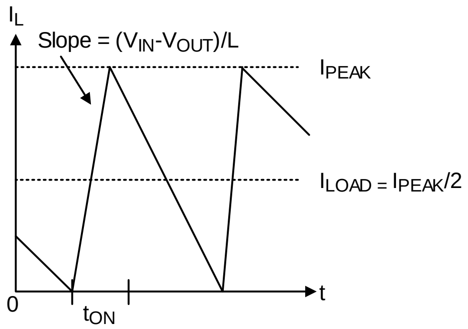


Figure 1. Boundary Condition of CCM/DEM

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade offs in PFM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

16.5 Ultrasonic Mode (ASM)

The RT6585C activates a unique type of diode emulation mode with a minimum switching frequency of 25kHz, called ultrasonic mode. This mode eliminates audio- frequency modulation that will otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate driver signal is “OR”ed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the controller will turn on UGATE and give it shorter on-time.

When the on-time expired, LGATE turns on until the inductor current goes to zero crossing threshold and keep both high-side and low-side MOSFET off to wait for the next trigger. Because shorter on-time causes a smaller pulse of the inductor current, the controller can keep output voltage and switching frequency simultaneously.

The on-time decreasing has a limitation and the output voltage will be lifted up under the slight load condition. The controller will turn on LGATE first to pull down the output voltage. When the output voltage is pulled down to the balance point of the output load current, the controller will proceed the short on-time sequence as the above description.

16.6 Linear Regulators (LDOx)

The RT6585C includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The regulators can supply up to 100mA for external loads. Bypass LDOx with 1μF(min) to 4.7μF (max), and the recommended value is 1μF. ceramic capacitor. When V_{OUT1} is higher than the switch over threshold (4.66V), an internal 1.5Ω P-MOSFET switch connects BYP1 to the LDO5 pin while simultaneously disconnects the internal linear regulator.

16.7 Current Limit Setting

The RT6585C has cycle-by-cycle current limit control and the OCP function only operation at CCM, it is disabled at DEM in order to reduce quiescent current. The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

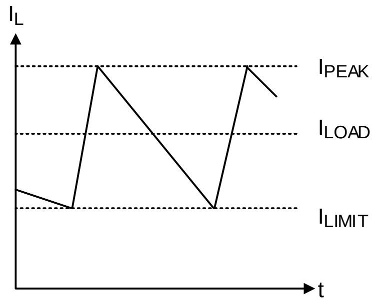


Figure 2. “Valley” Current Limit

The RT6585C uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIM} resistor between the CSx pin and GND sets the current-limit threshold. The resistor R_{ILIM} is connected to a current source from CSx which is 50μA (typ.) at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low-side MOSFET equals 1/8 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high-side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/8 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor according to the following equation:

$V_{LIMIT} = (R_{LIMIT} \times 50\mu A - 35mV)/8 = I_{LIMIT} \times R_S$

$R_{LIMIT} = ((I_{LIMIT} \times R_{DS(ON)}) \times 8 + 35mV)/50\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASEx and GND. Mount or place the IC close to the low-side MOSFET.

16.8 MOSFET Gate Driver (UGATEx, LGATEx)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOTx and PHASEx pins. A dead-time to prevent shoot through is internally generated from high-side MOSFET off to low-side MOSFET on and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATEx low is robust, with a 1Ω typical on- resistance. A 5V bias voltage is delivered from the LDO5 supply. The instantaneous drive current is supplied by an input capacitor connected between LDO5 and GND.

For high current applications, some combinations of high and low-side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing, and shoot through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time. See Figure 3.

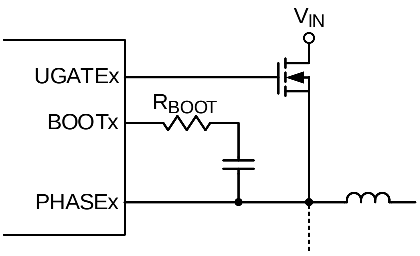


Figure 3. Increasing the UGATEx Rise Time

16.9 Soft-Start

The RT6585C provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft- start, it clamps the ramping of internal reference voltage which is compared with FBx signal. The typical soft-start duration is 0.9ms. An unique PWM duty limit control that prevents output overvoltage during soft-start period is designed specifically for FBx floating.

16.10 UVLO Protection

The RT6585C has LDO5 undervoltage lock out protection (UVLO). When the LDO5 voltage is lower than 3.9V (typ.) and the LDO3 voltage is lower than 2.5V (typ.), both switch power supplies are shut off. This is a non-latch protection

16.11 Power-Good Output (PGOOD)

PGOOD is an open-drain output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. For RT6585C, PGOOD is released when both output voltages are above 88% of nominal regulation point. The PGOOD signal goes low if either output turns off or is 20% below or 13% over its nominal regulation point.

16.12 Output Overvoltage Protection (OVP)

The output voltage can be continuously monitored for over- voltage condition. If the output voltage exceeds 13% of its set voltage threshold, the overvoltage protection is triggered and the LGATEx low-side gate drivers are forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and pulls the output voltage downward.

The RT6585C is latched once OVP is triggered and can only be released by either toggling ENx or cycling VIN.

There is a 1μs delay built into the overvoltage protection circuit to prevent false transition.

Note that latching LGATEx high will cause the output voltage to dip slightly negative due to previously stored energy in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the overvoltage condition is caused by a shorted in high-side switch, turning the low-side MOSFET on 100% will create an electrical shorted circuit between the battery and GND to blow the fuse and disconnecting the battery from the output.

16.13 Output Undervoltage Protection (UVP)

The output voltage can be continuously monitored for under- voltage condition. If the output is less than 52% (typ.) of its set voltage threshold, the undervoltage protection will be triggered and then both UGATEx and LGATEx gate drivers will be forced low. The UVP is ignored for at least

1.3ms (typ.) after a start-up or a rising edge on ENx. Toggle ENx or cycle VIN to reset the UVP fault latch and restart the controller.

16.14 Thermal Protection

The RT6585C features thermal shutdown to prevent damage from excessive heat dissipation. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitries are turned off during thermal shutdown. The RT6585C triggers thermal shutdown if LDO5 is not supplied from VOUT1, while input voltage on VIN and drawing current from LDO5 are too high. Nevertheless, even if LDO5 is supplied from VOUT1, overloading LDO5 can cause large power dissipation on automatic switches, which may still result in thermal shutdown.

16.15 Discharge Mode (Soft Discharge)

When ENx is low the output undervoltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

16.16 Standby Mode

When VIN rises POR threshold and ENx < 0.4V, RT6585C operate in standby mode, CH1 and CH2 is OFF state. For RT6585C, LDO5 and LDO3 are ON state and approximately consumes 30μA while in standby mode.

16.17 Power-Up Sequencing and On/Off Controls (ENx)

EN1 and EN2 control the power-up sequencing of the two channels of the Buck converter. The 0.4V falling edge threshold on ENx can be used to detect a specific analog voltage level and to shutdown the device. Once in shutdown, the 1.6V rising edge threshold activates, providing sufficient hysteresis for most applications.

Table 1. Operation Mode Truth Table

Mode	Condition	Comment
LDO Overcurrent Limit	LDOx < UVLO threshold	Transitions to discharge mode after VIN POR. LDO5 and LDO3 remain active.
Run	ENx = high, V_{OUT1} or V_{OUT2} are enabled	Normal Operation.
Overvoltage Protection	Either output >113% of the nominal level.	LGATEx is forced high. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENx.
Undervoltage Protection	Either output < 52% of the nominal level after 1.3ms time-out expires and output is enabled	Both UGATEx and LGATEx are forced low and enter discharge mode. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENx.
Discharge	Either output is still high in standby mode	During discharge mode, there is one path to discharge the output capacitors' residual charge to GND via an internal switch.
Standby	VIN > POR ENx < 0.4V	LDO3, LDO5 are active
Thermal Shutdown	T_J > 150°C	All circuitries are off. Exit by VIN POR.

Table 2. Enabling/PGOOD State

EN1	EN2	LDO5	LDO3	CH1 (5VOUT)	CH2 (3.3VOUT)	PGOOD
OFF	OFF	ON	ON	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	Low
OFF	ON	ON	ON	OFF	ON	Low
ON	ON	ON	ON	ON	ON	High

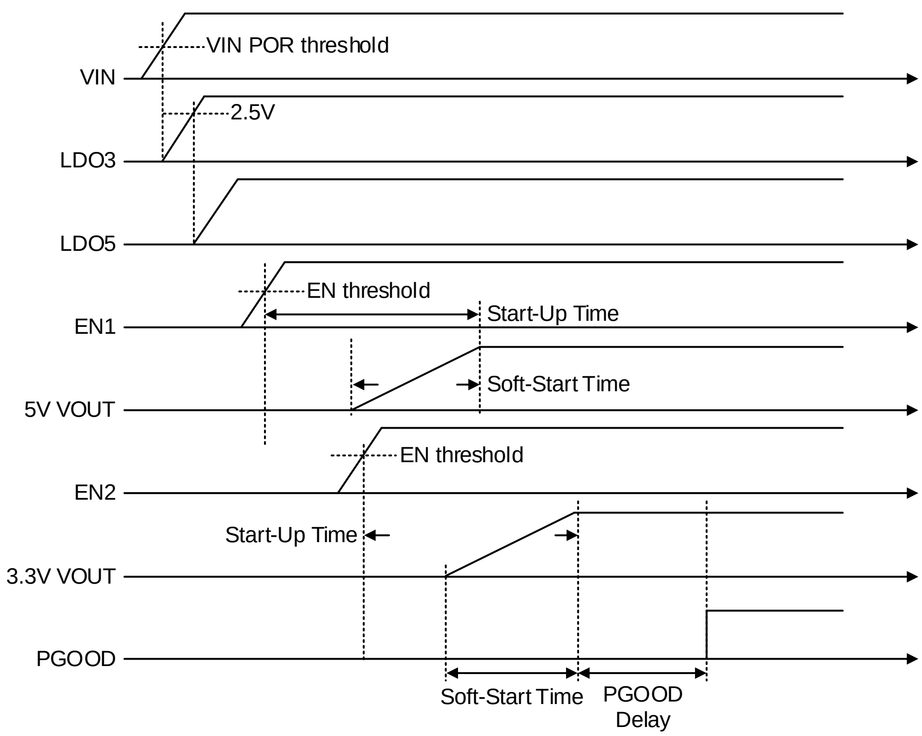


Figure 4. RT6585C Timing

16.18 Output Voltage Setting (FBx)

W Connect a resistive voltage divider at the FBx pin between V_{OUTx} and GND to adjust the output voltage from 2V to 5.5V for CH1 and 2V to 4V for CH2, as shown in Figure 5. The recommended R2 is between 100kΩ to 200kΩ, V_{OUT} (vally) and solve for R1 using the equation below:

$$V_{OUT(Valley)} = V_{FBx} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FBx} is 2V (typ.)

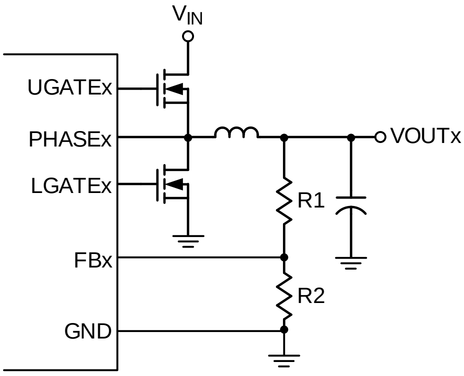


Figure 5. Setting V_{OUTx} with a resistive voltage divider

16.19 Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUTx})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK}:

$$I_{PEAK} = I_{LOAD(MAX)} + [\ (LIR/2) \times I_{LOAD(MAX)}\ ]$$

The calculation above shall serve as a general reference. To further improve transient response, the output inductance can be further reduced. Of course, besides the inductor, the output capacitor should also be considered when improving transient response.

16.20 Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from the equations below:

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUTx}(t_{ON} + t_{OFF(MIN)})\right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f}\right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot and overshoot voltage during load transient, V_{P-P} is the output ripple voltage, and $t_{OFF(MIN)}$ is the minimum off-time.

16.21 Selection Guide of MOSFET $R_{DS(ON)}$ for ZCD Function

Through the ZCD (Zero Current Detection) function, the IC can effectively reduce the switching frequency in DEM (Discontinuous Emission Mode), thereby improving power conversion efficiency. When ZCD is triggered, the IC cuts off the low-side MOSFET, causing both the high-side and low-side MOSFETs to be in an off state. The working principle of ZCD is as follows: when the low-side MOSFET conducts, and the inductor current (IL) passing through the $R_{DS(ON)}$ of the low-side MOSFET generates a voltage drop (VPHASE) that falls below the ZC threshold of the IC's internal comparator, ZCD is triggered. The IC then turns off the low-side MOSFET and enters DEM mode. The related waveforms can be seen in Figure 7.

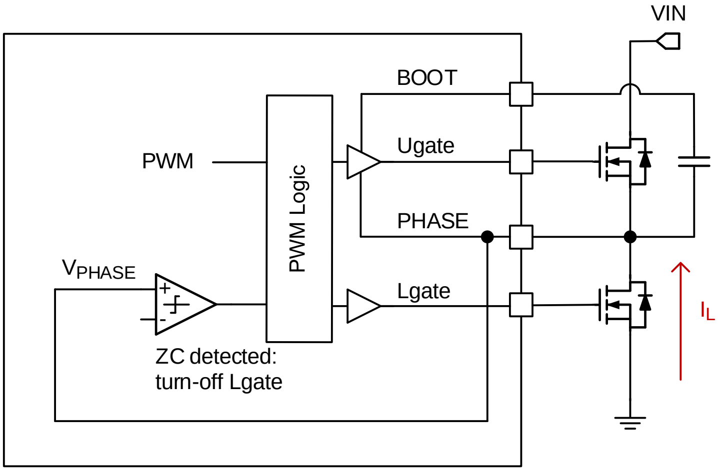


Figure 6. Functional Block Diagram for ZCD

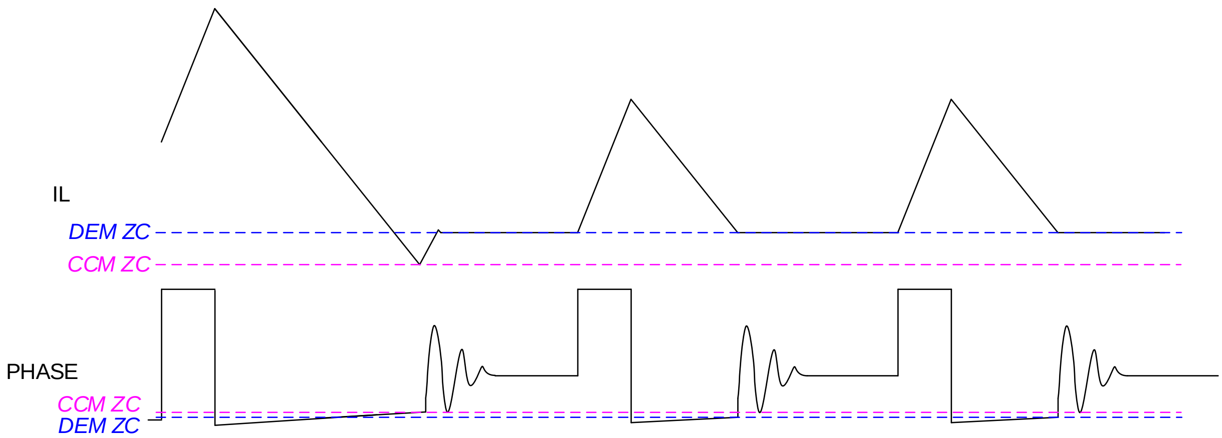


Figure 7. DEM Operation Diagram

To optimize the transition between DEM and CCM and to prevent unstable output voltage due to frequent switching, the ZCD current thresholds for CCM and DEM are designed with hysteresis. In CCM mode, the ZCD threshold is lowered to reduce the likelihood of triggering ZCD. Once in DEM, the ZCD current threshold is raised, making it easier to trigger ZCD in DEM mode. As shown in the Figure 8, when the inductor current is high and the IC is in CCM mode, the ZCD maintains a lower current threshold (CCM_ZC). After the inductor current decreases and triggers ZCD to enter DEM, the IC adjusts the ZCD current threshold upwards to DEM_ZC, which helps the IC to operate stably in DEM state.

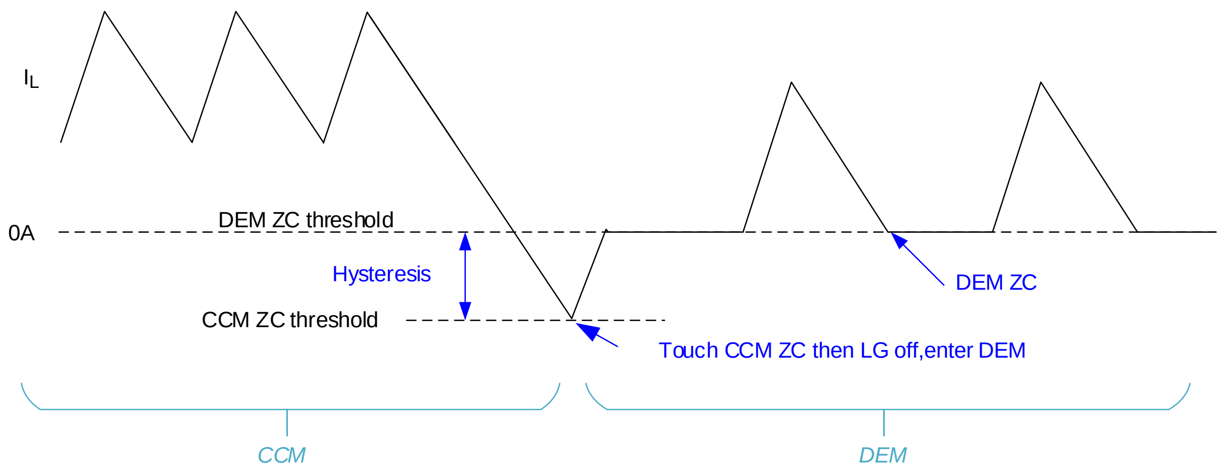


Figure 8. DEM Operation Diagram

The accuracy of ZCD is not only related to the internal design parameters of the IC but also to the external inductor current and the selected MOSFET's $R_{DS(ON)}$. To ensure that the IC operates correctly in DEM mode, the relationship between the external MOSFET and the inductor current must be considered.

$$R_{DS(ON),min} > \frac{\left|V_{ZC\_TH\_MAX}\right|}{\Delta I_L / 2}$$

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$

, where the $V_{ZC\_TH\_MAX}$ is the maximum ZCD threshold value in CCM mode, and it is important to note that this ZCD threshold is the maximum value of (PHASEx-GND) as shown in the electrical specification table. When evaluating the ZCD function, it is necessary to consider the operating conditions of the IC as well as the variance in external component parameters.

16.22 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (30°C /W) = 3.33W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

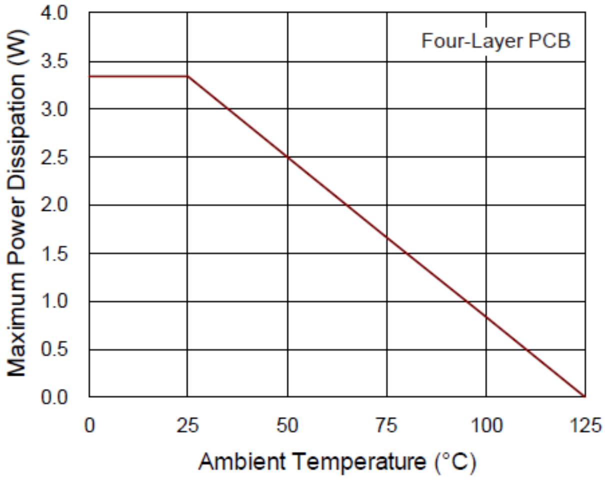


Figure 9. Derating Curve of Maximum Power Dissipation

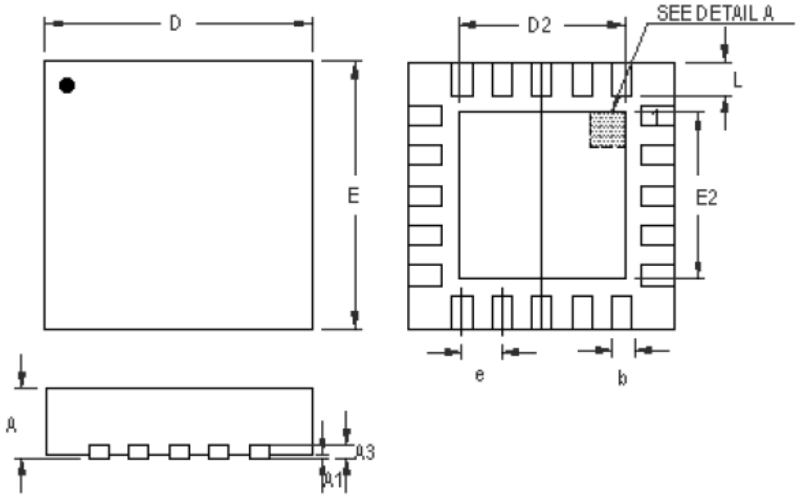
16.23 Layout Considerations

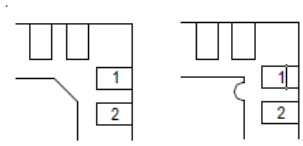
Layout is very important in high frequency switching converter design. Improper PCB layout can radiate excessive noise and contribute to the converter's instability. Certain points must be considered before starting a layout with the RT6585C.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as FBx, PGOOD, and should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place ground terminal of VIN capacitor(s), VOUTx capacitor(s), and Source of low-side MOSFETs as close to each other as possible. The PCB trace of PHASEx node, which connects to Source of high-side MOSFET, Drain of low-side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension





DETAIL A

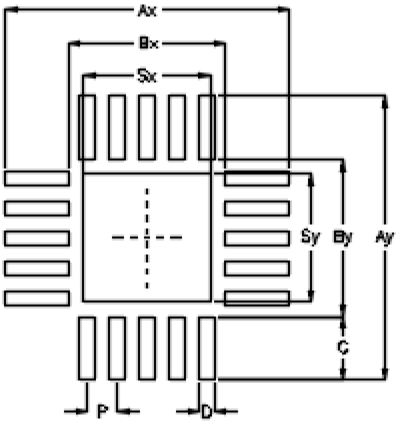
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

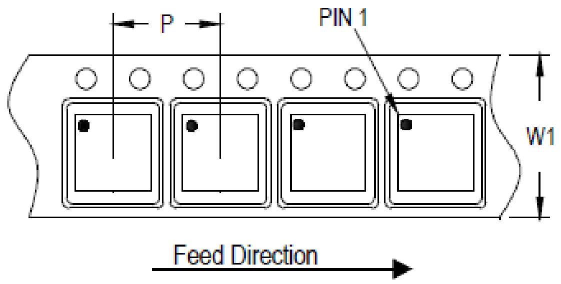
18 Footprint Information

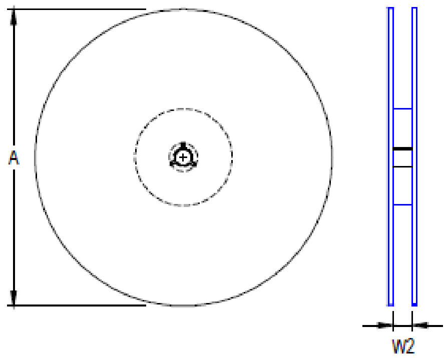


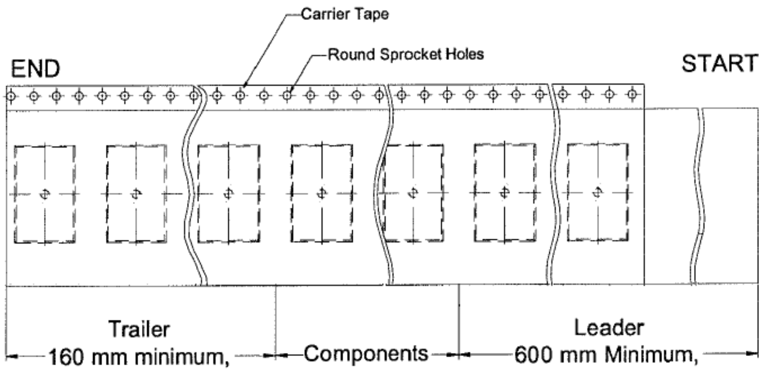
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

19 Packing Information

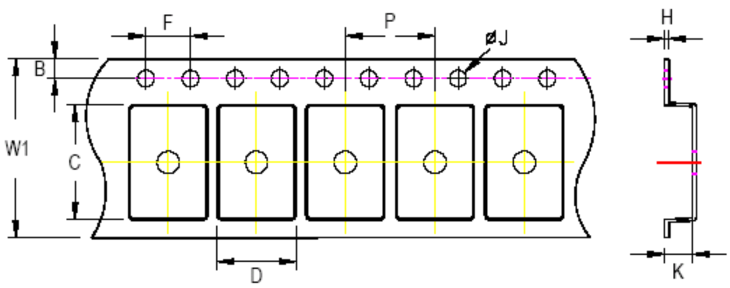
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
02	2024/5/13	Modify	General Description on P1 Ordering Information on P1 Electrical Characteristics on P7 Application Information on P23, P24 Packing Information on P28, P29, P30

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