High Efficiency Single Synchronous Buck PWM Controller

General Description

The RT6542A PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The RT6542A supports on chip voltage programming function between 0.85V and 1.05V by controlling GX digital inputs.

The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT6542A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs and enter diode emulation mode at light load condition. The buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The RT6542A is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.7V.

The RT6542A is available in a WDFN-14L 3x2 package.

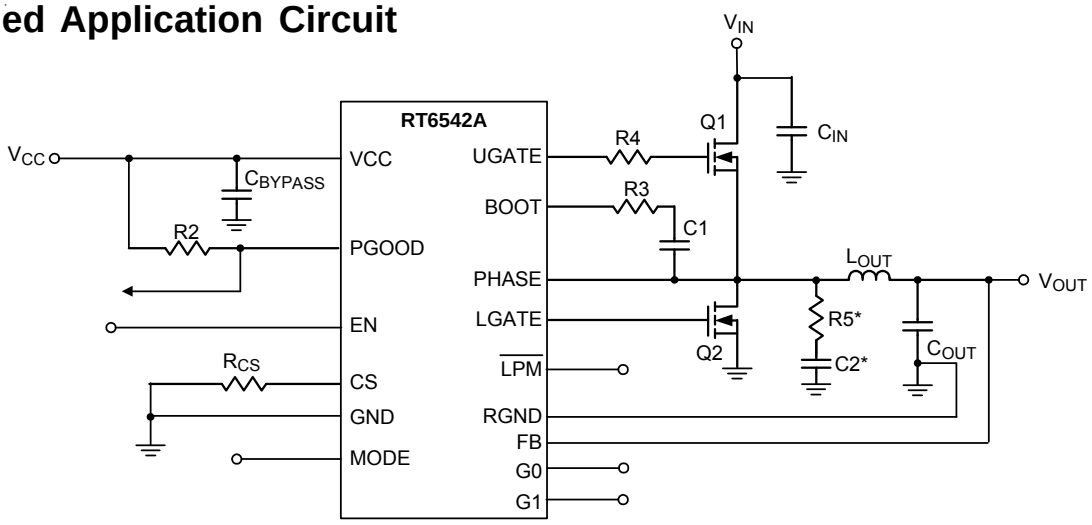
Features

- **Intel Cannon VR Support**
- **Built-in 1% Reference Voltage**
- **2-Bit Programmable Output Voltage with Integrated Transition Support**
- **Support Intel $\overline{\text{LPM}}$ (Low-Power Mode) Feature**
- **4700ppm/°C Programmable Current Limit by Low-Side $R_{DS(ON)}$ Sensing**
- **3V to 26V Battery Input Range**
- **Internal Voltage Ramp Soft-Start Control**
- **Drives Large Synchronous Rectifier FETs**
- **Integrated Boost Switch**
- **Over/Under-Voltage Protection**
- **Thermal Shutdown**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**
- **Tiny 14-Lead WDFN Package**

Applications

- Notebook Computers
- CPU/GPU Core Supply
- Chipset/RAM Supply
- Generic DC-DC Power Regulator

Simplified Application Circuit



Ordering Information

RT6542A □□

- Package Type
  QW : WDFN-14L 3x2 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

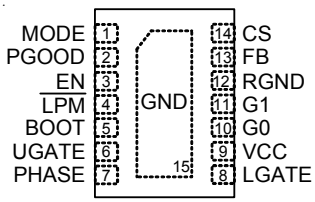
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

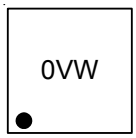
Pin Configuration

(TOP VIEW)



WDFN-14L 3x2

Marking Information



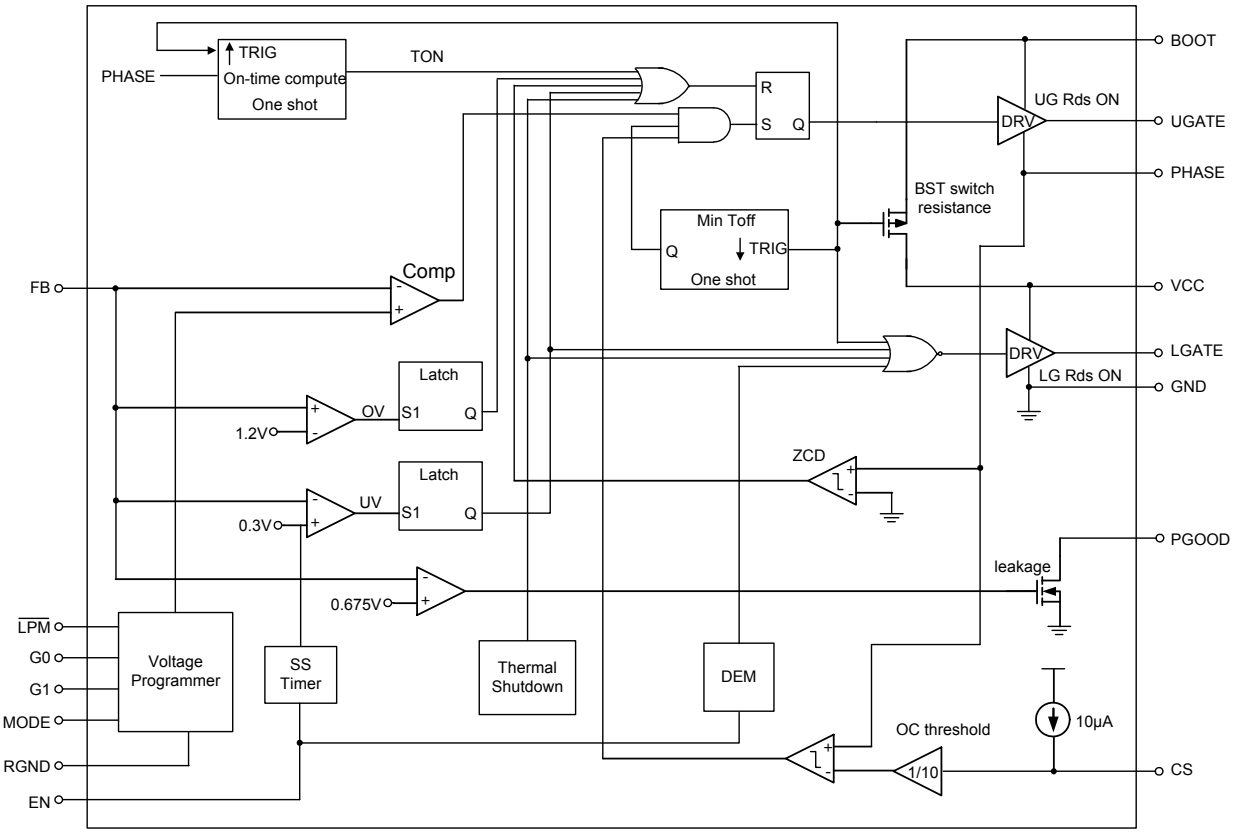
0V : Product Code

W : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	MODE	VCCIO/VPRIMCORE/V1.05A select pin.
2	PGOOD	Open drain power good indicator. High impedance indicates power is good.
3	EN	PWM enable control input. Do not leave this pin floating.
4	$\overline{\text{LPM}}$	Low power mode control pin.
5	BOOT	BOOT bootstrap supply for high-side gate driver.
6	UGATE	High-side gate driver output.
7	PHASE	Switch node. External inductor connection for VDDQ and behave as the current sense comparator input for Low-Side MOSFET $R_{DS(ON)}$ sensing.
8	LGATE	Low-side gate driver output.
9	VCC	Supply voltage input for the analog supply and LGATE gate driver.
10	G0	2-bit input pin.
11	G1	2-bit input pin.
12	RGND	Remote voltage sense ground pin.
13	FB	Output voltage feedback input. Connect VOUT to converter output node.
14	CS	Current limit threshold setting input. Connect a setting resistor to GND and the current limit threshold is equal to 1/10 of the voltage at this pin.
15 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT6542A is a constant on-time synchronous step-down controller. In normal operation, the high-side N-MOSFET is turned on when the output voltage is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. When the soft-start is finished, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The current limit threshold can be set with an external voltage setting resistor on the CS pin.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and under-voltage protection. When the output voltage exceeds 1.2V (Typ.), UGATE goes low and LGATE is forced high. When the feedback voltage is less than 0.3V (Typ.), under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until VCC is re-supplied and exceeds the POR rising threshold voltage or EN is reset.

Absolute Maximum Ratings (Note 1)

- VCC, VOUT, PGOOD, EN, CS, G0, G1, $\overline{LPM}$ to GND ---------- –0.3V to 6.5V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 100ns ---------- –8V to 38V
- BOOT to PHASE
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-14L 3x2 ---------- 2.71W
- Package Thermal Resistance (Note 2)
  - WDFN-14L 3x2, θ_{JA} ---------- 36.9°C/W
  - WDFN-14L 3x2, θ_{JC} ---------- 10.9°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, PHASE ---------- 3V to 26V
- Control Voltage, V_{CC} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, V_{IN} = 8V, V_{EN} = 5V, V_{CS} = 1V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Supply Voltage	V_{CC}		4.5	--	5.5	V
V_{CC} Quiescent Supply Current	I_Q	FB forced above the regulation point, EN = 5V, $\overline{LPM}$ = 5V	--	200	--	μA
	I_{Q_LPM}	FB forced above the regulation point, EN = 5V, $\overline{LPM}$ = 0V, VCCIO	--	30	--	μA
V_{CC} Shutdown Supply Current	I_{SD}	EN = 0V	--	--	10	μA
VFB Error Comparator Threshold		G0 = 5V, G1 = 5V, MODE = floating	–0.5	--	0.5	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency		V_{IN} = 12V at CCM	--	560	--	kHz
Minimum Off-Time			250	400	550	ns
Current Sensing						
CS Current			9	10	11	μA
CS Current TC			--	4700	--	PPM/°C
zero Crossing Threshold		GND – PHASE	–8	--	4	mV
Protection Function						
Current Limit Threshold Offset		GND – PHASE = VCS/10	–10	--	10	mV
Negative Current Limit Threshold Offset		PHASE – GND = VCS/10	–15	--	15	mV
UV Trip Level		UV detect, falling edge	0.25	0.3	0.35	V
UVP Delay		V_{FB} = 0.2V	--	5	--	μs
OV Trip Level		OV detect, rising edge	1.14	1.2	1.26	V
OVP Delay		V_{FB} = 1.31V	--	5	--	μs
V_{CC} UVLO Threshold		Rising edge	3.9	4.2	4.5	V
V_{CC} UVLO Hysteresis			--	100	--	mV
Thermal Shutdown		Latch	--	150	--	°C
Start Up & VID						
V_{OUT} Soft-Start		EN high to V_{OUT} = 1.05V	--	2.4	--	ms
Start Up Blanking Time		From EN = high	--	7.4	--	ms
Driver On-Resistance						
UGATE Driver (pull up)	$R_{UGATEsr}$	BOOT-PHASE forced to 5V	--	2.5	5	Ω
UGATE Driver (sink)	$R_{UGATEsk}$	BOOT-PHASE forced to 5V	--	1.5	3	Ω
LGATE Driver (pull up)	$R_{LGATEsr}$	LGATE, high state	--	2.5	5	Ω
LGATE Driver (pull down)	$R_{LGATEsk}$	LGATE, low state	--	0.8	1.6	Ω
Dead Time		UGATE rising	--	20	--	ns
		LGATE rising	--	30	--	ns
Internal Boost Charging Switch-On Resistance		VCC to BOOT, 10mA	--	--	80	Ω
LOGIC I/O						
EN Input Voltage		Controller OFF	--	--	0.4	V
		Controller ON	1.2	--	--	V
G0, G1, $\overline{LPM}$ Input Voltage		Logic Low	--	--	0.3	V
		Logic High	0.8	--	--	V
MODE Select	Logic-Low	VPRIMCORE	--	--	0.8	V
	Logic-High	VCCIO	2.7	--	--	V
	Float	V1.05A	1.8	--	2.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD (upper side threshold decide by OV threshold)						
Trip Threshold (falling)		Hys = 3%	0.625	0.675	0.725	V
Propagation Delay		Falling edge, with respect to PGOOD threshold	--	3	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High state, forced to 5V	--	--	1	μA

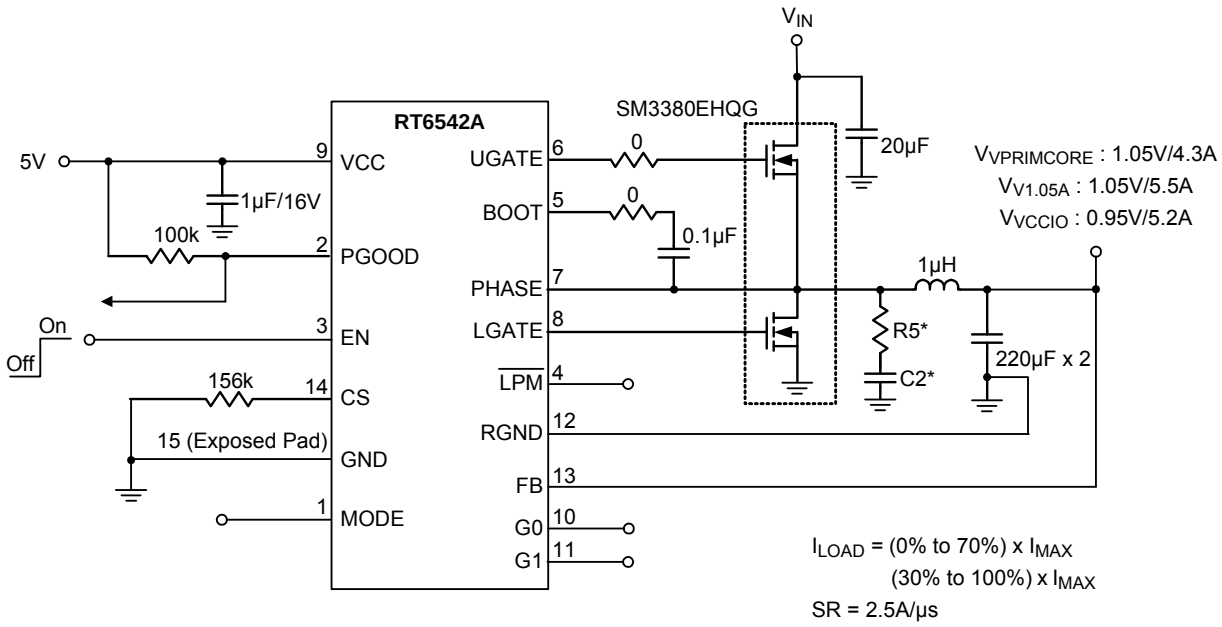
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

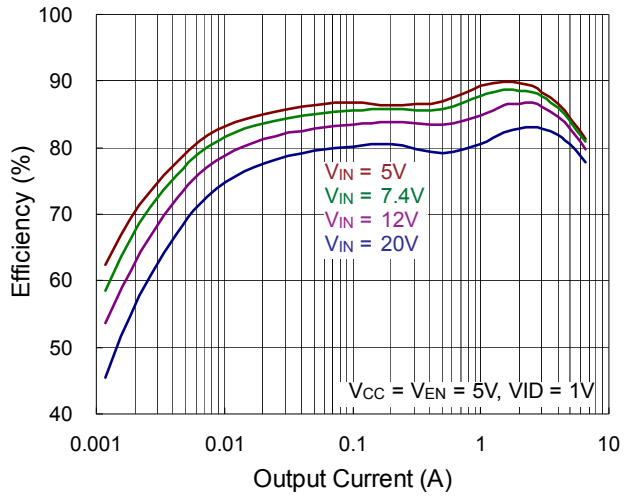
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

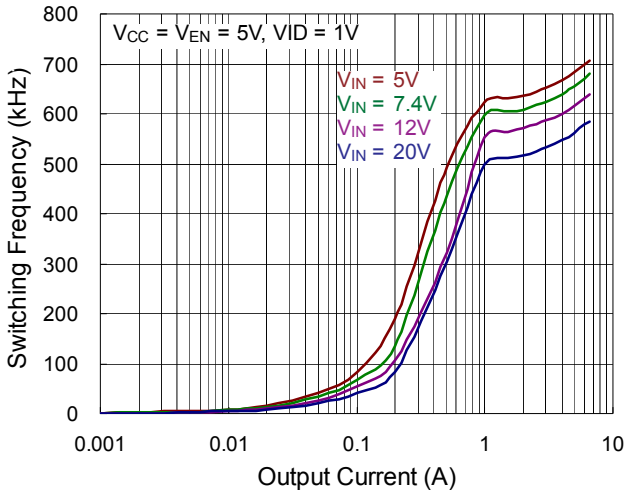


Typical Operating Characteristics

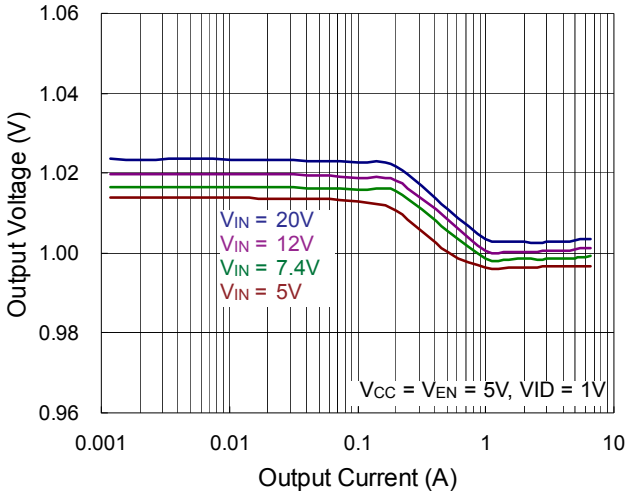
Efficiency vs. Output Current



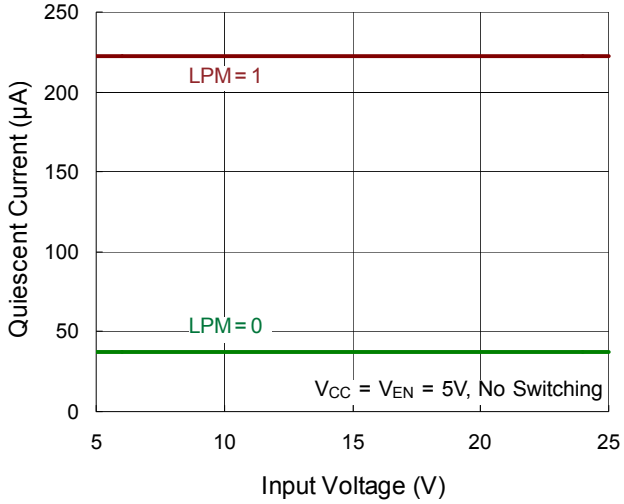
Switching Frequency vs. Output Current



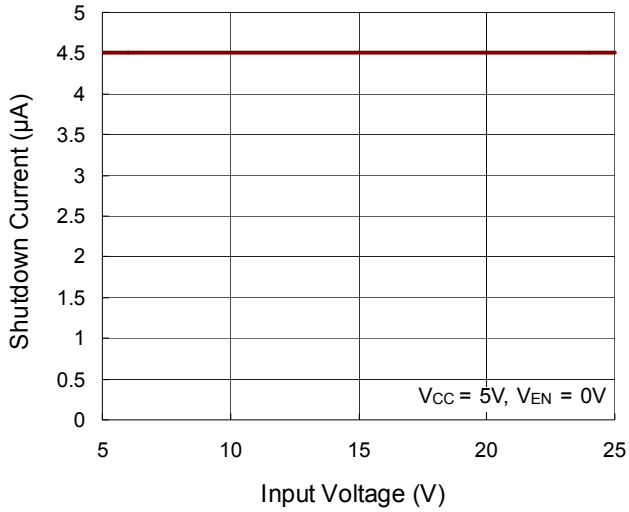
Output Voltage vs. Output Current



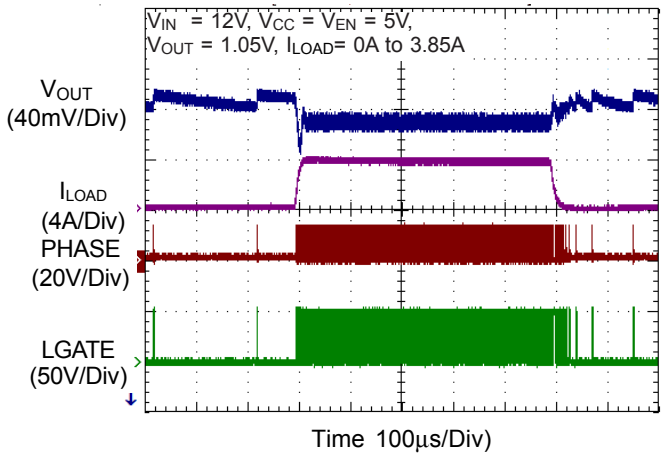
Quiescent Current vs. Input Voltage



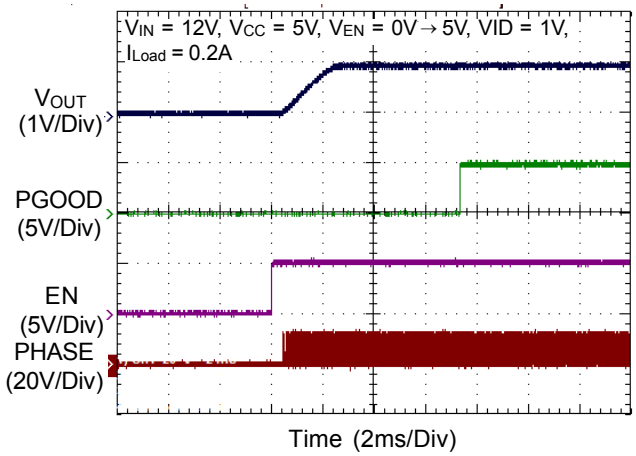
Shutdown Current vs. Input Voltage



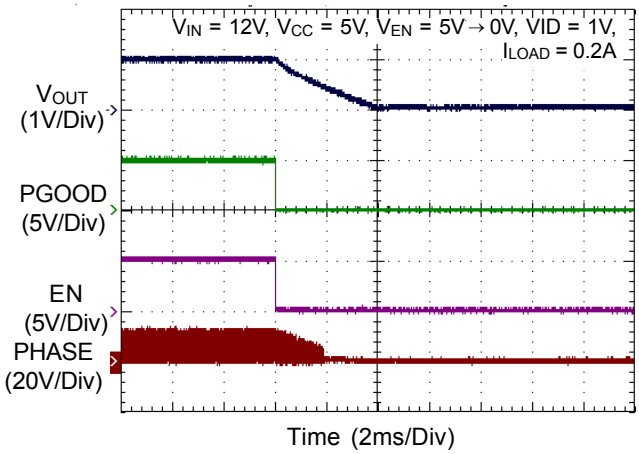
Load Transient Response



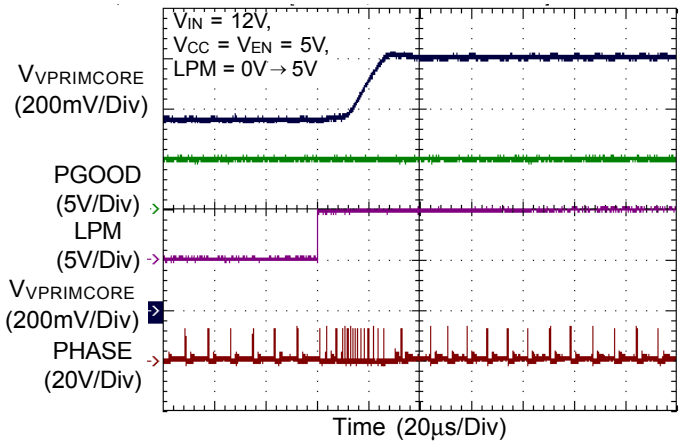
Power On from EN



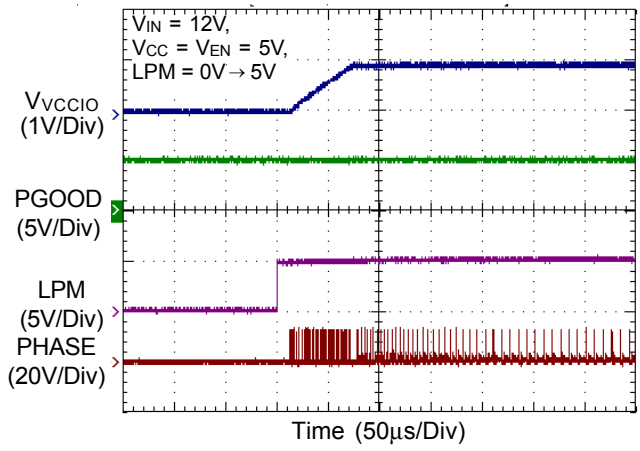
Power Off from EN



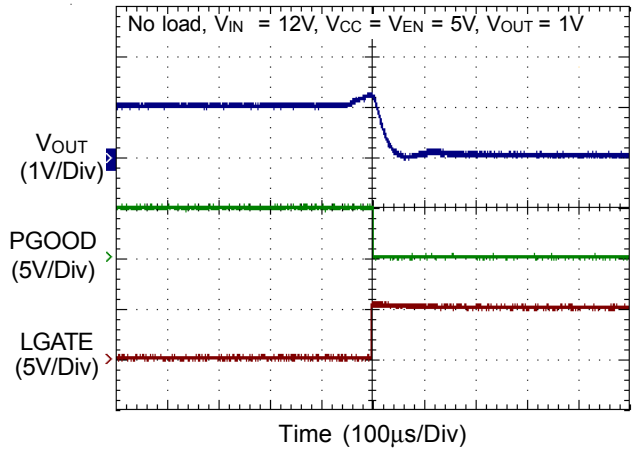
LPM Ramp Up (VPRIMCORE)



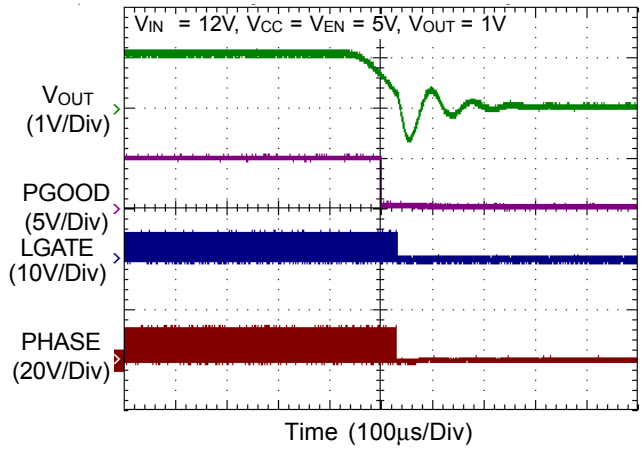
LPM Ramp Up (VCCIO)



Over-Voltage Protection



Under-Voltage Protection



Application Information

The RT6542A is of a constant on-time PWM controller which provides four DC feedback voltages by controlling the G0 and G1 digital input. The constant on-time PWM control

scheme handles wide input / output ratios with ease and provides 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs, while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™, DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Referring to the function diagrams of the RT6542A, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the high-side MOSFET is turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.)

On-Time Control (t_{ON})

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high-side switch directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

Diode-Emulation Mode

The RT6542A automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing V_{OUT} ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial negative current when the inductor freewheeling current becomes negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that is required for the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

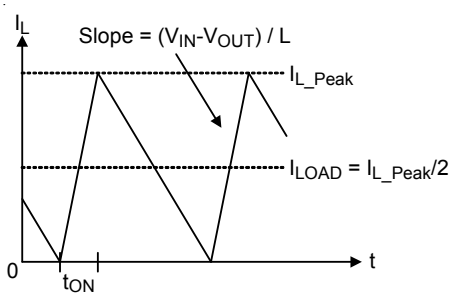


Figure 1. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The

disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

$\overline{\text{LPM}}$ (Low Power Mode) and Output Voltage Setting

The RT6542A can support three rails VR , that are VPRIMCORE , V1.05A , VCCIO.

We can selected VR by Mode pin. When Mode pin is equal logic-low , VR is in VPRIMCORE. When Mode pin is equal logic-high, VR is in VCCIO. When Mode pin is floating, VR is in V1.05A. The VR output voltage is set by G1/G0 pin and $\overline{\text{LPM}}$ pin as listed in Table1.

Only VPRIMCORE and VCCIO rails can support low power mode ($\overline{\text{LPM}}$) , where the output voltage of VPRIMCORE is decay to 0.75V by set $\overline{\text{LPM}}$ pin from logic-high to logic-low , and VCCIO output voltage is decay to 0V when $\overline{\text{LPM}}$ pin from logic-high to logic-low.

When VR in V1.05A , the $\overline{\text{LPM}}$ pin must always high , that is V1.05A cannot support low power mode. While VR in VPRIMCORE and VCCIO , the $\overline{\text{LPM}}$ pin is assert , the PGOOD output must remains high impedance. The device also achieves a dynamic output voltage change by dynamic G1/G0 pins. This feature helps the system to minimize power consumption in standby or idle mode.

Table 1. VID Table Definition

VR	Mode Logic	$\overline{\text{LPM}}$	VID Setting		V_{OUT} (V)	Timing (LPM L to H)	Slew Rate (mV/μs)
			G1 Logic	G0 Logic			
VPRIMCORE	0	0	X	X	0.75	Tramp-up < 40μs 0.75V to 1.05V	15
		1	0	0	1.05 (Default)		
		1	0	1	1		
		1	1	0	0.95		
		1	1	1	0.9		
V1.05A	Floating	Fixed 1	X	X	1.05	NA	15
		1	0	0	1.05 (Default)		
		1	0	1	1		
		1	1	0	0.975		
		1	1	1	0.95		
VCCIO	1	0	X	X	0	Tramp-up < 100μs 0V to 0.95V	15
		1	0	0	0.975		
		1	0	1	0.95 (Default)		
		1	1	0	0.875		
		1	1	1	0.85		

Output Voltage Transition Operation

The digital input control pins G0 and G1 allows V_{OUT} to transition to both higher and lower values. For a downward transition, the rapid change of Gx from high to low will suddenly cause V_{FB} to drop to a new internal V_{REF}. At this time the LGATE will drive high to turn on the low-side MOSFET and draw current from the output capacitor via the inductor. LGATE will remain on until V_{FB} falls to the new internal V_{REF}, at which point a normal UGATE switching cycle begins, as shown in Figure 2. For a down transition, the low-side MOSFET remains on until VFB reaches the new internal V_{REF}. Thus, the negative inductor current will be increased. If the negative current become large enough to trigger NOCP, the low-side MOSFET will be turned off to prevent large negative current from damaging the component. Refer to the Negative Over Current Limit section for a full description.

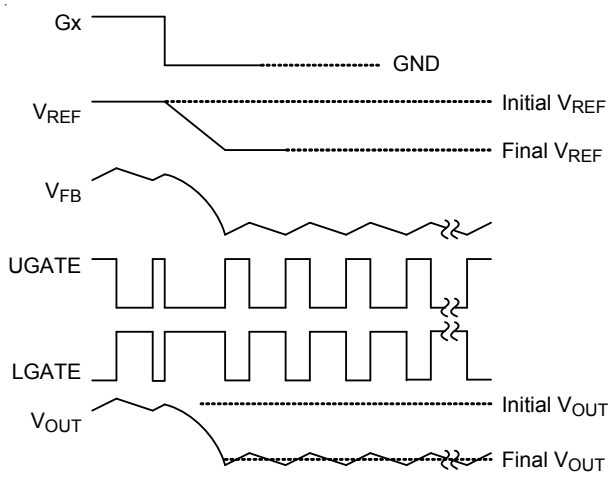


Figure 2. Output Voltage Down Transition

For an upward transition (from lower to higher V_{OUT}) as shown in Figure 3, Gx changes from low to high and causes V_{FB} to rise to a new internal V_{REF}. This quickly trips the V_{FB} comparator regardless of whether DEM is active or not, generating an UGATE on-time and causing a subsequent LGATE to be turned on. At the end of the minimum off-time (400ns), if V_{FB} is still below the new internal V_{REF}, another UGATE on-time will be started. This sequence continues until the FB pin exceeds the new internal V_{REF}.

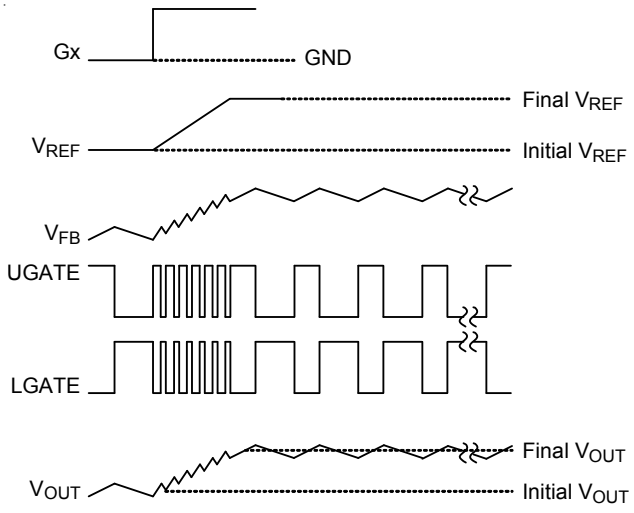


Figure 3. Output Voltage Up Transition

If the V_{OUT} change is significant, there can be several consecutive cycle of UGATE on-time followed by minimum LGATE time. This can cause a rapid increase in inductor current : typically it only takes a few switching cycles for inductor current to rise up to the current limit. At some point the V_{FB} will rise up to the new internal VREF and the UGATE pulses will cease, but the inductor's LI^2 energy must then flow into the output capacitor. This can create a significant overshoot, as shown in Figure 4.

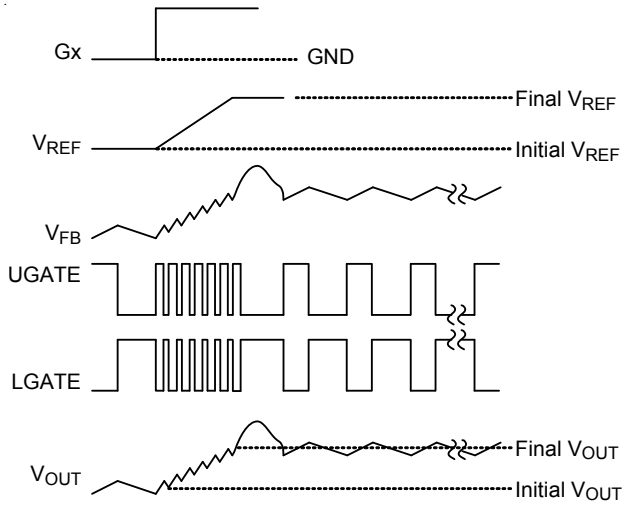


Figure 4. Output Voltage Up Transition with Overshooting

This overshoot can be approximated by the following equation, where I_{CL} is the current limit, V_{FINAL} is the desired set point for the final voltage, L is in μH and C_{OUT} is in μF.

$$V_{MAX} = \sqrt{\left(\frac{I_{CL}^2 \times L}{C_{OUT}}\right) + V_{FINAL}^2}$$

Current Limit Setting (OCP)

The RT6542A has a cycle-by-cycle current limiting control. The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at the CS pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure.5). In order to provide both good accuracy and a cost effective solution, the RT6542A supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The CS pin should be connected to GND through the trip voltage setting resistor, R_{CS}. The 10μA CS terminal source current, I_{CS}, and the trip voltage setting resistor, R_{CS}, set the CS trip voltage, V_{CS}, as in the following equation.

$$V_{CS}(mV) = R_{CS}(k\Omega) \times 10(\mu A)$$

The Inductor current can be monitored by the voltage between GND and the PHASE pin. Hence, the PHASE pin should be connected to the drain terminal of the low-side MOSFET. ICS has temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$.

GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET.

While the comparison is being done during the OFF state, V_{CS} sets the valley level of the inductor current. Thus, the load current at over-current threshold, I_{LOAD_OC}, can be calculated as follows :

$$I_{LOAD\_OC} = \frac{V_{CS}}{10 \times R_{DS(ON)}} + \frac{I_{ripple}}{2}$$

$$= \frac{V_{CS}}{10 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over-current condition, the current to the load exceeds the current to the output capacitor, thus causing the output voltage to fall. Eventually the voltage crosses the under-voltage protection threshold and the device shuts down.

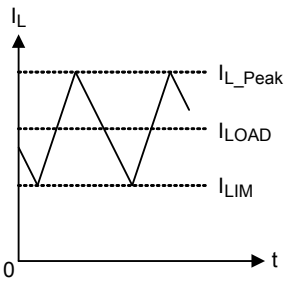


Figure 5. "Vally" Current Limit

Negative Over Current Limit (PWM Only Mode)

The RT6542A supports cycle-by-cycle negative over current limiting in CCM Mode only. The over current limit is set to be negative but is the same absolute value as the positive over current limit. If output voltage continues to rise, the low-side MOSEFT remains on. Thus, the inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the low-side MOSFET is turned off and the current flows towards VIN through the body diode of the high-side MOSFET. Because this protection limits the discharge current of the output capacitor, the output voltage tends to rise, eventually hitting the over-voltage protection threshold and shutting down the device. If the device hits the negative over current threshold again before output voltage is discharged to the target level, the low-side MOSFET is turned off and the process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low-side MOSFET is turned off, the high-side MOSFET is then turned on, and the device resumes normal operation.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the VCC supply.

The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. The low-side driver is designed to drive high current, low $R_{DS(ON)}$ NMOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 0.8Ω typical on resistance. A 5V bias voltage is delivered from the V_{CC} supply. The instantaneous drive current is supplied by the flying capacitor between VCC and GND.

For high current applications, some combinations of high and low-side MOSFETs might be encountered that will cause excessive gate drain coupling, which can lead to efficiency killing, EMI-producing shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time, as shown in Figure 6.

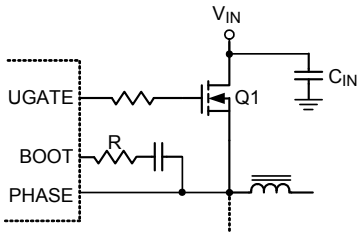


Figure 6. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the feedback voltage is above 1.2V or below 0.3V, PGOOD will be pulled low. PGOOD is allowed to be high until soft-start ends and the output reaches 85% of its set voltage. There is a 3μs delay built into PGOOD circuitry to prevent false transition. When G0 or G1 changes, PGOOD remains in its present state for 32 clock cycles. Meanwhile, V_{OUT} or V_{FB} regulates to the new level.

POR , UVLO and Soft-Start

Power On Reset (POR) occurs when VCC rises above 4.2V (typ). After POR is triggered, the RT6542A will reset the fault latch and prepare the PWM for operation. Below 3.6V (typ.), the VCC Under-Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from the power supply input after EN is enabled. It clamps the ramping of the internal reference voltage which is compared with the FB signal. The typical soft-start duration is 1.2ms.

Over-Voltage Protection (OVP)

The output voltage can be continuously monitored for over-voltage protection. When VFB exceeds 1.2V, over-voltage protection is triggered and the low-side MOSFET is latched on. This activates the low-side MOSFET to discharge the output capacitor. The RT6542A is latched once OVP is triggered and can only be released by VCC or EN power on reset. There is a 5μs delay built into the over-voltage protection circuit to prevent false transitions.

Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under-voltage protection. When V_{FB} is less than 0.3V, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if PHASE is greater than 1V, the LGATE is forced high until PHASE is lower than 1V. There is a 5μs delay built into the under-voltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 3.4ms.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of peak-to-peak ripple current to the maximum average inductor current. Select a low pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit. For CPU core voltage converters and other applications where the output is subject to violent load transient, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain at an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-14L 3x2 package, the thermal resistance, θ_{JA}, is 36.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (36.9°C/W) = 2.71W for a WDFN-14L 3x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

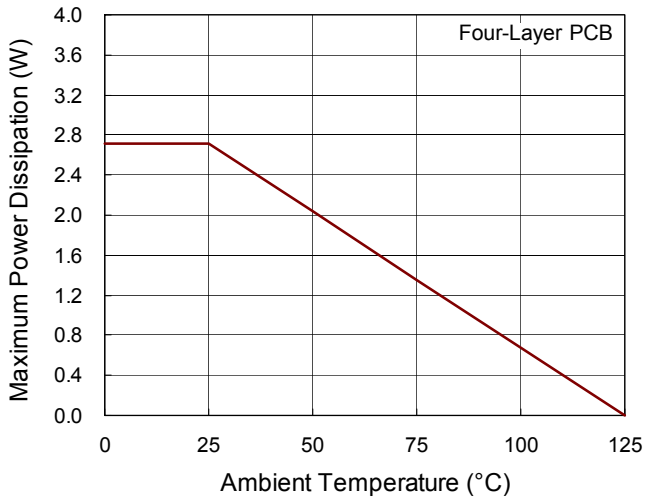


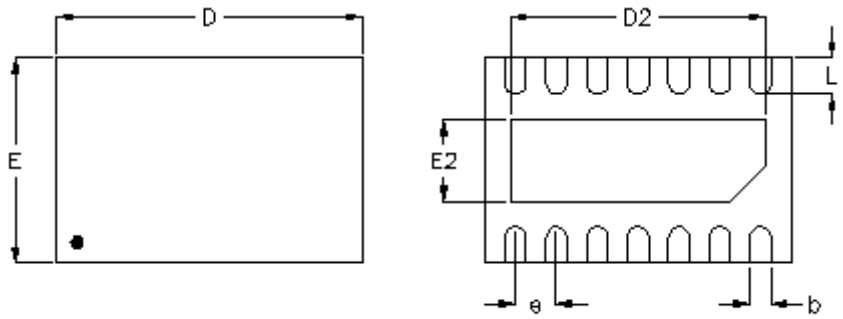
Figure 7. Derating Curve of Maximum Power Dissipation

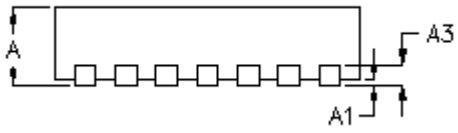
Layout Considerations

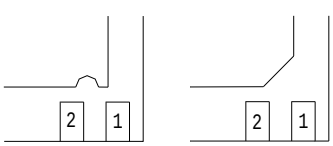
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to converter instability. For best performance of the RT6542A, the following guidelines should be strictly followed.

- Connect an RC low-pass filter from VCC, (1μF and 10Ω are recommended). Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should be kept away from high voltage switching nodes to prevent it from coupling.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components pertaining to FB, GND, EN, PGOOD, CS and VCC should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to prevent it from coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension







DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.450	2.550	0.096	0.100
	Option2	2.550	2.650	0.100	0.104
E		1.950	2.050	0.077	0.081
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.400		0.016	
L		0.300	0.400	0.012	0.016

W-Type 14L DFN 3x2 Package

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