3A, 17V Input, ACOT® Step-Down Buck Converter with Overcurrent Protection for Both High-Side and Low-Side MOSFETs

1 General Description

The RT6263A/B is a simple, easy-to-use 3A synchronous step-down converter with an input supply voltage range of 4.5V to 17V. The device features an accurate reference voltage and integrates low R_{DSON} power MOSFETs to achieve high efficiency.

The RT6263A/B adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate at a nearly constant switching frequency over the line, load, and output voltage range. The RT6263A operates in automatic PSM, which maintains high efficiency during light load operation. The RT6263B operates in Forced PWM, which helps meet tight voltage regulation accuracy requirements.

The RT6263A/B senses the current through both the high-side and low-side MOSFETs for robust overcurrent protection (OCP). The device features cycle-by-cycle overcurrent protection to prevent the device from catastrophic damage in output short circuit, overcurrent, or inductor saturation conditions. The RT6263A/B offers programmable start-up by connecting a capacitor to the external SS pin. The device also includes input undervoltage-lockout, output undervoltage protection, and over-temperature protection (OTP) to ensure safe and smooth operation under all operating conditions.

The recommended junction temperature range is –40°C to 125°C.

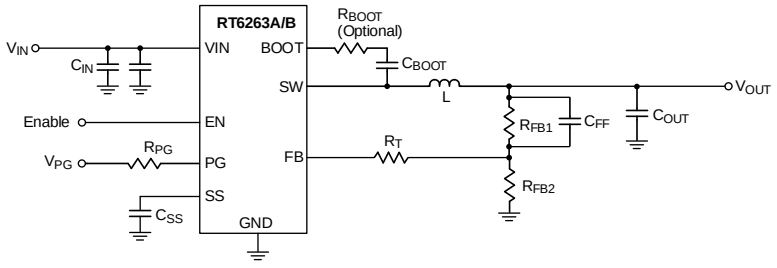
2 Features

- **3A Converter Integrated 66mΩ and 36mΩ FETs**
- **Input Supply Voltage Range: 4.5V to 17V**
- **Output Voltage Range: 0.765V to 7V**
- **Advanced Constant On-Time (ACOT®) Control**
  - **Ultrafast Transient Response**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **High Accuracy Feedback Reference Voltage: Typically ± 1%**
- **Optional Operation Modes:**
  - **RT6263A: Power Saving Mode (PSM)**
  - **RT6263B: Forced PWM Mode**
- **Fixed Switching Frequency: 650kHz**
- **Enable Control and Externally Adjustable Soft-Start**
- **Input Undervoltage-Lockout (UVLO)**
- **Protection Functions**
  - **Output Undervoltage Protection (UVP) with Hiccup Mode**
  - **Overcurrent Protection (OCP) for High-Side and Low-Side MOSFETs and Over-Temperature Protection OTP**
- **Power-Good Indication**

3 Applications

- Set-Top Boxes
- LCD TVs
- Home Networking Devices
- Surveillance
- General Purpose

4 Simplified Application Circuit



5 Ordering Information

RT6263A/B □□□

Package Type(1)
J8F: TSOT-23-8 (FC)

Lead Plating System
G: Richtek Green Policy Compliant(2)

UVP Option
H: Hiccup

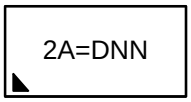
Operation Mode
A: Automatic PSM
B: Forced PWM

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

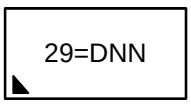
6 Marking Information

RT6263AHGJ8F



2A= : Product Code
DNN : Date Code

RT6263BHGJ8F



29= : Product Code
DNN : Date Code

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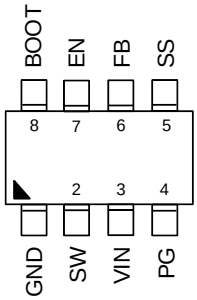
7 Pin Configuration

(TOP VIEW)

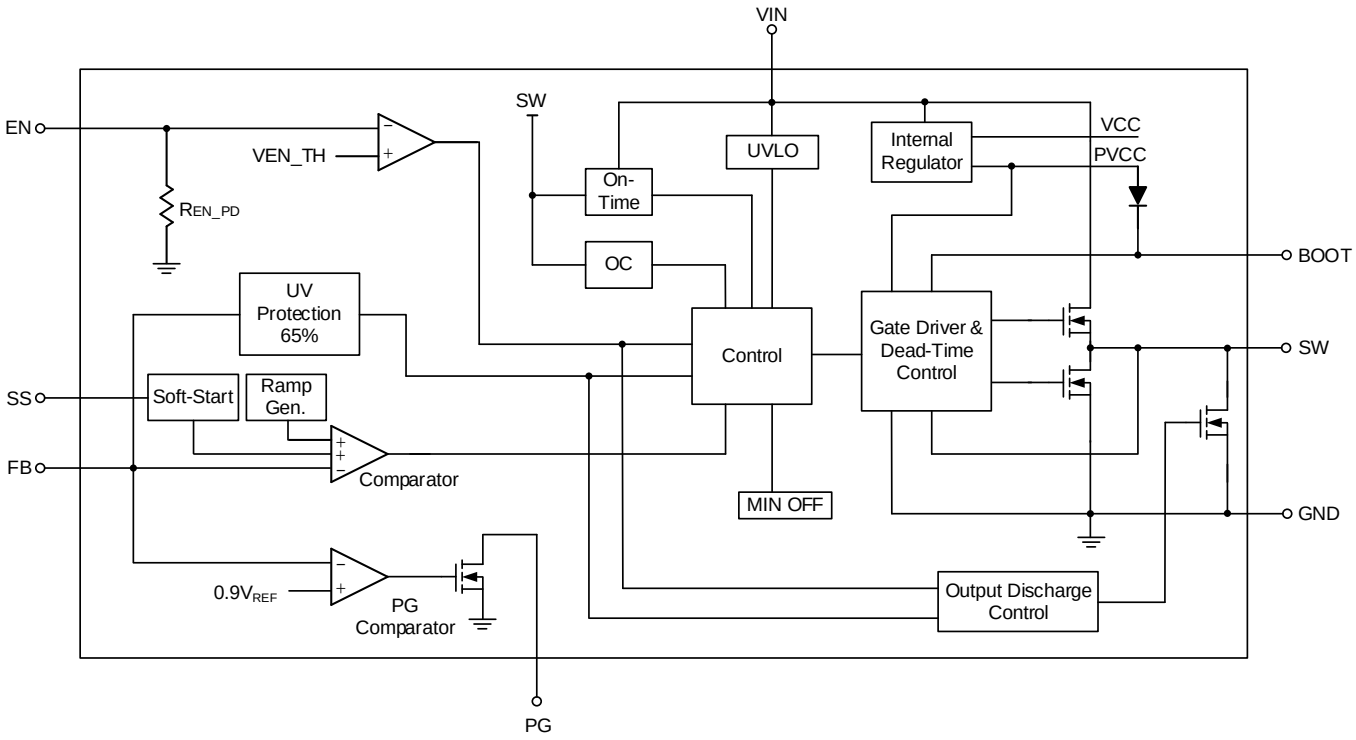


TSOT-23-8 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Power ground.
2	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor and bootstrap capacitor.
3	VIN	Power input. The input voltage range is from 4.5V to 17V. Connect input bypass capacitors directly to this pin and the GND pins. An MLCC with a capacitance higher than 20μF is recommended.
4	PG	Open-drain output for power-good indication. This pin will be pulled low to GND if any internal protection is triggered during the start-up interval.
5	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and GND to set the soft-start time. Do not leave this pin unconnected. A capacitor of 8.2nF is recommended.
6	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at the feedback reference voltage.
7	EN	Enable control input. Connecting this pin to logic high enables the device, and connecting this pin to GND disables the device.
8	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the SW pin.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Enable Voltage, EN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to 20.3V

  <100ns ---------- –5V to 25V
- BOOT Voltage, BOOT ---------- –0.3V to 26V
- BOOT to SW, $V_{BOOT} - V_{SW}$ ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- Power Dissipation, P_D @ T_A = 25°C

  TSOT-23-8 (FC) ---------- 1.6W

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 4.5V to 17V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		TSOT-23-8 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	86	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	108.2	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	62.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	11.21	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.64	°C/W

Note 5. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are simulated on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Voltage	V_{IN}		4.5	--	17	V
Undervoltage-Lockout Threshold	V_{UVLO}		3.7	4	4.3	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVOL_HYS}		--	400	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	3	10	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.8V	--	180	280	μA
Soft-Start						
Soft-Start Current	I_{SS}		--	6	--	μA
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}		1.16	1.25	1.34	V
EN Input Voltage Falling Threshold	V_{EN_F}		1.01	1.1	1.19	
EN Pin Pull-Down Resistance	R_{EN_PD}	EN pin resistance to GND, V_{EN} = 12V	225	450	900	kΩ
Feedback Voltage and Discharge Resistance						
Feedback Voltage	V_{FB}	V_{OUT} = 1.05V	758	765	772	mV
FB Pin Current	I_{FB}	V_{FB} = 0.8V, T_A = 25°C	–0.1	0	0.1	μA
Discharge Resistance	R_{DISCHG}	V_{EN} = 0V, V_{SW} = 1V	--	100	200	Ω
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}	V_{BOOT} – V_{SW} = 4.8V	--	66	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	36	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}		--	5.6	--	A
Low-Side Switch Current Limit	I_{LIM_L}		3.3	4.2	--	
Low-Side Switch Negative Current Limit	I_{NOC}	Forced PWM mode only	--	2.5	--	A
Switching Frequency						
Switching Frequency	f_{SW}	V_{OUT} = 1.05V, PWM mode	--	650	--	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	60	--	ns
Minimum Off-Time	t_{OFF_MIN}	V_{FB} = 0.5V	--	200	260	ns
Output Undervoltage Protections						
Output Undervoltage Protection Threshold	V_{UVP}	Hiccup detect	--	65	--	%
Hiccup Power On-Time	t_{HICCUP_ON}	Relative to SS time	--	1	--	cycle
Hiccup Power Off-Time	t_{HICCUP_OFF}	Relative to SS time	--	7	--	cycles
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	155	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	35	--	
Power-Good Function						
Power-Good Voltage Rising Threshold	V_{PG_R}	V_{FB} rising, PG from low to high	85	90	95	%
Power-Good Voltage Falling Threshold	V_{PG_F}	V_{FB} rising, PG from high to low	--	85	--	
Power-Good Sink Current	I_{PG}	V_{PG} = 0.5V	0.5	1	--	mA

15 Typical Application Circuit

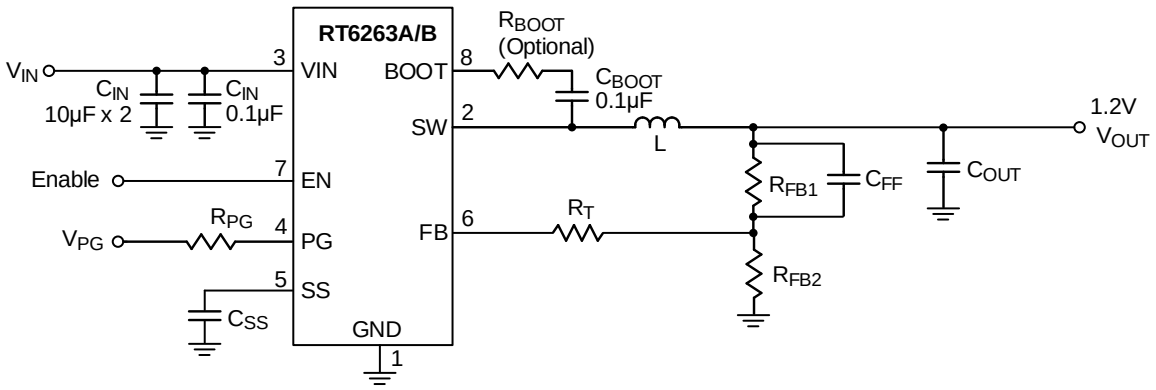


Table 1. Recommended Components Selection

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FF} (pF)	R_T (kΩ)	L (µH)	C_{OUT} (µF)
5.0	54.9	10	10 to 100	10	2.2 to 4.7	20 to 68
3.3	33.2	10	10 to 100	10	1.5 to 4.7	20 to 68
2.5	22.6	10	10 to 100	10	1.5 to 4.7	20 to 68
1.8	13.7	10	10 to 100	10	1.5 to 4.7	20 to 68
1.5	9.53	10	--	--	1.0 to 4.7	20 to 68
1.2	5.76	10	--	--	1.0 to 4.7	20 to 68
1.0	3.09	10	--	--	1.0 to 4.7	20 to 68

Table 2. Recommended External Components

Component	Description	Vendor P/N
C_{IN}	10µF, 25V, X5R, 0805	GRM21BR61E106MA73 (MURATA) 0805X106M250 (WALSIN)
C_{OUT}	22µF, 6.3V, X5R, 0603	GRM187R60J226ME15 (MURATA) 0603X226M6R3 (WALSIN)
L	2.2µH	74404054022 (WE) LQH5BPN2R2N38 (MURATA)
	4.7µH	74404054047 (WE) LQH5BPN4R7N38 (MURATA)

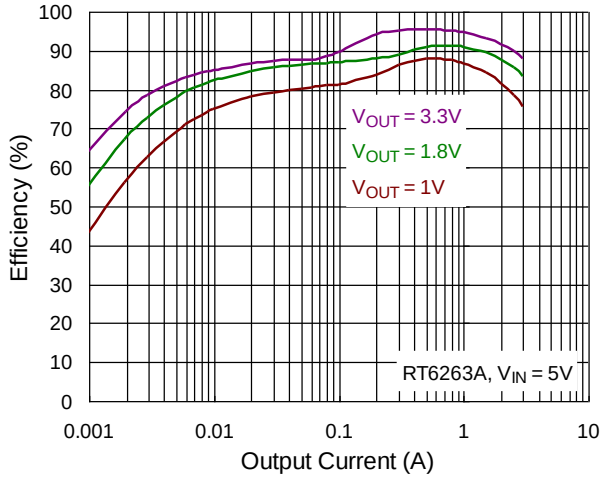
Note 7. Considering the effective capacitance de-rating, which is related to the biased voltage level and the size of the capacitor, the effective capacitance of C_{OUT} should meet 18µF when 3.3V ≤ V_{OUT} ≤ 5V and 16µF when V_{OUT} < 3.3V.

The effect of a higher C_{FF} value (>100pF) may not be obvious. Furthermore, it probably results in worse load regulation. Evaluating the load regulation is suggested if a higher C_{FF} is applied.

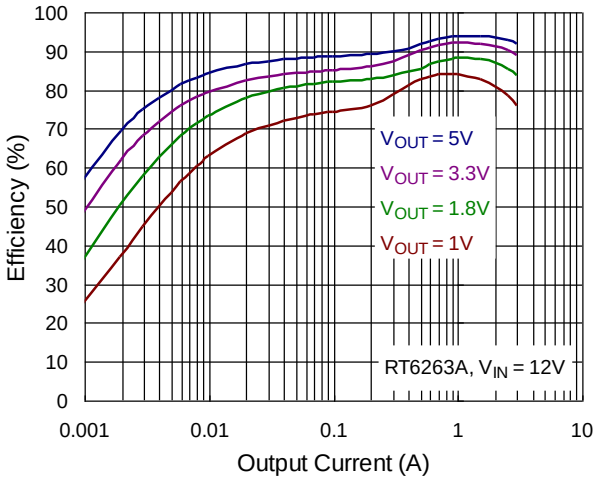
16 Typical Operating Characteristics

L: WE-74404054022 (DCR = 19mΩ) for V_{OUT} = 1V and 1.8V.
L: WE-74404054047 (DCR = 30mΩ) for V_{OUT} = 3.3V and 5V.

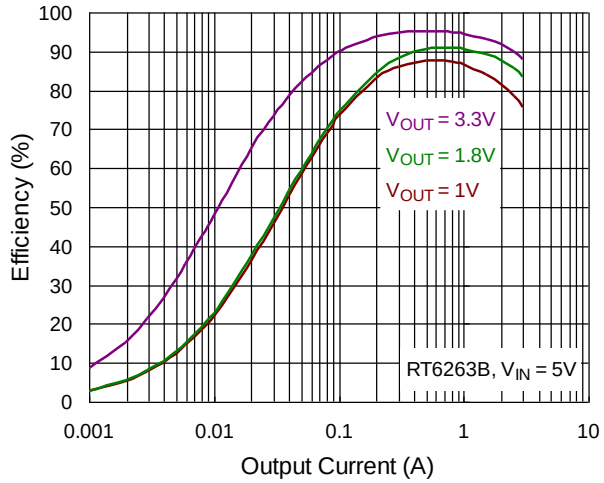
Efficiency vs. Output Current



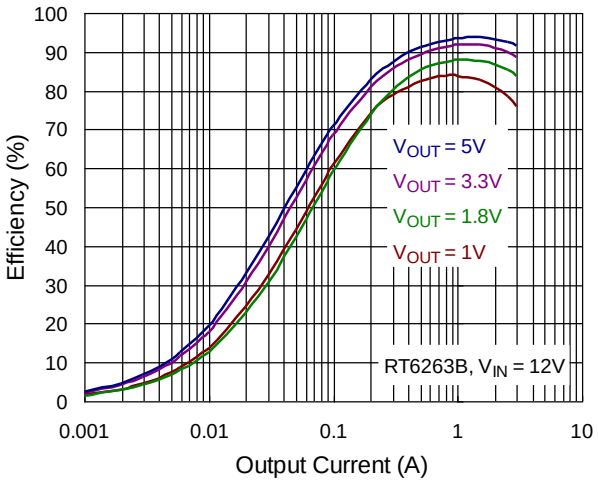
Efficiency vs. Output Current



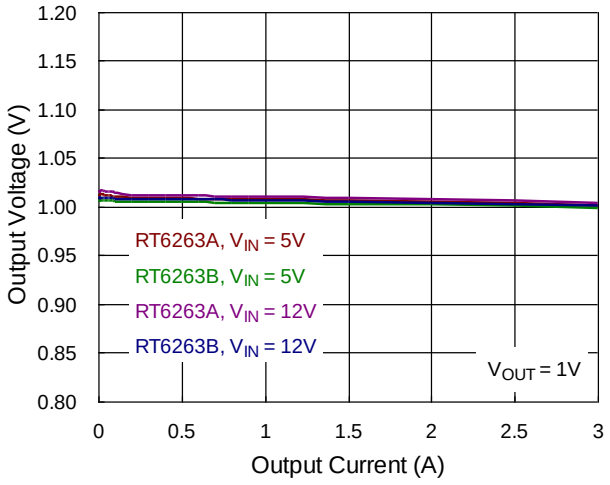
Efficiency vs. Output Current



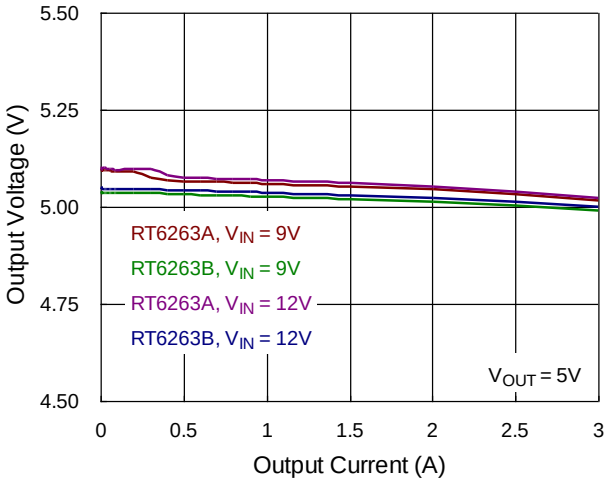
Efficiency vs. Output Current



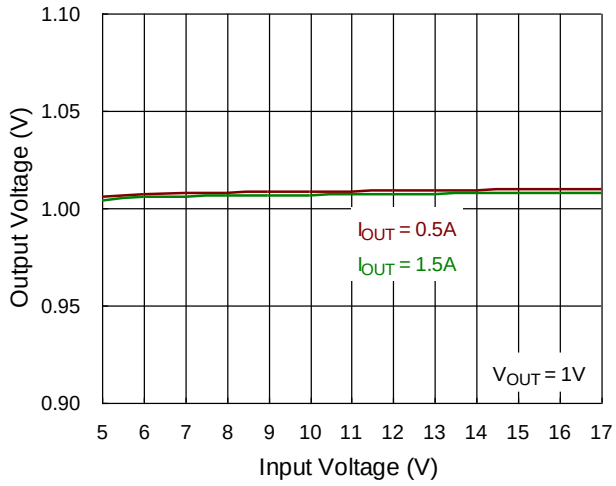
Output Voltage vs. Output Current



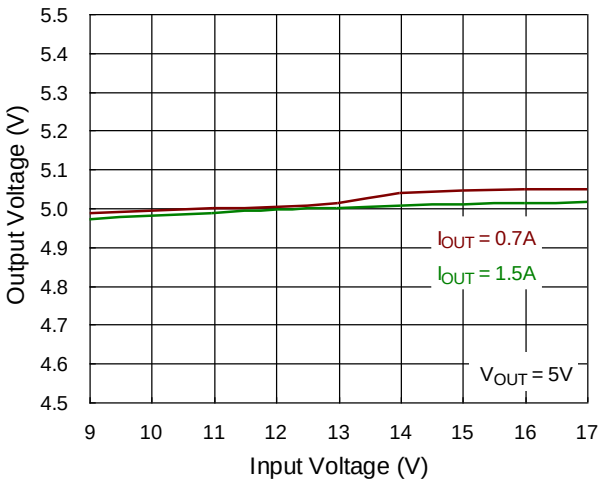
Output Voltage vs. Output Current



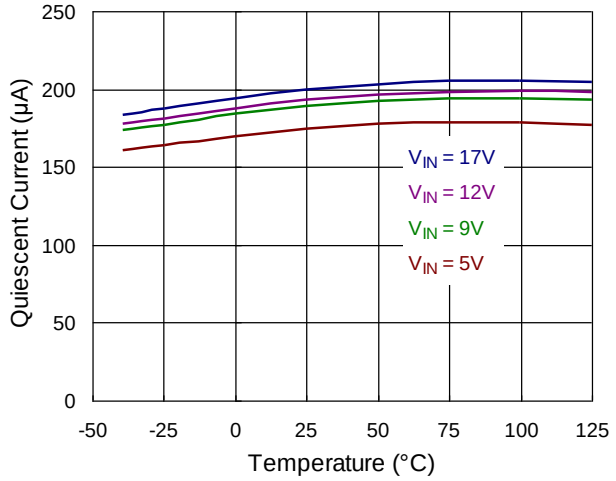
Output Voltage vs. Input Voltage



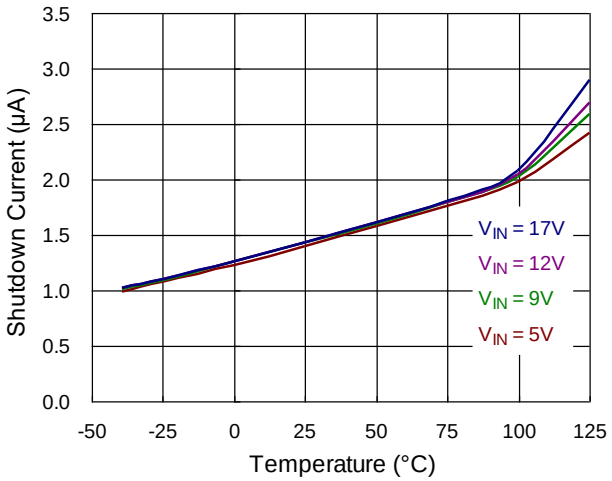
Output Voltage vs. Input Voltage



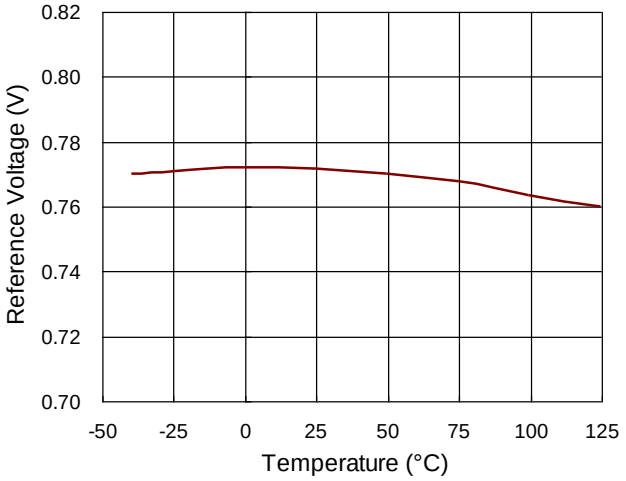
Quiescent Current vs. Temperature



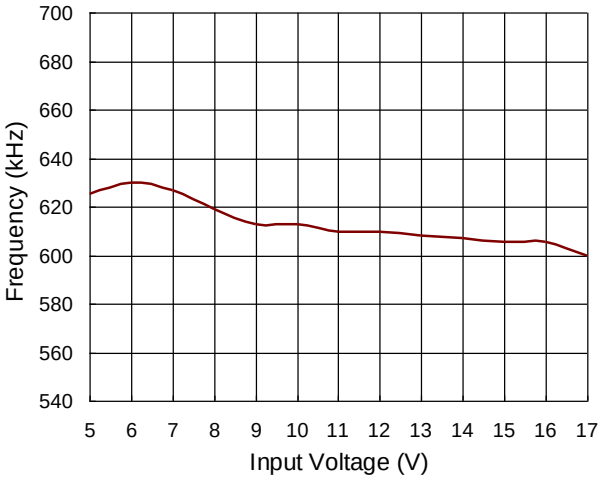
Shutdown Current vs.Temperature



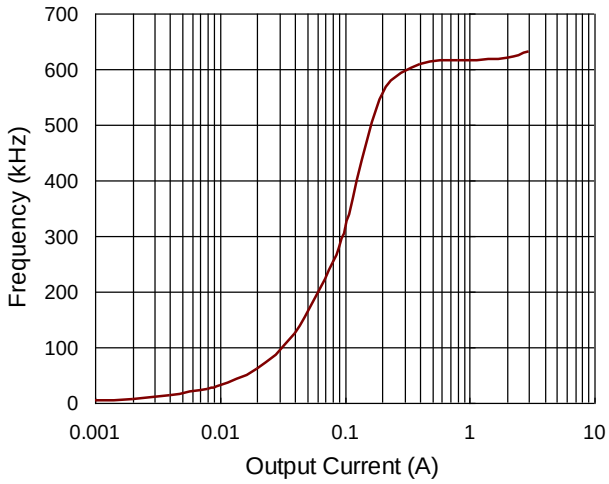
Reference Voltage vs.Temperature



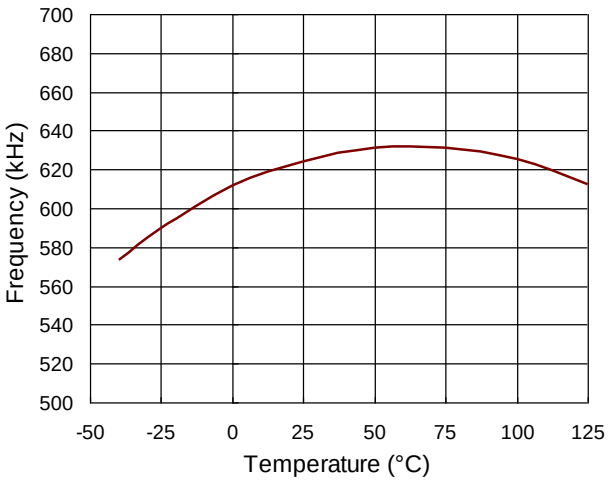
Frequency vs. Input Voltage



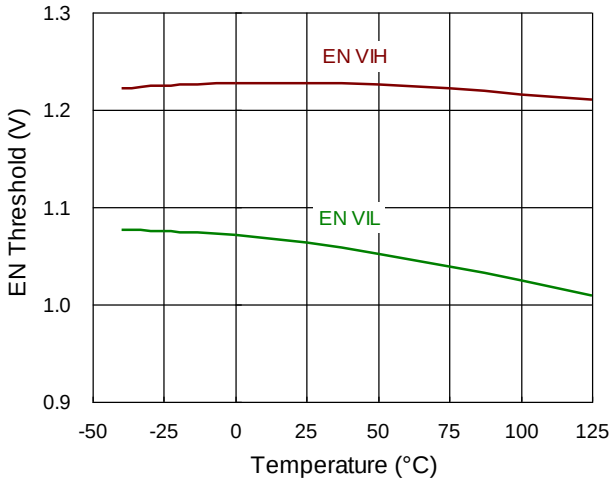
Frequency vs. Output Current



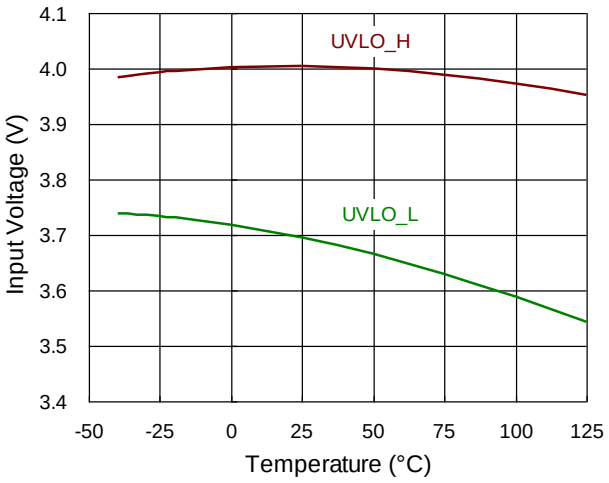
Frequency vs. Temperature



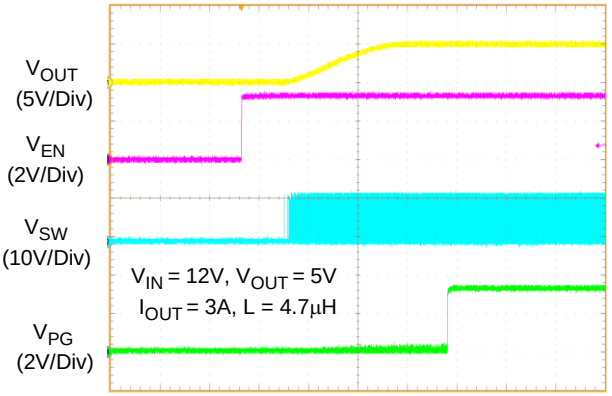
EN Threshold vs. Temperature



UVLO vs. Temperature

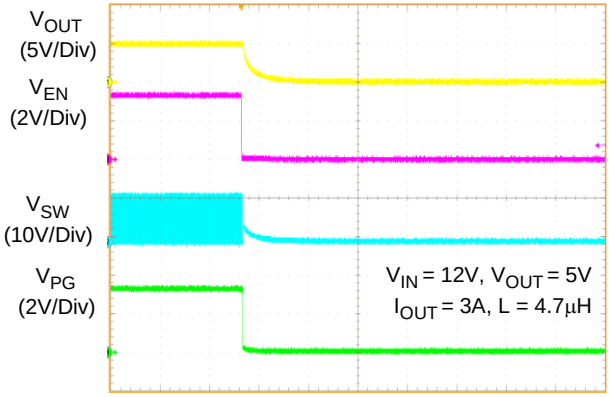


Power On from EN



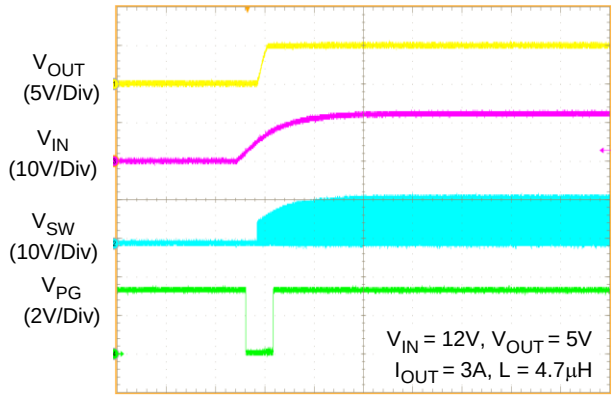
Time (500µs/Div)

Power Off from EN

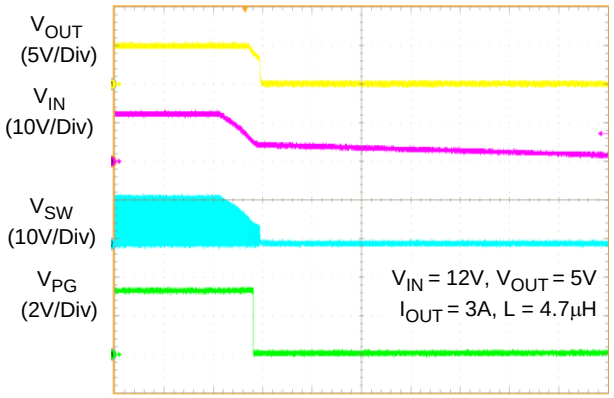


Time (200µs/Div)

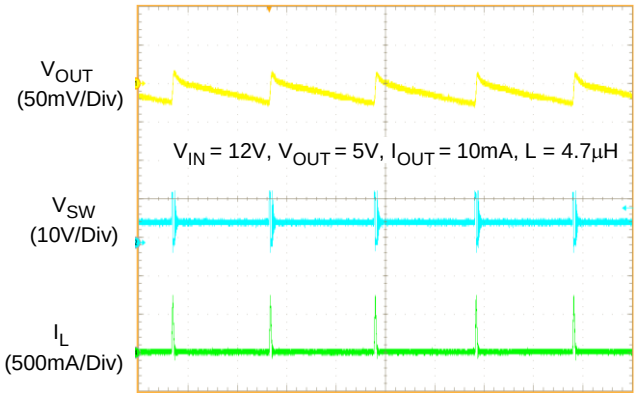
Power On from VIN



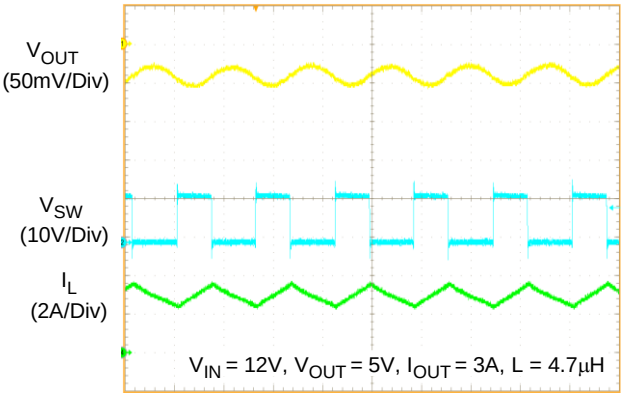
Power Off from VIN



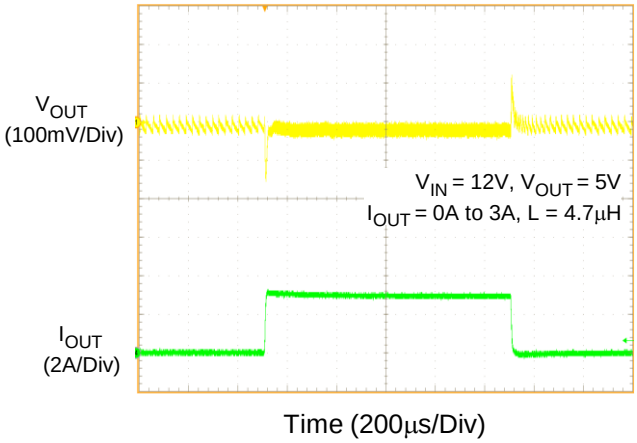
Output Ripple as I_{OUT} = 10mA



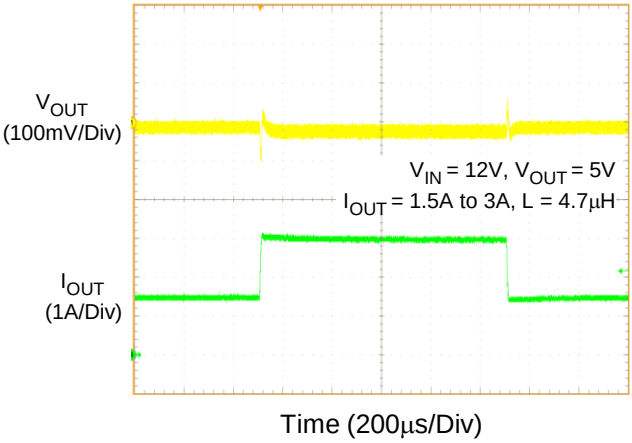
Output Ripple as I_{OUT} = 3A



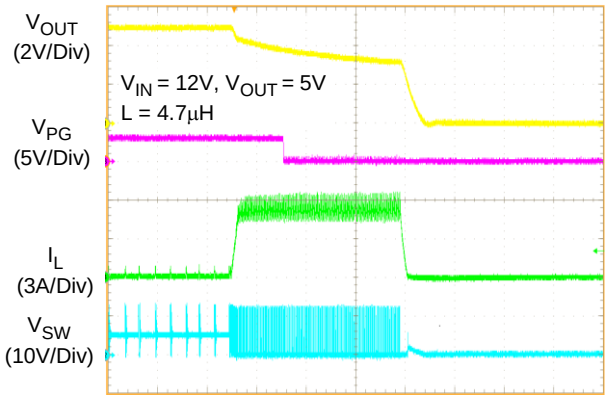
Load Transient (No Load to Full Load)



Load Transient (Half Load to Full Load)

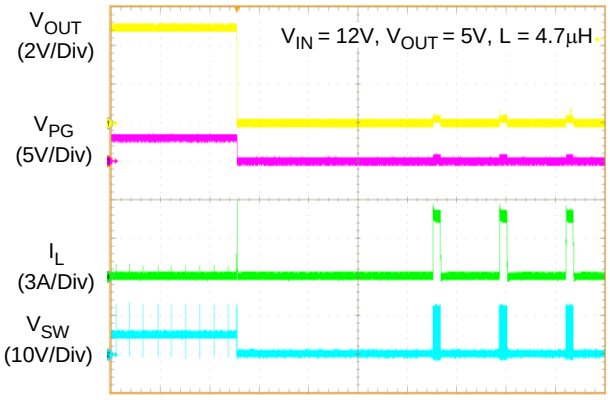


Overcurrent Protection and UVP



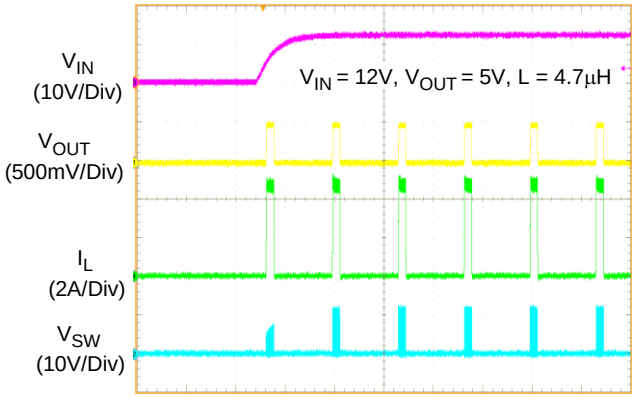
Time (50µs/Div)

Short Circuit Protection



Time (10ms/Div)

Short Circuit before Power On



Time (10ms/Div)

17 Operation

The RT6263A/B is a high-efficiency, synchronous step-down converter that can deliver up to 3A output current from a 4.5V to 17V input voltage.

17.1 Advanced Constant On-Time Control and PWM Operation

The RT6263A/B adopts ACOT® control for its ultrafast transient response, low external component count, and stability with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (200ns, typical) has timed out and the inductor current is below the current-limit threshold, then the internal on-time one-shot circuitry is triggered, and the high-side switch is turned on. Since the minimum off-time is short, the device exhibits an ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to the input voltage and directly proportional to the output voltage to achieve a pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer expires, the high-side switch is turned off, and the low-side switch is turned on until the on-time one-shot is triggered again. To achieve stable operation with low ESR ceramic output capacitors, an internal ramp signal is added to the feedback reference voltage to simulate the output voltage ripple.

17.2 Power Saving Mode (RT6263A Only)

The RT6263A automatically enters power saving mode (PSM) at light load to maintain high efficiency. As the load current decreases, the inductor current ripple valley eventually touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. In this case, the output capacitor is only discharged by the load current so that the switching frequency decreases. As a result, the light-load efficiency can be enhanced due to lower switching loss.

17.3 Enable Control

The RT6263A/B provides an EN pin as an external chip enable control to enable or disable the device. If V_{EN} is held below the logic-low threshold voltage (V_{EN_F}) of the enable input (EN), the converter will disable the output voltage; that is, the converter is disabled, and switching is inhibited even if the VIN voltage is above the VIN undervoltage-lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (10μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_R}) while the VIN voltage is higher than the UVLO threshold, the device will be turned on; that is, switching is enabled, and soft-start sequence is initiated. An internal resistor R_{EN_PD} from EN to GND allows the EN pin to float, shutting down the chip. See Enable Operation.

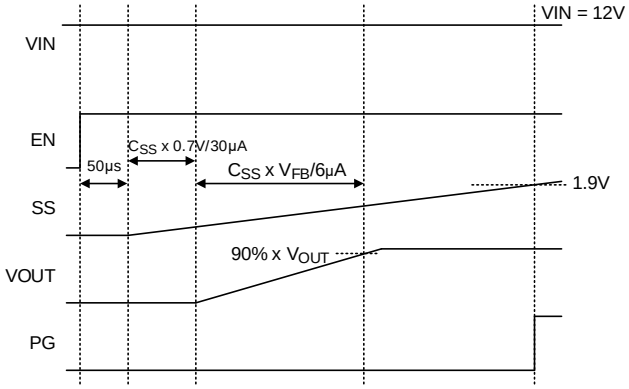
17.4 Soft-Start (SS)

The soft-start function is used to prevent large inrush currents when the converter is being powered up. The RT6263A/B provides the SS pin, allowing the soft-start time to be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to GND. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 6μA) to generate a soft-start ramp voltage, and the internal reference voltage follows this slew rate. The output voltage can be built smoothly due to the method described above, so the SS pin should not be left unconnected to prevent overshoot voltage during the soft-start interval. After the SS pin voltage rises above 1.9V (typical) and V_{FB} reaches 90% of the reference voltage, the open-drain output of PG will become high impedance to indicate a power-good status. The typical start-up waveform shown below indicates the sequence and timing between the output voltage and the related voltages.

See Soft-Start Function.

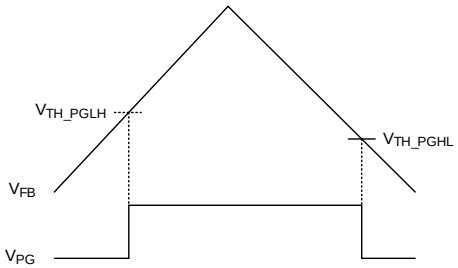
17.5 Pre-Bias

If there is a residual voltage on the output voltage before start-up, both the internal HSFET and LSFET are prohibited from switching until the internal V_{REF} ramps up higher than the feedback voltage. When the soft-start ramp is higher than the feedback voltage, switching will begin, and the output voltage will smoothly rise from the pre-biased level to its regulated target.



17.6 Power-Good Indication

The RT6263A/B features an open-drain output for power-good indication to monitor the output voltage status. The logic delay of the comparator prevents false flags during short excursions, such as line and load transients. Connect PG to VOUT or an external voltage that is below 5.5V. The power-good function is activated after the soft-start is finished and controlled by a comparator connected to the feedback signal V_{FB}. After a certain delay time, when V_{FB} reaches the power-good voltage rising threshold (V_{PG_R}) (typically 90% of the reference voltage), the PG pin becomes high impedance to hold the V_{PG} logic high. Conversely, the PG pin is forced to logic-low when V_{FB} falls to the power-good voltage falling threshold (V_{PG_F}) (typically 85% of the reference voltage). Furthermore, this pin is also forced to logic-low if any internal protection is triggered. The power-good indication profile is shown below.



17.7 Input Undervoltage-Lockout

In addition to the EN pin, the RT6263A/B also provides enable control via the VIN pin. It features an undervoltage-lockout (UVLO) function that monitors the internal linear regulator voltage (VCC). If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. This ensures that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - V_{UVLO\_HYS}$), switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

17.8 Output Undervoltage Protection and Hiccup Mode

The RT6263A/B features output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the feedback voltage, V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold, typically 65% of the internal feedback reference voltage, the UV comparator will go high, turning off both the internal high-side and low-side MOSFET switches. If the output undervoltage condition persists, the RT6263A/B will enter output undervoltage protection in hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF},

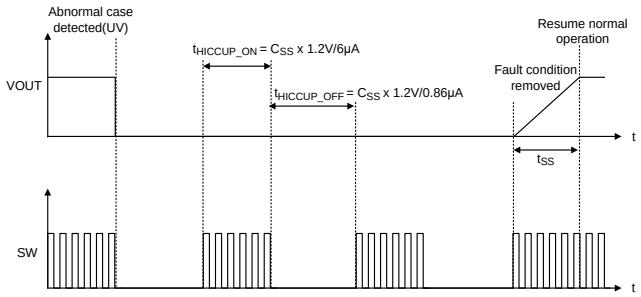
$t_{HICCUP\_OFF} = C_{SS} \times 1.2V/0.86\mu A$

, and then attempt to recover automatically for t_{HICCUP_ON},

$t_{HICCUP\_ON} = C_{SS} \times 1.2V/6\mu A$.

After completion of the soft-start sequence, the converter will resume normal operation if the fault condition is removed; otherwise, the RT6263A/B stays in auto-recovery until the fault condition is cleared.

The hiccup mode allows the circuit to operate safely while an overload or short-circuit condition occurs, and it allows the converter to resume normal operation rapidly once the fault condition is cleared.



17.9 Overcurrent Protection

The RT6263A/B features cycle-by-cycle overcurrent protection on both the high-side and low-side MOSFETs and prevents the device from catastrophic damage in output short-circuit, overcurrent, or inductor saturation conditions.

The high-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch current limit (I_{LIM_H}) after a certain delay when the high-side switch is turned on each cycle. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET overcurrent protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (which is clamped by the low-side current limit), the output capacitor needs to supply the extra current causing the output voltage to begin to drop. If the output voltage drops below the output undervoltage protection trip threshold, the IC will stop switching to avoid excessive heat.

17.10 Negative Overcurrent Limit

The RT6263B is forced to PWM and allows for negative current operation.

In case of PWM operation, high negative current may be generated if an external power source is unexpectedly tied to the output terminal.

Due to the risk described above, the internal circuit monitors the negative current during each on-time interval of the low-side MOSFET and compares it with the NOC threshold.

Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of the output inductor. This behavior can keep the valley of the negative current at the NOC threshold to protect the low-side MOSFET. However, the negative current cannot be limited to the NOC threshold once the minimum off-time is reached.

17.11 Over-Temperature Protection

The RT6263A/B includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down the switching operation when the junction temperature exceeds the over-temperature protection threshold (T_{OTP}). Once the junction temperature cools down by the over-temperature protection hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon for operational purposes. Continuous operation above the specified absolute maximum operating junction temperature may impair the reliability of the device or permanently damage it.

17.12 Output Discharge

The RT6263A/B features a discharge function that discharges the output power under conditions such as when the EN pin goes low, during UVP, and during OTP. The output discharge resistance is typically 100Ω.

18 Application Information

(Note 8)

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which store and deliver energy to the load, and form a second-order low-pass filter to smooth out the switch node voltage and maintain a regulated output voltage.

18.1 Inductor Selection

Inductor selection involves trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with this device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current equal to 20% to 50% of the IC's rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

$I_{L(PEAK)}$ should not exceed the minimum value of the IC's upper current limit level. Additionally, the current flowing through the inductor is the sum of the inductor ripple current and the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the device's switch current limit. For this reason, the most conservative approach is to specify an inductor with a saturation current rating that is equal to or greater than the switch current limit rather than the peak inductor current.

Considering the typical application circuit for a 1.2V output at 3A and an input voltage of 12V, and using an inductor ripple of 1A (33% of the IC's rated current), the calculated inductance value is:

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1A} = 1.66\mu H$$

For the typical application, a standard inductance value of 1.5μH can be selected.

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1.5\mu H} = 1.1A \text{ (37\% of the IC rated current)}$$

$$\text{and } I_{L(PEAK)} = 3A + \frac{1.1A}{2} = 3.55A$$

For the 1.5μH value, the inductor's saturation and thermal rating should be at least 3.55A. For a more conservative approach, the rating for inductor saturation current must be equal to or greater than the switch current limit of the device rather than the inductor peak current.

For EMI-sensitive applications, choosing a shielded type inductor is preferred.

18.2 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to achieve this without causing a large variation in input voltage. The waveforms of C_{IN} ripple voltage and ripple current are shown in Figure 1. The peak-to-peak voltage ripple on the input capacitor can be estimated using the equation below:

$$\Delta V_{CIN} = D \times I_{OUT} \times \left(\frac{1-D}{C_{IN} \times f_{SW}} \right) + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, so the ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated using the equation below:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where $\Delta V_{CIN\_MAX} \leq 200mV$

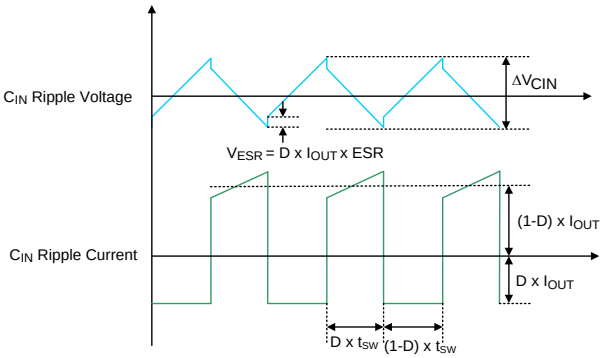


Figure 1. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current, which is given by:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worst-case $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when using these capacitors at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the RT6263A/B circuit is plugged into a live power supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rated voltage. This situation is easily avoided by placing a low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitor of 0.1μF should be placed close to the VIN and GND pins. This capacitor should be 0402 or 0603 in size.

18.3 Output Capacitor Selection

The RT6263A/B is optimized for ceramic output capacitors, and the best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

18.4 Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple passing through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor's capacitance (COUT) and its equivalent series resistance (R_{ESR}) must be taken into consideration. The output peak-to-peak ripple voltage (V_{RIPPLE}) caused by the inductor current ripple (ΔI_L) is characterized by two components; ESR ripple ($V_{RIPPLE(ESR)}$) and capacitive ripple ($V_{RIPPLE(C)}$), and can be expressed as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

When ceramic capacitors are used, both parameters should be estimated due to the extremely low ESR and relatively small capacitance. Referring to the RT6263A/B's typical application circuit for a 1.2V application, the actual inductor current ripple (ΔI_L) is 1.1A, and the output capacitor is 2 x 22μF (Murata ceramic capacitor: GRM219R60J226ME47), V_{RIPPLE} can be obtained as follows:

The ripple caused by ESR (2mΩ) can be calculated as:

$$V_{RIPPLE(ESR)} = 1.1A \times 2m\Omega = 2.2mV$$

Considering the capacitance derating, the effective capacitance is approximately 18μF when the output voltage is 1.2V, and another parameter is:

$$V_{RIPPLE(C)} = \frac{1.1A}{8 \times 2 \times 18\mu F \times 650kHz} = 5.9mV$$

$$V_{RIPPLE} = 2.2mV + 5.9mV = 8.1mV$$

18.5 Output Transient Undershoot and Overshoot

In addition to the voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up or down abruptly. The ACOT® transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load transients.

Both undershoot voltage and overshoot voltage consist of two factors: the voltage steps caused by the output capacitor's ESR and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to evaluate if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges with the chosen inductor value.

The amplitude of the ESR step, either up or down, is a function of the load step and the ESR of the output capacitor:

$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time, since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as follows:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The real on-time will slightly extend due to the voltage drop related to the output current; however, this on-time compensation can be neglected. Additionally, the minimum on-time is 60ns (typical). If the calculated on-time is smaller than the minimum on-time, it and VOUT will both be clamped. Calculate the output voltage sag as follows:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Because some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR should be taken into consideration when calculating the V_{SAG} and V_{SOAR}.

18.6 Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground, with the midpoint connected to FB. The output voltage is set according to the following equation:

$V_{OUT} = 0.765V \times (1 + R_{FB1}/R_{FB2})$

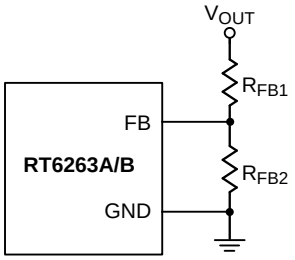


Figure 2. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R_{FB2} between 10kΩ and 100kΩ to minimize power consumption without excessive noise pickup and calculate R_{FB1} as follows:

$$R_{FB1} = \frac{R_{FB2} \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with a tolerance of 1% or better.

18.7 Feed-forward Capacitor Selection (C_{FF})

The RT6263A/B is optimized for low duty cycle applications and the control loop is stable with low ESR ceramic output capacitors. In higher duty cycle applications (higher output voltages or lower input voltages), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Due to the large internal ripple in this condition, the response may become slower and underdamped. This situation will result in a ringing waveform at the output terminal. In the case of high output voltage applications, the phenomenon described above is more visible due to the large attenuation in the feedback network. As shown in Figure 3, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

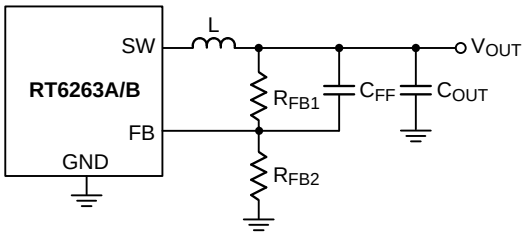


Figure 3. Feedback Loop with Feedforward Capacitor

Loop stability can be evaluated by observing the load transient response. A load step with a speed that exceeds the converter's bandwidth must be applied. For ACOT®, the loop bandwidth can be in the range of 100 to 200kHz, so a load step with a maximum rising time of 500ns (dI/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current-limit threshold. A load transient from 30% to 60% of the maximum load is reasonable, as shown in Figure 4.

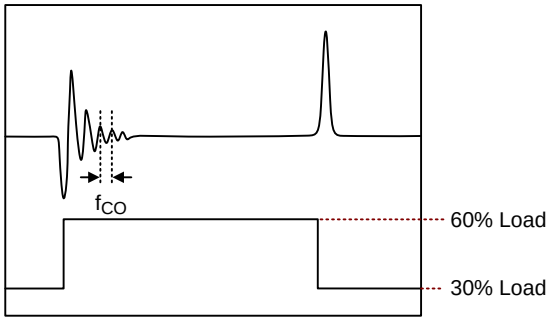


Figure 4. Example of Measuring the Converter BW by Fast Load Transient

C_{FF} can be calculated based on the following equation:

$$C_{FF} = \frac{1}{2\pi \times BW} \sqrt{\frac{1}{R_{FB1}} \times \left(\frac{1}{R_{FB1}} + \frac{1}{R_{FB2}} \right)}$$

Figure 5 shows the transient performance with and without a feedforward capacitor.

Note that after defining the C_{FF}, also evaluate the load regulation, because the feedforward capacitor might inject an offset voltage into V_{OUT}, causing V_{OUT} inaccuracy. If the output voltage is out of specification due to the calculated C_{FF}, decrease the value of the feedforward capacitor C_{FF} or place a series resistor from R_T to the FB pin.

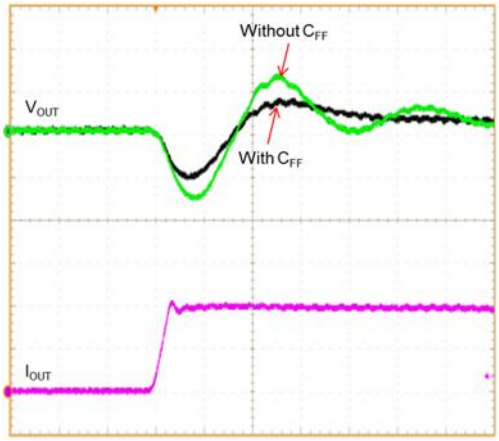


Figure 5. Load Transient Response with and without Feedforward Capacitor

18.8 Enable Operation

The RT6263A/B is enabled when the VIN pin voltage rises above V_{UVLO} and the EN pin voltage exceeds V_{EN_H}. The RT6263A/B is disabled when the VIN pin voltage falls below $V_{UVLO} - V_{UVLO\_HYS}$ or when the EN pin voltage is below V_{EN_F}. An internal pull-down resistor R_{EN_PD}, which is connected from EN to GND, ensures that the chip remains in shutdown even if the EN pin is floated.

For automatic start-up, the EN pin, which has a high-voltage rating, can be connected directly to the input supply V_{IN}, as shown in Figure 6.

The built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to VIN by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 7, to introduce an additional delay. The time delay can be calculated using the equation below, based on the EN's internal threshold at which switching operation begins.

$$C_{EN} = \frac{t}{R_{th} \times \ln \frac{V_{th}}{V_{th} - V_{EN\_H}}}$$

, where

$R_{th} = R_{EN} // R_{EN\_PD}$

$$V_{th} = V_{IN} \times \frac{R_{EN\_PD}}{R_{EN\_PD} + R_{EN}}$$

An external MOSFET can be used for logic control, as shown in Figure 8. In this case, R_{EN} is connected between VIN and the EN pin. The MOSFET Q1 will be controlled by logic to pull down the EN pin.

If it is desired to shut down the device using the EN pin before V_{IN} falls below the UVLO threshold, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 9. For a given R_{EN1}, R_{EN2} can be found using the equation below for the desired V_{IN} stop voltage.

$$V_{IN\_STOP} \times \frac{R_{EN2} // R_{EN\_PD}}{R_{EN1} + R_{EN2} // R_{EN\_PD}} < V_{EN\_L}$$

After R_{EN1} and R_{EN2} are defined, the input voltage V_{IN_START} can be obtained from:

$$V_{EN\_H} \times \frac{R_{EN1} + R_{EN2}//R_{EN\_PD}}{R_{EN2}//R_{EN\_PD}} = V_{IN\_START}$$

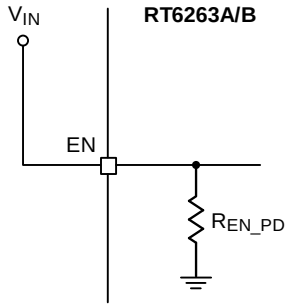


Figure 6. Automatic Start-Up Setting

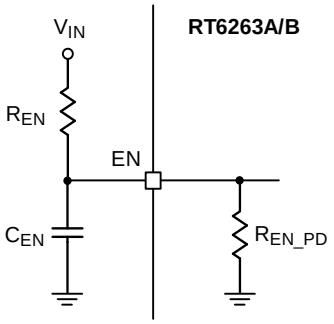


Figure 7. External Timing Control

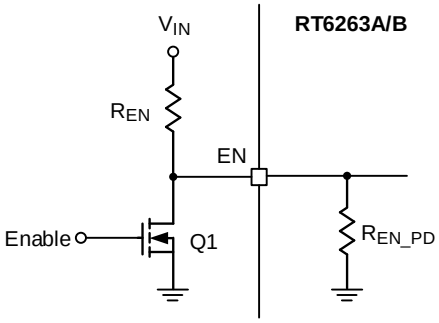


Figure 8. Digital Enable Control Circuit

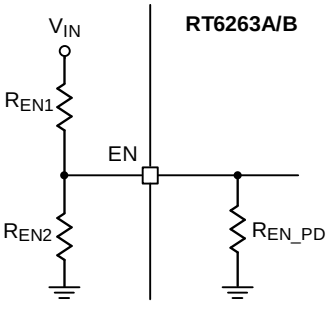


Figure 9. Resistor Divider for Lockout Threshold Setting

If V_{IN} shuts down faster than V_{OUT} and V_{OUT} is larger than 3.7V, the buck converter becomes a boost converter and generates negative current. To prevent this condition, EN should be shut down before V_{IN} falls below V_{OUT}. Therefore, a resistor divider for the lockout threshold is recommended.

18.9 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage (V_{IN}). Specifically, the bootstrap capacitor is charged through an internal diode to a voltage approximately equal to PVCC each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1µF, 0603 or 0402 ceramic capacitor is recommended, and the capacitor should have a 6.3 V or higher voltage rating.

18.10 External Bootstrap Diode (Optional)

A 0.1µF low-ESR ceramic bootstrap capacitor is connected between the BOOT and SW pins to supply the high-side gate driver. It is recommended to add an external bootstrap diode between an external 5V supply and the BOOT pin, as shown in Figure 10, to enhance efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V supply from the system, or a 5V output voltage generated by the RT6263A/B. Note that the BOOT voltage (V_{BOOT}) must be lower than 5.5V.

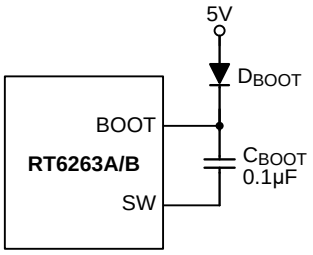


Figure 10. External Bootstrap Diode

18.11 External Bootstrap Resistor (Optional)

The gate driver of an internal power MOSFET, used as a high-side switch, is optimized for turning on the switch. The gate driver is not only fast enough to reduce switching power loss, but also slow enough to minimize EMI. The EMI issue is worse when the switch is turned on rapidly due to the induced high di/dt noise. When the high-side switch is turned off, the discharging time on the SW node is relatively slow because during the dead time, both the high-side and low-side MOSFETs are turned off. In some cases, it is desirable to reduce EMI further, even at the expense of additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small bootstrap resistor, R_{BOOT}, between the BOOT pin and the external bootstrap capacitor, as shown in Figure 11. The recommended range for R_{BOOT} is several ohms to 47 ohms, and it can be 0402 or 0603 in size.

This will slow down the turn-on rate of the high-side switch and the rise rate of V_{SW}. To enhance EMI performance and enhance the internal MOSFET switch, the recommended application circuit, shown in Figure 12, includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor, R_{BOOT}, placed between the BOOT pin and the capacitor/diode connection.

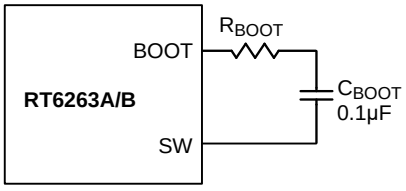


Figure 11. External Bootstrap Resistor at the BOOT Pin

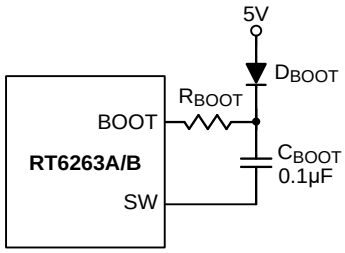


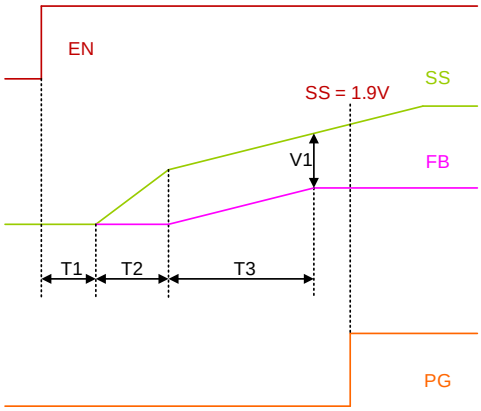
Figure 12. External Bootstrap Diode and Resistor at the BOOT Pin

18.12 Soft-Start Function

The RT6263A/B provides an adjustable soft-start function. When the EN pin becomes logic-high, the soft-start current (I_{SS}) begins to charge the capacitor (C_{SS}) which is connected from the SS pin to GND. The soft-start function is used to prevent large inrush current while the converter is in the power-up stage. The soft-start time can be programmed by the external capacitor C_{SS} connected between SS and GND. An internal current source I_{SS} (6µA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during the soft-start interval. The typical soft-start time is calculated as follows:

$$t_{SS} = C_{SS} \times 0.7V/30\mu A + C_{SS} \times V_{FB}/I_{SS}$$

, where t_{SS} = SS rises to FB settled point (T2 + T3).



T1 : EN delay, from EN going high to SS start rising, T1 = 50µs;
T2 : Speed up SS, from SS rising to FB rising, T2 = C_{SS} x 0.7/30µA;
T3 : Normal SS, from FB rising to settled, T3 = C_{SS} x V_{FB}/I_{SS};
V1 : Offset voltage between SS and FB, V1 = 700mV;
PG goes high after SSOK (SS = 1.9V)

Figure 13. Operation of SS Pin when Starting

18.13 Power-Good Indication

The PG pin is an open-drain output for power-good indication and should be connected to an external voltage source through a pull-up resistor. The voltage source can be an external voltage supply or the output of the RT6263A/B, and it must be lower than 5.5V to avoid the risk of damage to this pin. It is recommended to connect a 100kΩ resistor between the external voltage source and the PG pin.

The power-good function is activated after the soft-start is completed and is controlled by the feedback signal V_{FB}. During the soft-start, this pin stays in logic-low, and it is only allowed to transition to logic-high once the soft-start cycle is complete. After a certain delay time, when V_{FB} reaches the power-good voltage rising threshold (V_{PG_R}), typically 90% of the reference voltage, the PG pin becomes high impedance to hold the V_{PG} logic high. Conversely, the PG pin is forced to logic-low when V_{FB} falls to the power-good voltage falling threshold (V_{PG_F}),

typically 85% of the reference voltage. Furthermore, this pin is also forced to logic-low if any internal protection is triggered.

18.14 Thermal Consideration

In many applications, the RT6263A/B does not generate much heat due to its high efficiency and the low thermal resistance of its TSOT-23-8(FC) package. However, in applications where the RT6263A/B runs at a high ambient temperature and high input voltage, the generated heat may exceed the maximum junction temperature of the part.

The RT6263A/B includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. If the junction temperature reaches approximately 155°C, the RT6263A/B stops switching the power MOSFETs until the temperature cools down by 35°C.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

, where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating conditions, the maximum junction temperature is 125°C. TA is the ambient operating temperature, and $\theta_{JA(EFFECTIVE)}$ is the system-level junction-to-ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be enhanced by providing a heat sink with surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

As an example, considering the case when the RT6263A is used in an application where V_{IN} = 12V, I_{OUT} = 3A, f_{SW} = 650kHz, and V_{OUT} = 3.3V. The efficiency at 3.3V, 3A is 85.9% when using WE-74404054047 (4.7μH, 30mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from the manufacturer's website and it is 102mW. In this case, the power dissipation of the RT6263A is:

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.25W$$

Considering the system-level $\theta_{JA(EFFECTIVE)}$ is 68.7°C/W (other heat sources are also considered), the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 1.25W \times 68.7°C/W + 25°C = 110.9°C$$

Figure 14 shows the RT6263A/B R_{DSON} versus different junction temperatures. If the application requires a higher ambient temperature, we might need to recalculate the device power dissipation and the junction temperature of the device based on a higher R_{DSON} since it increases with temperature.

Using a 35°C ambient temperature as an example. Since the variation of the junction temperature is dominated by the ambient temperature, the T'_J at a 35°C ambient temperature can be pre-estimated as:

$$T'_J = 110.9°C + \left(35°C - 25°C\right) = 120.9°C$$

According to Figure 14, the increase in R_{DSON} can be found as:

$\Delta R_{DS(ON)\_H}$ = 90.5mΩ (at 120.9°C) − 88mΩ (110.9°C) = 2.5mΩ

$\Delta R_{DS(ON)\_L}$ = 44.7mΩ (at 120.9°C) − 43.7mΩ (110.9°C) = 1mΩ

The external power dissipation caused by the increase in R_{DSON} at higher temperatures can be calculated as

$$\Delta P_{D,RDS(ON)} = (3A)^2 \times \frac{3.3}{12} \times 2.5m\Omega + (3A)^2 \times \left(1 - \frac{3.3}{12}\right) \times 1m\Omega$$

= 0.013W

As a result, the new power dissipation is 1.263W due to the variation in R_{DSON}. Therefore, the estimated new junction temperature is:

T'_J = 1.263W × 68.7°C/W + 35°C = 121.77°C

If the application requires a higher ambient temperature that may exceed the recommended maximum junction temperature of 125°C, care should be taken to reduce the temperature rise of the part by using a heat sink or increasing air flow.

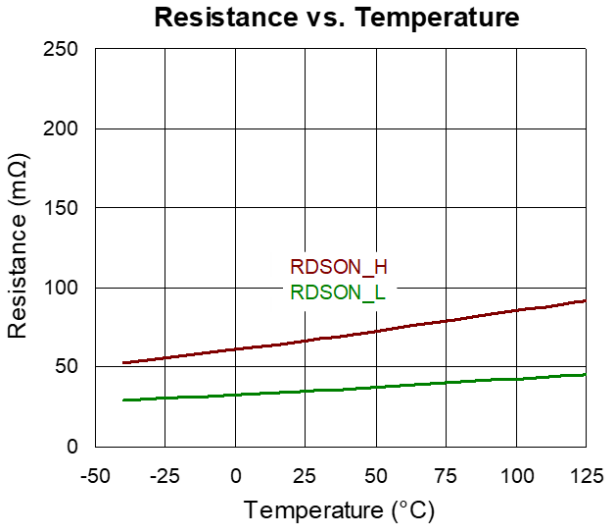


Figure 14. RT6263A/B $R_{DS(ON)}$ vs. Temperature

18.15 Layout Considerations

Follow the PCB layout guidelines below for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable and jitter-free operation. The high-current path comprising the input capacitor, high-side FET, inductor, and output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The main MLCC capacitors should be placed on the same layer as the RT6263A/B.
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect the feedback network behind the output capacitors. Place the feedback components close to the FB pin.
- For better thermal performance, design a wide and thick plane for the GND pin or add a lot of vias to the GND plane.

An example of a PCB layout guide is shown in Figure 15.

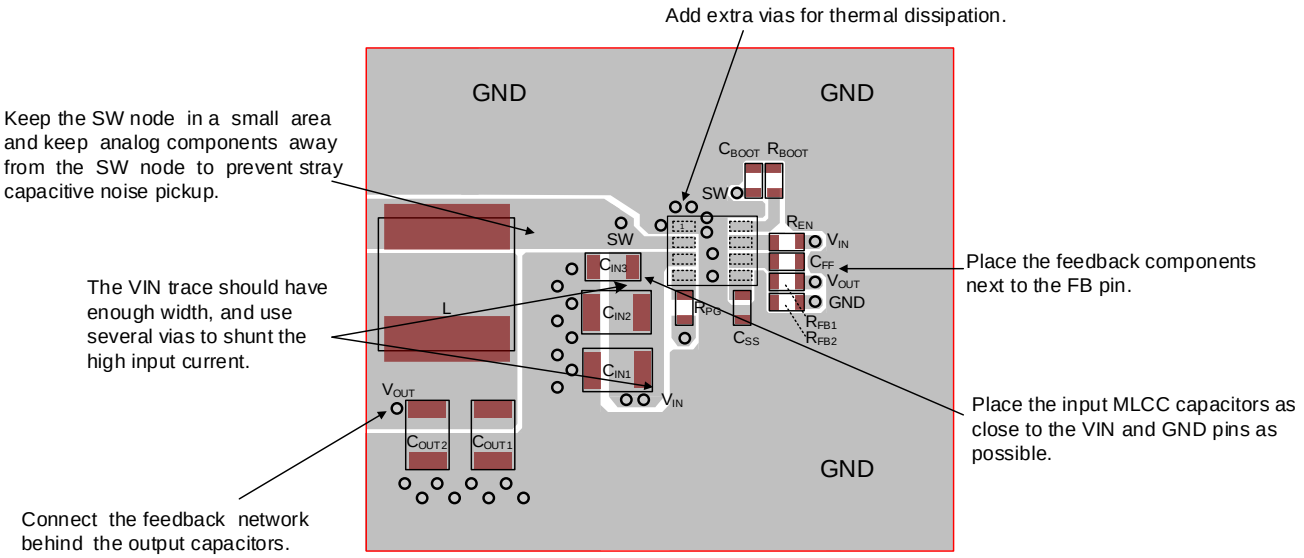
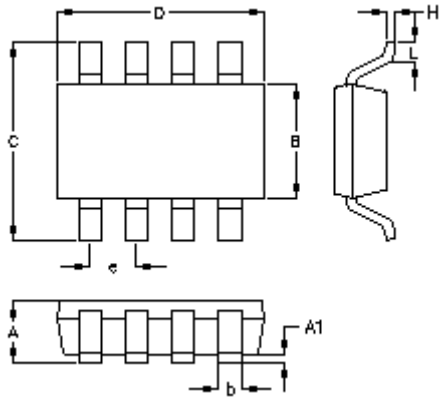


Figure 15. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

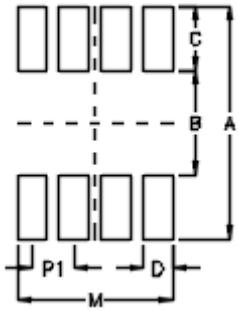
19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package

20 Footprint Information

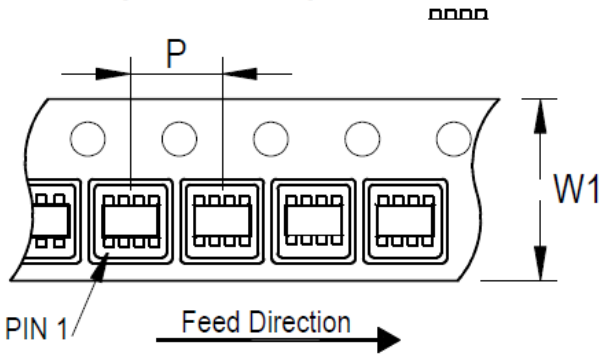


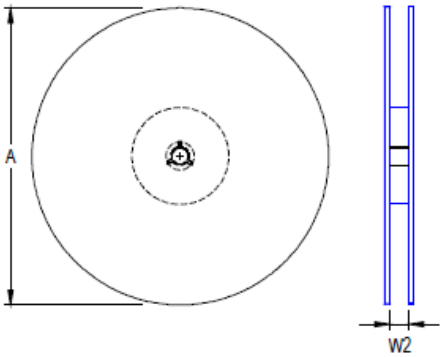
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-28/TSOT-28(FC)/SOT-28	8	0.65	3.60	1.60	1.00	0.45	2.40	±0.10

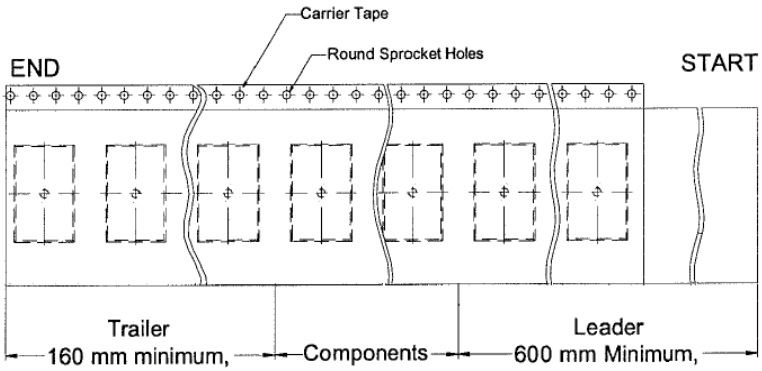
21 Packing Information

21.1 Tape and Reel Data

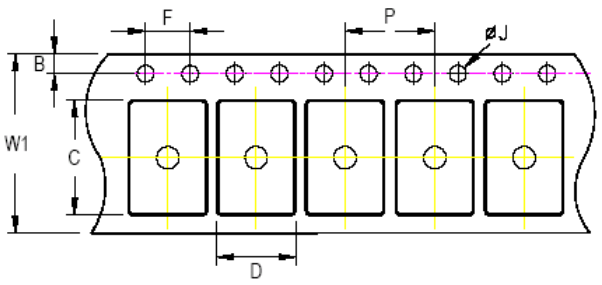
SOT/TSOT-23-6/8:

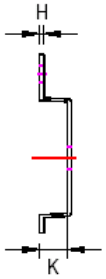






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
TSOT-23-8	8	4	180	7	3,000	160	600	8.4/9.9





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.2mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-8	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
04	2024/1/15	Modify	*General Description on page 1* *Ordering Information on page 2* *Functional Block Diagram on page 4* *Operation on page 7* *Application Information on page 17*
05	2024/5/9	Modify	*Ordering Information on page 2* *Operation on page 7* *Packing Information on page 33, P34, P35*
06	2024/11/26	Modify	*Changed the name of pin 4 to PG.* *General Description on page 1* *Functional Pin Description on page 4* *Operation on page 15 to 18* *Application Information on page 19 to 30* *Packing Information on page 33, 34*

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