ISL22414

Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power, SPI® Bus, 256 Taps

FN6424
Rev 2.00
September 21, 2015

The ISL22414 integrates a single digitally controlled potentiometer (DCP), control logic and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the SPI serial interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR control the position of the wiper. At power-up the device recalls the contents of the DCP's IVR to the WR.

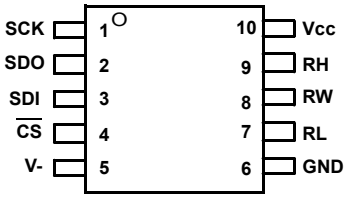
The ISL22414 also has 14 General Purpose non-volatile registers that can be used as storage of lookup table for multiple wiper position or any other valuable information.

The ISL22414 features a dual supply that is beneficial for applications requiring a bipolar range for DCP terminals between V- and VCC.

The DCP can be used as three-terminal potentiometer or as two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Pinout

ISL22414
(10 LD MSOP)
TOP VIEW



Features

- 256 resistor taps
- SPI serial interface with write/read capability
- Daisy Chain Configuration
- Shutdown mode
- Non-volatile EEPROM storage of wiper position
- 14 General Purpose non-volatile registers
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- Wiper resistance: 70Ω typical @ 1mA
- Standby current <2.5µA max
- Shutdown current <2.5µA max
- Dual power supply
  - VCC = 2.25V to 5.5V
  - V- = -2.25V to -5.5V
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40°C to +125°C
- Military temperature range: -55 to +125°C
- 10 Lead MSOP
- Pb-free (RoHS compliant)

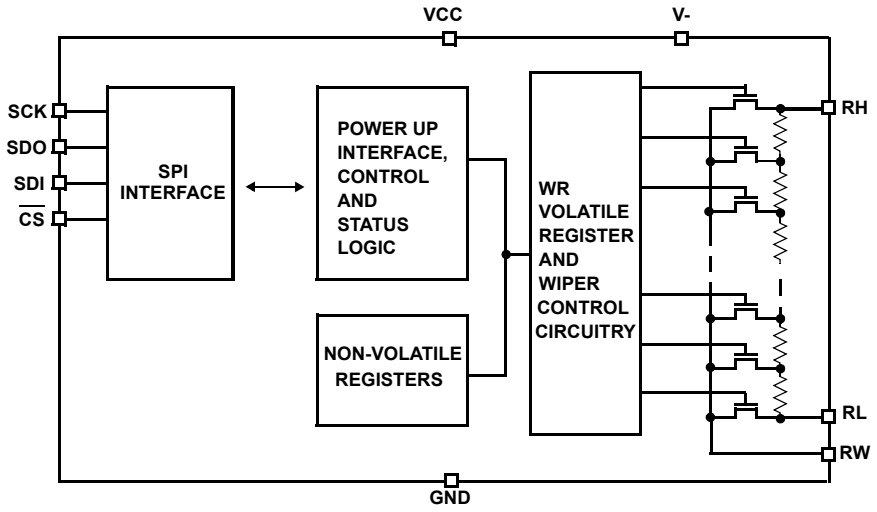
Ordering Information

PART NUMBER (NOTES 1, 2)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL22414TFU10Z	414TZ	100	-40 to +125	10 Ld MSOP	M10.118
ISL22414TFU10Z-TK	414TZ	100	-40 to +125	10 Ld MSOP	M10.118
ISL22414UFU10Z **(No longer available, Recommended Replacement ISL22414TFU10Z-TK)**	414UZ	50	-40 to +125	10 Ld MSOP	M10.118
ISL22414UFU10Z-TK **(No longer available, Recommended Replacement ISL22414TFU10Z-TK)**	414UZ	50	-40 to +125	10 Ld MSOP	M10.118
ISL22414WFU10Z **(No longer available, Recommended Replacement ISL22414TFU10Z-TK)**	414WZ	10	-40 to +125	10 Ld MSOP	M10.118
ISL22414WFU10Z-T7A	414WZ	10	-40 to +125	10 Ld MSOP	M10.118
ISL22414WFU10Z-TK	414WZ	10	-40 to +125	10 Ld MSOP	M10.118
ISL22414WMU10Z **(No longer available, Recommended Replacement ISL22414TFU10Z-TK)**	414WM	10	-55 to +125	10 Ld MSOP	M10.118
ISL22414WMU10Z-T7A **(No longer available, Recommended Replacement ISL22414TFU10Z-TK)**	414WM	10	-55 to +125	10 Ld MSOP	M10.118

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Please refer to TB347 for details on reel specifications.

Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	SCK	SPI interface clock input
2	SDO	Data Output of the SPI serial interface
3	SDI	Data Input of the SPI serial interface
4	$\overline{CS}$	Chip Select active low input
5	V-	Negative power supply pin
6	GND	Device ground pin
7	RL	“Low” terminal of DCP
8	RW	“Wiper” terminal of DCP
9	RH	“High” terminal of DCP
10	VCC	Power supply pin

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
V- . . . . . -6V to 0.3V
Voltage at any DCP pin with Respect to GND . . . . . V- to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A @ +125°C
ESD
Human Body Model 3kV
Machine Model 400V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
10 Lead MSOP 132
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range
Full Industrial . . . . . -40°C to +125°C
Military . . . . . -55°C to +125°C
Power Rating 15mW
V_{CC} . . . . . 2.25V to 5.5V
V- . . . . . -2.25V to -5.5V
Max Wiper Current Iw . . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
R_{TOTAL}	RH to RL Resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RH to RL Resistance Tolerance		**-20**		**+20**	%
	End-to-End Temperature Coefficient	W option		±150		ppm/°C
		U, T option		±50		ppm/°C
V_{RH}, V_{RL}	DCP Terminal Voltage	V_{RH} and V_{RL} to GND	**V-**		**V_{CC}**	V
R_W	Wiper Resistance	RH - floating, V_{RL} = V-, force Iw current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$		70	**250**	Ω
$C_H/C_L/C_W$	Potentiometer Capacitance	See “DCP Macro Model” on page 8		10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from V- to V_{CC}	**-1**	0.1	**1**	µA
VOLTAGE DIVIDER MODE (V- @ RL; V_{CC} @ RH; measured at RW, unloaded)						
INL (Note 9)	Integral Non-linearity Monotonic Over All Tap Positions	W option	**-1.5**	±0.5	**1.5**	LSB (Note 5)
		U, T option	**-1.0**	±0.2	**1.0**	LSB (Note 5)
DNL (Note 8)	Differential Non-linearity Monotonic Over All Tap Positions	W option	**-1.0**	±0.4	**1.0**	LSB (Note 5)
		U, T option	**-0.5**	±0.15	**0.5**	LSB (Note 5)
ZSerror (Note 6)	Zero-scale Error	W option	**0**	1	**5**	LSB (Note 5)
		U, T option	**0**	0.5	**2**	
FSerror (Note 7)	Full-scale Error	W option	**-5**	-1	**0**	LSB (Note 5)
		U, T option	**-2**	-1	**0**	
TC_V (Note 10)	Ratiometric Temperature Coefficient	DCP register set to 80 hex		±4		ppm/°C

Analog Specifications

Over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
f_{cutoff}	-3dB Cut Off Frequency	Wiper at midpoint (80hex) W option (10k)		1000		kHz
		Wiper at midpoint (80hex) U option (50k)		250		kHz
		Wiper at midpoint (80hex) T option (100k)		120		kHz
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 14)	Integral Non-linearity	W option	**-3**	±1.5	**3**	MI (Note 11)
		U, T option	**-1**	±0.3	**1**	MI (Note 11)
RDNL (Note 13)	Differential Non-linearity	W option	**-1.5**	±0.4	**1.5**	MI (Note 11)
		U, T option	**-0.5**	±0.15	**0.5**	MI (Note 11)
Roffset (Note 12)	Offset	W option	**0**	1	**5**	MI (Note 11)
		U, T option	**0**	0.5	**2**	MI (Note 11)
TC_R (Notes 15)	Resistance Temperature Coefficient	DCP register set between 32 hex and FF hex		±50		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = 5.5V, V- = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)		0.36	**1**	mA
		V_{CC} = 2.25V, V- = -2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)		0.13	**0.4**	mA
I_{V-1}	V- Supply Current (volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)	**-1**	-0.18		mA
		V- = -2.25V, V_{CC} = 2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)	**-0.4**	-0.06		mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = 5.5V, V- = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)		1	**2**	mA
		V_{CC} = 2.25V, V- = -2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)		0.3	**0.7**	mA
I_{V-2}	V- Supply Current (non-volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)	**-2**	-1.2		mA
	V- Supply Current (non-volatile write/read)	V- = -2.25V, V_{CC} = 2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)	**-0.7**	-0.4		mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, SPI interface in standby state		0.2	1.5	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, SPI interface in standby state		1	2.5	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, SPI interface in standby state		0.1	1	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, SPI interface in standby state		0.5	2	µA

Operating Specifications Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
I_{V-SB}	V- Current (Standby)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, SPI interface in standby state	-2.5	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, SPI interface in standby state	-4	-3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, SPI interface in standby state	-1.5	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, SPI interface in standby state	-3	-1		µA
I_{SD}	V_{CC} Current (Shutdown)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, SPI interface in standby state		0.2	1.5	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, SPI interface in standby state		1	2.5	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, SPI interface in standby state		0.1	1	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, SPI interface in standby state		0.5	2	µA
I_{V-SD}	V- Current (Shutdown)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, SPI interface in standby state	-2.5	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, SPI interface in standby state	-4	-3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, SPI interface in standby state	-1.5	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, SPI interface in standby state	-3	-1		µA
I_{LkgDig}	Leakage Current, at Pins SCK, SDI, SDO and $\overline{CS}$	Voltage at pin from GND to V_{CC}	**-0.5**		**0.5**	µA
t_{WRT}	DCP Wiper Response Time	$\overline{CS}$ rising edge to wiper new position		1.5		µs
$t_{ShdnRec}$	DCP Recall Time From Shutdown Mode	$\overline{CS}$ rising edge to wiper stored position and RH connection		1.5		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	**1.9**		**2.1**	V
VccRamp	V_{CC} Ramp Rate		**0.2**			V/ms
t_D	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and SPI Interface in standby state			**5**	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		**1,000,000**			Cycles
	EEPROM Retention	Temperature T ≤ +55ºC	50			Years
t_{WC} (Note 16)	Non-volatile Write Cycle Time			12	**20**	ms
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	SCK, SDI, and $\overline{CS}$ Input Buffer LOW voltage		**-0.3**		**0.3*V_{CC}**	V
V_{IH}	SCK, SDI, and $\overline{CS}$ Input Buffer HIGH Voltage		**0.7*V_{CC}**		**V_{CC}+0.3**	V
Hysteresis	SCK, SDI, and $\overline{CS}$ Input Buffer Hysteresis		**0.05*V_{CC}**			V
V_{OL}	SDO Output Buffer LOW Voltage	I_{OL} = 4mA for Open Drain output, pull-up voltage Vpu = V_{CC}	**0**		**0.4**	V

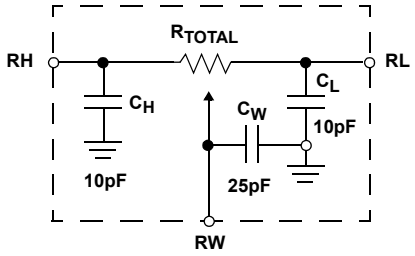
Operating Specifications Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
R_{pu} (Note 17)	SDO Pull-up Resistor Off-chip	Maximum is determined by t_{RO} and t_{FO} with maximum bus load Cb = 30pF, f_{SCK} = 5MHz			**2**	kΩ
Cpin	SCK, SDI, SDO and $\overline{CS}$ Pin Capacitance			10		pF
f_{SCK}	SPI Frequency				**5**	MHz
t_{CYC}	SPI Clock Cycle Time		**200**			ns
t_{WH}	SPI Clock High Time		**100**			ns
t_{WL}	SPI Clock Low Time		**100**			ns
t_{LEAD}	Lead Time		**250**			ns
t_{LAG}	Lag Time		**250**			ns
t_{SU}	SDI, SCK and $\overline{CS}$ Input Setup Time		**50**			ns
t_H	SDI, SCK and $\overline{CS}$ Input Hold Time		**50**			ns
t_{RI}	SDI, SCK and $\overline{CS}$ Input Rise Time		**10**			ns
t_{FI}	SDI, SCK and $\overline{CS}$ Input Fall Time		**10**		**20**	ns
t_{DIS}	SDO output Disable Time		**0**		**100**	ns
t_{SO}	SDO Output Setup Time		**50**			ns
t_V	SDO Output Valid Time		**150**			ns
t_{HO}	SDO Output Hold Time		**0**			ns
t_{RO}	SDO Output Rise Time	R_{pu} = 2k, Cbus = 30pF			**60**	ns
t_{FO}	SDO Output Fall Time	R_{pu} = 2k, Cbus = 30pF			**60**	ns
t_{CS}	CS Deselect Time		**2**			µs

NOTES:

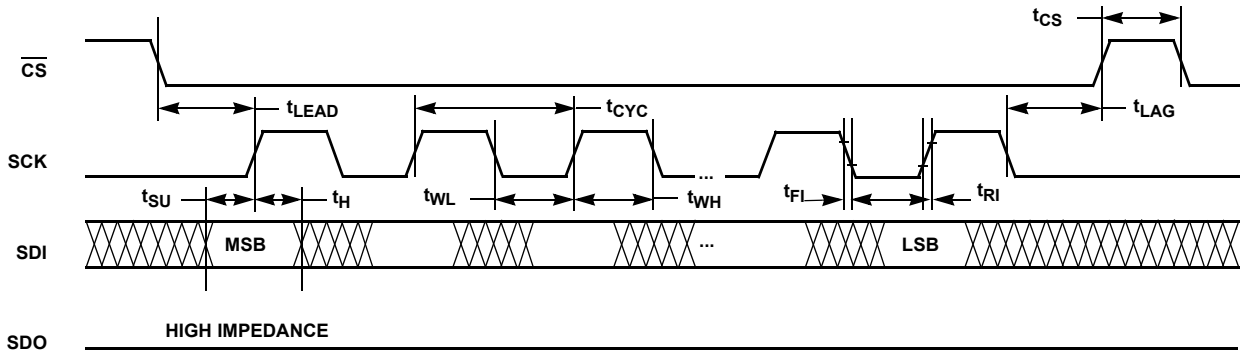
4. Typical values are for T_A = +25°C and 3.3V supply voltage.
5. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
6. ZS error = $V(RW)_0$/LSB.
7. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
8. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
9. INL = $[V(RW)_i – i • LSB – V(RW)]$/LSB for i = 1 to 255
10. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{\Delta T°C}$ for i = 16 to 255 decimal, T = -40°C to +125°C or T = -55°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
11. MI = $|RW_{255} – RW_0|/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
12. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{255}/MI, when measuring between RW and RH.
13. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 1 to 255.
14. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 1 to 255.
15. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{\Delta T°C}$ for i = 16 to 255, T = -40°C to +125°C or T = -55°C to +125°C. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.
16. t_{WC} is the time from the end of a Write sequence of SPI serial interface, to the end of the self-timed internal non-volatile write cycle.
17. R_{pu} is specified for the highest data rate transfer for the device. Higher value pull-up can be used at lower data rates.
18. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DCP Macro Model

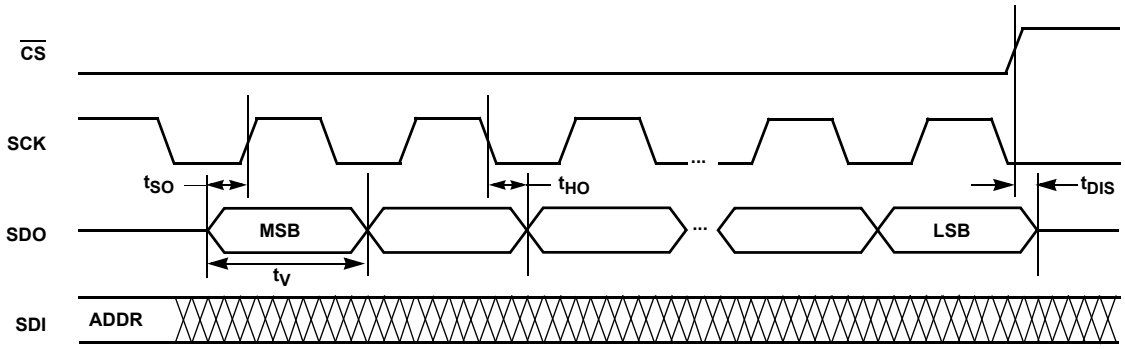


Timing Diagrams

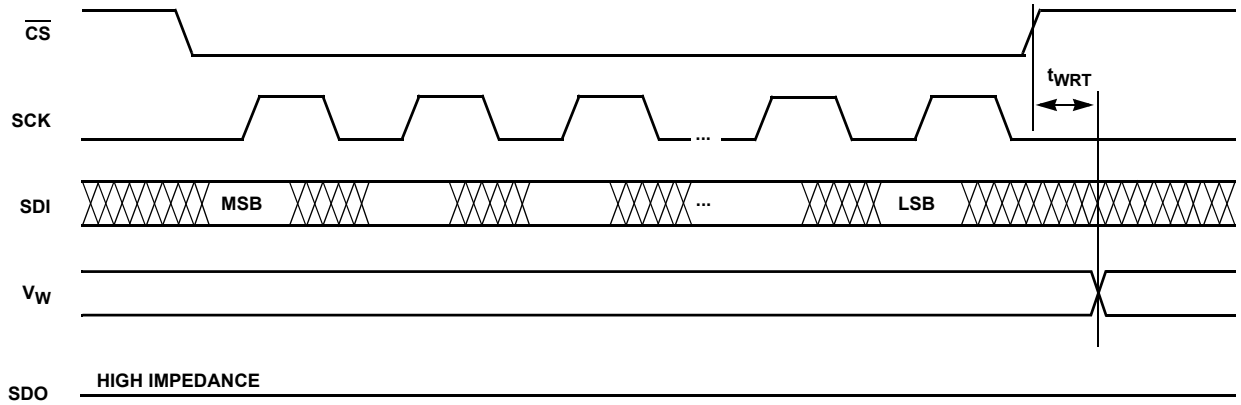
Input Timing



Output Timing



XDCP Timing (for All Load Instructions)



Typical Performance Curves

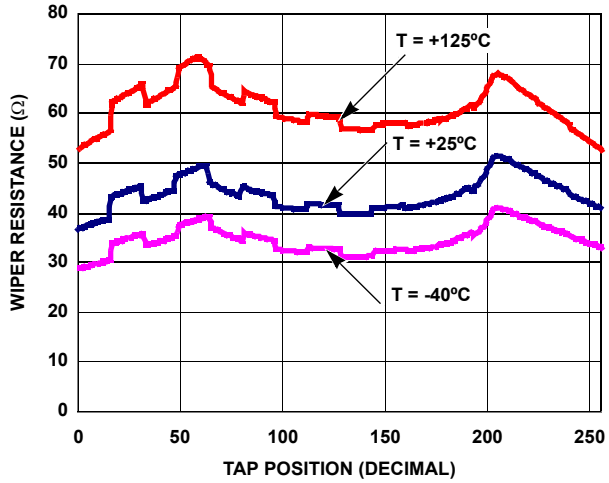


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

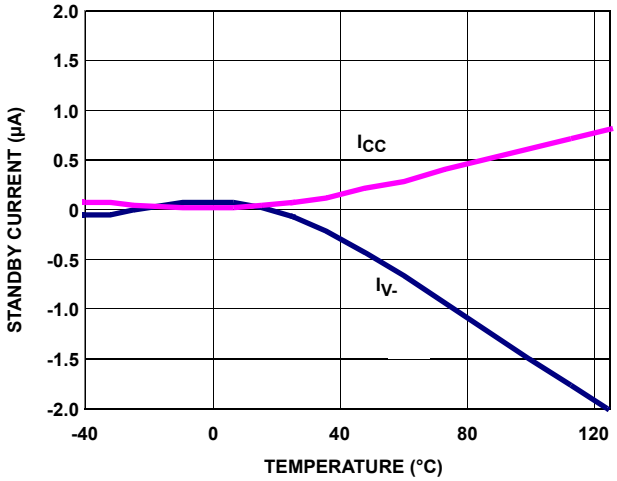


FIGURE 2. STANDBY I_{CC} AND I_{V-} vs TEMPERATURE

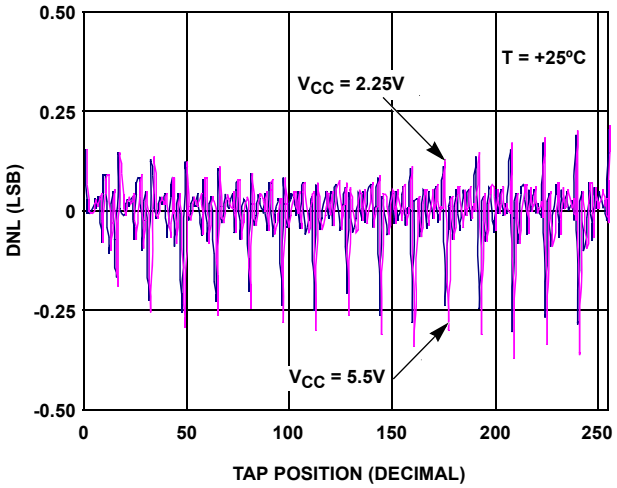


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

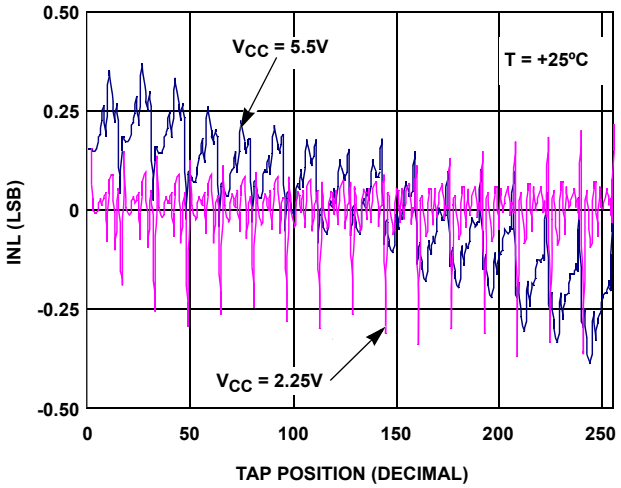


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

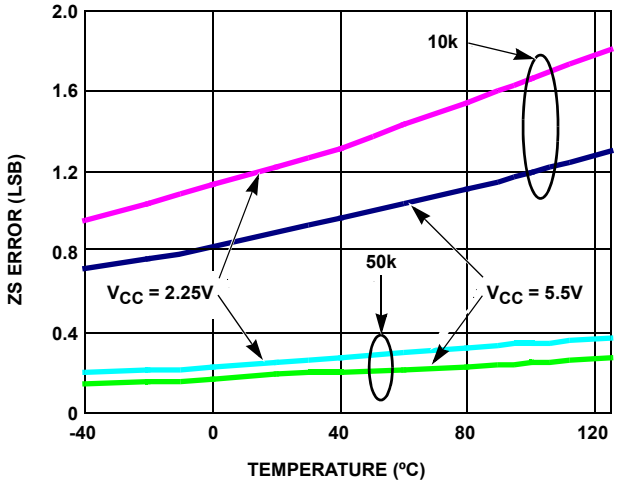


FIGURE 5. ZS ERROR vs TEMPERATURE

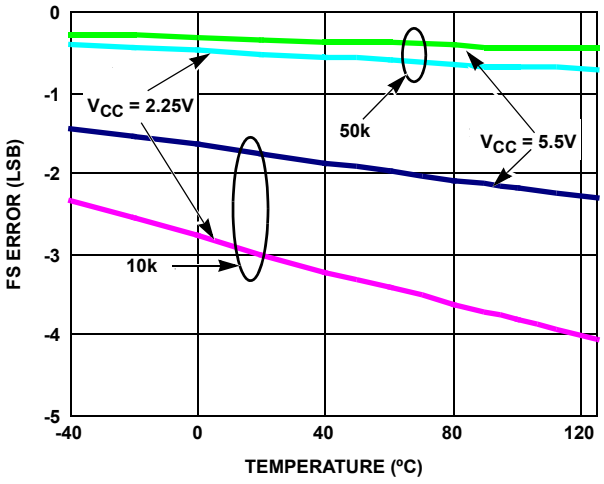


FIGURE 6. FS ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

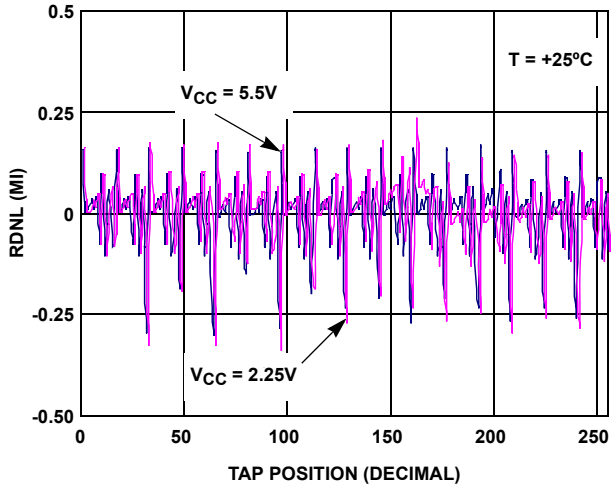


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

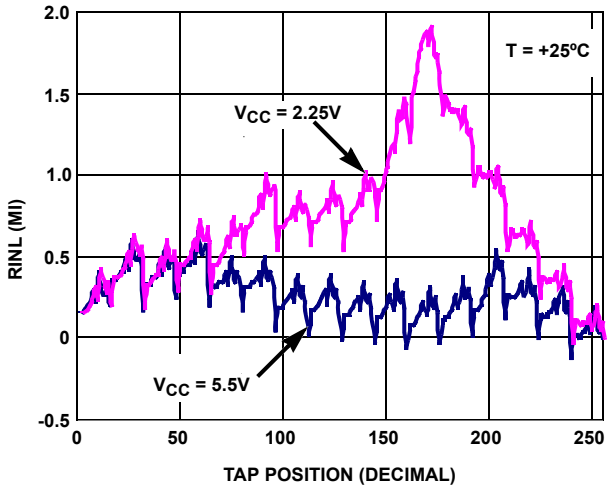


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

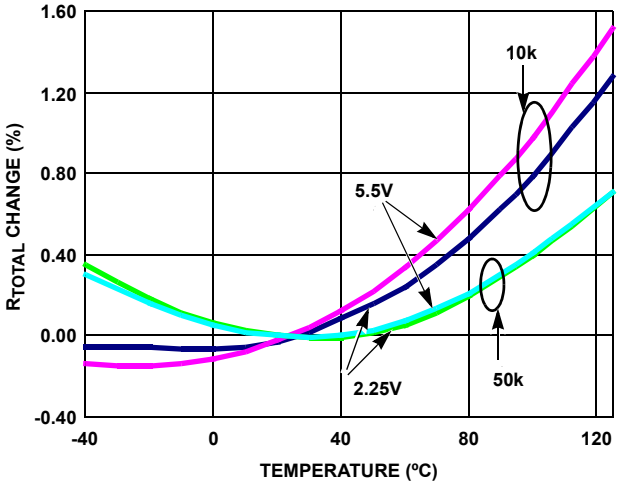


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

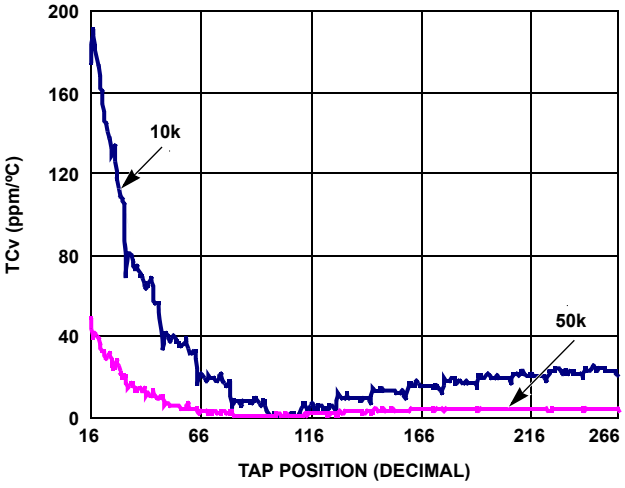


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

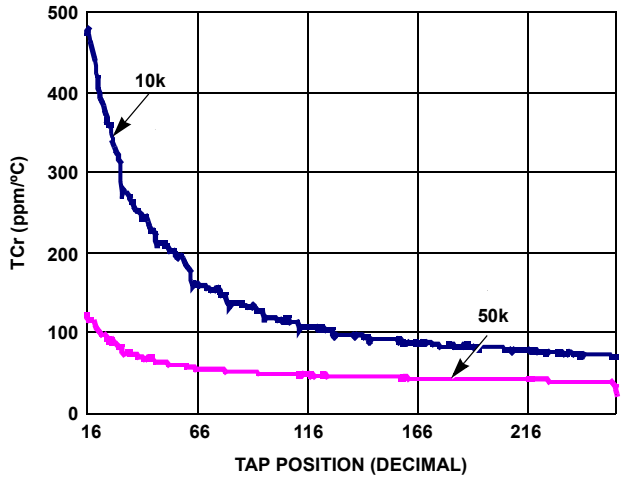


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

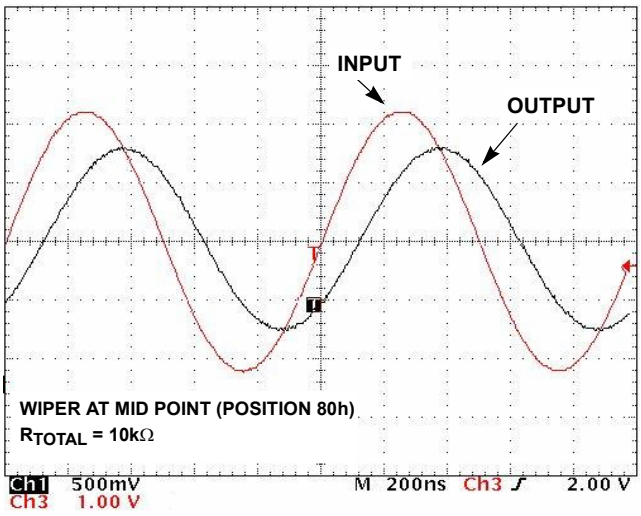


FIGURE 12. FREQUENCY RESPONSE (1MHz)

Typical Performance Curves (Continued)

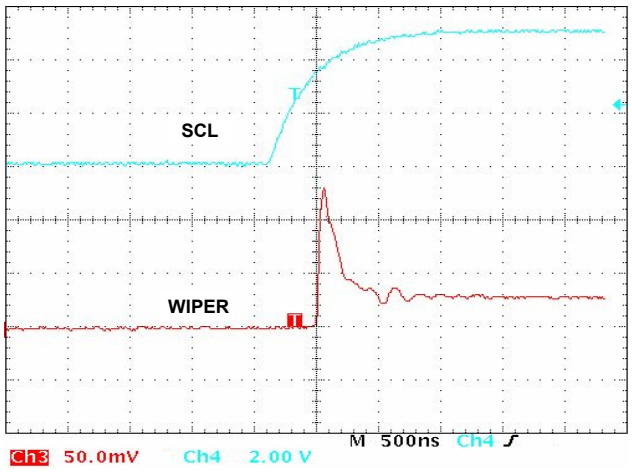


FIGURE 13. MIDSCALE GLITCH, CODE 7Fh TO 80h

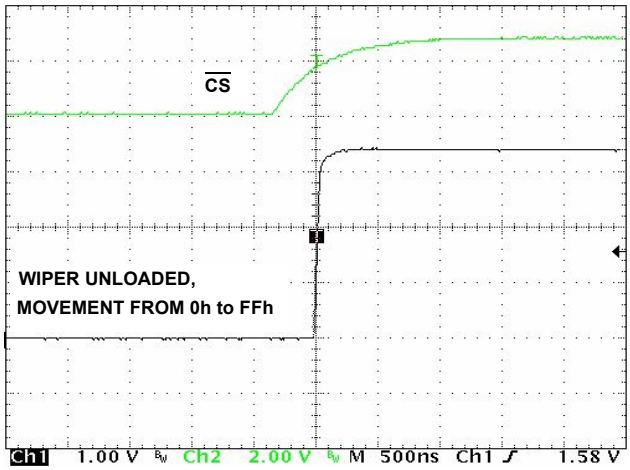


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometer Pins

RH AND RL

The high (RH) and low (RL) terminals of the ISL22414 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 255 decimal, the wiper will be closest to RH, and with the WR set to 0, the wiper is closest to RL.

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

Bus Interface Pins

SERIAL CLOCK (SCK)

This is the serial clock input of the SPI serial interface.

SERIAL DATA OUTPUT (SDO)

The SDO is a serial data output pin. During a read cycle, the data bits are shifted out on the falling edge of the serial clock SCK and will be available to the master on the following rising edge of SCK.

The output type is configured through ACR[1] bit for Push- Pull or Open Drain operation. Default setting for this pin is Push-Pull. An external pull up resistor is required for Open Drain output operation. Note, the external pull up voltage not allowed beyond VCC.

SERIAL DATA INPUT (SDI)

The SDI is the serial data input pin for the SPI interface. It receives device address, operation code, wiper address and data from the SPI remote host device. The data bits are shifted in at the rising edge of the serial clock SCK, while the $\overline{CS}$ input is low.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ LOW enables the ISL22414, placing it in the active power mode. A HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation after power up. When $\overline{CS}$ is HIGH, the ISL22414 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.

Principles of Operation

The ISL22414 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and the SPI serial interface providing direct communication between host and potentiometer and memory. The resistor array is comprised of individual resistors connected in a series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the content of the IVR is recalled and loaded into the WR to set the wiper to the initial position.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[7:0]= 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR[7:0]= FFh), its wiper terminal (RW) is

closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22414 is being powered up, the WR is reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reloaded with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the SPI serial interface as described in the following sections.

Memory Description

The ISL22414 contains one non-volatile 8-bit Initial Value Register (IVR), fourteen non-volatile 8-bit General Purpose (GP) registers, volatile 8-bit Wiper Register (WR), and volatile 8-bit Access Control Register (ACR). The memory map of ISL22414 is in Table 1.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
10	N/A	ACR
F	Reserved	
E	General Purpose	N/A
D	General Purpose	N/A
C	General Purpose	N/A
B	General Purpose	N/A
A	General Purpose	N/A
9	General Purpose	N/A
8	General Purpose	N/A
7	General Purpose	N/A
6	General Purpose	N/A
5	General Purpose	N/A
4	General Purpose	N/A
3	General Purpose	N/A
2	General Purpose	N/A
1	General Purpose	N/A
0	IVR	WR

The non-volatile register (IVR) at address 0, contains initial wiper position and volatile register (WR) contains current wiper position.

The register at address 0Fh is a read-only reserved register. Information read from this register should be ignored.

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
BIT NAME	VOL	$\overline{SHDN}$	WIP	0	0	0	SDO	0

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The $\overline{SHDN}$ bit (ACR[6]) disables or enables Shutdown mode. When this bit is 0, DCP is in Shutdown mode, i.e. DCP is forced to end-to-end open circuit and RW is shorted to RL as shown on Figure 15. Default value of $\overline{SHDN}$ bit is 1.

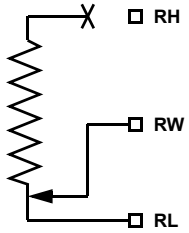


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

Setting $\overline{SHDN}$ bit to 1 is returned wiper to prior to Shutdown Mode position.

The WIP bit (ACR[5]) is a read-only bit. It indicates that non-volatile write operation is in progress. The WIP bit can be read repeatedly after a non-volatile write to determine if the write has been completed. It is impossible to write or read to the WR or ACR while WIP bit is 1.

The SDO bit (ACR[1]) configures type of SDO output pin. The default value of SDO bit is 0 for Push - Pull output. SDO pin can be configured as Open Drain output for some application. In this case, an external pull up resistor is required. See “Applications Information” on page 14.

SPI Serial Interface

The ISL22414 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL22414. SCK and $\overline{CS}$ lines are controlled by the host or master. The ISL22414 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

The SPI protocol contains Instruction Byte followed by one or more Data Bytes. A valid Instruction Byte contains instruction as the three MSBs, with the following five register address bits (see Table 3).

The next byte sent to the ISL22414 is the Data Byte.

TABLE 3. INSTRUCTION BYTE FORMAT

BIT #	7	6	5	4	3	2	1	0
	I2	I1	I0	R4	R3	R2	R1	R0

Table 4 contains a valid instruction set for ISL22414.

There are only sixteen register addresses possible for this DCP. If the [R4:R0] bits are zero, then the read or write is to either the IVR or the WR register (depends of VOL bit at ACR). If the [R4:R0] are 10000, then the operation is on the ACR.

Write Operation

A Write operation to the ISL22414 is a two or more bytes operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW. Then host send a valid Instruction Byte, followed by one or more Data Bytes to SDI pin. The host terminates the write operation by pulling the $\overline{CS}$ pin from LOW to HIGH. Instruction is executed on rising edge of $\overline{CS}$. For a write to address 0, the MSB of the byte at address 10h (ACR[7]) determines if the Data Byte is to be written to volatile or both volatile and non-volatile registers. Refer to “Memory Description” and Figure 16. Note, the internal non-volatile write cycle starts with the rising edge of $\overline{CS}$ and requires up to 20ms. During non-volatile write cycle the read operation to ACR register is allowed to check WIP bit.

Read Operation

A Read operation to the ISL22414 is a four byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW. Then host send a valid Instruction Byte, followed by “dummy” Data Byte, NOP Instruction Byte and another “dummy” Data Byte to SDI pin. The SPI host receives the Instruction Byte (instruction code + register address) and requested Data Byte from SDO pin on the rising edge of SCK during third and fourth bytes respectively. The host terminates the read operation by pulling the $\overline{CS}$ pin from LOW to HIGH (see Figure 17). Reading from the IVR will not change the WR, if its contents are different.

TABLE 4. INSTRUCTION SET

INSTRUCTION SET								OPERATION
I2	I1	I0	R4	R3	R2	R1	R0	
0	0	0	X	X	X	X	X	NOP
0	0	1	X	X	X	X	X	ACR READ
0	1	1	X	X	X	X	X	ACR WRITE
1	0	0	R4	R3	R2	R1	R0	WR, IVR, GP or ACR READ
1	1	0	R4	R3	R2	R1	R0	WR, IVR, GP or ACR WRITE

where X means “do not care”

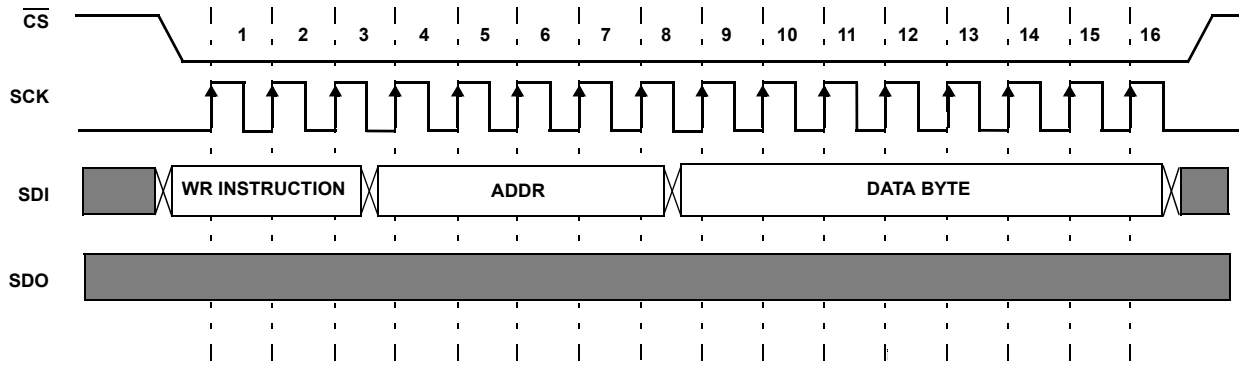


FIGURE 16. TWO BYTE WRITE SEQUENCE

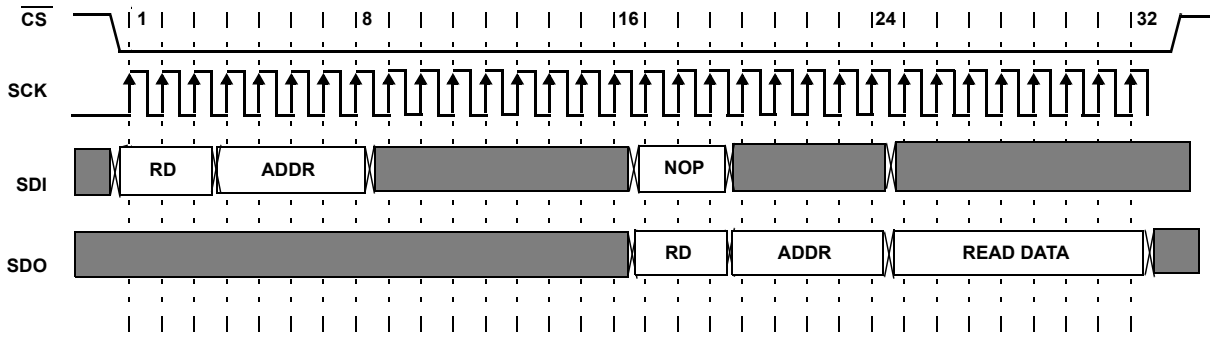


FIGURE 17. FOUR BYTE READ SEQUENCE

Applications Information

Communicating with ISL22414

Communication with ISL22414 proceeds using SPI interface through the ACR (address 10000b), IVR (address 00000b), WR (addresses 00000b) and General Purpose registers (addresses from 00001b to 01110b).

The wiper of the potentiometer is controlled by the WR register. Writes and reads can be made directly to these register to control and monitor the wiper position without any non-volatile memory changes. This is done by setting MSB bit at address 10000b to 1 (ACR[7] = 1).

The non-volatile IVR stores the power up position of the wiper. IVR is accessible when MSB bit at address 10000b is set to 0 (ACR[7] = 0). Writing a new value to the IVR register will set a new power up position for the wiper. Also, writing to this register will load the same value into the corresponding WR as the IVR. Reading from the IVR will not change the WR, if its contents are different.

Daisy Chain Configuration

When application needs more then one ISL22414, it can communicate with all of them without additional $\overline{CS}$ lines by daisy chaining the DCPs as shown on Figure 18. In Daisy Chain configuration the SDO pin of previous chip is connected to SDI pin of the following chip, and each $\overline{CS}$ and SCK pins are connected to the corresponding microcontroller pins in parallel, like regular SPI interface implementation. The Daisy Chain configuration can also be used for simultaneous setting of multiple DCPs. Note, the number of daisy chained DCPs is limited only by the driving capabilities of SCK and $\overline{CS}$ pins of microcontroller; for larger number of SPI devices buffering of SCK and $\overline{CS}$ lines is required.

Daisy Chain Write Operation

The write operation starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N number of two bytes write instructions on SDI line with reversed chain access sequence: the instruction byte + data byte for the last DCP in chain is going first, as shown on Figure 19, where N is a number of DCPs in chain. The serial data is going through DCPs from DCP0 to DCP(N-1) as follow: DCP0 --> DCP1 --> DCP2 --> ... --> DCP(N-1). The write instruction is executed on the rising edge of $\overline{CS}$ for all N DCPs simultaneously.

Daisy Chain Read Operation

The read operation consists two parts: first, send read instructions (N two bytes operation) with valid address; second, read the requested data while sending NOP instructions (N two bytes operation) as shown on Figure 20, and Figure 21.

The first part starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N two bytes read instruction on SDI line with reversed chain access sequence: the instruction byte + dummy data byte for the last DCP in chain is going first, followed by LOW to HIGH transition on $\overline{CS}$ line. The read instructions are executed during second part of read sequence. It also starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N number of two bytes NOP instructions on SDI line and LOW to HIGH transition of $\overline{CS}$. The data is read on every even byte during second part of read sequence while every odd byte contains instruction code + address from which the data is being read.

Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break within an extremely short period of time (<50ns). Two such code transitions are EFh to F0h, and 0Fh to 10h. Note, that all switching transients will settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

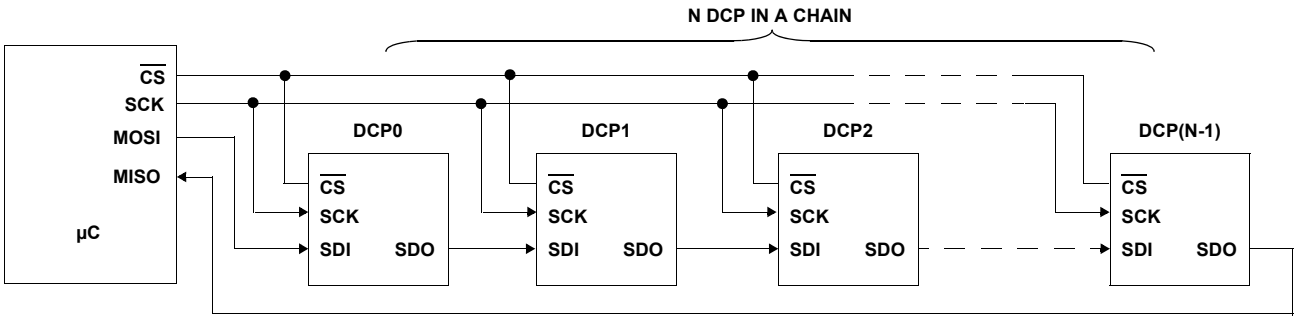


FIGURE 18. DAISY CHAIN CONFIGURATION

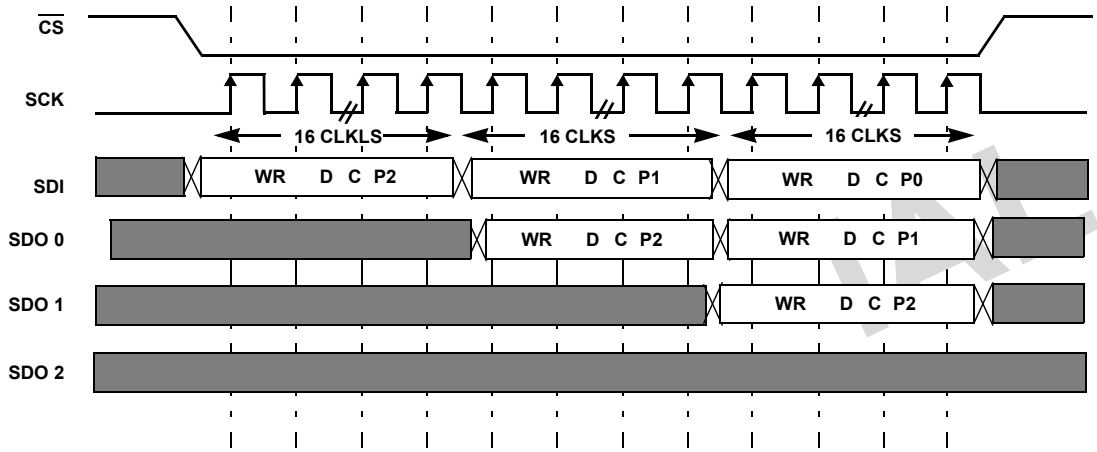


FIGURE 19. DAISY CHAIN WRITE SEQUENCE OF N = 3 DCP

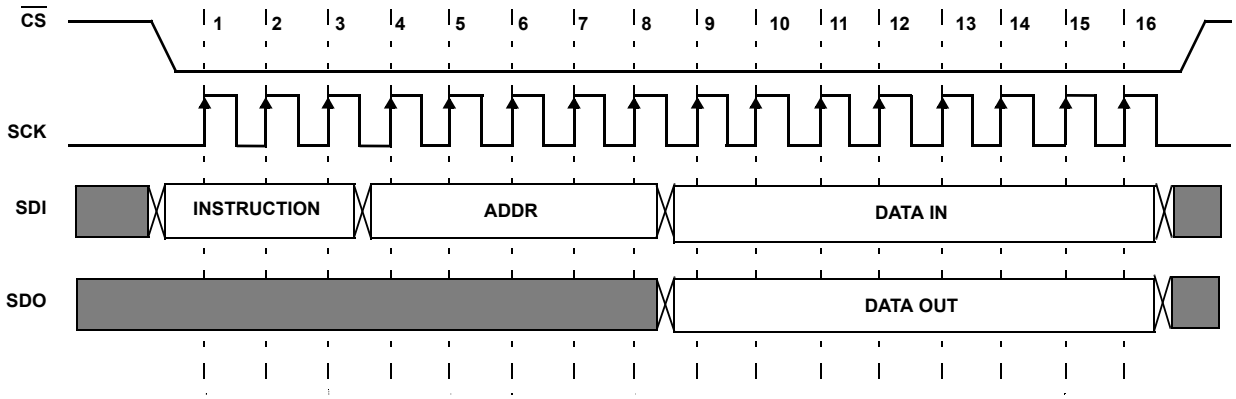


FIGURE 20. TWO BYTE OPERATION

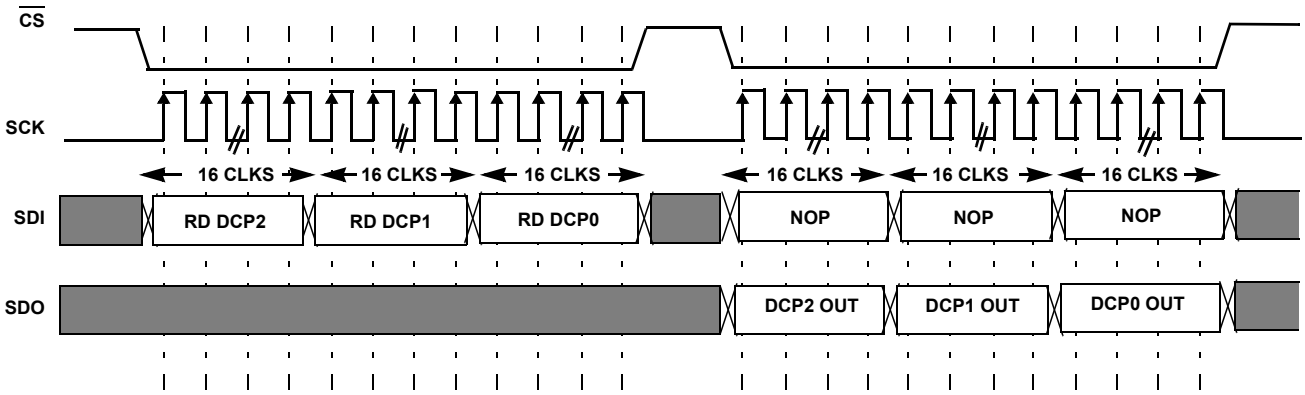


FIGURE 21. DAISY CHAIN READ SEQUENCE OF N = 3 DCP

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 21, 2015	FN6424	Added Rev History beginning with Rev 2 Added About Intersil Verbiage Updated Ordering Information on page 2 Updated POD M8.118 to most current version. Revision change is as follows: Updated to new POD template. Added land pattern

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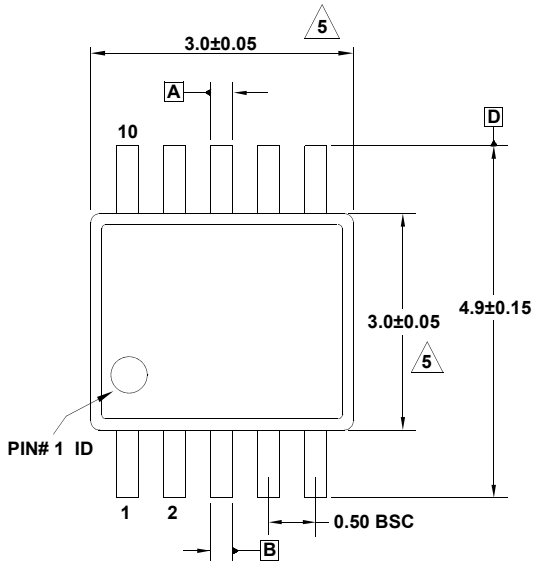
Package Outline Drawing

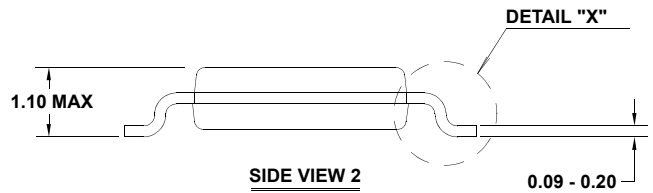
M10.118

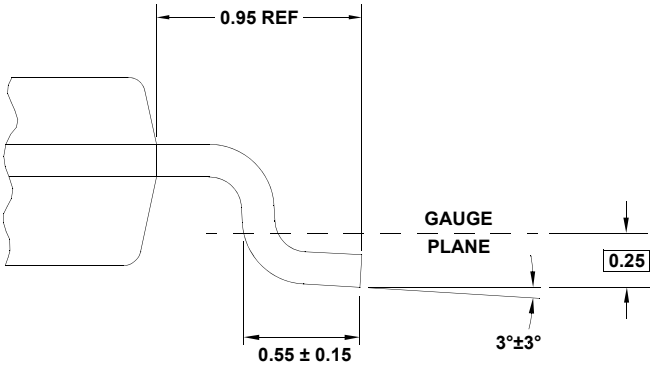
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 4/12

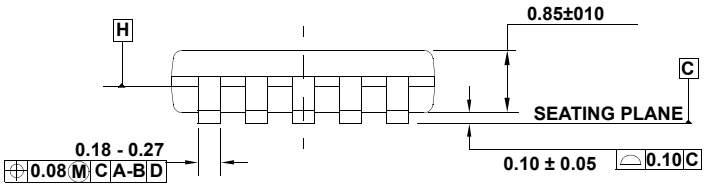


TOP VIEW

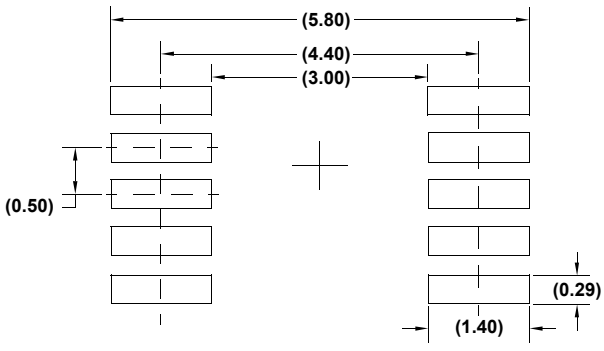




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

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