RVSW013 Dedicated Chip for Bidirectional Controller

2.5-10V ultra-wide voltage input

FEATURES

- Can be Used for PWM Control and Synchronous Rectification
- Synchronous Rectification Supports Both CCM and DCM Modes
- Constant Current Compensation Function under Voltage Limiting Protection Achieves Constant Current Discharge
- SSR Feedback can Enter CCM Mode Under Heavy Load
- SSR Feedback can Enter Intermittent Mode Under Extremely Light Load
- SSR Feedback Features a Direct Optocoupler Interface
- Light Load Analog Frequency Reduction Improves Efficiency and Reduces No-load Power Consumption
- Intelligent Identification for Mode Switching Realizes Bidirectional Control
- Internal Power MOSFET with Resistance as low as 30mΩ
- Programmable Maximum Peak Current Limit
- Programmable Soft-start Time
- Built-in Over-temperature Protection Function
- Shutdown Current in Enable Mode as low as 0.1uA
- Internally Integrated Self-power Supply Circuit
- QFN5x5 Package with Strong Heat Dissipation

APPLICATIONS

- Bidirectional Flyback Converters
- Industrial Power Conversion
- BMS Auxiliary Power Supplies
- Isolated Communication Power Supplies

DESCRIPTION

The RVSW013 is a dedicated controller for bidirectional converters, integrating a power MOSFET with an ultra-low on-resistance of 30mΩ. It supports two operating modes: PWM mode and synchronous rectification mode, in which the internal power MOSFET functions as a synchronous rectifier. An enable pin allows switching between these two modes, enabling seamless bidirectional energy conversion.

In PWM mode, RVSW013 offers optional voltage limiting protection, specifically designed for bidirectional converter applications. It operates in critical conduction mode (CRM) under heavy load conditions and features constant current compensation, which enhances output current regulation. Additionally, the device supports optocoupler-based secondary-side feedback (SSR control), allowing it to enter continuous conduction mode (CCM) during high load conditions, helping to reduce transformer size. Under light-load conditions, the switching frequency decreases with the load, improving efficiency at light load and reducing no-load power consumption.

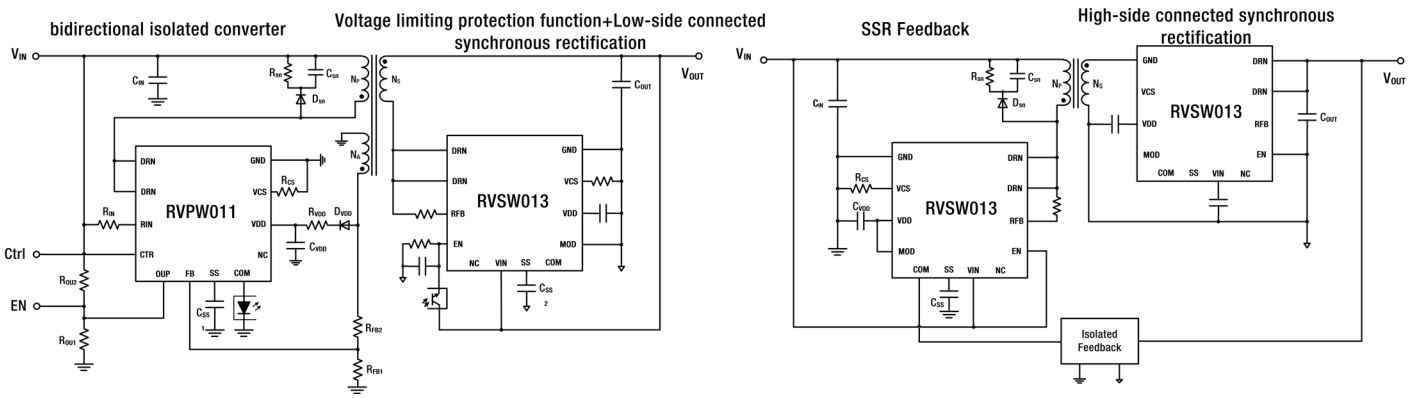
In synchronous-rectification mode, the same internal power MOSFET used in PWM mode operates as the synchronous rectifier. The device supports both CCM and DCM, and is capable of self-powered operation by drawing energy from the drain of the power transistor. This eliminates the need for an auxiliary winding, simplifying both transformer design and the surrounding circuitry.

RVSW013 also includes an intelligent mode detection feature, allowing it to reliably distinguish between PWM mode and synchronous rectification mode. In standby mode, when both function are disabled via the EN pin, the device achieves zero power consumption. With its ultra-low operating voltage range, RVSW013 is ideal for use in bidirectional single-cell battery charging and discharging applications.

Device Information

Part Number	Package	Weight(mg)	Size	SPQ
RVSW013	QFN5x5	61.12	5.0 mm x 5.0 mm	5000

SIMPLIFIED SCHEMATIC



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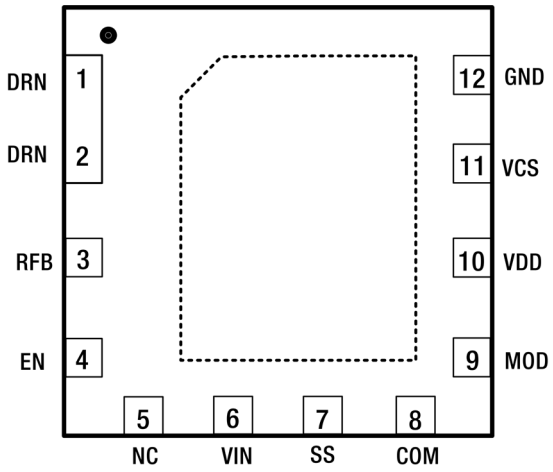
PINOUT AND FUNCTIONS



NAME	QFN12 PIN NUMBER	TYPE	DESCRIPTION
DRN	1,2	O	Pins 1 and 2 are connected together and serve as the drain of the internal LDMOS power transistor.
RFB	3	I	A. Output voltage feedback pin; a resistor is connected between it and VIN. It adjusts the duty cycle by detecting the current through the resistor to achieve voltage limiting protection for the converter output. B. In SSR feedback, it can set the maximum operating frequency and maximum duty cycle.
EN	4	I	Selection pin for synchronous rectification and PWM control. A. When EN is low, the synchronous rectification function is selected. B. When EN is high, the PWM control function is selected.
NC	5	-	Non-functional pin with no electrical connection.
VIN	6	I	A. When VIN<6.4V, VIN to VDD is a linear regulator with a steady-state output of 2.65V; when VIN ≥6.4V, VDD increases with VIN. B. In PWM control, VIN is used as the detection pin for startup and lockout thresholds. C. In voltage limiting protection, the voltage difference between the source (SRC) and the drain (DRN) reflects the converter output voltage.
SS	7	I	Soft-start Pin. An internal 22μA current source flows out of this pin to charge the external soft-start capacitor. The ramp voltage generated by charging controls the duty cycle modulation voltage to rise gradually, ensuring the duty cycle of the converter increases gradually at startup.
COM	8	I	Loop feedback pin for SSR mode.
MOD	9	-	Selection pin for voltage limiting protection and SSR feedback. When EN is high (PWM control mode is selected), the feedback mode is determined by the logic level of MOD: A. If MOD is low, voltage limiting protection is selected, with output voltage feedback through the RFB pin. B. If MOD is high, SSR feedback is selected, with output voltage feedback through the COM pin.
VDD	10	P	Chip power supply port. A linear regulator is integrated between DRN and VDD, allowing power to be taken from DRN.
VCS	11	I	Peak current threshold setting pin. Connecting a resistor (tens of kΩ) to GND can set the range of maximum and minimum peak currents for internal lossless current sampling.
GND	12	P	Chip reference ground. This port is the signal ground for internal control logic and the source of the internal LDMOS power transistor.
EP	-	P	Die attach pad. This pad is bonded to the bottom of the die and can be connected to GND. It should be fully connected to the PCB to facilitate heat dissipation from the die.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN, EN, RFB relative to GND	V_{RIN},V_{OUP},V_{CTR}	-0.3	13	V
VDD relative to GND	V_{DD}	-0.3	7	
DRN relative to GND	V_{DRN}	-1.5	45	
DRN relative to GND(transient<20nS)		-2.5		
Other pins relative to GND	V_{COM}, V_{CS}, V_{SS}, V_{MOD}	-0.3	6	
Maximum junction temperature	T_{JMAX}		150	°C
Storage temperature	T_{stg}	-55	150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	ESD immunity	Human Body Mode (HBM), per ESDA/JEDEC JS-001-2017, (Zap 1 pulse, Interval:>=0.1S)	±2000	V
		Charged Device Model (CDM), per ESDA/JEDEC JS-002-2014	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM is safe for manufacturing under standard ESD control procedures.
(2) JEDEC document JEP157 states that 250-V CDM is safe for manufacturing under standard ESD control procedures.

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
QFN5x5	62.5	3.11	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
Drain voltage of power transistor	V_{DRN}			40	V
VIN input voltage	V_{IN}	2.5		10	
External resistor on VCS	R_{CS}	10			kΩ
Operating ambient temperature	T_A	-40		125	°C
Thermal resistance, junction to ambient	$R_{\theta JA}$		62.5		°C/W
Thermal resistance, junction to case	Ψ_{JT}		3.1		°C/W

Electrical Characteristics

Unless otherwise specified, the following parameters were measured under the condition of V_{DD}= 5V , V_{IN}=5V, V_{DRN}=12V, and temperature=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ONSYN)}$	VDD Startup Voltage During Synchronous Rectification	DRN=EN=0, V_{DD} Voltage Rise	3.37	3.55	3.73	V
$V_{DD(ONPWM)}$	VDD Startup Voltage in PWM Mode	VIN=EN=2.5V, V_{DD} Voltage Rise	1.5	1.8	2.1	V
$I_{VDD(OFFSYN)}$	VDD Latch Voltage During Synchronous Rectification	DRN=EN=0, V_{DD} Voltage Drop	3.12	3.3	3.48	V
$I_{VDD(OFFPWM)}$	VDD Latch Voltage in PWM Mode	VIN=EN=2.5V, V_{DD} Voltage Drop	1.3	1.61	1.9	V
$I_{VDD(REG1)}$	Steady-State Output from VIN to VDD		2.5	2.65	2.8	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD(REG2)}$	Steady-State Output from DRN to VDD	VDD connected to GND via a 10k resistor	4.4	5.2	6	V
$V_{DD(CLAMP)}$	VDD Clamp Voltage	V_{EN}=0V, the input current of VDD is 0.2mA	5.8	6.5	7	V
$I_{VDD(Q)}$	VDD Static Power Consumption	Voltage Clamping Protection Mode	1.1	1.6	2.1	mA
VIN						
$V_{IN(ON)}$	VIN Startup Voltage	V_{IN} Voltage Rise	1.7	2.1	2.4	V
$V_{IN(OFF)}$	VIN Latch Voltage	V_{IN} Voltage Drop	1.7	1.93	2.2	V
$V_{IN(LDO)}$	Maximum Input Range of VIN-to-VDD Linear Regulation	VDD gradually rise from the steady-state voltage	5.7	6.4	7.0	V
VCS						
$V_{CS(MAX1)}$	Maximum Threshold Initial Voltage Under Voltage Limiting Protection	R_{CS}=22kΩ	1.1	1.17	1.25	V
$V_{CS(MAX2)}$	Maximum Threshold Voltage in SSR Mode	R_{CS}=22kΩ	1.22	1.3	1.38	V
$V_{CS(MIN1)}$	Minimum Threshold Voltage Under Voltage Limiting Protection	R_{CS}=22kΩ	480	520	560	mV
$V_{CS(MIN2)}$	Minimum Threshold Voltage in SSR Mode	R_{CS}=22kΩ	250	300	350	mV
K_{CS}	Proportional Coefficient Between Power Transistor Peak Current and VCS Current		0.8×10^5	10^5	1.2×10^5	A/A
RFB						
$I_{RFB(REG)}$	Steady-State Current		94	100	106	µA
A_V	EA Low-Frequency Gain			1400		V/V
$t_{D(SAMP)}$	Sampling Delay Time		200	300	400	nS
$f_{MAX(RFB)}$	Maximum Operating Frequency of Voltage Limiting Protection Function		320	360	400	kHz
$f_{MIN(RFB)}$	Minimum Operating Frequency of Voltage Limiting Protection Function		1.0	1.4	1.8	kHz
$t_{ON(MAX)}$	Maximum On-time of Voltage Limiting Protection Function		11.1	12.5	13.8	uS
COM						
$f_{MAX1(SSR)}$	Selectable Maximum Operating Frequency I in SSR Mode	V_{EN}=V_{MOD}=5V, V_{RFB}=V_{IN}	320	360	400	kHz
$f_{MAX2(SSR)}$	Selectable Maximum Operating Frequency II in SSR Mode	V_{EN}=V_{MOD}=5V, RFB floating	180	200	220	kHz
$D_{MAX1(SSR)}$	Selectable Maximum Duty Cycle I in SSR Mode	V_{EN}=V_{MOD}=5V, V_{RFB}=V_{IN}	80	84	88	%
$D_{MAX2(SSR)}$	Selectable Maximum Duty Cycle II in SSR Mode	V_{EN}=V_{MOD}=5V, RFB floating	85	91	96	%
D_{MIN}	Minimum Duty Cycle				0	%
$V_{COM(SKIP)}$	Threshold Voltage for Intermittent Operation Mode	V_{COM} gradually rises	0.6	0.77	1.1	V
$V_{COM(HYS)}$	Hysteresis Voltage for Intermittent Operation Mode	V_{COM} gradually decreases		15		mV
$V_{COM(OPEN)}$	COM Pin Open-Circuit Voltage		3.8	4.2	4.5	V
t_{OVLD}	Overload Protection Timing			3×2^{12}		T_{SW}
$t_{SLEEP(SR)}$	Self-recovery Protection Mode Sleep Time		520	750	980	mS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{COM(OLP)}$	Open-loop Protection Threshold Voltage		3.8	4.2	4.5	V
I_{COM}	COM Pin Short-circuit Current	V_{COM}=0V	1.12	1.4	1.68	mA
$V_{COM(DMAX)}$	COM Pin Voltage at Maximum Duty Cycle		3.5	3.8	4.1	V
EN						
$V_{EN(H)}$	EN High-level Voltage	V_{EN} gradually rises	0.66	0.96	1.26	V
$V_{EN(L)}$	EN Low-level Voltage	V_{EN} gradually decreases	0.57	0.87	1.17	V
$R_{EN(IN)}$	EN Input Resistance		130	185	240	kΩ
MOD						
$V_{MOD(H)}$	MOD High-level Voltage	V_{MOD} gradually rises	0.66	0.96	1.26	V
$V_{MOD(L)}$	MOD Low-level Voltage	V_{MOD} gradually decreases	0.57	0.87	1.17	V
$R_{MOD(IN)}$	MOD Input Resistance		350	500	650	kΩ
SS						
$V_{SS(OPEN)}$	Soft-start Pin Open-circuit Voltage		3.8	4.2	4.5	V
I_{SS}	External Soft-start Current		18	22	36	μA
$R_{SS(DIS)}$	Soft-start Bleed Resistor		138	173	208	Ω
DRN						
$R_{DS(ON)}$	Power Transistor On-resistance	I_{DS}=4A, T=25°C		30		mΩ
		I_{DS}=4A, T=125°C		45		mΩ
$V_{th(on)}$	Synchronous Rectification Turn-on Threshold		-116	-85	-58	mV
$V_{th(off)}$	Synchronous Rectification Turn-off Threshold		-4	-1	2	mV
T_{B_ON}	Synchronous Rectification Detection Blanking Time		300	380	460	nS
$t_{ON(MIN)}$	Minimum On-time	VCS is left floating. The drain is connected to a 20Ω pull-up resistor with a pull-up voltage of 20V		200		nS
Other Protection Functions						
T_{SHDN}	Over-temperature Protection Threshold	In PWM mode	145	165	175	°C
$T_{SHDN(HYS)}$	Over-temperature Protection Hysteresis	In PWM mode		20		°C

Typical Characteristics

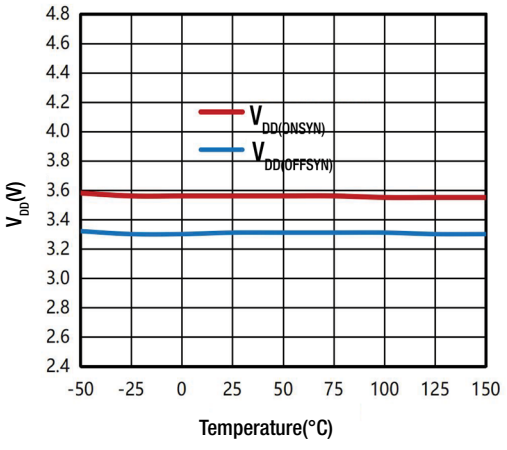


Fig. 1 Curves of $V_{DD(ONSYN)}$ & $V_{DD(OFFSYN)}$ vs. Temperature

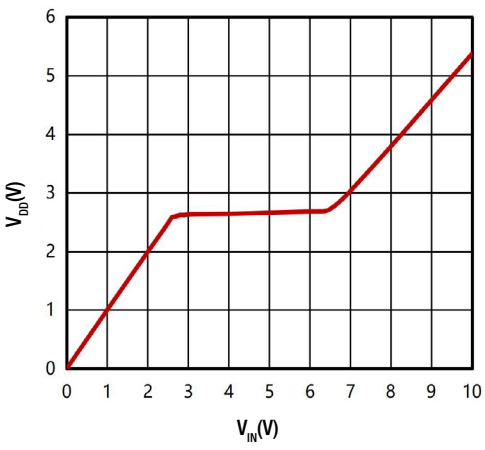


Fig. 2 Curve of V_{DD} vs. V_{IN}

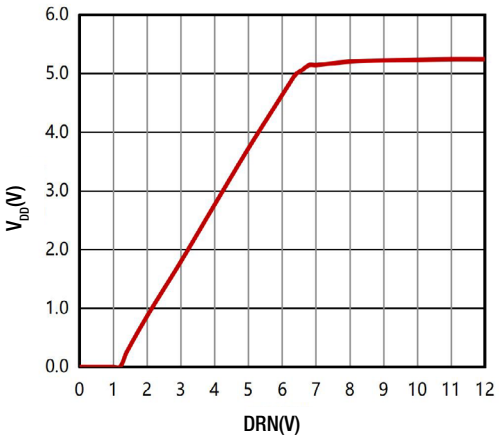


Fig. 3 Curve of V_{DD} vs. DRN
(VDD is connected to GND via a 10k resistor)

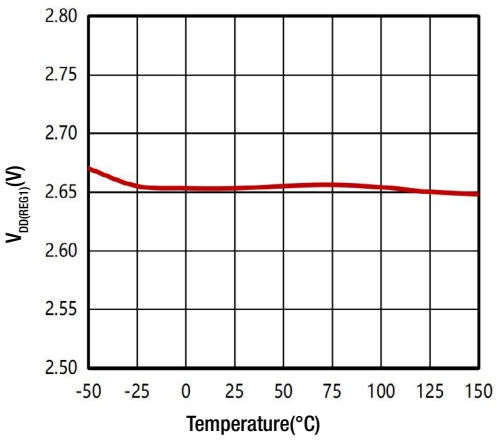


Fig. 4 Curve of $V_{DD(REG1)}$ vs. Temperature

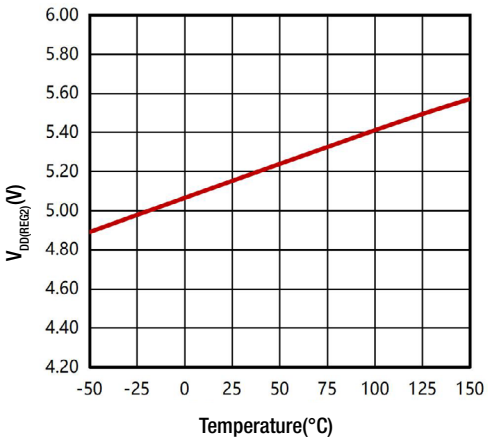


Fig. 5 Curve of $V_{DD(REG2)}$ vs. Temperature

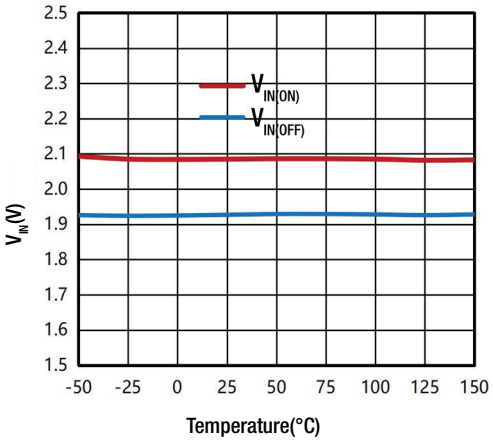


Fig. 6 Curves of $V_{IN(ON)}$ and $V_{IN(OFF)}$ vs. Temperature

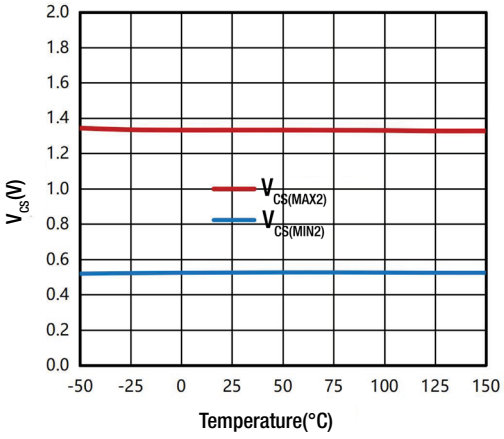


Fig. 7 Curves of $V_{CS(MAX2)}$ and $V_{CS(MIN2)}$ vs. Temperature

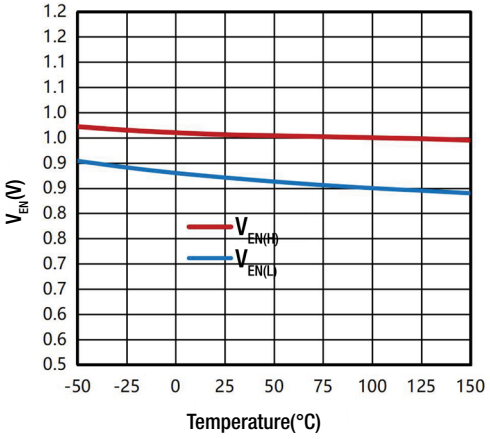


Fig. 8 Curves of $V_{EN(H)}$ and $V_{EN(L)}$ vs. Temperature

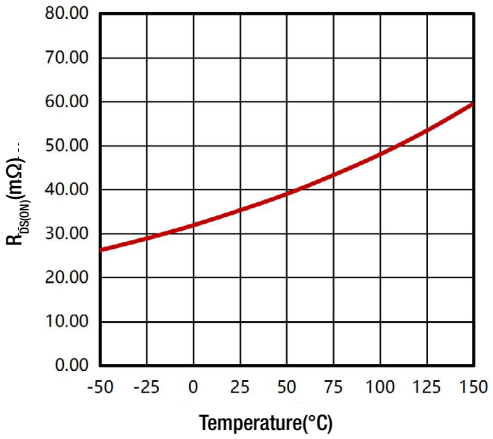


Fig. 9 Curve of $R_{DS(ON)}$ vs. Temperature

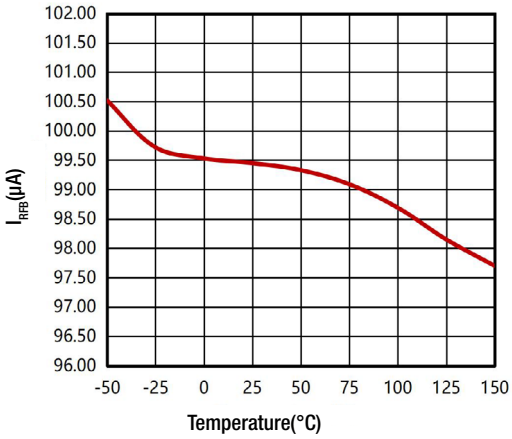


Fig. 10 Curve of I_{RFB} vs Temperature

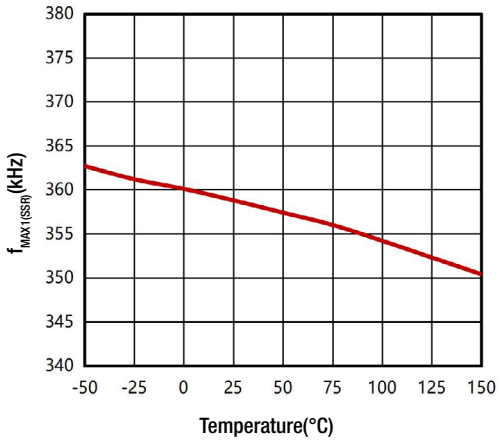


Fig. 11 Curve of $f_{MAX1(SSR)}$ vs. Temperature

DETAILED DESCRIPTION

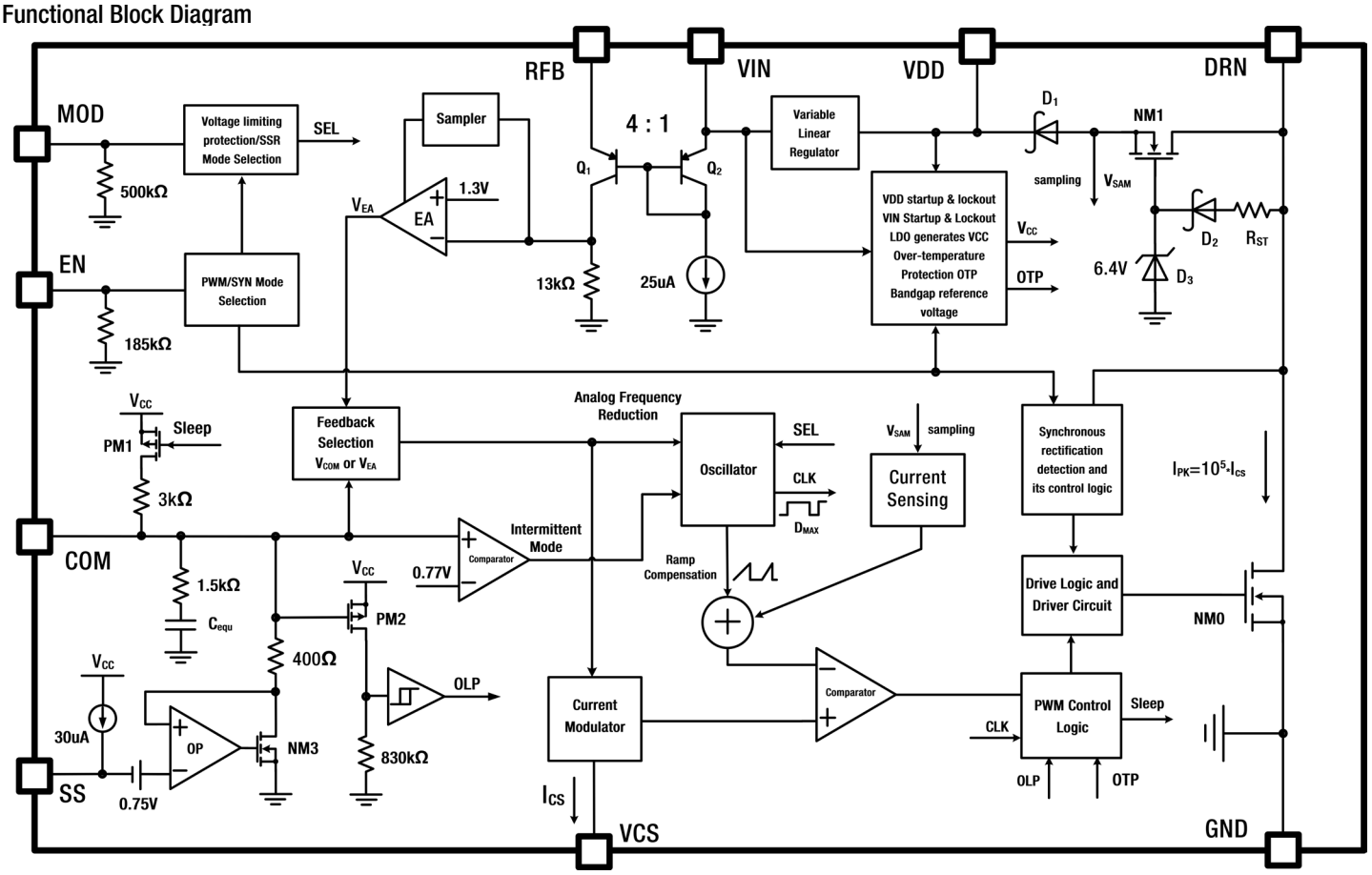
Overview

The RVSW013 is a dedicated controller IC for bidirectional converters, capable of operating in either PWM mode or synchronous rectification mode. Mode selection is achieved by adjusting the logic voltage on the mode control pin, enabling seamless bidirectional operation. During discharge, RVSW013 functions as a PWM converter, while during charging, it operates as a synchronous rectifier.

The device integrates a low-resistance nLDMOS power transistor with an on-resistance as low as 30mΩ, which serves as either the main switching device in PWM mode or as the synchronous rectifier in rectification mode (SR). The peak current in PWM mode can be configured via the VCS pin, offering flexibility in current regulation. With a high level of integration, RVSW013 simplifies external circuitry and reduces component count. Its ultra-low operating voltage range makes it particularly well-suited for bidirectional charging and discharging of single-cell batteries.

In PWM mode, RVSW013 supports two feedback options: voltage limiting protection and optocoupler-based secondary-side regulation (SSR). The voltage limiting function, designed specifically for bidirectional topologies, operates in boundary conduction mode (BCM) under heavy load and includes constant current compensation to enhance current regulation accuracy. Alternatively, the SSR feedback mode enables operation in continuous conduction mode (CCM) under high-load conditions, helping to reduce transformer size. In both feedback configurations, the device supports load-dependent frequency modulation, decreasing the switching frequency under light-load conditions. This improves light-load efficiency and significantly reduces no-load power consumption.

Functional Block Diagram



Feature Description

Dual-path Self-power Supply and Startup via VDD, VIN, and DRN

The RVSW013 features an internal control circuit powered through the VDD pin, supported by two integrated linear regulators that charge the external VDD capacitor. The first regulator path is a low-dropout variable linear regulator connected from VIN to VDD. When VIN < 6.4V (typical), the regulator functions in low-dropout mode, maintaining a steady-state VDD output of 2.65V. When VIN ≥ 6.4V, the VDD voltage increases proportionally with VIN, as illustrated in Figure 2 Typical Characteristic Curves. The second regulator path operates from DRN to VDD, using a Zener-diode-clamped gate voltage to control a startup transistor. This path provides a steady-state VDD output of 5.2V, with the VDD-DRN relationship shown in Figure 3.

In PWM mode, RVSW013 monitors the VIN voltage to determine startup and undervoltage lockout conditions. When VIN exceeds $V_{IN(ON)}$, the DRN pin is allowed to output drive pulses. If VIN drops below $V_{IN(OFF)}$, an undervoltage lockout is triggered and pulse output is disabled. Although the steady-state output from the VIN-based regulator is limited to 2.65V, it reliably supplies the minimum VDD voltage required by the PWM control circuit, even at very low VIN levels (e.g., 2.2V typical). As PWM operation progresses, the DRN voltage rises, enabling the second regulator to further increase VDD. This elevated VDD not only satisfies the control circuit's voltage needs but also helps reduce the on-resistance of the internal power transistor. When the VDD voltage exceeds 2.65V, the first regulator naturally ceases operation, preventing backflow to VIN.

In synchronous rectification mode, the device instead monitors VDD for startup and undervoltage lockout. When VDD exceeds $V_{DD(ONSYN)}$, synchronous rectification is enabled. If VDD falls below $V_{DD(OFFSYN)}$, an undervoltage lockout condition disables the synchronous rectifier. According to flyback converter operation principles, the DRN voltage platform, during the transformer's excitation phase, charges VDD. This mechanism allows VDD to exceed the startup threshold even when VIN is low, ensuring proper synchronous rectification even at very low converter output voltages. Once VDD surpasses 2.65V, the first linear regulator is automatically disabled, and the charge on VDD is isolated from VIN, avoiding unwanted backflow.

Power Transistor Peak Current Setting

In PWM mode, the RVSW013 monitors the on-voltage drop across the internal power MOSFET (NM0) at the source of the startup transistor (NM1). This voltage is mirrored to a current-sampling transistor, which is of the same type as NM0 but features a higher on-resistance. An operational amplifier is used to drive this mirroring process, thereby generating a current in the sampling transistor that is proportional to the peak current IPK flowing through NM0.

This sampled current is then compared with a modulation current produced by the current modulator circuit connected to the VCS pin. The modulation current I_{CS} is determined by the voltage at the VCS pin and the value of the external resistor R_{CS}. The result of this comparison defines the PWM pulse width, enabling accurate peak current control. Internally, the operating current of the power MOSFET is scaled to be 100,000 times the modulation current I_{CS}, ensuring precise current-mode regulation and high current-sensing accuracy with minimal power loss.

The value of R_{CS} can be calculated using the following formula:

$$R_{CS} = 10^5 \times \frac{V_{CS(MAX)}}{I_{PK}}$$

In SSR mode, the maximum threshold voltage at the VCS pin, $V_{CS(MAX)}$, is fixed at a typical value of 1.3V. In voltage limiting protection mode, this threshold varies with the input voltage V_{IN}, as illustrated in Figure 10 Typical Characteristic Curves. When V_{IN} is below 4.8V, $V_{CS(MAX)}$ increases linearly with V_{IN}, approximately following the formula $V_{CS(MAX)}$= 1.17V + 0.1×V_{IN}. When V_{IN} exceeds 4.8V, $V_{CS(MAX)}$remains nearly constant. I_{PK} denotes the maximum peak current of the primary winding in the flyback converter.

Voltage Limiting Protection Function - RFB Pin

Mode Selection: To enable the voltage limiting protection function, two conditions must be met. First, the voltage at the EN pin must exceed the high-level threshold $V_{EN(H)}$, indicating that the EN pin is driven by a high logic level and thereby selecting the PWM operating mode. At the same time, the voltage at the MOD pin must be lower than $V_{MOD(L)}$, confirming that the MOD pin is pulled low to activate the voltage limiting protection function. When both conditions are satisfied, the converter enters a mode in which output voltage limiting is enabled via the RFB pin.

Output Voltage Sampling: The voltage limiting protection operates based on the principle that the voltage across the transformer's primary winding during the demagnetization phase reflects the output voltage of the flyback converter. By sampling this voltage, the converter can estimate and limit the output voltage. A sampling resistor RFB is connected between the RFB pin and DRN. During the demagnetization phase, the RFB pin is clamped to V_{IN}, so the voltage across RFB corresponds to the voltage across the transformer's main winding. The resulting current through RFB generates a voltage VFB across the internal 13kΩ resistor inside the RVSW013, enabling accurate voltage sensing. The waveform of VFB is illustrated in Figure 12.

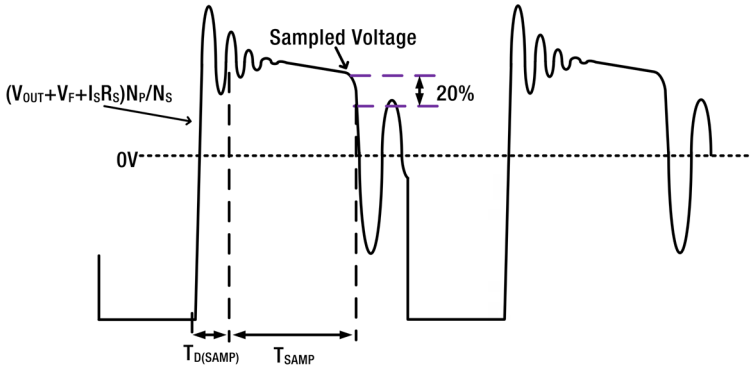


Fig. 12

RVSW013 internally compares the sampled voltage VFB against a 1.3V reference using a differential amplifier. The resulting amplified output dynamically adjusts the duty cycle of the power switch, thereby regulating the converter's operation. This control loop stabilizes the inflection point of the VFB waveform-occurring at the end of the transformer demagnetization phase-at precisely 1.3V. Under these steady-state conditions, the current flowing through the external RFB resistor is maintained at 100μA. It can be calculated as:

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_P}{N_S} = 100\mu A \times R_{FB}$$

$$V_{OUT} = 100\mu A \times \frac{N_S}{N_P} \times R_{FB} - V_F - I_S R_S$$

Output Voltage Regulation and Sampling Accuracy: Where N_P and N_S are the turns of the transformer's primary and secondary windings, respectively, RFB is the sampling resistor connected between the RFB and DRN pins, V_F is the forward voltage drop of the output diode, I_S is the secondary-side output current, and R_S represents the total resistance in the transformer's secondary output loop. As indicated in the voltage calculation formula, the product $I_S R_S$ influences the output load regulation and should be minimized for improved performance. To mitigate this effect, the RVSW013 samples the voltage VFB at the end of the demagnetization phase while operating in Boundary Conduction Mode (BCM) or Discontinuous Conduction Mode (DCM), where I_S=0. This ensures that the output voltage is no longer influenced by $I_S R_S$, thus significantly improving the accuracy of the sampled voltage.

RVSW013 determines the end of the demagnetization phase by detecting a 20% drop in the sampled voltage VFB. Upon detection, the sampler latches the output of the internal differential amplifier (EA). Due to the intentional delay in the EA's response, the latched value effectively captures the voltage just before the drop, ensuring precise sampling. During the initial demagnetization stage, resonance between the transformer's leakage inductance and parasitic capacitance can introduce significant fluctuations in VFB. To avoid incorrect sampling during this period, the sampler includes a built-in sampling delay $T_{D(SAMP)}$, during which it remains inactive. Once this delay elapses, the sampler becomes active for a time window T_{SAMP}, during which the peak-to-peak resonance ripple must be limited to 80% of the sampling platform voltage (approximately 260mV).

Note: Connecting a filter capacitor between the RFB pin and GND is not recommended, as it can distort the VFB waveform, degrading output voltage accuracy-especially at switching frequencies in the hundreds of kHz. Additionally, under light-load conditions, the short demagnetization time may cause oscilloscope probe parasitics to distort VFB, leading to incorrect output voltage readings.

Current Modulator: The duty-cycle modulation voltage V_{EA} generates a pulse-width modulated current across the external resistor connected to the VCS pin, as illustrated in Figure 13, which shows the relationship between V_{EA}, V_{CS}, and switching frequency f_{DRN}. The V_{CS} voltage tracks changes in V_{EA}, producing a corresponding current through the external resistor of the current modulator. This current controls the peak current of the power transistor NM0, thus regulating the converter's output voltage. When V_{EA} exceeds 2.1V, V_{CS} reaches its maximum threshold of $V_{CS(MAX)}$=1.17V+0.1×V_{IN}, thereby limiting the peak current of NM0. To ensure sufficient demagnetization time for accurate output voltage sampling, the minimum V_{CS} is clamped at $V_{CS(MIN)}$=520mV, which corresponds to the minimum energy transfer per switching cycle. Under no-load conditions, additional dummy loads may be required to prevent output voltage overshoot.

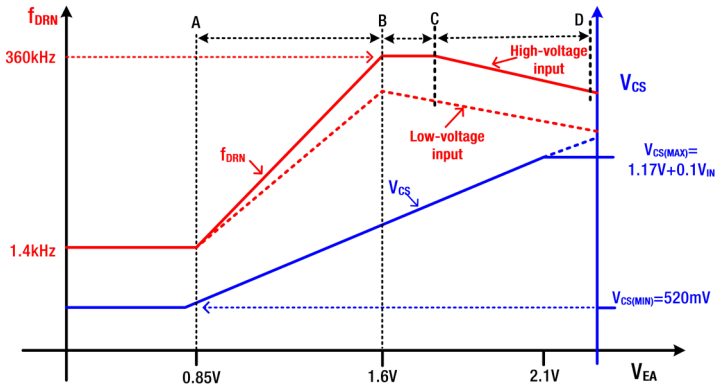


Fig. 13 Curves of switching frequency and peak current modulation vs. V_{EA}

PWM Control: The pulse-width modulation current serves as the positive input to the PWM comparator, while the negative input is composed of the sum of the induced current and the slope compensation current. The comparator compares these inputs and generates the pulse-width signal to drive the power switch NM0, thereby regulating and stabilizing the converter's output voltage at its rated value. In BCM operation, the formulas for output power and frequency are:

$$P_{OUT} = 0.5 \times I_{PK} \times V_{IN} \times D \times \eta$$

Where I_{PK} is the peak current of the power transistor, V_{IN} is the input voltage, η is the transformer efficiency, and D is the duty cycle, calculated as:

$$D = \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

Where N_{PS} is the turns ratio of the transformer's primary to secondary windings, and V_F is the voltage drop of the output diode. The formula for operating frequency is:

$$f_{DRN} = \frac{V_{IN}}{L_P \times I_{PK}} \times \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

PFM Control: The operating frequency of the RVSW013 varies according to three distinct states depending on the load conditions. During Boundary Conduction Mode (BCM) operation, as illustrated in the C-D phase of Figure 13, a decrease in converter load causes the modulation voltage V_{EA} and peak current to gradually decrease. This results in shorter excitation and demagnetization times, leading to a gradual increase in switching frequency, as described by the f_{DRN} formula. As the load reduces further, the operating frequency may reach the maximum limit of 360kHz, which is most common under light load and high input voltage conditions, represented by the red solid line in the B-C phase. At this point, the switching frequency is capped at 360 kHz, and the device exits BCM, entering Discontinuous Conduction Mode (DCM), where switching no longer occurs at the first resonant valley. Under even lighter loads, the RVSW013 activates an analog frequency reduction function designed to enhance light-load efficiency and minimize no-load power consumption. In this mode, as the load continues to decrease, V_{EA} and the operating frequency decrease accordingly. However, since output voltage sampling can only occur during the transformer's demagnetization phase, the minimum operating frequency is limited to f_{MIN}=1.4kHz to maintain regulation accuracy.

Optocoupler Isolated Feedback SSR Mode - COM Pin

Mode Selection: The optocoupler-isolated feedback SSR mode is an alternative PWM operating mode of the RVSW013. To enable this mode, the voltage at the EN pin must first exceed the high-level threshold $V_{EN(H)}$, indicating that the EN pin is connected to a high logic level and enabling PWM operation. Simultaneously, the voltage at the MOD pin must also exceed $V_{MOD(H)}$, confirming that the MOD pin is at a high logic level and selecting the SSR feedback mode within PWM operation. In this configuration, closed-loop feedback is achieved through the COM pin. When the RFB pin is connected directly to V_{IN}, the oscillator operates at a maximum frequency of 360kHz with a maximum duty cycle of 84%. Alternatively, a resistor can be placed between the RFB and DRN pins to set the operating frequency according to system requirements, with a recommended resistor value of R_{FB}= N_{PS}×(V_{OUT}+ V_F)/50μA. In the event of an output short circuit, the switching frequency is automatically limited to 200kHz to reduce stress on the power transistor. If the RFB pin is left floating or connected to GND through a resistor (with a recommended value of 200kΩ), the oscillator's maximum operating frequency is reduced to 200kHz, while the maximum duty cycle is increased to 91%.

Current Modulator: The pulse-width modulation voltage V_{COM} generates a modulation current across the external resistor connected to the VCS pin. This current defines the voltage at the VCS pin, as illustrated by the V_{CS} versus V_{COM} characteristic curve shown in Figure 14. The modulation current is used by the current modulator to control the peak current through the power transistor NM0, thereby adjusting the converter's output voltage. When V_{COM} exceeds 2.1V, the voltage at the VCS pin reaches its maximum value, $V_{CS(MAX)}$, which limits the peak current of NM0 to ensure safe operation.

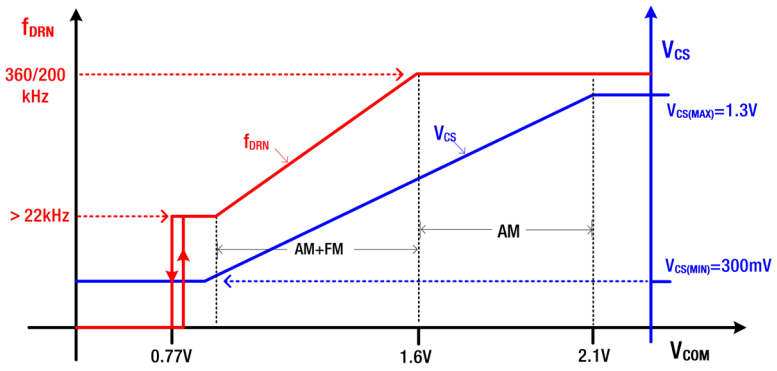


Fig. 14 Curve of switching frequency and peak current modulation vs. V_{COM}

PWM Control: The pulse-width modulation current acts as the positive input to the internal PWM comparator, while the combined current from the primary-side current sense and the slope compensation circuitry forms the negative input. Based on this comparison, the comparator generates a suitable pulse-width signal to drive the power switch and regulate the converter's output voltage at its rated level. The RVSW013 supports two maximum duty cycle options-84% or 91%-depending on the configuration of the RFB pin. To prevent subharmonic oscillation when the duty cycle exceeds 50%, internal slope compensation is applied. In order to minimize the adverse effects of slope compensation on load capability under low input voltage, the slope compensation current is only activated when the duty cycle exceeds 35%. Below this threshold, slope compensation is disabled. The slope compensation current reaches its peak when the duty cycle reaches its maximum value of either 84% or 91%, depending on the RFB configuration.

PFM Control: To improve efficiency under light-load conditions and reduce power consumption during no-load operation, the RVSW013 incorporates an analog frequency reduction function when operating in SSR feedback mode. As the converter load decreases, the modulation voltage V_{COM} also decreases. When the load falls to approximately 30% of the converter's maximum output power, the switching frequency begins to decrease. If V_{COM} drops to the skip mode threshold voltage $V_{COM(SKIP)}$), the DRN output is disabled, entering an intermittent operation mode that significantly reduces power consumption. DRN resumes pulse output only when V_{COM} rises above $V_{COM(SKIP)}$+15mV, allowing for efficient reactivation of switching operation as load increases.

Synchronous Rectification

Mode Selection: When the EN pin is connected to a low logic level, the RVSW013 enters synchronous rectification mode. The key timing behavior of this function is illustrated in Figure 15 The device identifies the excitation phase of the converter by detecting the relative maximum voltage of the V_{DRN} signal. Once this maximum is detected, an enable signal (T_{EN}) is generated. The synchronous rectification switch is then turned on when V_{DRN} drops below the turn-on threshold $V_{th(on)}$. If no relative maximum voltage is detected, the switch remains off, even if V_{DRN} falls below $V_{th(on)}$, effectively preventing false activation due to resonant negative voltage. After the synchronous rectification switch is turned on, and a defined blanking time T_{B_ON} has elapsed, the switch is turned off once V_{DRN} rises above the turn-off threshold $V_{th(off)}$, corresponding to the natural decrease in conduction current.Let me know if you'd like a version annotated with figure references, timing explanations, or formatted for documentation use.

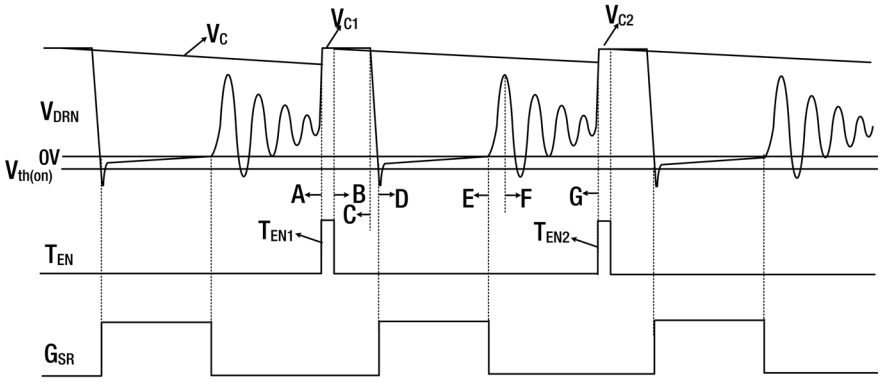


Fig. 15 Synchronous Rectification Detection Timing Diagram

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