

General Description

The TQP369182 is a general-purpose buffer amplifier that offers high dynamic range in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 20.7 dB gain, +28 dBm OIP3, and 3.9 dB Noise Figure while drawing 45 mA current. The device combines dependable performance with consistent quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The device is housed in a lead-free/green/RoHS-compliant industry-standard SOT-89 package.

The TQP369182 consists of a Darlington-pair amplifier using TriQuint's high reliability InGaP/GaAs HBT process technology. Only DC-blocking capacitors, a bias resistor, and an inductive RF choke are required for operation.

This broadband MMIC amplifier can be directly applied to various current and next generation wireless technologies such as CDMA, W-CDMA, and LTE. In addition, the TQP369182 will work for other applications within the DC to 6 GHz frequency range.



SOT-89 Package

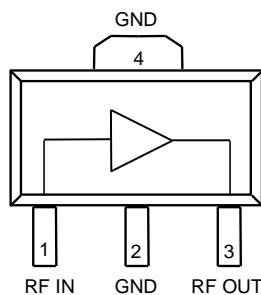
Product Features

- DC-6000 MHz
- Flat, broadband frequency response
- 20.7 dB Gain at 1.9 GHz
- 3.9 dB Noise Figure at 1.9 GHz
- +28 dBm Output IP3 at 1.9 GHz
- +15.1 dBm P1dB at 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Single Supply, 45 mA Current
- SOT-89 Package

Applications

- Wireless Infrastructure
- CATV / SATV / MoCA
- Point to Point
- Defense & Aerospace
- Test & Measurement Equipment
- General Purpose Wireless

Functional Block Diagram



Ordering Information

Part No.	Description
TQP369182	InGaP / GaAs HBT Gain Block
TQP369182-PCB	500–6000 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 13" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+24 dBm
Device Voltage (V _{CC})	+4.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
T _{CASE}	-40		+85	°C
T _j (for >10 ⁶ hours MTTF)			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: I_{CC}=45 mA, T_{CASE}= +25°C, 50Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		DC		6000	MHz
Test Frequency			1900		MHz
Gain		19.2	20.7	22.2	dB
Input Return Loss			-21		dB
Output Return Loss			-20		dB
Output P1dB			+15.1		dBm
Output IP3	P _{out} =0 dBm/tone, Δf= 1 MHz	+25.5	+28.0		dBm
Noise Figure			3.9		dB
Device Voltage (V _{CC})		3.0	3.9	4.5	V
Device Current (I _{CC})			45		mA
Thermal Resistance (θ _{jc})	Junction to case ⁽¹⁾			128	°C/W

Notes:

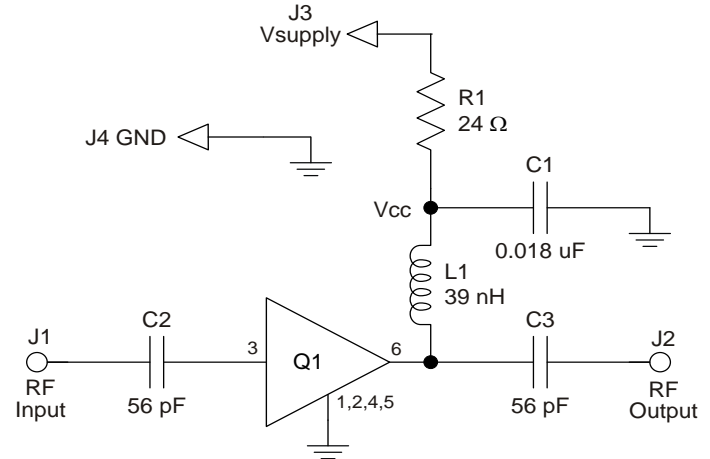
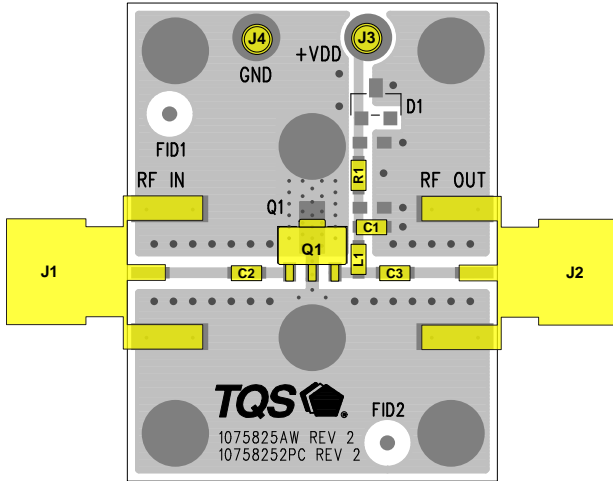
1. Thermal path is from the device junction through the package ground tab (pins 2,4) to the backside mounting surface.

S-Parameters

Test Conditions: $V_{CC}=+3.9$ V (typ.), $I_{CC}=45$ mA (typ.), $T_{CASE}=+25^{\circ}\text{C}$, 50Ω system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-23.9	-178.7	22.8	179.6	-24.4	1.2	-28.1	153.9
20	-23.4	-178.6	22.8	179.1	-24.4	0.7	-29.1	163.4
50	-23.2	176.2	22.8	178.2	-24.3	0.1	-29.4	173.6
100	-23.1	169.2	22.8	175.3	-24.3	-0.3	-28.9	169.4
200	-23.5	160.3	22.8	170.8	-24.2	-1.7	-29.7	159.7
500	-23.2	122.4	22.6	157.9	-24.3	-4.9	-29.7	159.4
900	-22.1	99.0	22.2	141.0	-24.3	-9.2	-29.5	149.7
1000	-21.3	90.5	22.2	136.9	-24.3	-10.4	-28.0	152.1
1500	-20.6	65.3	21.7	116.5	-24.2	-16.1	-25.1	146.4
1900	-19.0	44.7	21.3	101.2	-24.2	-20.8	-22.7	144.5
2000	-18.3	42.5	21.2	97.7	-24.2	-21.7	-22.8	147.2
2500	-18.3	29.6	20.6	79.1	-24.2	-26.5	-20.0	123.9
3000	-18.3	7.2	20.0	62.1	-24.2	-32.2	-17.6	119.9
3500	-17.4	-12.4	19.4	45.4	-24.2	-38.2	-17.1	116.3
4000	-19.8	-23.5	18.9	28.7	-24.0	-44.0	-15.6	102.9
4500	-20.8	-40.6	18.4	12.3	-24.2	-49.5	-14.7	97.0
5000	-24.1	-85.7	17.9	-3.3	-24.4	-55.5	-14.7	91.8
5500	-20.8	-124.5	17.6	-19.7	-24.4	-61.0	-13.6	88.7
6000	-23.0	-163.2	17.2	-35.3	-24.7	-64.9	-12.7	92.1

TQP369182-PCB Evaluation Board (500–6000 MHz)



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless otherwise stated.

Bill of Material – TQP369182-PCB

Reference Des.	Value	Description	Manuf.	Part Number
Q1	n/a	High Linearity LNA Gain Block	Qorvo	TQP369182
C1	0.018 μ F	Cap, Chip, 0603, 16V, X7R, 10%	various	
C2, C3	56 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
L1	39 nH	Inductor, 0603, 5%, CS Series	Coilcraft	
R1	24 Ω	Res, Chip, 0805, 1/10W, 5%	various	

Component Values for Specific Frequencies

Frequency (MHz)	50	500	900	1900	2200	2500	3500
L1	820 nH	220 nH	68 nH	27 nH	22 nH	18 nH	15 nH
C2, C3	.018 μ F	1000 pF	100 pF	68 pF	68 pF	56 pF	39 pF

Bias Resistor Values for Various Supply Voltages

V _{SUPPLY} (V)	5	6	7	8	9	10	12
R1	24 Ω	47 Ω	68 Ω	91 Ω	110 Ω	130 Ω	180 Ω
Component Size	0805	1206	1210	1210	1210	2010	2010

Typical Performance – TQP369182-PCB

Test conditions unless otherwise noted: $V_{SUPPLY} = +5\text{ V}$, $R_1 = 24\ \Omega$, $I_{CC} = 45\text{ mA}$, $T_{CASE} = +25^\circ\text{C}$

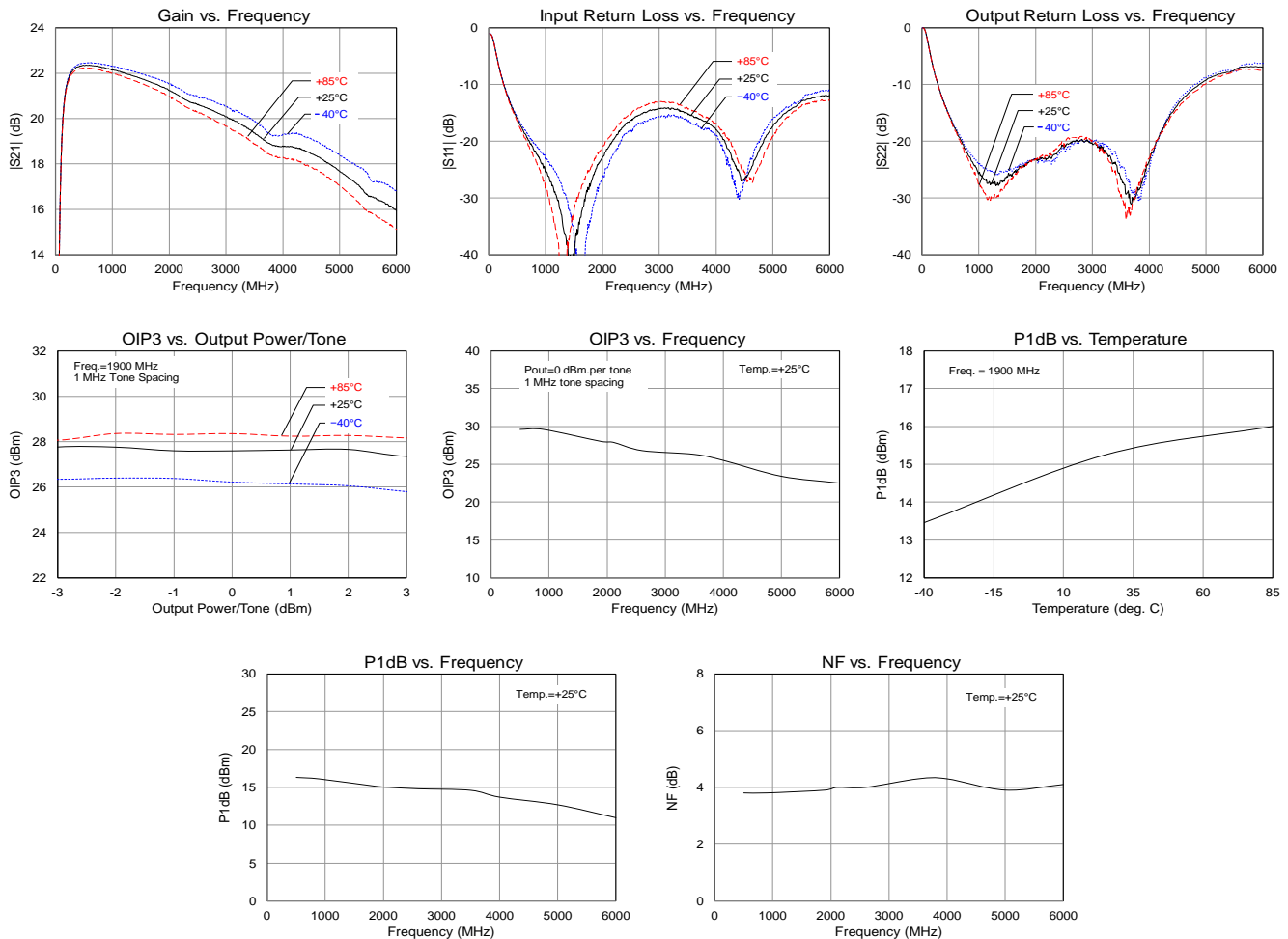
Parameter	Typical Value										Units
Frequency	500	900	1900	2100	2600	3500	4000	5000	6000		MHz
Gain	22.3	22.0	20.7	20.6	20.5	19.4	18.9	17.9	17.2		dB
Input Return Loss	-16.0	-24.4	-21.0	-21.1	-15.5	-17.4	-19.8	-24.1	-23.0		dB
Output Return Loss	-16.0	-28.0	-20.0	-23.1	-20.4	-17.1	-15.6	-14.7	-12.7		dB
Output P1dB	+16.3	+16.1	+15.1	+15.0	+14.8	+14.6	+13.7	+12.7	+11.0		dBm
OIP3	+29.6	+29.6	+28.0	+27.9	+26.8	+26.3	+25.5	+23.4	+22.5		dBm
Noise Figure	3.8	3.8	3.9	4.0	4.0	4.3	4.3	3.9	4.1		dB

Notes:

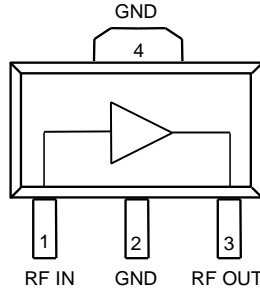
- OIP3 measured with two tones at an output power of 0 dBm / tone separated by 1 MHz.

Performance Plots – TQP369182-PCB

Test conditions unless otherwise noted: $V_{SUPPLY} = +5\text{ V}$, $R_1 = 24\ \Omega$, $I_{CC} = 45\text{ mA}$, $T_{CASE} = +25^\circ\text{C}$

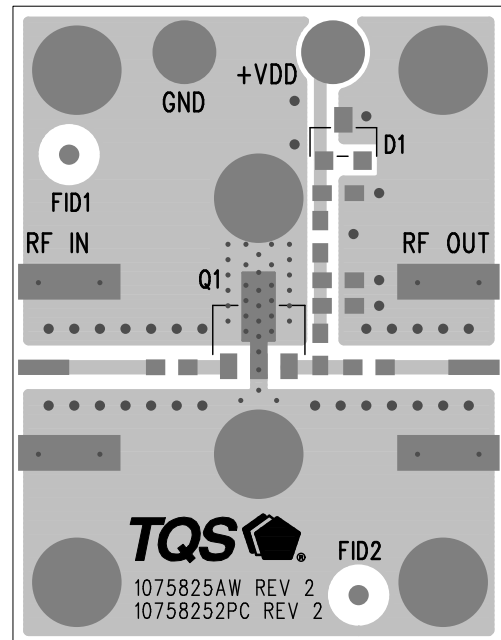
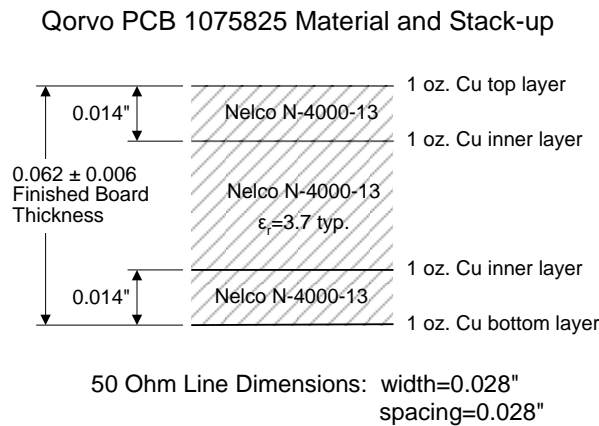


Pin Configuration and Description



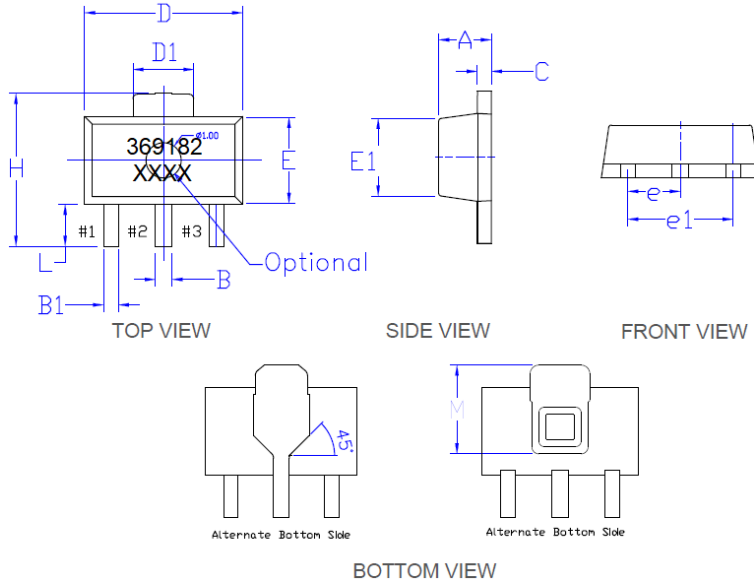
Pin No.	Label	Description
1	RF IN	RF input, matched to 50 ohms. External DC Block is required.
3	RF OUT	RF output / DC supply, matched to 50 ohms. External DC Block, bias choke, and dropping resistor is required.
2, 4, Backside Paddle	GND Paddle	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information



Package Marking and Dimensions

Marking: Part Number – 369182
Trace Code – XXXX up to 4 Characters assigned by sub-contractor

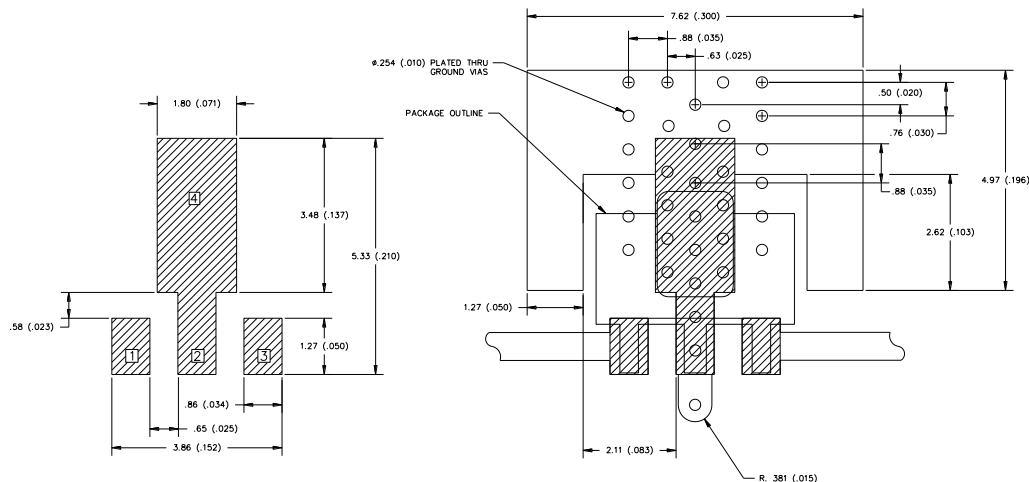


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.40	1.50	1.60
B	0.41	0.49	0.58
B1	0.34	0.42	0.50
C	0.35	0.40	0.44
D	4.40	4.50	4.60
D1	1.40	1.67	1.83
E	2.30	2.50	2.60
E1	1.77	2.31	2.57
e	1.45	1.50	1.55
e1	2.90	3.00	3.10
H	3.94	4.10	4.25
L	0.80	1.05	1.20
M	2.36 ref		

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

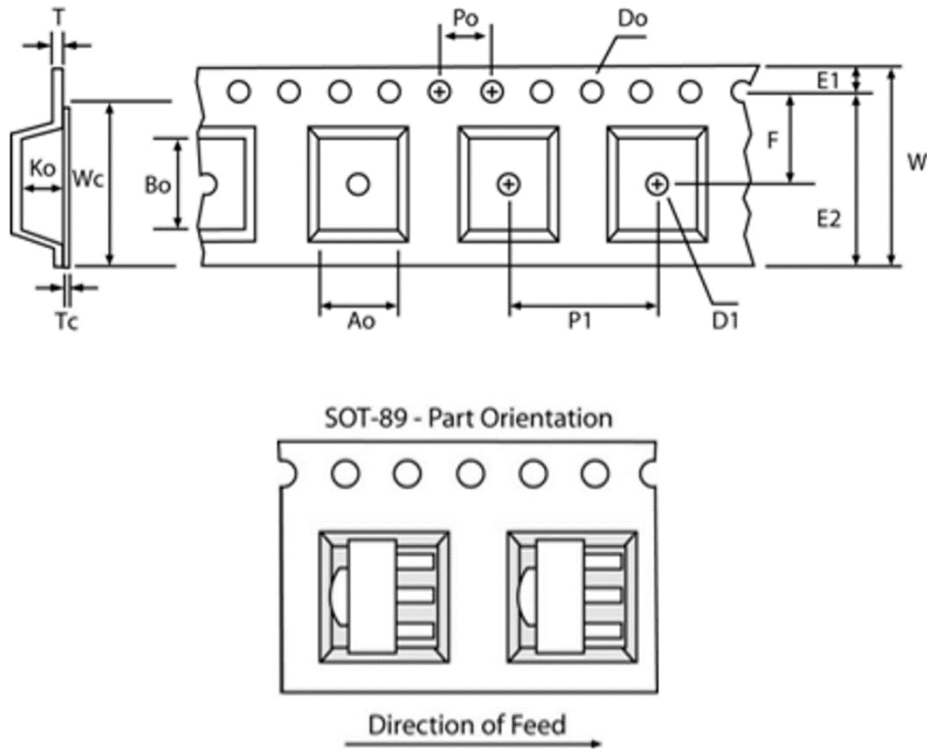
PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters [inches]. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for best electrical and thermal performance.

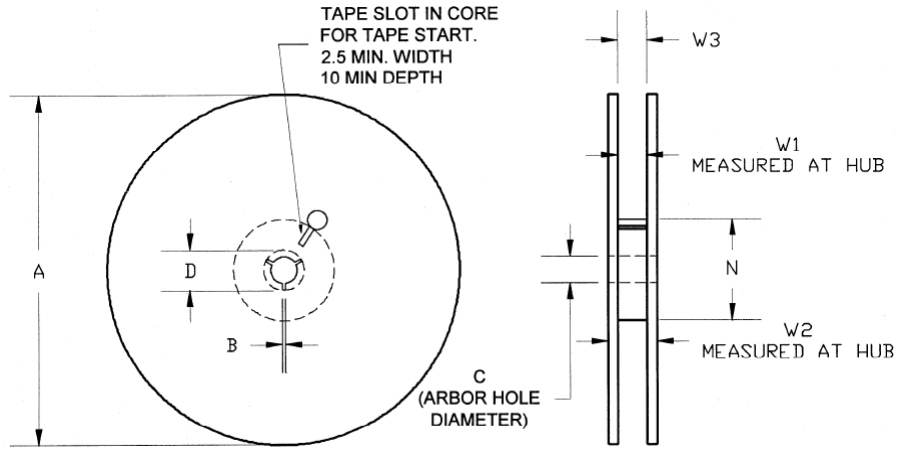
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.181	4.60
	Width	B0	0.193	4.90
	Depth	K0	0.075	1.90
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Annealed Matte Tin or Nickle Palladium Gold (NiPdAu)

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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