PAC5526

48V Charge Pump Motor Controller and Driver for BLDC Motors

1 Product Overview

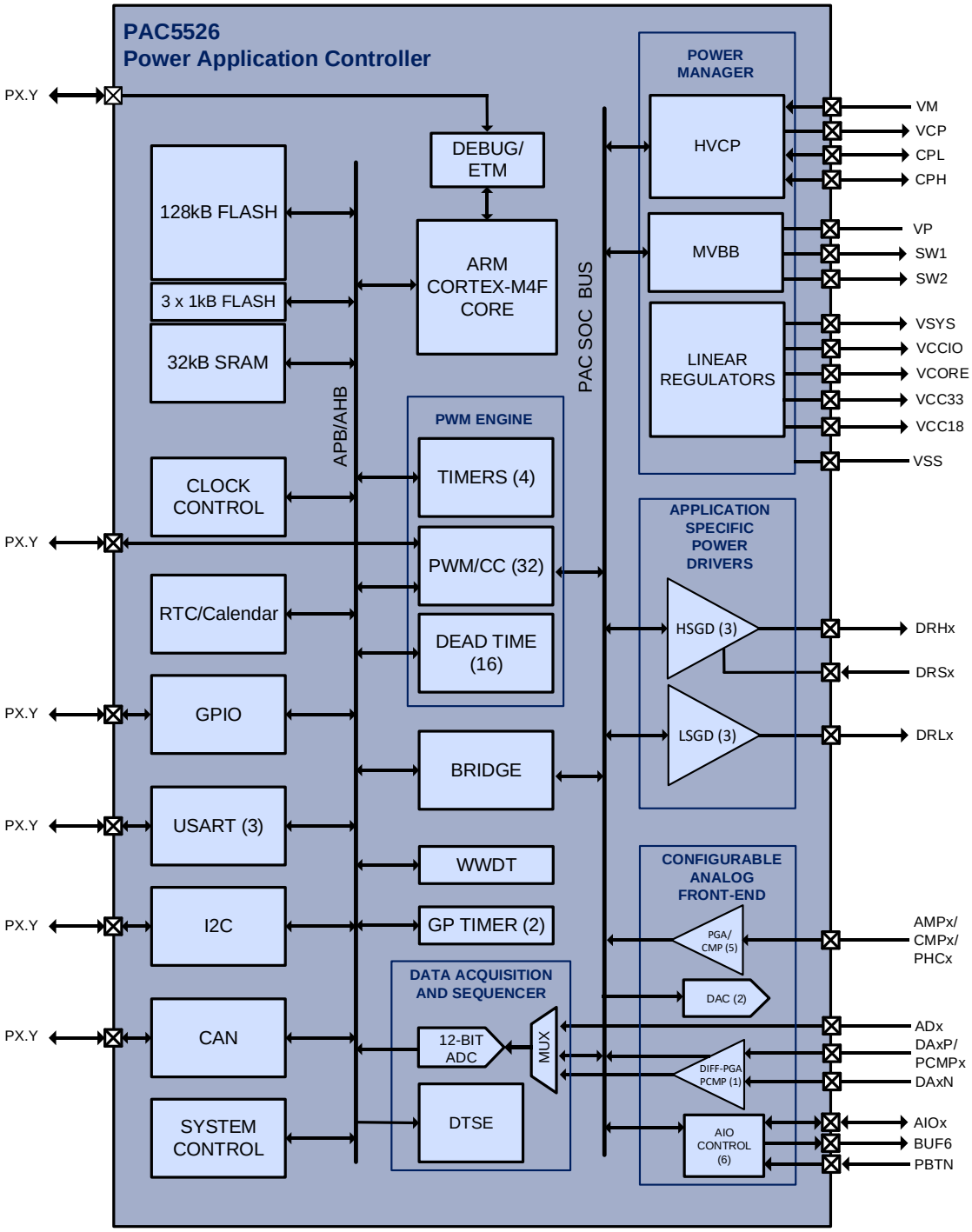
The PAC5526 is a 48V Power Application Controller® (PAC) product that is optimized for high-speed motor control and driving for battery powered BLDC motors. The PAC5526 integrates a 150MHz Arm® Cortex®-M4F 32-bit microcontroller core with a highly configurable Power Manager, Active-Semi's proprietary and patent-pending Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The PAC5526 features 128kB of embedded FLASH, 32kB of SRAM memory, a 2.5MSPS analog-to-digital converter (ADC) with programmable auto-sampling of up to 24 conversion sequences, 3.3V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Power Manager provides "all-in-one" efficient power management solution for the application. It features a charge pump, buck-boost converter and four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

The PAC5526 is available in a 48-pin, 6x6mm TQFN package.

2 Functional Block Diagram



3 Key Features

- **Power Manager**
  - Charge Pump DC/DC for high-side gate drive supply
    - Input Voltage: 6V – 48V
  - Buck-Boost Regulator for low-side gate drive supply
    - Configurable 10V or 12V
  - 4 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 6 Analog Front-End IO pins
  - 1 Differential Programmable Gain Amplifier
  - 5 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection and Current Limit
  - 2 10-bit DACs
- **Proprietary Application Specific Power Drivers**
  - 3 high-side gate drivers with programmable gate driving up to 1A
  - 3 high-side gate drivers with programmable gate driving up to 1A
  - 100% Duty Cycle
  - Cycle-by-cycle current limit
  - Configurable fault protection
- **3.3V I/Os**
- **150MHz Arm® Cortex®-M4F 32-bit Microcontroller Core**
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - 32-bit hardware divider
  - DSP Instructions and Saturation Arithmetic Support
  - Integrated sleep and deep sleep modes
  - Single-precision Floating Point Unit (FPU)
  - 8-region Memory Protection Unit (MPU)
  - Nested Vectored Interrupt Controller (NVIC) with 32 Interrupts with 8 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
  - Embedded Trace Macrocell (ETM) for in-system debugging at real-time without breakpoints
- **Memory**
  - 128kB FLASH
  - 32kB SRAM with ECC
  - 2 x 1kB INFO FLASH area for manufacturing information
  - 1 x 1kB INFO FLASH area for user parameter storage and application configuration or code
  - 4-Level Code Protection
- **Analog to Digital Converter (ADC)**
  - 12-bit, 2.5MSPS SAR ADC
  - Programmable Dynamic Triggering and Sampling Engine (DTSE)
- **I/O**
  - 20 general-purpose I/Os with tri-state, pull-up, pull-down and dedicated I/O supply
  - 10 I/Os can be configured as ADC input or digital I/O
  - Configurable weak pull-up and pull-down
  - Configurable drive strength (6mA to 25mA minimum)
  - Dedicated Integrated IO power supply (3.3V)

- Flexible peripheral MUX allowing each IO pin to be configured with one of up to 8 peripheral functions
- Flexible Interrupt Controller

- **Flexible Clock Control System (CCS)**
  - 300MHz PLL from internal 1.25% oscillator
  - 20MHz Ring Oscillator
  - 20MHz External Clock Input
- **Timing Generators**
  - Four 16-bit timers with up to 32 PWM/CC blocks
    - 16 Programmable Hardware Dead-time generators
    - Up to 300MHz input clock for high-resolution PWM
  - 16-bit Windowed Watchdog Timer (WWDT)
  - 24-bit Real-time Clock (RTC) with Calendar and Alarm Functions
  - 24-bit SysTick Timer
  - 2 x 24-bit General-purpose count-down timers with interrupt
  - Wake-up timer for sleep modes from 0.125s to 8s
- **Communication Peripherals**
  - 3 x USART
    - SPI or UART modes
    - SPI Master/Slave, up to 25MHz
    - UART, up to 1Mbps
  - I2C Master/Slave
  - CAN 2.0B Controller
  - Single Wire Debugger (SWD), JTAG
  - Embedded Trace Macrocell (ETM)
- **4-Level User-Configurable Code Protection**
- **96-bit Unique ID**
- **CRC Engine**
  - Offloads software for communications and safety protocol through hardware acceleration
  - Configurable Polynomial (CRC-16 or CRC-8)
  - Configurable Input Data Width, Input and Output Reflection
  - Programmable Seed Value

- **Physical**
  - T_A = -40°C to 125°C
  - QFN 6x6mm 48-pin package
    - Exposed pad for thermal management

4 Ordering Information

Part Number	Description
PAC5526QM-T	48V Charge Pump Motor Controller and Driver for BLDC Motors

Table of Contents

5 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Power Manager			
VM to VSS	Supply Input Voltage	-0.3 to 48	V
VCP to VM	Charge Pump Voltage	-0.3 to 14	V
CPH to VM		-0.3 to V_{CP} + 0.3	V
CPL to VSS		-0.3 to V_P	V
SW1 to VSS		-0.3 to V_M + 0.3	V
SW2 to VSS		-0.3 to V_P + 0.3	V
VP to VSS	Gate Drive Voltage	-0.3 to 14	V
VSYS to VSS	System Supply Voltage	-0.3 to 6	V
VCC33, VCCIO to VSS	3.3V Analog, IO LDO Voltage	-0.3 to 4.1	V
VCORE to VSS	Digital Logic Voltage	-0.3 to 1.44	V
VCC18 to VSS	FLASH Voltage	-0.1 to 2.5	V
Application Specific Power Driver™			
DRLx to VSS	Low-side Gate Drive Voltage	-0.3 to VP + 0.3	V
DRSx to VSS	Source Voltage	-6 to VCP + 0.3	V
dVDRSx/dt	DRSx allowable offset slew rate	5	V/ns
DRHx to respective DRSx	High-Side Gate driver offset voltage	-0.3 to 14	V
VSS, DRLx, DRHx RMS current		0.2	A_{RMS}
IO			
AIO[4,5, 7..9] to VSS	Analog IO Voltage	-0.3 to V_{SYS} + 0.3	V
AIO6	AIO Voltage	-0.3 to 6	V
PD<x>, PE<x>, PF<x>, PG<x> to VSS	MCU IO Voltage	-0.3 to V_{CCIO} + 0.3	V
$I_{PD<x>}$, $I_{PE<x>}$, $I_{PF<x>}$	MCU IO pin injection current	25	mA
$\sum I_{PD<x>}$, $\sum I_{PE<x>}$, $\sum I_{PF<x>}$	MCU IO sum of all pin injection current	50	mA
Temperature			
T_A	Ambient Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 140	°C
Electro-static Discharge (ESD)			
Human Body Model (HBM)	All pins	2	kV
Charge Device Model (CDM)	All pins	1	kV

Operation of this device outside the parameter ranges given above may cause permanent damage.

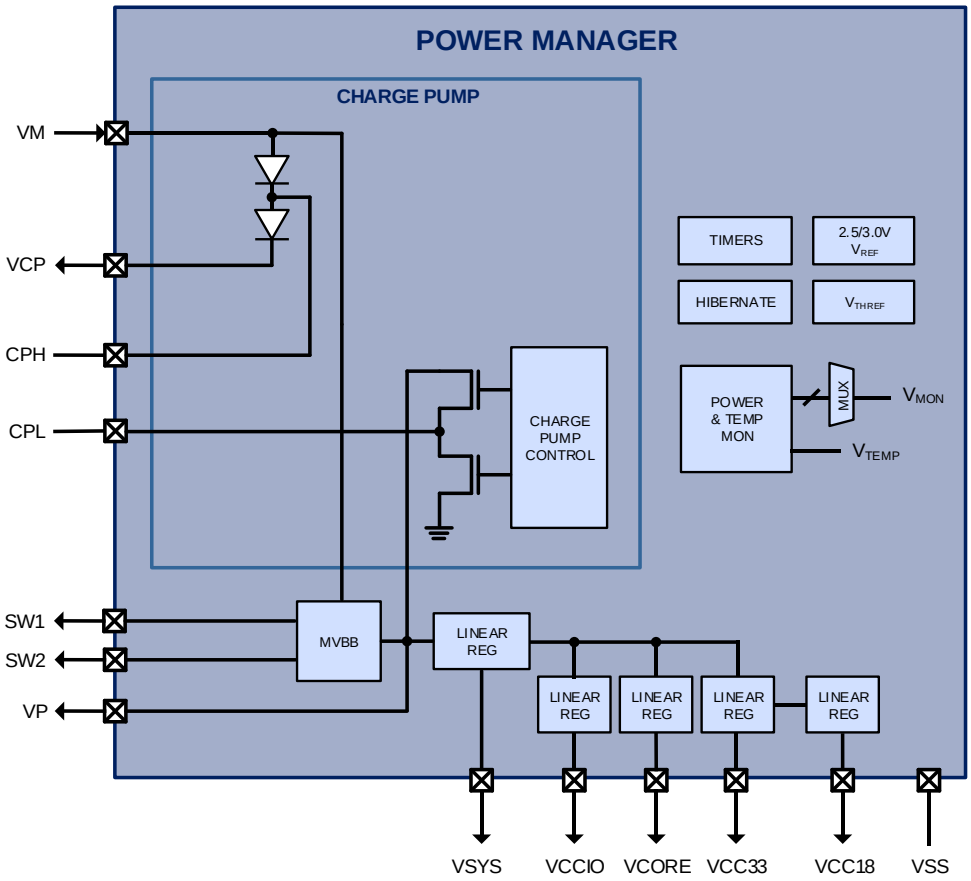
6 Power Manager

6.1 Features

- Charge Pump for high-side gate driver supply
  - Input Voltage: 6V - 48V
- Configurable Buck-Boost converter for low-side gate driver supply (10V/12V)
- 5 additional Linear regulators with power and hibernate management
- High-accuracy voltage reference for ADC and comparators
- Power and temperature monitor, warning, fault detection
- Extremely hibernate mode I_Q of 5µA at 18V input

6.2 System Block Diagram

Figure 1 Power Manager System Block Diagram



6.3 Functional Description

The Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a charge pump DC/DC to generate the supply (HVCP) for the integrated high-side gate drivers and a Buck-Boost Converter (MVBB) to generate the supply for the integrated low-side gate drivers. Five additional linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, V_{CC18} and V_{CORE} supplies for 5V system, 3.3V I/O, 3.3V mixed signal, MCU FLASH and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

6.3.1 High-Voltage Charge Pump (HVCP)

The Power Manager contains a charge pump that is used to generate V_{CP}, which is the high- side gate driver supply voltage. The charge pump maintains a voltage of $V_M + V_P$ for the high-side driver supply.

The positive terminal of the battery supply is connected to the VM pin on the PAC5526. This supply should be bypassed to ground using a high-value electrolytic capacitor in a parallel with a 0.1µF ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor should be connected with a trace shorter than 10mm to the pin.

The charge pump requires a capacitor between the VM and VCP pins, to act as a storage capacitor for the high-side gate driver supply. The nominal value of this capacitor should be 1µF. A flying capacitor should be placed between the CPH and CPL pins with a nominal value of 0.1µF.

6.3.2 Medium-Voltage Buck Boost (MVBB)

The Power Manager contains a Buck-Boost regulator that is used to generate the low-side gate drive supply (V_P). A 10µH value inductor should be placed between the SW1 and SW2 pins on the PAC5526 for this regulator. It is desirable to eliminate unwanted parasitic effects so this inductor should be placed as close as possible to the PAC5526.

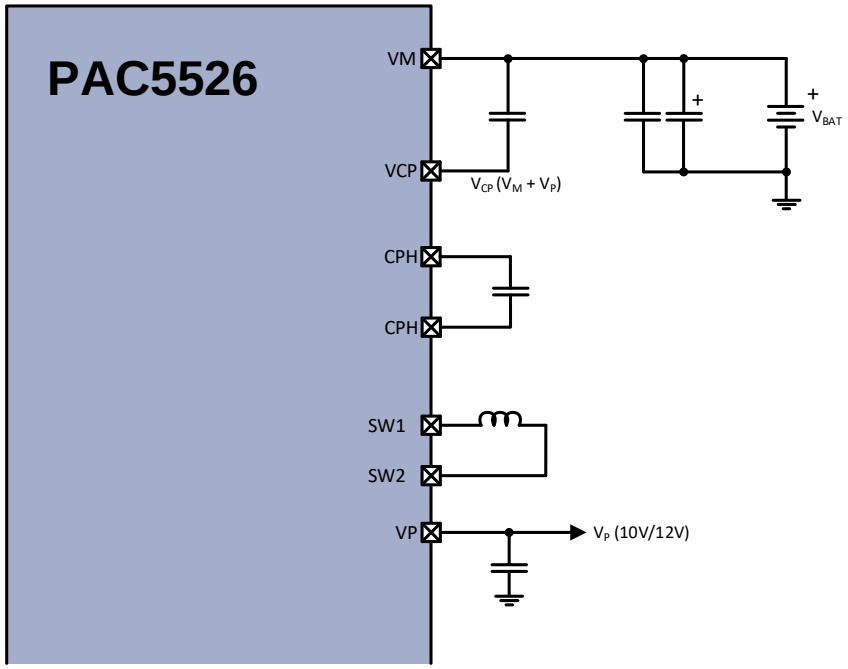
The output of the MVBB may be configured to be either 10V or 12V, to work with a range of different applications and inverters. This regulator supplies the other LDO sub-regulators in the device (V_{SYS}, V_{CCIO}, V_{CORE} and V_{CC33}).

Unlike an LDO, the Buck-Boost regulator maintains the low-side gate driver voltage across a wide range of motor voltage (VM) supply inputs. This makes the low side of the inverter more efficient and allows more options for MOSFET selection for the inverter.

6.3.3 HVCP and MVBB Circuit Connections

The figure below shows the typical circuit connections for the HVCP and MVBB on the PAC5526.

Figure 2 Power Manager Circuit Connections



6.3.4 Linear Regulators

The Power Manager includes five linear regulators:

- VSYS – 5V, 100mA
- VCC33 – 3.3V, 40mA
- VCCIO – 3.3V, 40mA
- VCC18 – 1.8V, 20mA
- VCORE – 1.2V, 40mA

The VSYS regulator generates up to a 5V, 100mA supply for the other LDOs (VCCIO, VCORE and VCC33). This can also act as a system supply for other peripherals on the PCB. The total amount of supply for VSYS is 100mA, which includes the needs of the other LDOs above.

Once VSYS is above 4.5V, the four additional linear regulators for VSYS, VCCIO, VCC33, and VCORE supplies sequentially power up. Figure 3 shows typical circuit connections for the linear regulators.

The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 and VCORE regulators generate 3.3V and 1.2V, respectively. When VSYS, VCCIO, VCC33, VCC18 and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

Each of the LDOs above must be bypassed externally to ground as shown below. See the Electrical Characteristics for details on recommended component values for bypass capacitors.

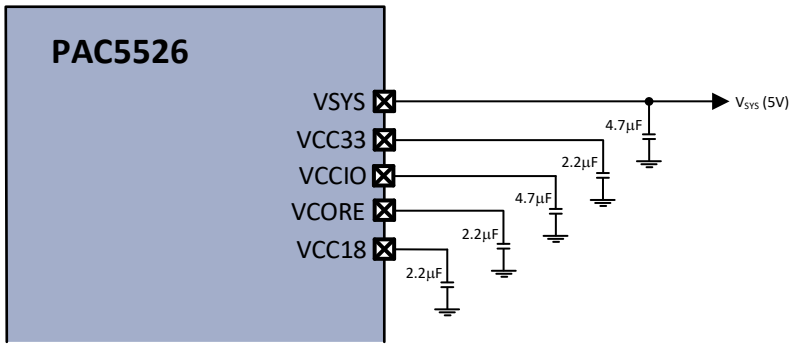


Figure 3 Linear Regulators Connections

6.3.5 Integrated VM Sensing

The Power Manager also integrates sensing of the battery voltage on VM, without the need for external components. This allows the user to sense VM for the application, without any additional components and without dedicating an external ADC channel for this purpose.

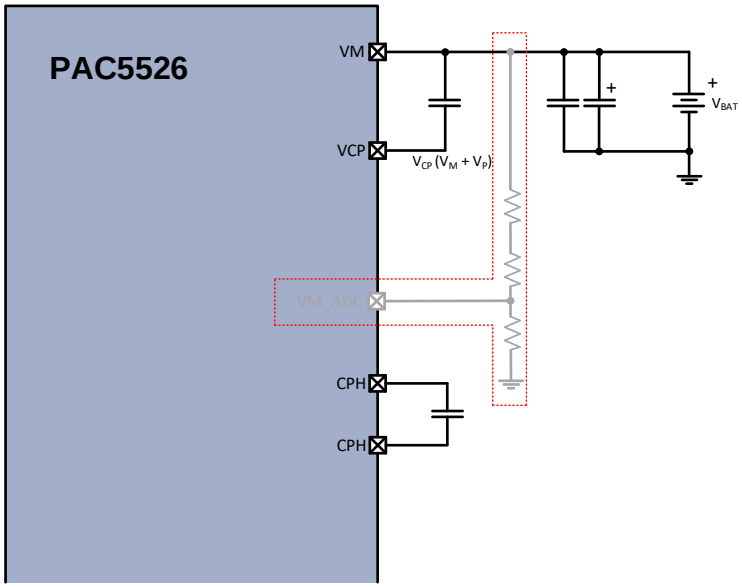
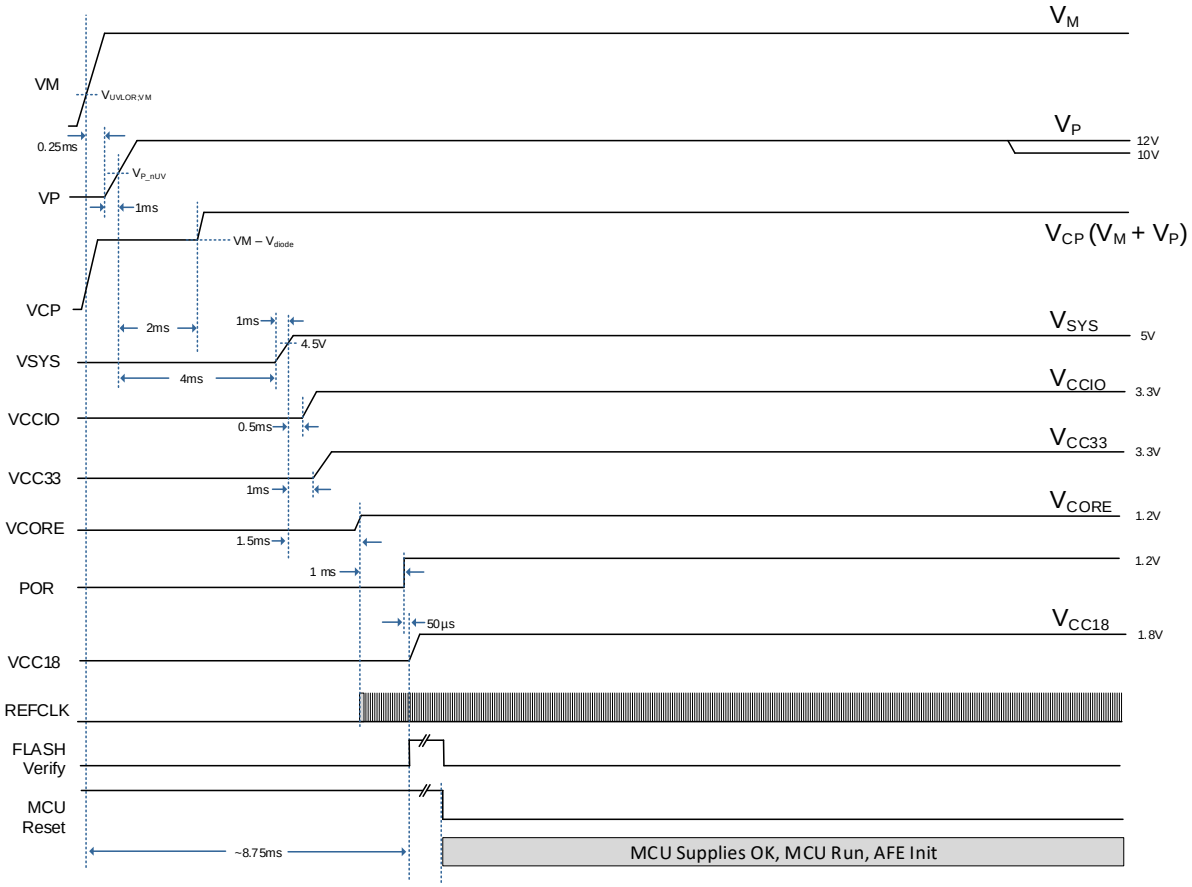


Figure 4 Integrated VM Sensing

6.3.6 Power-up Sequence

The Power Manager follows a typical power up sequence as shown below.

Figure 5 Power-up Sequence



A typical sequence begins with input power supply being applied on VM. During this time, VCP will be about one diode drop lower than VM. After VM has reached a safe threshold of 6V, there is a 0.25ms delay and then the MVBB is started and VP starts to rise. With the properly rated components for the MVBB and VP, VP will reach its UVLO threshold in 1ms. After an additional 2ms the charge pump output is turned on and VCP will start to rise toward its final value of VM + VP.

After VP rises above its UVLO threshold and 4ms has elapsed, the VSYS, VCCIO, VCC33 and VCORE LDOs are started in succession. After VCORE has reached its power good threshold, there is a 1ms delay and then the POR signal will be released from reset to the MCU. At this time, there is a 50µs delay and the VCC18 LDO for FLASH on the MCU is started.

When VCC18 starts to rise, then the MCU performs a FLASH checkerboard verify routine which verifies that FLASH memory is correctly being read. If the contents of FLASH are not properly read, this loop will be repeated until the FLASH checkerboard is successfully read (50µs delay, then re-read FLASH). After this has successfully been read then the MCU is released from reset and begins executing instructions. At this time, the user may re-program the VP output of the MVBB to either 10V or 12V.

6.3.7 Hibernate Mode

The PAC5526 can go into an ultra-low power hibernate mode during operation. The MCU may set a timer to wake-up from hibernate mode, or rely on an external AIO6 push-button (PBTN, see *Push Button* description in *Configurable Analog Front End*).

In hibernate mode, only a minimal amount (typically 5µA at 18V) of current is used by V_M, and the Power Manager and all internal regulators are shut down to eliminate power drain from the output supplies.

The system exits hibernate mode after a wake-up timer duration (configurable from 8ms to 4s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

6.3.8 Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CORE} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 170°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CORE}, $0.2 \cdot (V_{CP}-V_M)$, $0.4 \cdot V_{CC33}$, $0.4 \cdot V_{CCIO}$, $0.4 \cdot V_{SYS}$, $0.05 \cdot V_M$, V_{PTAT}, $0.1 \cdot V_P$.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt to the microcontroller. This warning allows the microcontroller to safely power down the system.

This value has a compensation coefficient available in INFO FLASH that can be used to obtain an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be calculated by the following formula:

T_{KELVIN} = 300 * (VPTAT + 0.075) / (VT300K + 0.075)

VPTAT can be read by the ADC by setting the ADC MUX using the voltage monitoring signals above.

For more information on the location of this temperature coefficient, see the PAC5526 Device User Guide.

6.3.9 Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC, the DACs, and the 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

6.4 Electrical Characteristics

The Electrical Characteristics for the MMPM are shown below.

6.4.1 HVCP Electrical Characteristics

Table 1 HVCP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Input Supply (VM)						
$I_{HIB;VHM}$	VM hibernate mode supply current	Hibernate mode active		5		µA
$I_{OP;VM}$	VM operating mode supply current		9		11	mA
$V_{OP;VM}$	VM operating voltage range		6		40	V
$V_{UVLOR;VM}$	VM under-voltage lockout rising			5.7	6	V
$V_{UVLO\_HYS;VM}$	VM under-voltage lockout hysteresis			0.3		V
$V_{OVLOR;VM}$	VM over-voltage lockout rising		45			V
$V_{OVLO\_HYS;VM}$	VM over-voltage lockout hysteresis			3		V
Charge Pump Supply (VCP)						
$I_{OP;VCP}$	VCP operating output current	Steady state		4		mA
$V_{OP;VCP}$	VCP operating voltage range	6V < VM < 40V		VM + VP		V
C_{VCP}	VCP capacitor value			1		µF
$V_{UVLOR;CP}$	Charge Pump UVLO rising			VM + 6.5		V
$V_{UVLOF;CP}$	Charge Pump UVLO falling			VM + 5		V
$R_{OUT;VCP}$	Charge Pump output resistance			45		Ω

VM = 18V and T_A = -40°C to 125°C unless otherwise specified

6.4.2 MVBB Electrical Characteristics

Table 2 HVCP Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Input Supply (VM)							
$I_{Q;VP}$	VP Quiescent supply current	VSYS, VCCIO, VCC33 and VCORE regulators only			1.8		mA
V_P	VP output voltage	Load = 10µA to 100mA; VM = 6V to 40V	VP = 10V		10		V
			VP = 12V	-6%	12	6%	V
V_{P_nUV}	VP output voltage turn-on	LDO and charge pump enabled threshold; Hysteresis = 0.2V			4.5		V
V_{P_OK}	VP output voltage power OK	Relative to VP			90		%
$V_{OVLO;VP}$	VP over-voltage protection	Externally forced			15		V
$I_{VP;ILIM}$	VP peak output current			100			mA
$I_{MVBB;ILIM}$	MVBB current limit	Peak inductor current limit			650	850	mA
$F_{S;MVBB}$	MVBB Switching Frequency				1.33		MHz
	MVBB Inductor Value	Recommendation is 10µH/0.9A		10-20%	10	22+20%	µH
R_{DSG}	Discharge resistance	VP=5V			3		kΩ

VM = 18V and T_A = -40°C to 125°C unless otherwise specified

6.4.3 Linear Regulators Electrical Characteristics

Table 3 Linear Regulators Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{SYS}	VSYS output voltage	Load = 10µA to 50mA external load	4.8	5	5.18	V
V_{CCIO}	VCCIO output voltage	Load = 10mA	3.152	3.3	3.398	V
V_{CC33}	VCC33 output voltage	Load = 10mA	3.185	3.3	3.415	V
V_{CORE}	VCORE output voltage	Load = 10mA		1.2		V
V_{CC18}	VCC18 output voltage			1.8		V
$I_{OUT;VSYS}$	VSYS regulator current output	External load	50			mA
C_{VSYS}	VSYS bypass capacitor value	External VSYS Load < 5mA		4.7		µF
		External VSYS Load >= 5mA		10		µF
$I_{LIM;VCCIO}$	VCCIO regulator current limit		40	60		mA
$I_{LIM;VCC33}$	VCC33 regulator current limit		40	60		mA
$I_{LIM;VCORE}$	VCORE regulator current limit		40	60		mA
k_{SCFB}	Short-circuit current fold-back			50		%
$V_{DO;VSYS}$	VSYS dropout voltage	VP = 5V, I_{VSYS} = 50mA external load		200		mV
$V_{UVLO;VSYS}$	VSYS under-voltage lockout threshold	VSYS rising, hysteresis = 0.3V	4.35	4.5	4.65	V
k_{POKIO}	VCCIO power OK threshold	VCCIO rising, hysteresis = 10%	85	90	95	%
k_{POK33}	VCC33 power OK threshold	VCC33 rising, hysteresis = 10%	85	90	95	%
$k_{POKCORE}$	VCORE power OK threshold	VCORE falling, hysteresis = 10%	85	90	95	%
$R_{DSG;VSYS}$	VSYS discharge resistance			2.5		kΩ
$R_{DSG;LDO}$	LDO output discharge resistance			330		Ω

VM = 18V and T_A = -40°C to 125°C unless otherwise specified

6.4.4 Power System Electrical Characteristics

Table 4 Power System Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{REF}	Reference Voltage	T_A = 25°C	2.487	2.5	2.513	V
		T_A = -40°C to 125°C	2.463	2.5	2.537	V
k_{MON}	Power monitoring voltage (V_{MON}) coefficient	VCORE		1		V/V
		VSYS, VCCIO, VCC33		0.4		
		VP		0.1		
		VCP-VM		0.2		
		T_A = 25°C	2.487	2.5	2.513	V
		T_A = -40°C to 125°C	2.463	2.5	2.537	V

7 Configurable Analog Front-End (CAFE)

7.1 Features

- 6 Analog Front-End IO pins
- 1 Differential Programmable Gain Amplifier (Differential or Single-ended mode)
- 5 Single-ended Programmable Gain Amplifiers
- Programmable Over-Current Protection and Current Limit
- 7 Comparators
- 2 10-bit DACs
- V_{REF} buffered output
- Buffered output on AIO7
- DAC output to pin
- Total Hibernate Wake-up using timer or programable polarity push-button

7.2 System Block Diagram

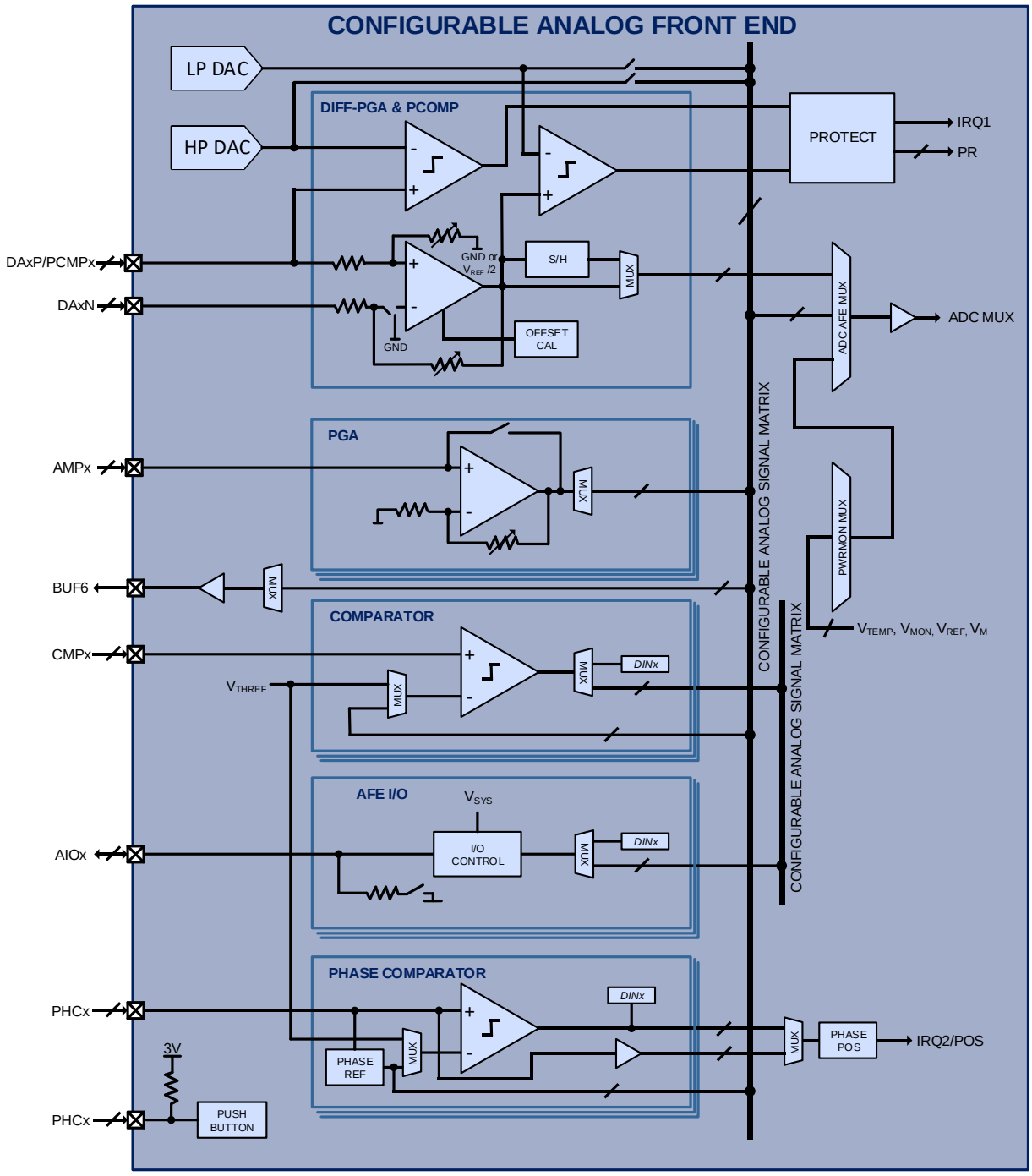


Figure 6 CAFE System Block Diagram

7.3 Functional Description

The device includes a Configurable Analog Front-End™ accessible through 6 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 1 differential programmable gain amplifier, 5 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 6 protection comparators, and buffer outputs.

These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

7.3.1 Differential Programmable Gain Amplifier (DA)

The DA may be configured to be either in differential or single-ended mode.

When configured for differential mode, the DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The gain is programmable and can be configured to be 1x, 2x, 4x, 8x and 16x for zero-ohm signal source impedance. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 80k / (80k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

When configured for single-ended mode, the DAxP input and the internal analog ground are connected to the differential amplifier to provide a single-ended infinite impedance amplifier. The gain is programmable and can be configured to be 1x, 2x, 4x, 8x and 16x.

In either mode, the amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring.

7.3.2 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SSA}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

7.3.3 General-Purpose Comparator (CMP)

The general-purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM. Each general-purpose comparator has two mask bits to prevent or allow rising or falling edge of its output to trigger second microcontroller interrupt INT2, where INT2 can be configured to active protection event PR.

7.3.4 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (VTHREF) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection. The phase comparators have configurable asymmetric hysteresis.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

7.3.5 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The high-speed protection (HP) comparator compares the AIO<n+1> pin to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt IRQ1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. This protection event can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

7.3.6 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to AIO6 and AIO7 through output buffers.

7.3.7 Analog Front End I/O (AIO)

Up to 6 AIOx pins are available in the device, depending on the product[1]. In the analog front-end I/O mode, the pin can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit or multiplexed to one of the signals in the configurable digital signal matrix CDSM. The signal can be set to active high (default) or active low, with V_{SYS} supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt IRQ2.

7.3.8 Push Button (PBTN)

The push button PBTN, when enabled, can be used by the MCU to detect a push button event and to put the system into an ultra low-power hibernate mode. Once the system is in hibernate mode, PBTN can be used to wake up the system.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 4s during normal operation. The PAC5526 may configure the push-button polarity to either active-low or active-high.

When configured for active-low, the push-button will be pulled up to 3.6V using a 50k resistor. Pulling the signal to ground will raise the push-button event.

When configured for active-high, the push-button will be pulled to ground using a 300k resistor. Pulling the pin above 2.2V will raise the push-button event. An internal built-in Zener diode is used to clamp the pin at 5.5V. An external resistor may be needed to clamp the current so that it does not exceed 0.5mA.

7.3.9 HP DAC and LP DAC

The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

[11] See the pin configuration and description for specific information on which pins are available in this product.

7.3.10 ADC Analog Input

The PAC5526 has several different analog input channels that may be used for analog-to-digital conversions using the MCU ADC. The diagram below shows the hierarchy of MUXes that are available for analog signal sampling.

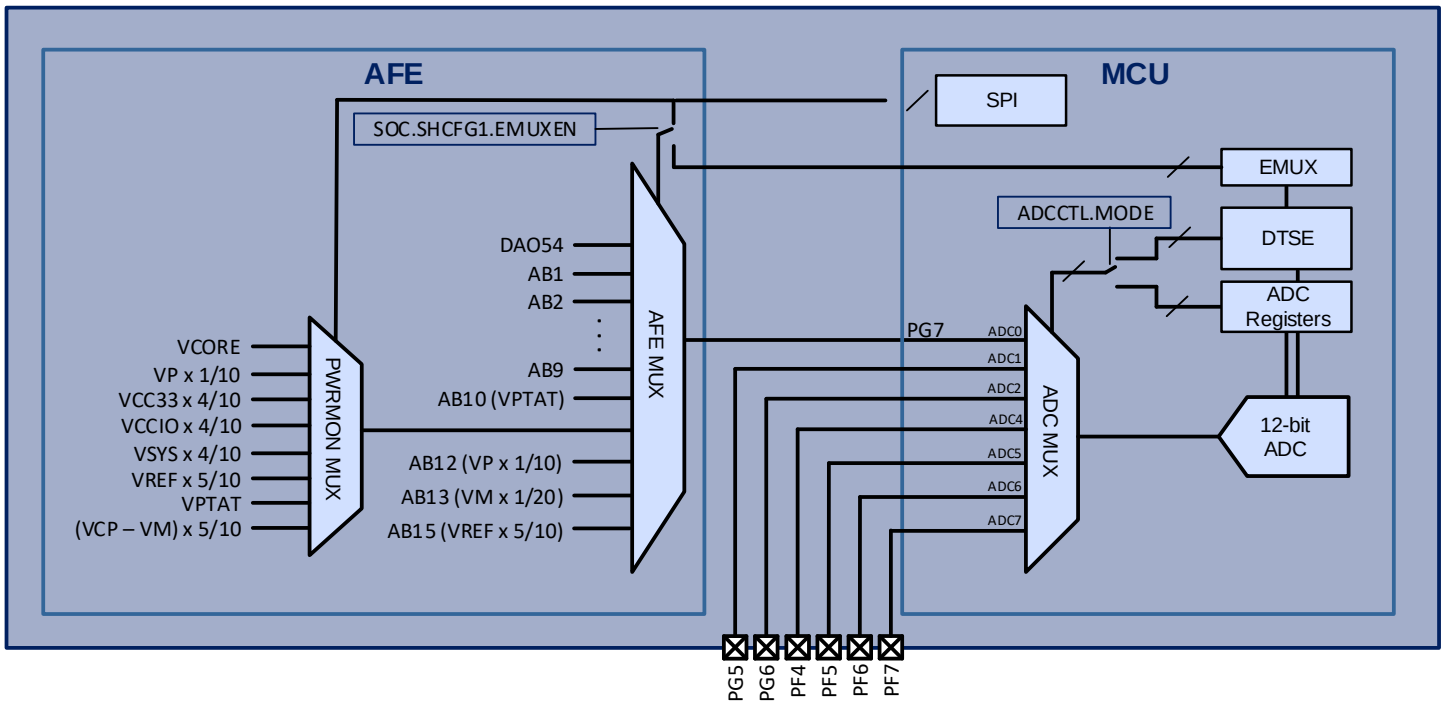


Figure 7 ADC Analog Input

The PAC5526 contains three analog MUXes as shown in the figure above:

- ADC MUX
- AFE MUX
- PWRMON MUX

The ADC MUX is an 8-channel MUX local to the ADC on MCU that is directly controlled by either by registers in the MCU, or automatically by the ADC DTSE. The output of the ADC MUX is sampled by the ADC. The ADC0 input to the ADC MUX is connected to the AFE MUX. ADC MUX input channels ADC1, ADC2 and ADC4-ADC7 are directly connected to package pins on the PAC5526.

The AFE MUX is a 16-to-1 multiplexer that selects between the a differential programmable gain amplifier output, AB1 through AB9, temperature monitor signal (VPTAT), power monitor signal (from the PWRMON MUX), attenuated VP voltage and attenuated VM voltage. The output of the AFE MUX is connected to channel ADC0 on the ADC MUX on the MCU. The ADC AFE MUX can be directly controlled or automatically scanned by the DTSE through the high-speed EMUX channel select.

The PWRMON MUX is an 8-channel MUX that selects between the internal regulators on the PAC5526 for diagnostic purposes. The output of the PWRMON MUX is connected to channel AB11 on the AFE MUX. The MUX channel select is available through the SPI SOC bus between the MCU and AFE.

For more information on controlling the various MUXes for ADC and DTSE sampling, see the PAC5526 User Guide.

7.3.11 Configurable Analog Signal Matrix (CASM)

The CASM has 9 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general-purpose comparator or phase comparator
- Routing the 10-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

7.3.12 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general-purpose comparator output signals to DB1 through DB7

7.3.13 Temperature Protection

The PAC5526 has two level of temperature protection. When the device reaches an internal temperature of 140°C, there is a mask-able interrupt that may be generated on IRQ1 to the MCU. The MCU may use this information to change the application behavior or disable the motor. The temperature warning status is cleared when the internal temperature falls below the temperature warning hysteresis threshold after the blanking time.

When the device reaches an internal temperature of 170C, the device will shut down all power supplies and gate drivers. The device will re-start when the internal temperature falls below the temperature fault hysteresis threshold after the blanking time.

7.4 Electrical Characteristics

The Electrical Characteristics for the CAFE are shown below.

7.4.1 Differential Programmable Gain Amplifier (DA)

Table 5 DA Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150		µA
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio	Gain = 8x, V_{DAxP}=V_{DAxN}=0V; T_A = 25°C	55	80		dB
	Slew rate	Gain = 8x	10			V/µs
$R_{INDIF;DA}$	Differential input impedance			80		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value			360	ns
$A_{VZI;DA}$	Differential amplifier gain (zero-ohm source impedance)	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP}=V_{DAxN}=0V,		8		
		T_A = 25°C	-2		2	%
		Gain = 16x		16		

T_A = -40°C to 125°C unless otherwise specified

7.4.2 Single-Ended Programmable Gain Amplifier (SA)

Table 6 SA Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	120	µA
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{OS;AMP}$	Input offset voltage	Gain = 8x	-10		10	mV
	Slew rate[2]	Gain = 8x	8	12		V/µs
$t_{ST;AMP}$	Settling time[2]	To 1% of final value		150	300	ns
$A_{V;AMP}$	Amplifier gain	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx}=125mV, T_A = 25°C	-2		2	%
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

T_A = -40°C to 125°C unless otherwise specified

7.4.3 General Purpose Comparator (CMP)

Table 7 CMP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;CMP}$	Operating supply current	Each enabled amplifier		35		µA
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$V_{OS;CMP}$	Input offset voltage	VCMPx=2.5V, TA=25°C	-10		10	mV
$V_{HYS;CMP}$	Hysteresis			22		mV
$t_{DEL;CMP}$	Comparator delay				1	µs

T_A = -40°C to 125°C unless otherwise specified.

[2] Guaranteed by design

7.4.4 Phase Comparator (PHC)

Table 8 PHC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;PHC}$	Operating supply current	Each enabled amplifier		35		µA
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$V_{OS;PHC}$	Input offset voltage	V_{PCMPx}=2.5V, T_A=25°C	-10		10	mV
$V_{HYS;PHC}$	Hysteresis			23		mV
$t_{DEL;PHC}$	Comparator delay	10mV difference input			1	µs

T_A = -40°C to 125°C unless otherwise specified.

7.4.5 Special Mode Electrical Characteristics (BUF)

Table 9 BUF Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ICMR;BUF}$	Input common mode range		0		3.5	V
$I_{CC;BUF}$	Operating supply current			60		µA
$V_{INOFF;BUF}$	Input to output offset voltage		-20		20	mV
$I_{OUT;BUF}$	Output current			2		mA
$C_{OUT;BUF}$	Output capacitance		0		2.2	nF

T_A = -40°C to 125°C unless otherwise specified.

7.4.6 Special Mode Electrical Characteristics (AIO<9:7>)

Table 10 Special Mode Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC}$	Operating supply current	Each enabled comparator		60		µA
$V_{HYS;SPEC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0 mV)		0		mV
		AIO<9:7>HYS = 01b (6 mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (12 mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (24 mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0 mV)		0		mV
		AIO<9:7>HYS = 01b (24 mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (48 mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (96 mV)	72	96	120	mV

T_A = -40°C to 125°C unless otherwise specified

7.4.7 VREF Reference Buffer (AIO7)

Table 11 VREF Reference Buffer Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ICMR;RBUF}$	Input common mode range		0.5		3.5	V
$I_{CC;RBUF}$	Operating supply current	Each enabled comparator		250		µA
$V_{INOFF;RBUF}$	Input offset voltage		-12		12	mV
$I_{OUT;RBUF}$	Output current		1			mA
C_{OUT}	Output capacitance		0		2.2	nF

T_A = -40°C to 125°C unless otherwise specified.

7.4.8 Analog Front End (AIO) Electrical Characteristics

Table 12 AIO Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode		1		MΩ
$V_{OL;AIO}$	Low-level output voltage	$I_{AIO<9:0>}$=7mA, pen-drain output mode			0.3	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

T_A = -40°C to 125°C unless otherwise specified

7.4.9 Push-Button (PBTN) Electrical Characteristics

Table 13 PBTN Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3.6V, push-button input mode; Active-low		50		kΩ
$R_{PD;PBTN}$	Pull-down resistance	To VSSA, push-button input mode; Active-high		300		kΩ

T_A = -40°C to 125°C unless otherwise specified

7.4.10 HP DAC and LP DAC Electrical Characteristics

Table 14 HPDAC and LPDAC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DACREF}	DAC reference voltage	T_A = 25°C	-0.5%	2.5	0.5%	V
		T_A = -40°C to 125°C	-0.9%	2.5	0.9%	
	HP 10-bit DAC INL		-2.5		2.5	LSB
	HP 10-bit DAC DNL		-2.5		2.5	LSB
	LP 10-bit DAC INL		-2.5		2.5	LSB
	LP 10-bit DAC DNL		-2.5		2.5	LSB

T_A = -40°C to 125°C unless otherwise specified

7.4.11 Temperature Protection Electrical Characteristics

Table 15 PBTN Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{WARN}	Temperature warning threshold			140		ºC
$T_{WARN;HYS}$	Temperature warning hysteresis			10		ºC
$T_{WARN;BLANK}$	Temperature warning blanking			10		µs
T_{FAULT}	Temperature fault threshold			165		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			10		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		µs

8 Application Specific Power Drivers™ (ASPD)

8.1 Features

- 3 high-side gate drivers with programmable gate driving up to 1A
- 3 low-side gate drivers with programmable gate driving up to 1A
- 100% duty cycle
- Cycle-by-cycle current limit
- Configurable fault protection

8.2 System Block Diagram

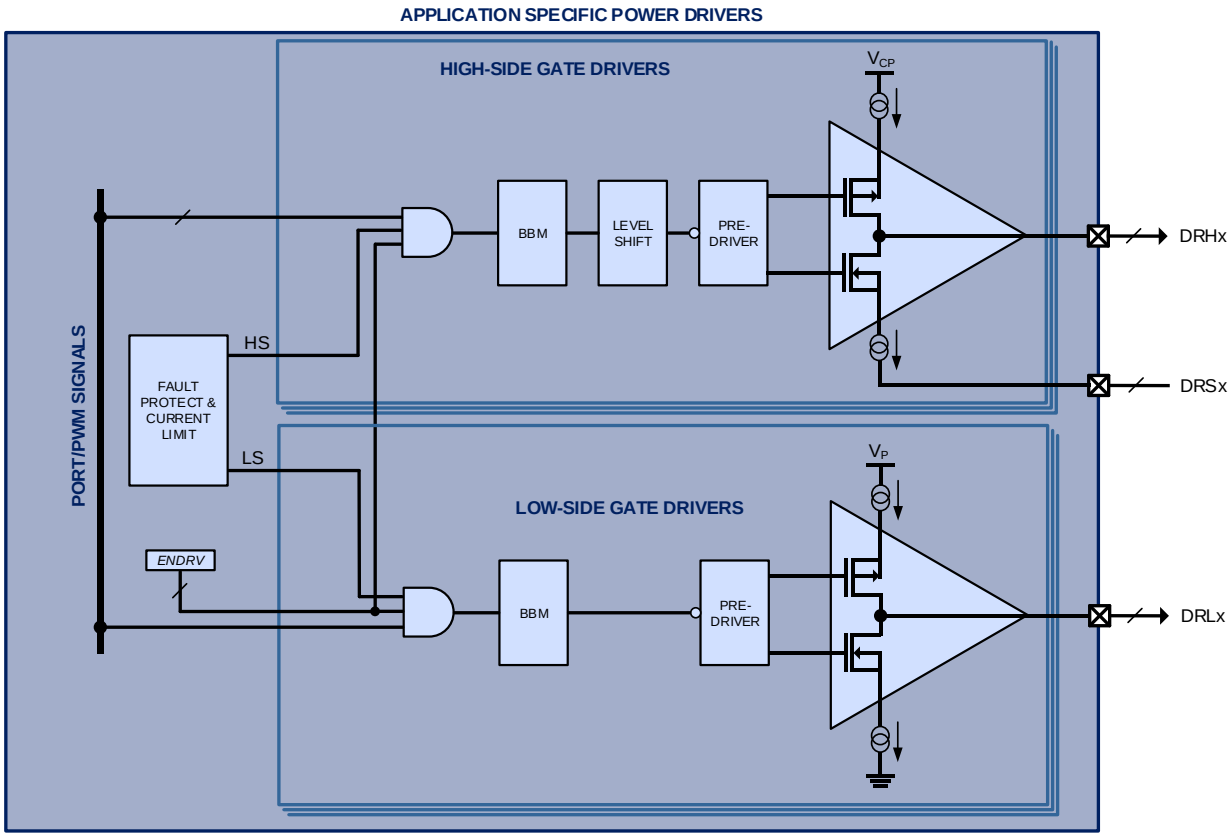


Figure 8 ASPD System Block Diagram

8.3 Functional Description

The Application Specific Power Drivers™ (ASPD) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

The high-side gate drivers are supplied by the charge pump output (VCP) which regulates to a voltage of VM + VP. The low-side gate drivers are supplied by VP MVBB (Medium-Voltage Buck-Boost). This converter may be configured to output 10V or 12V (default).

Each gate driver may be configured with variable current limit for internal gate driver slew rate control, to avoid external passive series components.

The figure below shows typical gate driver connections.

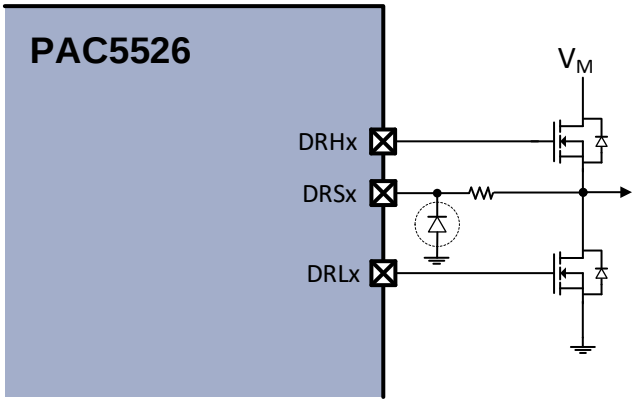


Figure 9 Typical Gate Driver Connections

8.4 Low-Side Gate Drivers

The DRLx low-side gate driver drives the gate of an external MOSFET switch between the low-level VSS power ground rail and high-level VP supply rail. The DRLx output pin has sink and source programmable output current capability of 1A.

Each low-side gate driver is controlled by a microcontroller PWM signal port which generates a PWM signal for on/off control of the gate driver. The gate driver may be configured for cycle-by-cycle current limit control (CBCCTL), which is described in the Configurable Analog Front-End section.

8.5 High-Side Gate Drivers

The DRHx high-side gate driver drives the gate of an external MOSFET switch between its low-level DRSx driver source and the motor voltage + charge pump output voltage (VM + VCP) during steady-state.

Each low-side gate driver is controlled by a microcontroller PWM signal port which generates a PWM signal for on/off control of the gate driver. The gate driver may be configured for cycle-by-cycle current limit control (CBCCTL), which is described in the Configurable Analog Front-End section.

The DRHx output pin has sink and source programmable output current capability of 1A. The DRSx pin is designed to tolerate momentary switching negative spikes down to -6V without affecting the DRHx output state.

To ensure functionality and reliability, the DRSx pin must not exceed the peak and undershoot limit values shown. This should be verified by probing the DRSx pins directly relative to VSS pin. A small resistor and diode clamp for the DRSx pin can be used to make

sure that the pin voltage stays within the negative limit value. In addition, the high-side slew rate dV/dt must be kept within ±5V/ns for DRSx. This can be achieved by adding a resistor-diode pair in series, and an optional capacitor in parallel with the power switch gate.

8.6 Power Drivers Control

All power drivers are initially disabled from power-on-reset. To enable the power drivers, the MCU must first set the driver enable bit.

Refer to the PAC55XX Family User Guide and PAC5526 Device User Guide for additional information on power drivers control programming.

8.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as the protection event (PR) signal. The PR signal from the CAFE can be used to disable the low-side and high-side gate drivers depending on the PR mask bit settings.

8.8 Gate Driver Programmable Current

The PAC5526 high-side and low-side gate drivers support programmable current output. This allows the gate driver to internally control the slew rate to the MOSFET gate, which eliminates the need for external series components to control the slew rate.

For both the high-side and low-side gate drivers, the user may configure the source and sink current of the gate drivers, which will be used during the miller plateau of V_{GS} to control the slew rate. The user may configure the duration of the controlled current and the current output of the gate drivers during this time.

The user may configure the controlled current between 60mA and 1A in 8 steps for both the high-side and low-side gate drivers, for sink and source current independently.

For more information on the register settings for controlling duration and current output to the gate drivers, see the PAC5526 User Guide.

8.9 Electrical Characteristics

The Electrical Characteristics for the ASPD are shown below.

8.9.1 Low-Side Gate Drivers

Table 16 Low-Side Gate Drivers Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
$R_{PD;DRL}$	Pull-down resistor value	V_{DRL} = 3.5V, **ENDRV** = 0b or VP < $V_{UVLO;VP}$			5		kΩ
$T_{BLANK;DRL}$	Blanking time setting for driver DRLx to target value	000b			4.7		µs
		001b			2.5		
		010b			1.8		
		011b			1.3		
		100b			1.1		
		101b			0.9		
		110b			0.75		
		111b			0.5		
$I_{OHPK;DRL}$	High-level pulsed peak source current	10µs pulse; Overdrive voltage = 6V	000b		60		mA
			001b		120		
			010b		180		
			011b		240		
			100b		500		
			101b		750		
			110b		850		
			111b		1000		
$I_{OLPK;DRL}$	Low-level pulsed peak sink current	10µs pulse; Overdrive voltage = 3V	000b		70		mA
			001b		140		
			010b		210		
			011b		280		
			100b		540		
			101b		750		
			110b		850		
			111b		1000		

VP = 12V and T_A = 25°C unless otherwise specified

8.9.2 High-Side Gate Drivers

Table 17 High-Side Gate Drivers Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{DRS}	Level-shift driver source voltage range	Repetitive, 10µs pulse		-5		48	V
		Steady state		0		40	
$R_{PD;DRH}$	Pull-down resistor value				300		kΩ
$T_{BLANK;DRH}$	Blanking time setting for driver DRLx to target value	000b			4.7		µs
		001b			2.5		
		010b			1.8		
		011b			1.3		
		100b			1.1		
		101b			0.9		
		110b			0.75		
		111b			0.5		
$I_{OHPK;DRH}$	High-level pulsed peak source current	10µs pulse; Overdrive voltage = 6V	000b		60		mA
			001b		120		
			010b		180		
			011b		240		
			100b		500		
			101b		750		
			110b		850		
			111b		1000		
$I_{OLPK;DRH}$	Low-level pulsed peak sink current	10µs pulse; Overdrive voltage = 3V	000b		70		mA
			001b		140		
			010b		210		
			011b		280		
			100b		540		
			101b		750		
			110b		850		
			111b		1000		

VP = 12V and T_A = 25°C unless otherwise specified

9 SOC Control Signals

The MCU has access to the Analog Sub-system on the PAC5526 through certain digital peripherals. The functions that the MCU may access from the Analog Sub-System are:

- High-side and Low-side Gate Drivers
- SPI Interface for Analog Register Access
- ADC EMUX
- Analog Sub-system Interrupts

9.1 High-side and Low-Side Gate Drivers

The high-side and low-side gate drivers on the PAC5526 are controlled by PWM outputs of the timer peripherals on the MCU. The timer peripheral generates the PWM output. The PWM timer may be configured to generate a complementary PWM output (high-side and low-side gate drive signals) with hardware controlled dead-time.

These signals are sent to the gate drivers in the Analog Sub-system that create the high and low side gate drivers for the external inverter.

The user may choose to enable or not enable the DTG (Dead-time Generator). The diagram below shows the block diagram of the PWM timer, DTG and ASPD gate drivers.

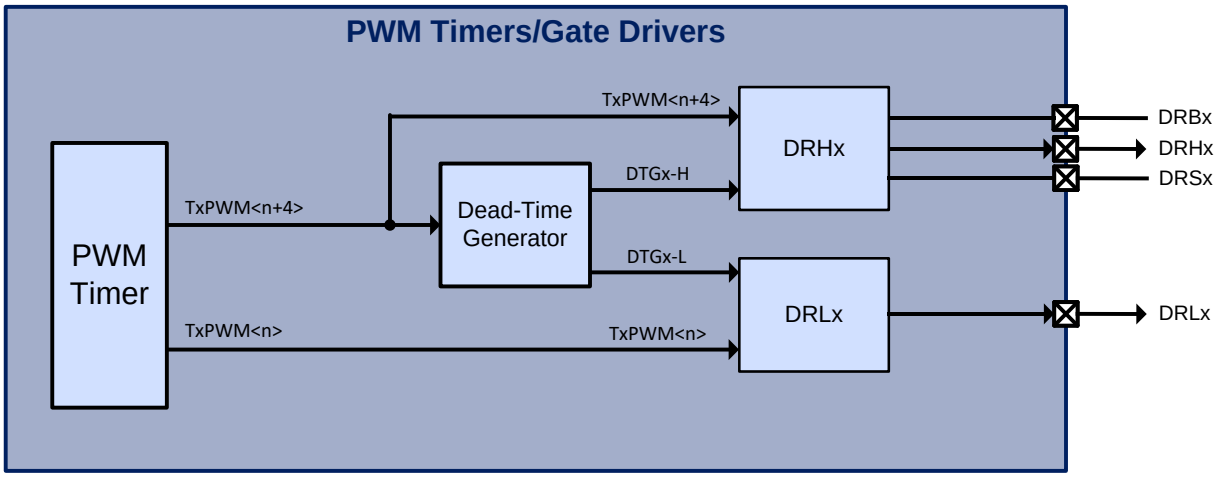


Figure 10 SOC Signals for Gate Drivers

Each timer peripheral that drives the DTG and ASPD Gate Drivers has two PWM outputs that are connected to the gate drivers: TxPWM<n> and TxPWM<n+4>. If the Dead-Time Generator is disabled TxPWM<n> is connected to the DRLx gate driver output and TxPWM<n+4> is connected to the DRHx gate driver output.

If the DTG is enabled, the TxPWM<n+4> is used to generate the complementary high-side and low-side output (DTGx-H and DTGx-L). DTGx-H is connected to the DRHx output and DTGx-L is connected to the DRLx output.

The MCU allows flexibility the assignment of PWM outputs to ASPD gate drivers. The tables below shows which PWM outputs are available for each gate driver.

For applications that drive half-bridge or full-bridge topologies, the DTG will be enabled to allow a complementary output with dead-time insertion.

Table 18 PWM to ASPD Gate Driver Options (DTG Enabled)

Gate Driver	PWM Input Options
DRH3/DRL0	TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4
DRH4/DRL1	TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5
DRH5/DRL2	TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6

For applications that are not driving half-bridge topologies, the DTG is disabled and the PWM outputs are directly connected to the gate drivers.

Table 19 PWM to ASPD Gate Driver Options (DTG Enabled)

Gate Driver	PWM Input Options
DRH3	TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4
DRH4	TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5
DRH5	TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6
DRL0	TAPWM0 TBPWM0 TCPWM0 TDPWM0
DRL1	TAPWM1 TBPWM1 TCPWM1 TDPWM1
DRL2	TAPWM2 TBPWM2 TCPWM2 TDPWM2

9.2 SPI SOC Bus

The SPI SOC bus is used for reading and writing registers in the Analog Sub-System. The PAC5526 allows both USARTA and USARTB to be used as the SPI master to read and write registers in the Analog Sub-System.

The table below shows which peripherals and which IO pins should be used for this interface.

Table 20 SPI SOC Bus Connections

SPI Signal	USART Signal	IO Pin
SCLK	USASCLK	PA3
	USBSCLK	PA3
MOSI	USAMOSI	PA4
	USBMOSI	PA4
MISO	USAMISO	PA5
	USBMISO	PA5
SS	USASS	PA6
	USBSS	PA6

9.3 ADC EMUX

The ADC EMUX is a write-only serial bus that the ADC DTSE uses for instructing the CAFE to perform MUX changes, activate Sample and Hold, etc.

The table below shows the MCU pins that are used by the ADC EMUX in the PAC5526.

Table 21 ADC EMUX SOC Bus Connections

SPI Signal	USART Signal	IO Pin
SCLK	USASCLK	PA3
	USBSCLK	PA3

9.4 Analog Interrupts

The Analog sub-system has two interrupts that it can generate for different conditions. The table below shows the two different interrupts, the interrupt conditions and the IO pin that the interrupts are connected to.

Table 22 Analog Interrupt SOC Bus Connections

SPI Signal	USART Signal	IO Pin
nIRQ1	HPCOMP/LPCOMP Comparator Protection for Over-current and Over-Voltage events	PA7
nIRQ2	BEMF and Special Mode Comparator, including phase to phase comparator, AIO6/AIO7/AIO8/AIO9 interrupt	PA0

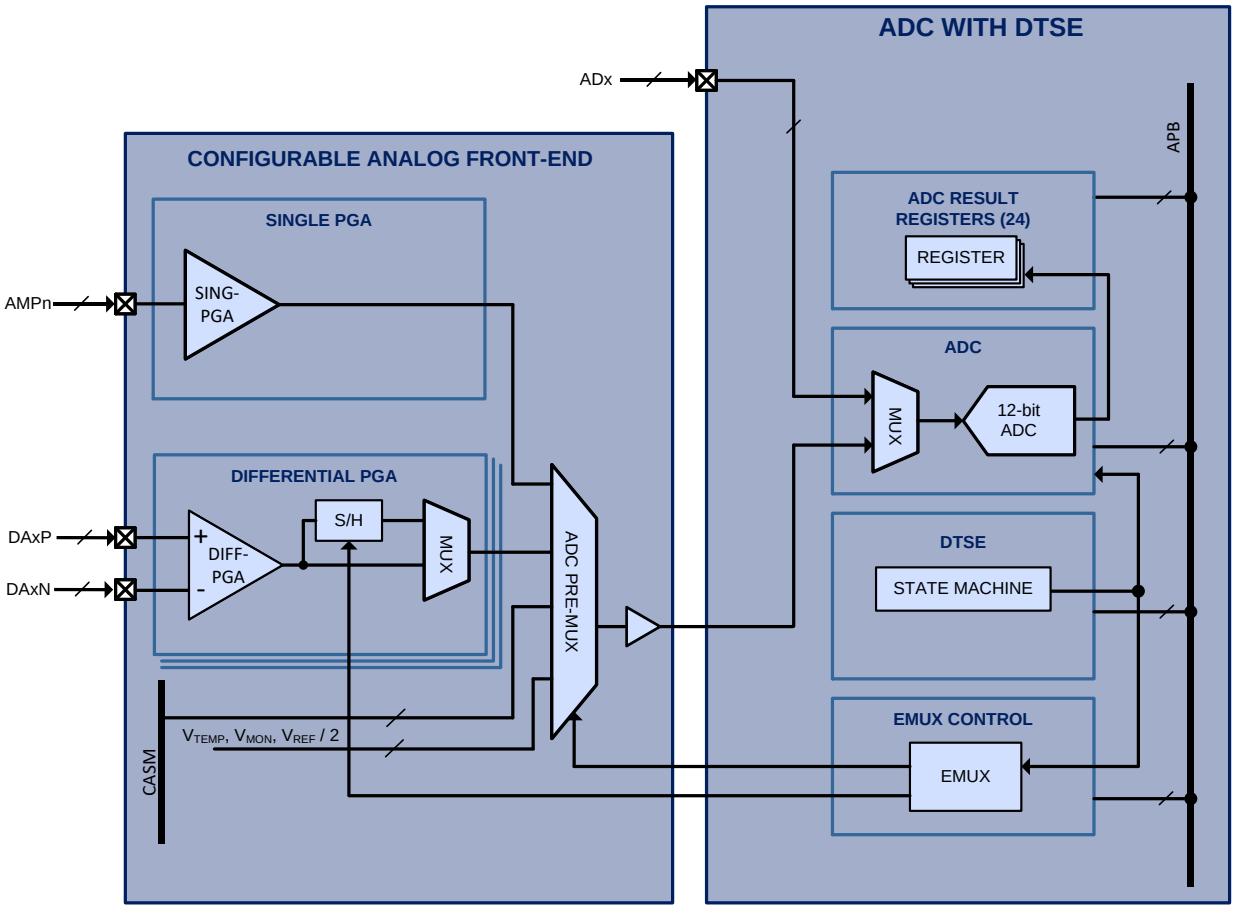
10 ADC/DTSE

10.1 Features

- 12-bit 2.5MSPS SAR ADC
- Configurable Dynamic Triggering and Sequence Engine (DTSE)
- High-speed sample and hold for current measurement
- Current, power and temperature monitoring using DTSE

10.2 System Block Diagram

Figure 11 ADC/DTSE System Block Diagram



10.3 Functional Description

10.3.1 ADC

The analog-to-digital converter (ADC) is a 12-bit successive approximation register (SAR) ADC with 400ns conversion time and up to 2.5 MSPS capability. The integrated analog multiplexer allows selection from up to 8 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs as well as temperature and V_{REF} / 2.

The ADC contains a power down mode, and the user may configure the ADC to interrupt the MCU for the completion of a conversion when in manual mode. The ADC may be configured for either repeating or non-repeating conversions or conversion sequences.

10.3.2 Dynamic Triggering and Sample Engine (DTSE)

The Dynamic Triggering and Sample Engine (DTSE) is a highly configurable automatic sequencer that allows the user to configure automatic sampling of their application-specific analog signals without any interaction from the micro-controller core. The DTSE also contains a pseudo-DMA engine that copies each of up to 24 conversion results to dedicated memory space and can interrupt the MCU when complete.

The DTSE has up to 32 input triggers, from PWM Timers A, B, C and D for either the rising, falling or rising and falling PWM edges. The user may also force any trigger sequence by writing a register via firmware. The user can configure the DTSE to chain from 1 to 24 conversions to any PWM trigger.

The DTSE has a flexible interrupt structure that allows up to 24 interrupts to be configured at the completion of any individual conversion. The user may configure one of four different IRQ signals when generating an interrupt during sequence conversions. The IRQ may be generated at the end of a conversion sequence, or at the end of a series of conversions. The user may select one of four IRQs for conversions, and each may be assigned a different interrupt priority.

Each of the 24 conversions has dedicated results registers, so that the pseudo-DMA engine has dedicated storage for each of the conversion results.

10.3.3 EMUX Control

A dedicated low latency interface controllable by the DTSE or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without microcontroller interaction.

For more information on the ADC and DTSE, see the PAC55XX Family User Guide.

10.4 Electrical Characteristics

The Electrical Characteristics for the ADC and DTSE are shown below.

Table 23 ADC/DTSE Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{ADCCLK}	ADC conversion clock input				40	MHz
$f_{ADCCONV}$	ADC conversion time				16	ADCCLK
		f_{ADCCLK} = 40MHz; PCx, PDx, PEx, PFx, PGx pins			400	ns
$t_{ADC;SH}$	ADC sample and hold time	f_{ADCCLK} = 40MHz;			800	ns
t_{ADCSH}	ADC sample and hold time	AIO[9:0] pins f_{ADCCLK} = 40MHz			100	ns
$t_{ADC;CVT}$	ADC analog conversion time				4	ADCCLK
C_{ADCIC}	ADC input capacitance	ADC MUX input		1		pF
	ADC resolution			12		bits
	ADC effective resolution		10.5			bits
	ADC differential non-linearity (DNL)	F_{ADCCLK} = 25MHz		±0.5		LSB
	ADC resolution	F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC integral non-linearity (INL)	F_{ADCCLK} = 25MHz		±0.5		LSB
	ADC differential non-linearity (DNL)	F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
V_{REFADC}	ADC reference input voltage	VREF = 2.5V		2.5		V
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz

T_A = -40°C to 125°C unless otherwise specified

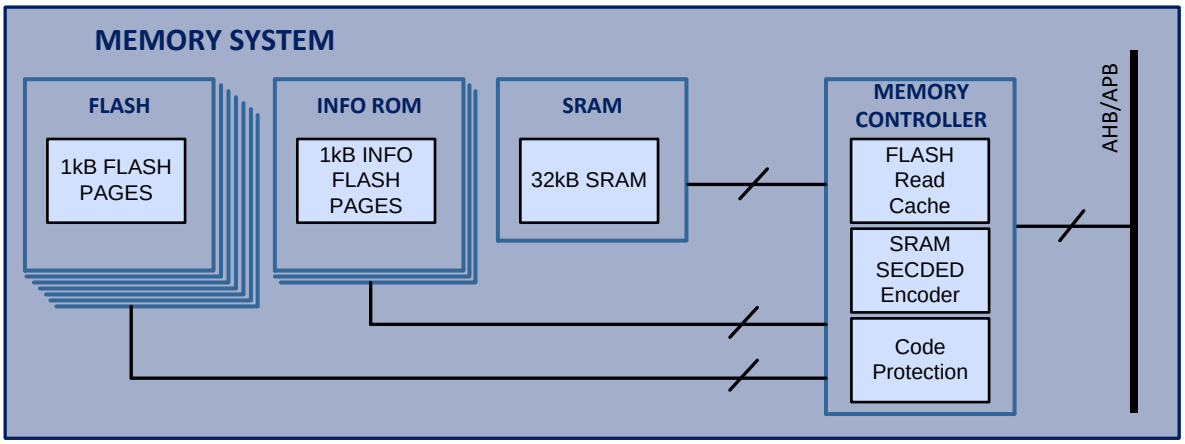
11 Memory System

11.1 Features

- 128kB Program FLASH
  - 30k Program/Erase cycles
  - 10 years data retention
  - FLASH look-ahead buffer for optimizing access
- 1kB INFO-1 FLASH
- 1kB INFO-2 FLASH
  - Device ID, Unique ID, trim and manufacturing data
- 32kB SRAM
  - 150MHz access for code or data
  - SECDE for read/write operations
- User-configurable Code Protection

11.2 System Block Diagram

Figure 12 Memory System Block Diagram



11.3 Functional Description

The PAC5526 contains multiple banks of FLASH memory, SRAM memory as well as peripheral control registers that are accessible to the MCU in a flat memory map.

11.3.1 Program FLASH

The PAC55XX Memory Controller provides access to 128 1kB pages of main program FLASH for a total of 128kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

The PAC55XX Memory Controller provides a FLASH read buffer that optimizes access from the MCU to the FLASH memory. This look ahead buffer monitors the program execution and fetches instructions from FLASH before they are needed to optimize access to this memory.

11.3.2 INFO FLASH

The PAC55XX Memory Controller provides access to the INFO-1, INFO-2 and INFO-3 FLASH memories, which are each a single 1kB page for a total of 3kB of memory.

INFO-1 and INFO-2 are read-only memories that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC55XX.

INFO-3 is available to the user for data or program storage.

11.3.3 SRAM

The PAC55XX Memory Controller provides access to the 32kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses.

The PAC55XX Memory Controller can read or write data from RAM up to 150MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH, INFO-1 or INFO-2 FLASH.

The PAC55XX Memory Controller also has an SECDED encoder, capable of detecting and correcting single-bit errors, and detecting double-bit errors. The user may read the status of the encoder, to see if a single-bit error has occurred. The user may also enable an interrupt upon detection of single-bit errors. Dual-bit errors can be configured to generate an interrupt in the PAC55XX.[3]

For more information on the PAC55XX Memory Controller, see the PAC55XX Family User Guide.

[3] Note that when writing half-word or single bytes to SRAM, the memory controller must perform a read-modify write to memory to perform the SECDED calculation. These operations will take more than one clock cycle to perform for this reason.

11.3.4 Code Protection

The PAC5526 allows the user to configure a 4-level code protection scheme to secure code from being read from the device.

There are four levels of code protection available as shown in the table below.

Table 24 Code Protection Levels

Level	Name	Features
0	UNLOCKED	▪ No restrictions
1	RW PROTECTION	▪ SWD enabled ▪ Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region
2	SWD DISABLED	▪ SWD disabled ▪ Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region
3	SWD PERMANENTLY DISABLED	▪ SWD disabled ▪ Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region ▪ No recovery

11.4 Electrical Characteristics

The Electrical Characteristics for the Memory System are shown below.

Table 25 Memory System Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
FLASH						
$t_{READ;FLASH}$	FLASH word read time		40			ns
$t_{WRITE;FLASH}$	FLASH work write time		30			µs
$t_{PERASE;FLASH}$	FLASH page erase time				2	ms
$t_{MERASE;FLASH}$	FLASH mass erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles		30k			cycles
$t_{DF;FLASH}$	FLASH data retention		10			years
SRAM						
$t_{ACC;SRAM}$	SRAM access time	HCLK = 150MHz; Word (32-bits), aligned	6.67			ns
		HCLK = 150MHz; Half-word (16-bits), byte (8-bits), aligned	6.67			ns

T_A = -40°C to 125°C unless otherwise specified

12 System and Clock Control (SCC)

12.1 Features

- 20MHz Ring Oscillator
- High-accuracy 1.25% trimmed 4MHz RC oscillator
- External Clock Input for External Clocks up to 20MHz
- PLL with 1MHz to 50MHz input, 62.5MHz to 300MHz output
- Clock dividers for all system clocks
- Clock gating for power conservation during low-power operation

12.2 System Block Diagram

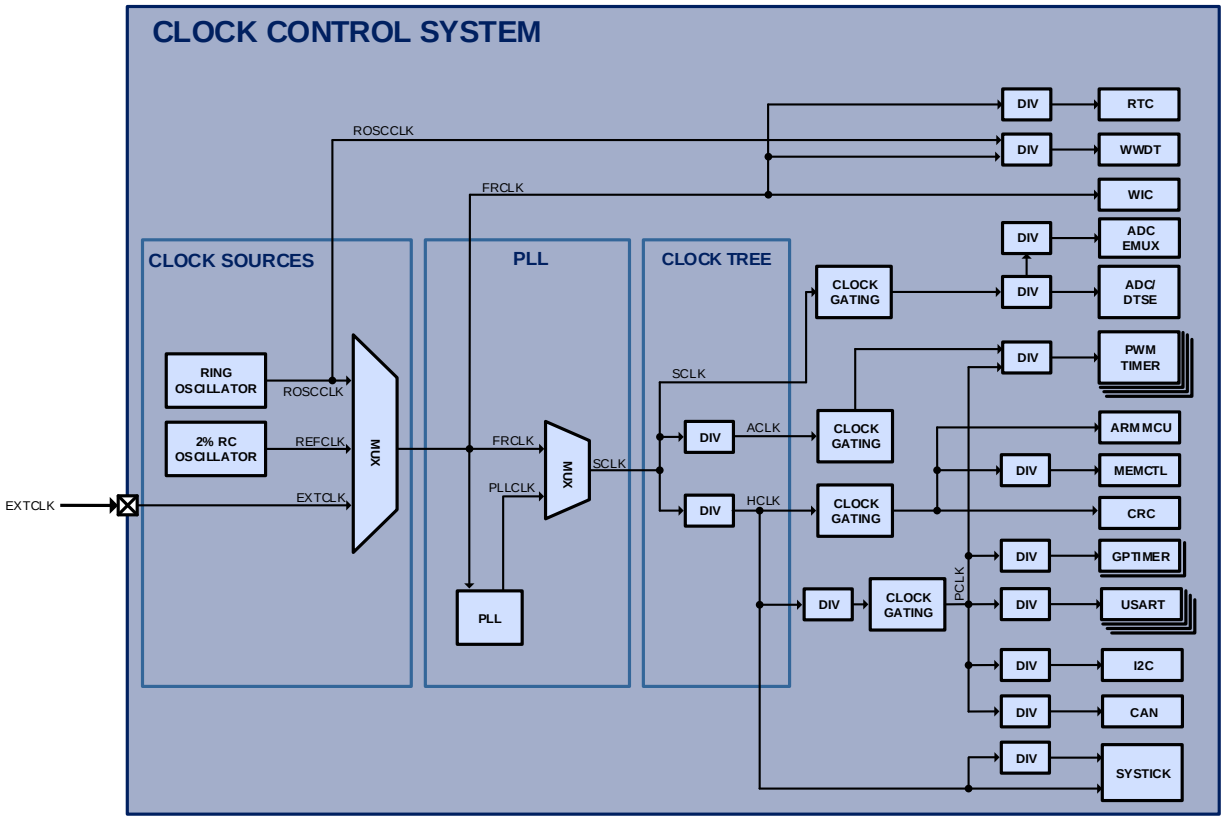


Table 26 Clock Control System Block Diagram

12.3 Functional Description

The Clock Control System (CCS) controls the clock system and clock gating for the PAC5526. There are three independent clock sources: the Ring Oscillator, Reference Clock and External Clock Input.

12.4 Clock Sources

12.4.1 Ring Oscillator

The Ring Oscillator (ROSC) is an integrated 20MHz clock oscillator that is the default system clock, and is available by default when the PAC55XX comes out of reset. The output of the ROSC is the ***ROSCCLK*** clock. The ***ROSCLK*** may be selected as the ***FRCLK*** clock and may supply the WWDT, for applications that need an independent clock source or need to continue to be clocked when the system is in a low-power mode.

The ROSC may be disabled by the user by a configuration register.

12.4.2 Reference Clock

The Reference Clock (***REFCLK***) is an integrated 2% trimmed 4MHz RC clock. This clock is suitable for many applications. This clock may be selected as the ***FRCLK*** and can be used as the input to the PLL and is used to derive the clock for the MMPM.

12.4.3 External Clock Input

The External Clock Input (EXTCLK) is a clock input available through the digital peripheral MUX, and allows the drive the clock system by a 50% duty cycle clock of up to 20MHz. This clock may be selected as FRCLK and can be used as the input the PLL (as long as the accuracy is better than +/- 2%).

12.5 PLL

The PAC55XX contains a Phase Lock Loop (PLL) that can generate very high clock frequencies up to 300MHz for the peripherals and timers in the device. The input to the PLL is the ***FRCLK*** and must be from the ***EXTCLK*** or ***REFCLK*** clock sources

The input to the PLL must be between 1MHz – 50MHz and the output can be configured to be from 62.5MHz to 300MHz. The user can configure the PLL to generate the desired clock output based on a set of configuration registers in the CCS. The output of the PLL is the ***PLLCLK*** clock. The user may configure a MUX to generate the SCLK clock from ***PLLCLK*** or from ***FRCLK***.

In addition to configuring the PLL output frequency, the PLL may be enabled, disabled and bypassed through a set of configuration registers in the CCS.

12.6 Clock Tree

The following are the system clocks available in the clock tree. See the section below to see which clocks are available for each of the digital peripherals in the system.

12.6.1 FRCLK

The free-running clock (***FRCLK***) is generated from one of the four clock sources (***ROSCCLK***, ***EXTCLK*** or ***REFCLK***). This clock may be used by the WWDT and the RTC, for configurations that turn off all other system clocks during low power operation.

The ***FRCLK*** or ***PLLCLK*** is selected via a MUX and the output becomes ***SCLK***.

12.6.2 SCLK

The System Clock (***SCLK***) generates two system clocks: ***ACLK*** and ***HCLK***. Each of these system clocks has their own 3b clock divider and is described below.

12.6.3 PCLK

The Peripheral Clock (***PCLK***) is used by most of the digital peripherals in the PAC55XX. This clock has a 3b clock divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, most of the peripherals that use ***PCLK*** also have their own clock dividers so that this clock can be further divided down to meet the application's needs.

12.6.4 ACLK

The Auxiliary Clock (***ACLK***) may be optionally used by the PWM timer block in the PAC55XX in order to generate a very fast clock for PWM output to generate the best possible accuracy and edge generation.

This clock has a 3b clock divider and also has clock gating support, which disables this clock output when the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, the ***ACLK*** is an optional input for just the PWM timer block in the PAC55XX.

12.6.5 HCLK

The AHB Clock (***HCLK***) is used by the Arm® Cortex®-M4 MCU and Memory Controller peripheral. This clock has a 3b divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

HCLK supplies PCLK with its clock source.

12.7 Electrical Characteristics

The Electrical Characteristics for the System and Clock Control module are shown below.

Table 27 System and Clock Control Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Clock Tree (FRCLK, FCLK, PCLK, ACLK, HCLK)						
f_{FRCLK}	Free-running clock frequency				25	MHz
f_{SCLK}	System clock frequency				300	MHz
f_{PCLK}	Peripheral clock frequency	After PCLK divider			150	MHz
f_{ACLK}	Auxiliary clock frequency	After ACLK divider			300	MHz
f_{HCLK}	High-speed clock frequency	After HCLK divider			150	MHz
Internal Oscillators						
$f_{ROSCCLK}$	Ring oscillator frequency			20		MHz
$f_{TRIM;REFCLK}$	Trimmed RC oscillator frequency	TA = 25°C	- 1.25%	4	1.25%	MHz
		TA = -40°C to 125°C	-2.25%	4	2%	MHz
$f_{JITTER;REFCLK}$	Trimmed RC oscillator clock jitter	TA = -40°C to 85°C		0.5		%
PLL						
$\mathbf{f_{IN;PLL}}$	PLL input frequency range		1		50	MHz
$\mathbf{f_{OUT;PLL}}$	PLL output frequency range		62.5		300	MHz
$\mathbf{t_{SETTLE;PLL}}$	PLL setting time	T_A = 25°C, PLL settled			15	µs
		T_A = 25°C, **PLLLOCK** = 1		200	500	µs
$\mathbf{t_{JITTER;PLL}}$	PLL period jitter	RMS		25		ps
		Peak to peak			100	ps
	PLL duty cycle		40	50	60	%
External Clock Input (EXTCLK)						
$\mathbf{f_{EXTCLK}}$	External Clock Input Frequency				20	MHz
	External Clock Input Duty Cycle		40		60	%
$\mathbf{V_{IH;EXTCLK}}$	External Clock Input high-level input voltage		2.1			V
$\mathbf{V_{IL;EXTCLK}}$	External Clock Input low-level input voltage				0.825	V

T_A = -40°C to 125°C unless otherwise specified

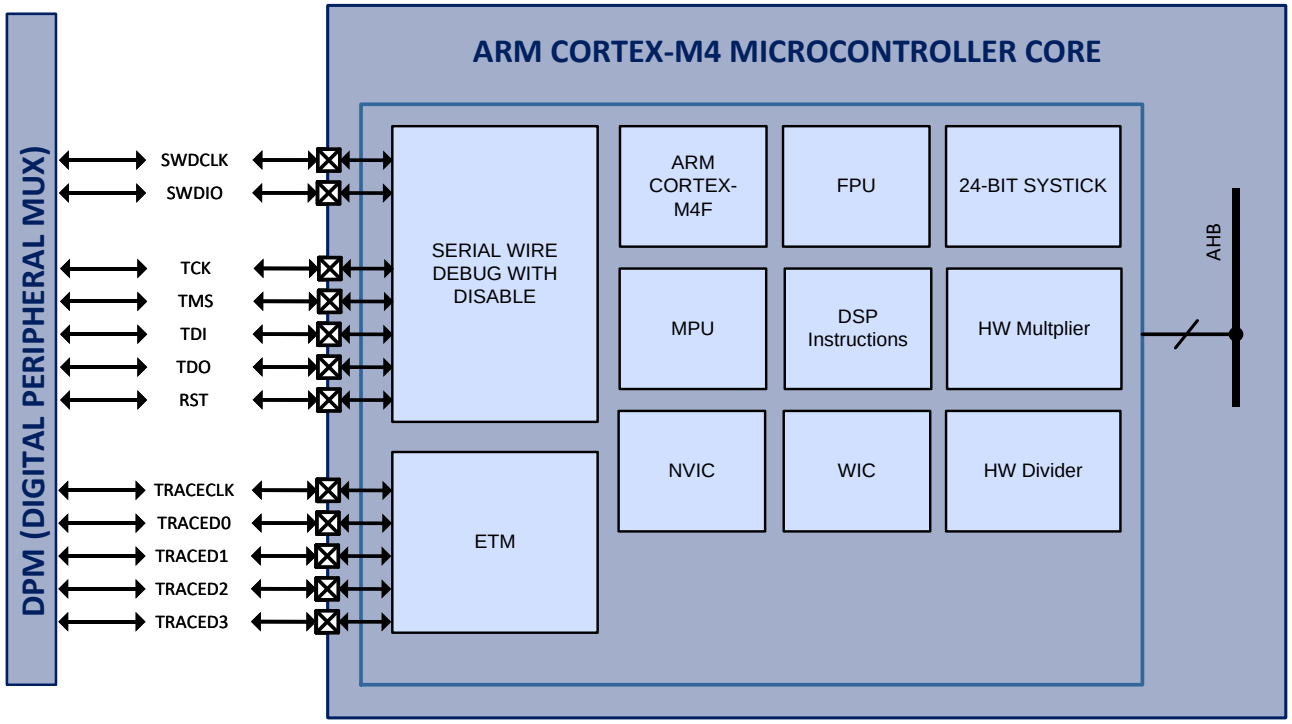
13 Arm® Cortex®-M4F MCU Core

13.1 Features

- Arm® Cortex®-M4F core
- SWD or JTAG Debug
- SWD/JTAG code security
- Embedded Trace Module (ETM) for instruction tracing
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC) with 29 user interrupts and 8 levels of priority
- Floating Point Unit (FPU)
- Wakeup Interrupt Controller (WIC)
- 24-bit SysTick Count-down Timer
- Hardware Multiply and Divide Instructions

13.2 System Block Diagram

Figure 13 Arm Cortex-M4F MCU System Block Diagram



13.3 Functional Description

The Arm® Cortex®-M4F microcontroller core is configured for little endian operation and includes hardware support for multiplication and division, DSP instructions as well as an IEEE754 single-precision Floating Point Unit (FPU).

The MCU also contains an 8-region Memory Protection Unit (MPU), as well as a Nested Vector Interrupt Controller (NVIC) that supports 29 user interrupts with 8 levels of priority. There is a 24-bit SysTick count-down timer.

The Arm® Cortex®-M4F supports sleep and deep sleep modes for low power operation. In sleep mode, the Arm® Cortex®-M4F is disabled. In deep sleep mode, the MCU as well as many peripherals are disabled. The Wakeup Interrupt Controller (WIC) can wake up the MCU when in deep sleep mode by using any GPIO interrupt, the Real-Time Clock (RTC) or Windowed Watchdog Timer (WWDT). The PAC55XX also supports clock gating to reduce power during deep sleep operation.

The debugger supports 4 breakpoint and 2 watch-point unit comparators using the SWD or JTAG protocols. The debug serial interfaces may be disabled to prevent memory access to the firmware during customer production.

For more information on the detailed operation of the Microcontroller Core in the PAC55XX, see the PAC55XX Family User Guide.

13.4 Application Typical Current Consumption

The MCU clock configuration and peripheral configuration have a large influence on the amount of load that the power supplies in the PAC55XX will have.

The table below shows a number of popular configurations and what the typical power consumption will be on the VSYS and VCORE power supplies in the PAC55XX.

Table 28 PAC55XX Application Typical Current Consumption

CLOCK CONFIGURATION	MCU PERIPHERALS	MCU STATE	IVSYS	IVCORE	IVCC33
CLKREF = 4MHz PLL Disabled ACLK=HCLK=PCLK=SCLK=MCLK = 16MHz ROSCCLK Enabled FRCLK MUX = ROSCCLK	All peripherals disabled	Halted	9.5mA	2.3mA	n/a
CLKREF = 4MHz PLLCLK = 30MHz ACLK=HCLK=PCLK=SCLK= 16MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	10.5mA	3.5mA	n/a
CLKREF = 4MHz PLLCLK = 150MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	20mA	13.5mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	22mA	15mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF ADCCLK = 40MHz	ADC enabled (repeated conversions)	Halted	36mA	16mA	13.5mA
CLKREF = 4MHz	All peripherals disabled	CPU Executes	8.5mA	2.2mA	n/a

PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF		instructions from FLASH			
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	Timer A enabled; TAPWM[7:0] enabled; Fs = 100kHz; 50% duty cycle	Halted	22mA	15mA	n/a

13.5 Electrical Characteristics

The Electrical Characteristics for the System and Clock Control module are shown below.

Table 29 System and Clock Control Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{HCLK}	MCU Clock				50	MHz
$I_{Q;VCORE}$	V_{CORE} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			2	mA
		PAC5526 Hibernate Mode			0	mA
$I_{Q;VSYS}$	V_{SYS} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			8	mA
		PAC5526 Hibernate Mode			15	µA
$I_{Q;VCCIO}$	VCCIO quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.15	mA
		PAC5526 Hibernate Mode			0	mA
$I_{Q;VCC33}$	VCC33 quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.4	mA
		PAC5526 Hibernate Mode			0	mA

14 IO Controller

14.1 Features

- 3.3V Input/Output, 4.6V input tolerant
- Push-Pull Output, Open-Drain Output or High-Impedance Input for each IO
- Configurable Pull-up and Pull-down for each IO (60k)
- Configurable Drive Strength for each IO (up to 24mA)
- Analog Input for some IOs
- Edge-sensitive or level-sensitive interrupts
- Rising edge, falling edge or both edge interrupts
- Peripheral MUX allowing up to 8 peripheral selections for each IO
- Configurable De-bouncing Circuit for each IO

14.2 System Block Diagram

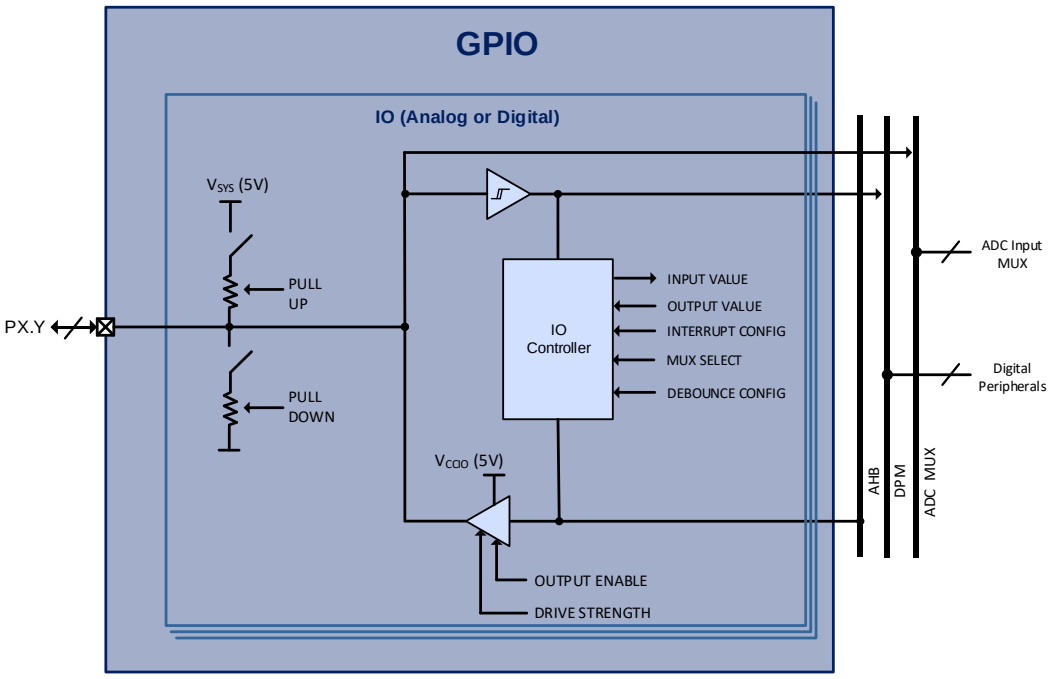


Figure 14 IO Controller System Block Diagram

14.3 Functional Description

14.3.1 IO Controller

The PAC55XX IO cells can be used for digital input/output and analog input for the ADC. All IOs are supplied by the V_{CCIO} (3.3V) power supply.

Each IO can be configured for digital push-pull output, open-drain output or high-impedance input. Each IO also has a configurable 60k weak pull-up or weak pull-down that can be enabled.

NOTE: Configuring both pull-up and pull-down at the same time may cause device damage and should be avoided.

Each IO has a configurable de-bouncing filter that can be enabled or disabled, to help filter out noise.

All IO have interrupt capability. Each pin can be configured for either level or edge sensitive interrupts, and can select between rising edge, falling edge and both edges for interrupts. Each pin has a separate interrupt enable and interrupt flag.

Some of the IO on the PAC5526 can be configured as an analog input to the ADC.

14.3.2 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply (VCCIO). Current will be injected into the GPIO when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, the PAC52XX family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

14.3.3 Peripheral MUX

The Peripheral MUX (DPM) allows the IO controller to select one of up to four peripheral functions for each IO pin. Note that if the pin is configured for analog input, the peripheral MUX is bypassed.

The Peripheral MUX for the PAC5526 is shown below.

Table 30 Peripheral MUX settings

	PERIPHERAL MUX SETTINGS								
PIN	S0	S1	S2	S3	S4	S5	S6	S7	ADC CH
PD4	GPIOD4	TBPWM4	TCPWM4	TDQEPIDX	TBQEPIDX	USDSCLK	TRACED3	USDMOSI	
PD5	GPIOD5	TBPWM5	TCPWM5	TDQEPPHA	TBQEPPHA	USDSS	CANRXD	USDMISO	
PD6	GPIOD6	TBPWM6	TCPWM6	TDQEPPHB	TBQEPPHB	USDMOSI	CANTXD	I2CSDA	
PE0	GPIOE0	TCPWM4	TDPWM0	TAIDX	TBIDX	USCCLK	I2CSCL	EMUXC	
PE1	GPIOE1	TCPWM5	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD	
PE2	GPIOE2	TCPWM6	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK	
PE3	GPIOE3	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD		
PF0	GPIOF0	TCPWM0	TDPWM0	TCK/SWDCL	TBIDX	USBSCLK	TRACED2	TRACECLK	
PF1	GPIOF1	TCPWM1	TDPWM1	TMS/SWDIO	TBPHA	USBSS	TRACED1	TRACED0	
PF2	GPIOF2	TCPWM2	TDPWM2	TDI	TBPHB	USBMOSI	TRACED0	TRACED1	
PF3	GPIOF3	TCPWM3	TDPWM3	TDO	FRCLK	USBMISO	TRACECLK	TRACED2	
PF4	GPIOF4	TCPWM4	TDPWM4		TCIDX	USDSCLK	TRACED3	EMUXC	ADC4
PF5	GPIOF5	TCPWM5	TDPWM5		TCPHA	USDSS		EMUXD	ADC5
PF6	GPIOF6	TCPWM6	TDPWM6		TCPHB	USDMOSI	CANRXD	I2CSCL	ADC6
PF7	GPIOF7	TCPWM7	TDPWM7			USDMISO	CANTXD	I2CSDA	ADC7
PG3	GPIOG3	TCPWM3	TDPWM3			USDMISO	TRACED2		
PG4	GPIOG4	TCPWM4	TDPWM4	EMUXD	I2CSCL	USDSS	TRACED3	TDQEPIDX	
PG5	GPIOG5	TCPWM5	TDPWM5	EMUXC		USDMOSI	CANRXD	TDQEPHA	ADC1
PG6	GPIOG6	TCPWM6	TDPWM6	I2CSDA		USDMISO	CANTXD	TDQEPPHB	ADC2

14.4 Electrical Characteristics

The Electrical Characteristics for the IO Controller are shown below.

Table 31 IO Controller Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IH}	High-level input voltage			2.1			V
V_{IL}	Low-level input voltage					0.825	V
I_{OL}	Low-level output sink current (Limited by I_{VSYS} and I_{VCCIO})	V_{OL} = 0.4V	DS = 6mA	6			mA
			DS = 8mA	8			
			DS = 11mA	11			
			DS = 14mA	14			
			DS = 17mA	17			
			DS = 20mA	20			
			DS = 22mA	22			
			DS = 25mA	25			
I_{OH}	High-level output source current (Limited by I_{VSYS} and I_{VCCIO})	V_{OH} = 2.4V	DS = 6mA			-6	mA
			DS = 8mA			-8	
			DS = 11mA			-11	
			DS = 14mA			-14	
			DS = 17mA			-17	
			DS = 20mA			-20	
			DS = 22mA			-22	
			DS = 25mA			-25	
I_{IL}	Input leakage current			-2		0.95	µA
R_{PU}	Weak pull-up resistance	When pull-up enabled		45	60	100	kΩ
R_{PD}	Weak pull-down resistance	When pull-down enabled		45	60	115	kΩ
$I_{INJ;GPIO}$	GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-15		15	mA
$\Sigma I_{INJ;GPIO}$	Sum of all GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-40		40	mA

T_A = -40°C to 125°C unless otherwise specified

15 Serial Interface

15.1 Features

- USART (UART or SPI master/slave)
- I2C master/slave
- CAN 2.0B controller

15.2 System Block Diagram

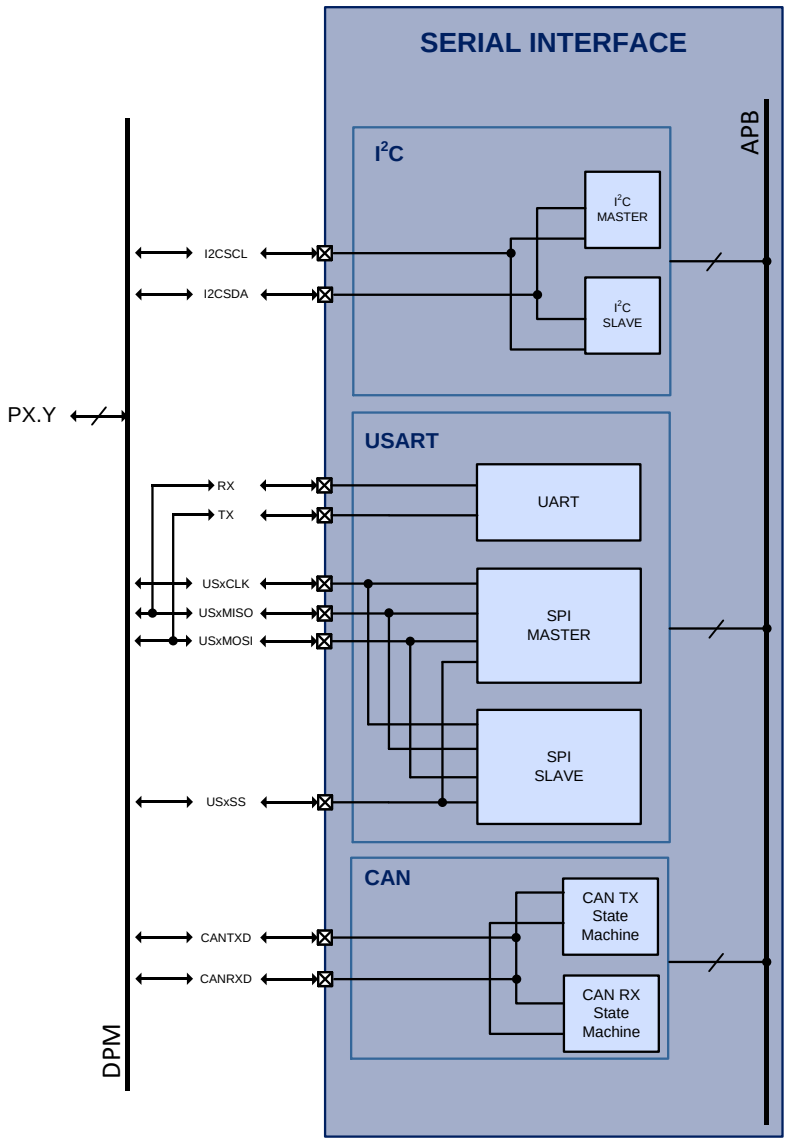


Figure 15 Serial Interfaces System Block Diagram

15.3 Functional Description

The PAC55XX has three types of serial interfaces: I²C, USART and CAN. The PAC55XX has one I²C controller, one CAN controller and up to 3 USARTs.

15.4 I²C Controller

The PAC55XX contains one I²C controller. This is a configurable APB peripheral and the clock input is PCLK. This peripheral has an input clock divider that can be used to generate various master clock frequencies. The I²C controller can support various modes of operation:

- I²C master operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit operations.

15.5 USART

The PAC55XX contains up to 2 Universal Synchronous Receive Transmit (USART) peripherals. Each USART is a configurable APB bus client and input clock is PCLK. These peripherals have a configurable clock divider that can be used to produce various frequencies for the UART or SPI master peripheral.

The number of these peripherals depends on the peripheral MUX configuration. See the IO Controller section on information on how to configure the peripheral MUX with the USART peripheral.

The USART peripheral supports two main modes: SPI mode and UART mode.

15.5.1 USART SPI Mode

- Master or slave mode operation
- 8-bit, 16-bit or 32-bit word transfers
- Configurable clock polarity (active high or active low)
- Configurable data phase (setup/sample or sample/setup)
- Interrupts and status flags for RX and TX operations
- Support for up to 25MHz SPI clock

15.5.2 USART UART Mode

- 8-bit data
- Programmable data bit rate

- Maximum baud rate of 1Mbaud
- RX and TX FIFOs
- Configurable stop bits (1 or 2)
- Configurable parity: even, odd, none
  - Mark/space support for 9-bit addressing protocols
- Interrupt and status flags for RX and TX operations

15.6 CAN

The PAC55XX contains one Controller Area Network (CAN) peripheral. The CAN peripheral is a configurable APB bus client and input clock is PCLK. This peripheral has a configurable clock divider that can be used to produce various frequencies for the CAN peripheral.

- CAN 2.0B support
- 1Mb/s data rate
- 64-byte receive FIFO
- 16-byte transmit buffer
- Standard and extended frame support
- Arbitration
- Overload frame generated on FIFO overflow
- Normal and Listen Only modes supported
- Interrupt and status flags for RX and TX operations

15.7 Dynamic Characteristics

The Dynamic Characteristics for the Serial Interfaces on the PAC5526 are shown below.

15.7.1 Serial Interface

Table 32 Serial Interface Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I2C						
f_{I2CCLK}	I^2C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Full-speed mode (400kHz)	2.8			MHz
		Fast mode (1MHz)	6.14			MHz
		High-speed mode (3.4MHz)	20.88			MHz
USART (UART mode)						
$f_{UARTCLK}$	USART input clock frequency				f_{PCLK}/16	MHz
$f_{UARTBAUD}$	UART baud rate	$f_{USARTCLK}$ = 7.1825MHz			1	Mbps
USART (SPI mode)						
f_{SPICLK}	USART input clock frequency	Master mode			50	MHz
		Slave mode			50	MHz
$f_{USARTSPICLK}$	USART SPI clock frequency	Master mode			25	MHz
		Slave mode			25	MHz
CAN						
f_{CANCLK}	CAN input clock frequency				50	MHz
f_{CANTX}	CAN transmit clock frequency				1	Mbps
f_{CANRX}	CAN receive clock frequency				1	Mbps

15.7.2 I2C Dynamic Characteristics

Table 33 I2C Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Full-speed mode	0		400	kHz
		Fast mode	0		1	MHz
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Full-speed mode	0		0.9	µs
		Fast mode	0			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
		Full-speed mode	100			ns
		Fast mode	50			ns
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Full-speed mode	20		300	ns
		Fast mode			120	ns
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Full-speed mode			300	ns
		Fast mode			120	ns
C_b	Capacitive load for each bus line	Standard mode, full-speed mode			400	pF
		Fast mode			550	pF

15.7.3 I2C Timing Diagram

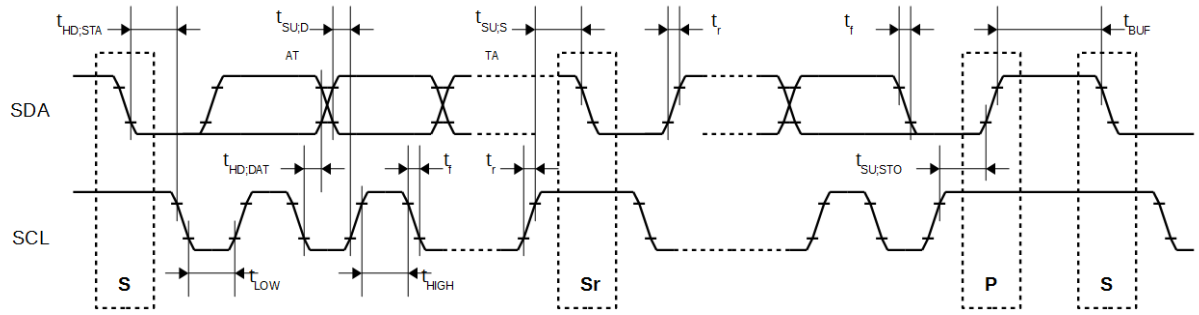


Figure 16 I2C Timing Diagram

16 PWM Timers

16.1 Features

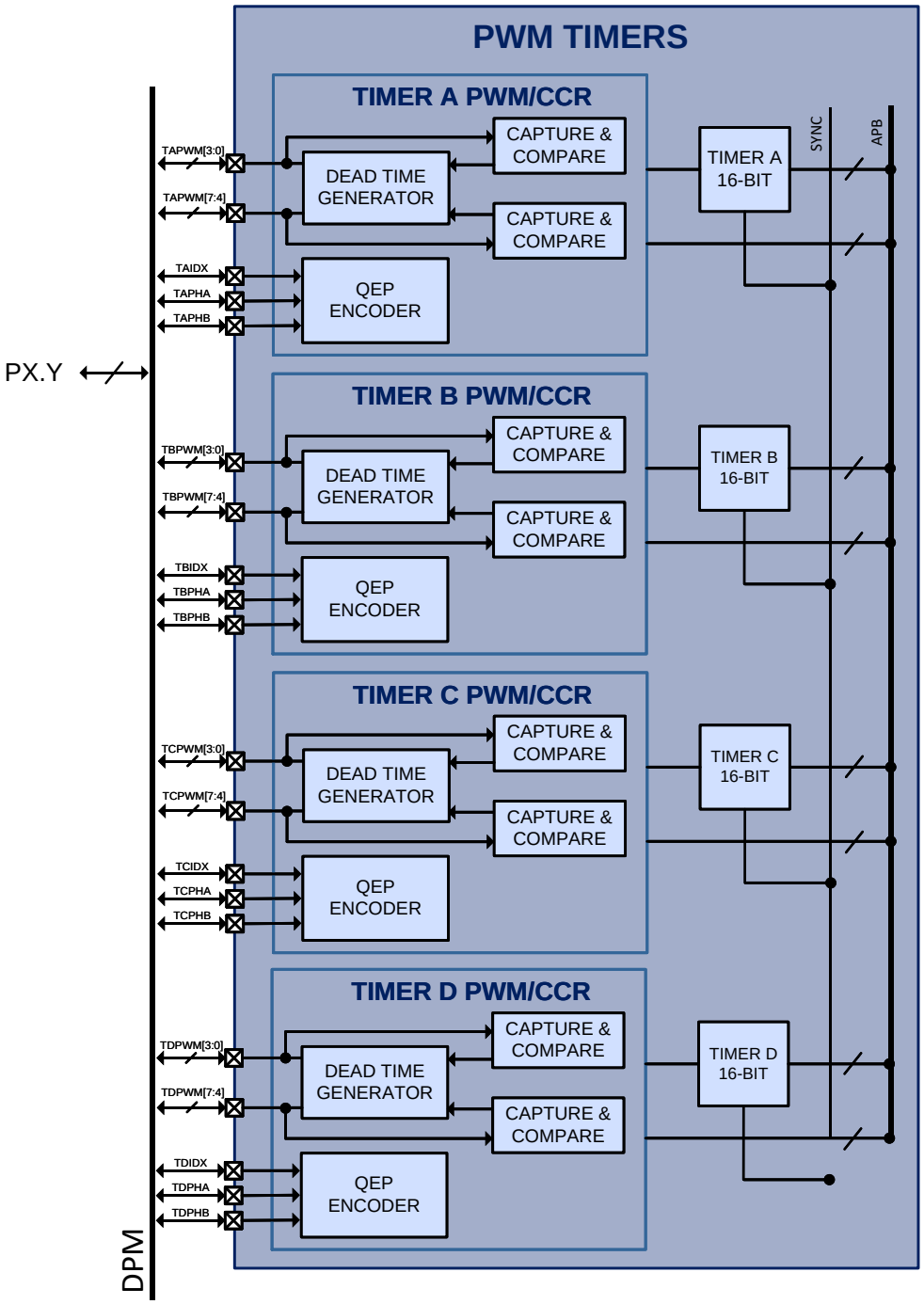
- Base timer features:
  - Configurable input clock source: PCLK or ACLK
  - Up to 300MHz input clock
  - 3-bit Input clock divider
  - Timer counting modes
    - Up, up/down and asymmetric
  - Timer latch modes
    - Latch when counter = 0
    - Latch when counter = period
    - Latch when CCR value written
    - Latch all CCR values at same time
  - Base timer interrupts
  - Single shot or auto-reload
- CCR/PWM Timer
  - PWM output or capture input
  - CCR interrupt enable
  - CCR interrupt skips
  - SW force CCR interrupt
  - CCR interrupt type
    - Rising, falling or both
  - CCR compare latch modes
    - Latch when counter = 0
    - Latch when counter = period
    - Latch immediate
  - CCR capture latch modes
    - Latch on rising edge
    - Latch on falling edge
    - Latch on both rising and falling edges
  - Invert CCR output
  - CCR phase delay for phase shifted drive topologies
  - ADC trigger outputs
    - PWM rising edge or falling edge
- Dead-time Generators (DTG)
  - DTG enabled
  - 12-bit rising edge delay

- 12-bit falling edge delay

- QEP Decoder
  - QEP encoder enabled
  - Direction status
  - Configurable Interrupts:
    - Phase A rising edge
    - Phase B rising edge
    - Index event
    - Counter wrap
  - 4 different counting modes for best resolution, range and speed performance

16.2 System Block Diagram

Figure 17 PWM Timers System Block Diagram



16.3 Functional Description

The PAC5526 contains four 16-bit timer units that may be used for PWM output and capture input. Each timer has a 16-bit time-base that may configure the counting style to up, up/down and up/down asymmetric modes. These modes can be used to support different drive topologies such as 120° trapezoidal and 180° sinusoidal.

Each base timer block may be clocked by either PCLK or ACLK. Configuring the timer to clock using ACLK allows higher PWM edge resolution by offering a clock that is up to 2X higher than the system clock. The base timer supports interrupts as well as single shot or auto-reload modes for maximum flexibility.

Each base timer has up to 8 CCR units that may be used for PWM output or capture input. When configured for PWM output, the user may configure a delay in order to support phase delay drive topologies. The CCR output may also be inverted in order to support full-bridge topologies.

The user may configure each CCR output rising or falling edge to interrupt the DTSE to begin a sequence of conversions.

17 General Purpose Timers

17.1 Features

- SOC Bus Watchdog Timer
- Hibernate Wake-up Timer
- Real-Time Clock with Calendar and Alarm
- Windowed Watchdog Timer (WWDT)
- 24-Bit General-purpose Timers

17.2 System Block Diagram

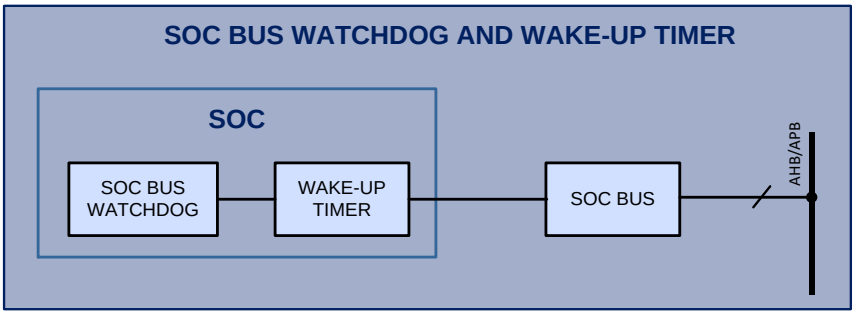


Figure 18 SOC and WWDT System Block Diagrams

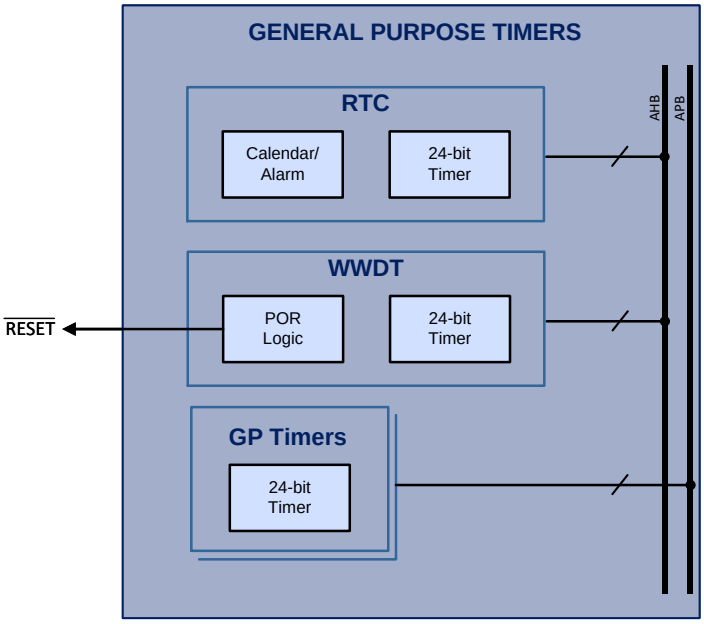


Figure 19 General-Purpose Timers System Block Diagrams

17.3 Functional Description

17.3.1 SOC Bus Watchdog Timer

The SOC Bus Watchdog Timer is used to monitor internal SOC Bus communication. It will trigger a device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

17.3.2 Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

17.3.3 Real-time Clock with Calendar (RTC)

The 24-bit real-time clock with calendar (RTC) is an AHB bus client and may also be used to measure long time periods and periodic wake up from sleep mode.

The RTC uses FRCLK as its clock source and has a divider that can be configured up to a /65536 input clock divider. In order to count accurately, the input clock divider must be configured to generate a 1MHz clock to the RTC.

The RTC counts the time (seconds, minutes, hours, days) since enabled. It also allows the user to set a calendar date to set an alarm function that can be configured to generate an interrupt to the NVIC when it counts to that value.

17.3.4 Windowed Watchdog Timer (WWDT)

The 24-bit windowed watchdog timer (WWDT) is an AHB bus client and can be used for long time period measurements or periodic wake up from sleep mode. Its primary use is to reset the system via a POR if it is not reset at a certain periodic interval.

The WWDT can be configured to use FRCLK or ROSCCLK as its clock source and has a divider that be configured up to a /65536 input clock divider.

The WWDT can be configured to allow only a small window when it is valid to reset the timer, to maximize application security and catch any stray code operating on the MCU.

The WWDT may be configured to enable an interrupt for the MCU, and the timer can be disabled when unused to save energy for low power operations.

17.3.5 GP Timer (GPT)

The PAC55XX contains two General Purpose (GP) Timers.

These timers are 24-bit timers and are both APB bus clients. These count-down timers use PCLK as their input clock and have a configurable divider of up to /32768. Each of the GPT can be configured to interrupt the MCU when they count down to 0.

18 CRC

18.1 Features

- 8-bit or 16-bit CRC
- User may select the polynomial through configuration:
  - CCITT CRC-16
  - IBM/ANSI CRC-16
  - Dallas/Maxim CRC-8
- Input data width: 8b or 32b
- Reflect input
- Reflect output
- Specify seed value

18.2 System Block Diagram

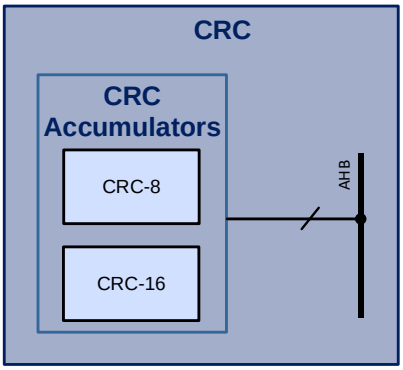


Figure 20 CRC System Block Diagram

18.3 Functional Description

The CRC peripheral can perform CRC calculation on data through registers from the MCU to accelerate the calculation or validation of a CRC for communications protocols or data integrity checks.

The CRC peripheral allows the calculation of both CRC-8 and CRC-16 on data. The CRC peripheral also allows the user to specify a seed value, select the data input to be 8b or 32b and to reflect the final output for firmware efficiency.

19 Application Block Diagram

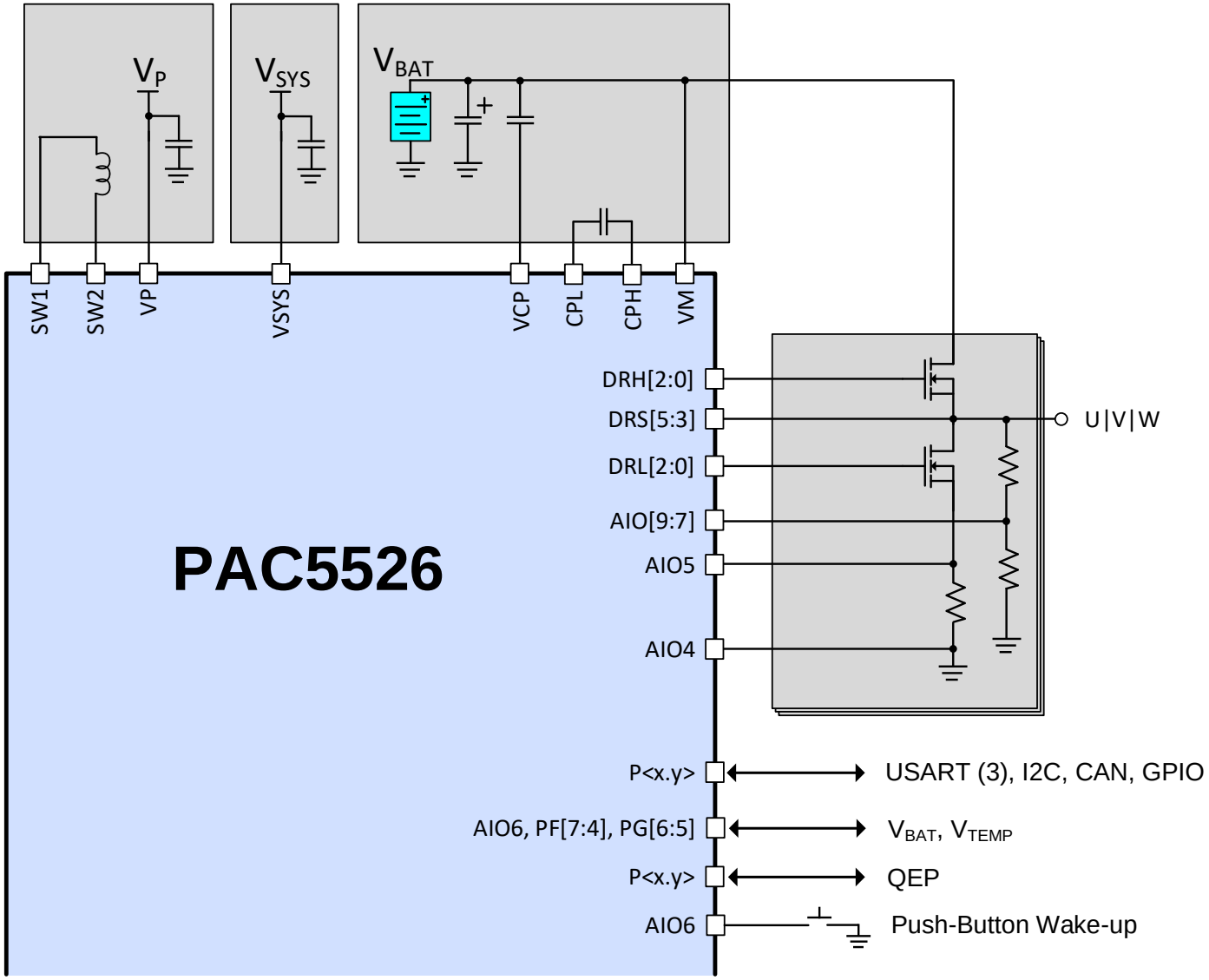


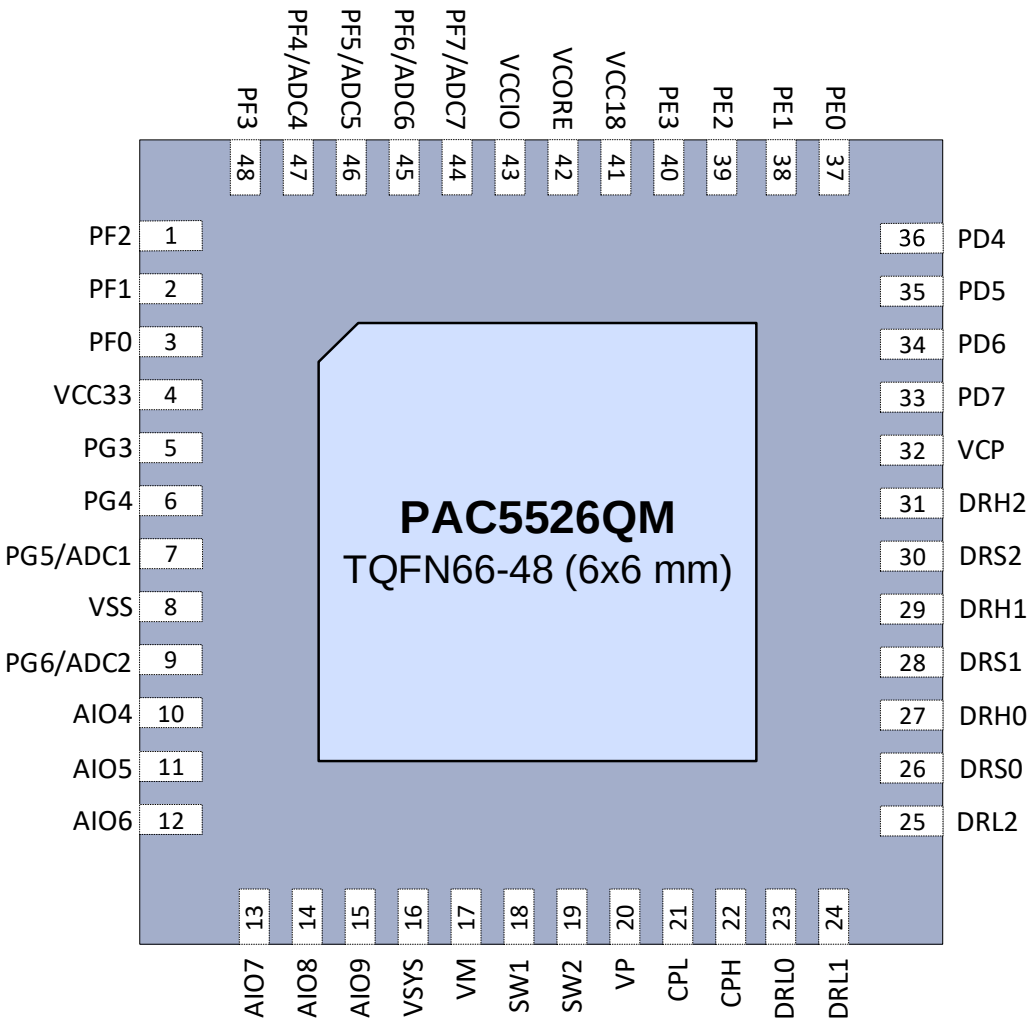
Figure 21 PAC5526 Application Block Diagram

20 Thermal Characteristics

Table 34 Thermal Characteristics

SYMBOL	PARAMETER	VALUE	UNIT
T_A	Operating ambient temperature range	-40 to 105	°C
T_J	Operating junction temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-55 to 150	°C
	Lead temperature (Soldering, 10 seconds)	300	°C
Θ_{JC}	Junction-to-case thermal resistance	2.897	°C/W
Θ_{JA}	Junction-to-ambient thermal resistance	23.36	°C/W

21 Pin Configuration and Description



Top View

21.1 Power Manager and System Pin Descriptions

Pin Number	Pin Name	Type	Description
4	VCC33	Power	Internally generated 3.3V power supply. Connect to a 10V/2.2µF ceramic capacitor from VCC33 to VSS close to the device.
8	VSS	Power	Ground.
16	VSYS	Power	5V System power supply. Connect to a 16V/4.7µF ceramic capacitor from VSYS to VSS close to the device.
17	VM	Power	Main power supply (Motor Voltage). Provides power to the charge pump as well as all LDOs. Connect a high value electrolytic capacitor in parallel with a 0.1µF ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
18	SW1	Power	Buck-boost switch-node 1. Connect to a 10µH/0.5A (no external load on VSYS) or 22µH/0.9A inductor (external load of up to 50mA on VSYS) between SW1 and SW2.
19	SW2	Power	Buck-boost switch-node 2. Connect to a 10µH/0.5A (no external load on VSYS) or 22µH/0.9A inductor (external load of up to 50mA on VSYS) between SW1 and SW2.
20	VP	Power	10V/12V Low-side driver power supply. Connect a 25V/22µF ceramic capacitor from VSYS to VSS close to the device.
21	CPL	Power	Charge Pump switch node. Connect a VM * 1.5V rated 0.1µF flying capacitor between CPL and CPH.
22	CPH	Power	Charge Pump switch node. Connect a VM * 1.5V rated 0.1µF flying capacitor between CPL and CPH.
32	VCP	Power	Charge Pump output. Connect a VP rated 1µF ceramic capacitor between the VCP and VM pins.
41	VCC18	Power	Internally generated MCU FLASH 1.8V power supply. Connect to a 6.3V/2.2µF ceramic capacitor from VCC18 to VSS close to the device.
42	VCORE	Power	Internally generated digital I/O 1.2V power supply. Connect a 6.3V/2.2µF ceramic capacitor from VCCIO to VSS close to the device.
43	VCCIO	Power	Internally generated digital I/O 3.3V power supply. Connect a 10V/2.2µF ceramic capacitor from VCCIO to VSS close to the device.
EP	EP (VSS)	Power	Exposed pad. Must be connected to VSS in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

21.2 CAFE Pin Descriptions

Pin Number	Pin Name	Function	Type	Description
10	AIO4	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
11	AIO5	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
12	AIO6	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
13	AIO7	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
14	AIO8	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
15	AIO9	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

21.3 ASPD Pin Descriptions

Pin Number	Pin Name	Type	Description
23	DRL0	Analog	Low-side gate driver 0.
24	DRL1	Analog	Low-side gate driver 1.
25	DRL2	Analog	Low-side gate driver 2.
26	DRS0	Analog	High-side gate driver source 3.
27	DRH0	Analog	High-side gate driver 3.
28	DRS1	Analog	High-side gate driver bootstrap 3.
29	DRH1	Analog	High-side gate driver source 4.
30	DRS2	Analog	High-side gate driver 4.
31	DRH2	Analog	High-side gate driver bootstrap 4.

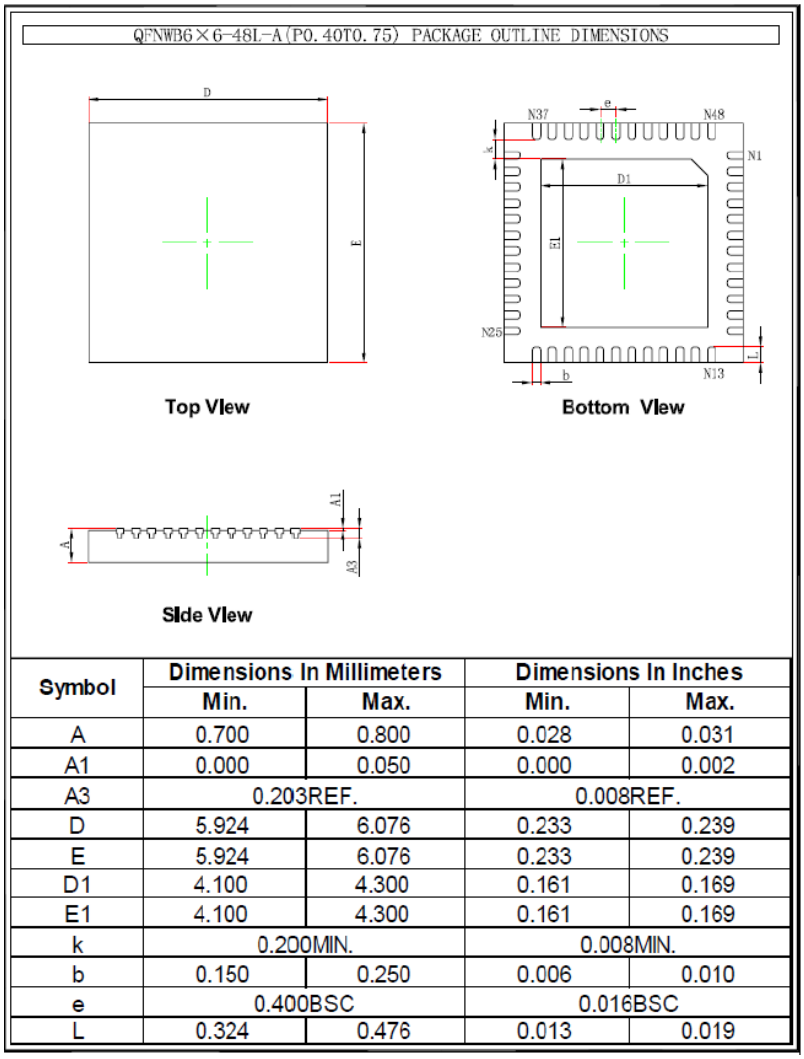
21.4 I/O Ports Pin Descriptions

Pin Number	Pin Name	Function	Type	Description
1	PF2	PF2	I/O	I/O port PF2.
2	PF1	PF1	I/O	I/O port PF1.
3	PF0	PF0	I/O	I/O port PF0.
5	PG3	PG3	I/O	I/O port PG3.
6	PG4	PG4	I/O	I/O port PG4.
7	PG5/ADC1	PG5	I/O	I/O port PG5.
		ADC1	Analog Input	ADC input ADC1.
9	PG6/ADC2	PG6	I/O	I/O port PG6.
		ADC2	Analog Input	ADC input ADC2.
33	PD7	PD7	I/O	I/O port PD7.
34	PD6	PD6	I/O	I/O port PD6.
35	PD5	PD5	I/O	I/O port PD5.
36	PD4	PD4	I/O	I/O port PD4.
37	PE0	PE0	I/O	I/O port PE0.
38	PE1	PE1	I/O	I/O port PE1.
39	PE2	PE2	I/O	I/O port PE2.
40	PE3	PE3	I/O	I/O port PE3.
44	PF7/ADC7	PF7	I/O	I/O port PF7.
		ADC7	Analog Input	ADC input ADC7.
45	PF6/ADC6	PF6	I/O	I/O port PF6.
		ADC6	Analog Input	ADC input ADC6.
46	PF5/ADC5	PF5	I/O	I/O port PF5.
		ADC5	Analog Input	ADC input ADC5.
47	PF4/ADC4	PF4	I/O	I/O port PF4.
		ADC4	Analog Input	ADC input ADC4.
48	PF3	PF3	I/O	I/O port PF3.

22 Mechanical Information

Package Marking and Dimensions

Marking: Part number – PAC5526QM



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.924	6.076	0.233	0.239
E	5.924	6.076	0.233	0.239
D1	4.100	4.300	0.161	0.169
E1	4.100	4.300	0.161	0.169
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400BSC		0.016BSC	
L	0.324	0.476	0.013	0.019

Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

23 Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

24 Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

25 REVISION HISTORY

Revision	Description
DS141020	Initial release

26 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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