Title	***Reference Design Report for 60 W USB PD 3.0 Power Supply with 3.3 V – 21 V PPS Output Using InnoSwitch™3-PD PowiGaN™ INN3879C-H801***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A; or 3.3 V – 21 V / 3 A PPS Outputs
Application	USB PD / PPS Power Adaptor
Author	Applications Engineering Department
Document Number	RDR-838
Date	November 16, 2021
Revision	3.4

Summary and Features

- InnoSwitch3-PD - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage switch, USB PD controller, synchronous rectification and FluxLink™ feedback
  - Sophisticated telemetry and comprehensive protection features
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with high margin (>2.0%)
  - 5 V Output: 87.88% at 115 VAC (6.48% margin); 86.94% at 230 VAC (5.14% margin)
  - 9 V Output: 90.04% at 115 VAC (3.44% margin); 89.99% at 230 VAC (2.69% margin)
  - 15 V Output: 90.79% at 115 VAC (3.09% margin); 91.38% at 230 VAC (2.48% margin)
  - 20 V Output: 90.92% at 115 VAC (2.92% margin); 91.72% at 230 VAC (2.72% margin)
- Micro stepping of voltages (20 mV) and CC thresholds (50 mA) in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <35 mW no-load input power at 230VAC
- Meets CISPR22 / EN55022 Class B Conducted EMI standard
- Low component count, high power density

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200   Fax: +1 408 414 9201
www.power.com

- Total part count: 61
- Power density: 15.7 W / inch3 without enclosure (2.24” x 2.24” x 0.76” form factor)

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 60 W USB PD 3.0 power supply using InnoSwitch3-PD INN3879C-H801, which features an integrated USB PD controller within the IC. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 3 A (Fixed Supply)
- PDO2: 9 V / 3 A (Fixed Supply)
- PDO3: 15 V / 3 A (Fixed Supply)
- PDO4: 20 V / 3 A (Fixed Supply)
- PDO5: 3.3 V – 21 V / 3 A (Programmable Power Supply)

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-PD controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, transformer documentation, and performance data.

Figure 1 – Populated Circuit Board Photograph - Top.

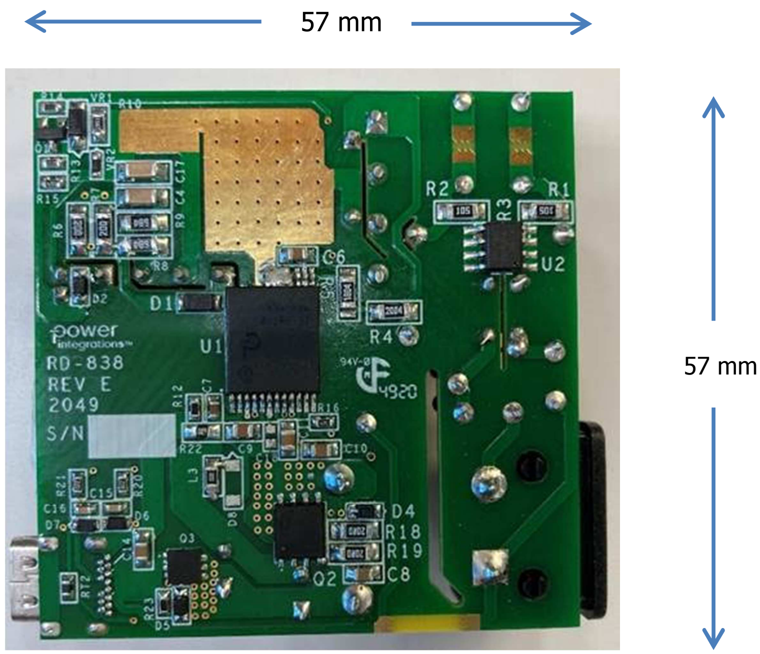


Figure 2 – Populated Circuit Board Photograph - Bottom.

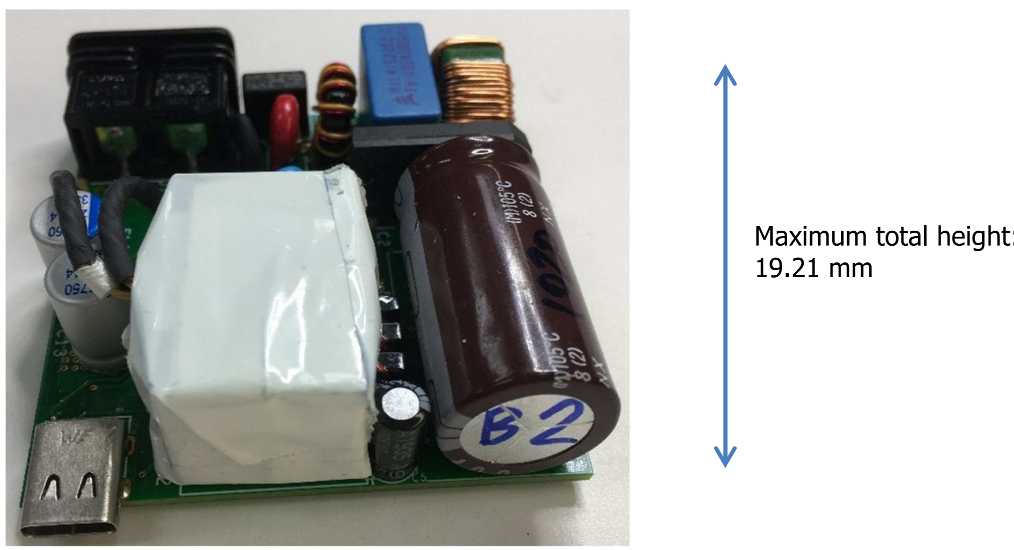


Figure 3 – Populated Circuit Board Photograph (Side View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				35	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			150	mV	Measured at End of Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	η_{5V}	87.4			%	Measured at 115 VAC from AC Receptacle to End of Cable.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			200	mV	Measured at End of Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	η_{9V}	89.5			%	Measured at 115 VAC from AC Receptacle to End of Cable.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			250	mV	Measured at End of Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	η_{15V}	90.3			%	Measured at 115 VAC from AC Receptacle to End of Cable.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			250	mV	Measured at End of Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			3.0	A	±3%
Average Efficiency	η_{20V}	90.4			%	Measured at 115 VAC from AC Receptacle to End of Cable.
Continuous Output Power	$P_{OUT(20\ V)}$			60	W	
3.3 – 21 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT(MAX)}$			21	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT(MIN)}$	3.3			V	APDO Minimum Voltage.
Output Voltage Ripple 1	$V_{RIPPLE1(PPS)}$			250	mV	15 V – 21 V PPS, measured at End of Cable (20 MHz Bandwidth).
Output Voltage Ripple 2	$V_{RIPPLE2(PPS)}$			200	mV	Below 9 V PPS voltage, measured at the End of Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(PPS)}$			3.0	A	±3%
PPS Voltage Step	$V_{STEP(PPS)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PPS)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(20\ V)}$			60	W	

Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Note A: Output Voltage Regulation compliant with USB PD 3.0 Specifications.
B: Output Voltage Ripple measured at the end of cable with the probe having decoupling capacitors 47 μF electrolytic and 100 nF ceramic in parallel.
C: Maximum Operating Current for the Fixed Supply PDO. Output Over Current Protection Threshold nominally set at 250 mA above the Operating Current requested by the USB PD Sink.
D: Output Current Limit Accuracy is within ±150 mA for Operating Current between 1 A and 3 A, or ±5% for Operating Current >3 A; compliant with USB PD 3.0 Specifications.

Note: To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

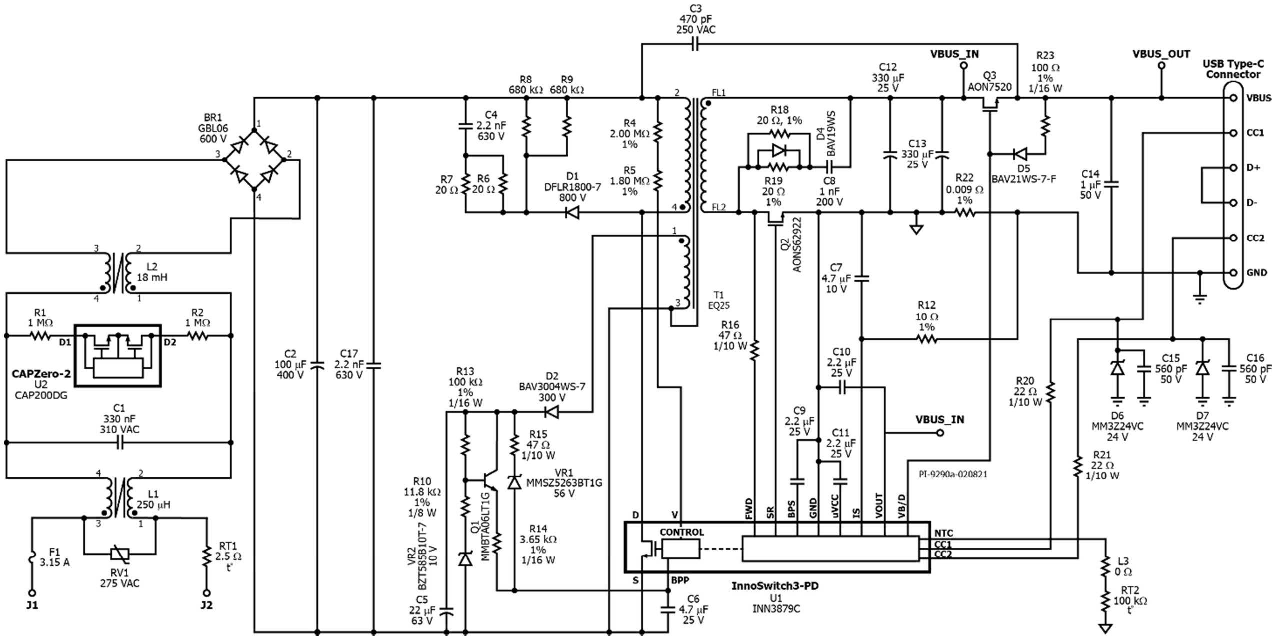


Figure 4 – Schematic.

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

Fuse F1 isolates the circuit and provides protection from component failure, and thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Varistor RV1 provides safety during high voltage transients in case of input line surge.

Common mode chokes L1 and L2 with capacitors C1, C3 and C17 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across C2.

Resistors R1 and R2 along with CapZero-2 IC U2 discharge capacitor C1 when the power supply is disconnected from AC mains.

4.2 *InnoSwitch3-PD IC Primary*

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-PD IC U1. Resistors R4 and R5 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost RCD clamp formed by diode D1, resistors R6, R7, R8 and R9, and capacitor C4 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C6 when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R14 limits the current being supplied to the BPP pin of the InnoSwitch3-PD IC U1. A linear regulator composed of resistors R10 and R13, BJT Q1 and Zener diode VR2 ensures sufficient current flows through R14 such that the internal current source of U1 is not required to charge C6 during normal operation.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes excess current to flow into the BPP pin of InnoSwitch3-PD IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-PD controller will latch off and prevent any further increase in output voltage. Resistor R15 limits the current injected to BPP pin.

4.3 *InnoSwitch3-PD IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-PD IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side FET (or SR FET) Q2 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber, R18, R19, C8 and D4.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R16 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9 connected to the BPS pin of InnoSwitch3-PD IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R22. The current measurement is filtered with decoupling capacitor C7 and resistor R12, and it is monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the firmware up to approximately 32 mV is used. Once the threshold is exceeded, the InnoSwitch3-PD IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-PD IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C9 via resistor R16 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-PD IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the firmware and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C10 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-FET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. Q3 is controlled by the VB/D pin on the InnoSwitch3-PD IC. Resistor R23, and diode D5 are connected across the Source and Gate terminals of the Q3 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitor C14 is needed at the output for ESD protection.

In this design, USB PD communication occurs over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

Capacitor C11 provides decoupling to the µVCC supply of the InnoSwitch3-PD IC U1. Capacitors C15 and C16, resistors R20 and R21 and Zener diodes D6 and D7 provide protection from ESD to pins CC1 and CC2.

5 PCB Layout

PCB copper thickness is 0.062 inches.

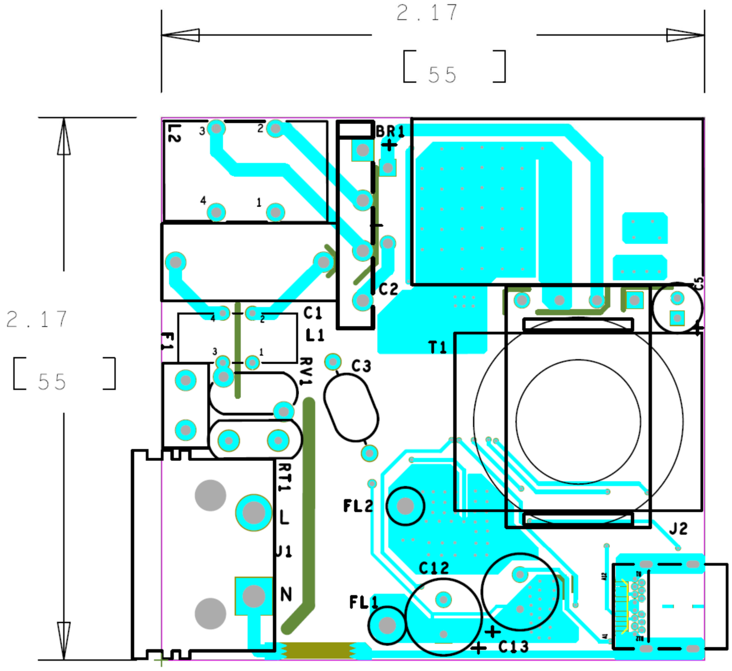


Figure 5 – Printed Circuit Layout, Top.

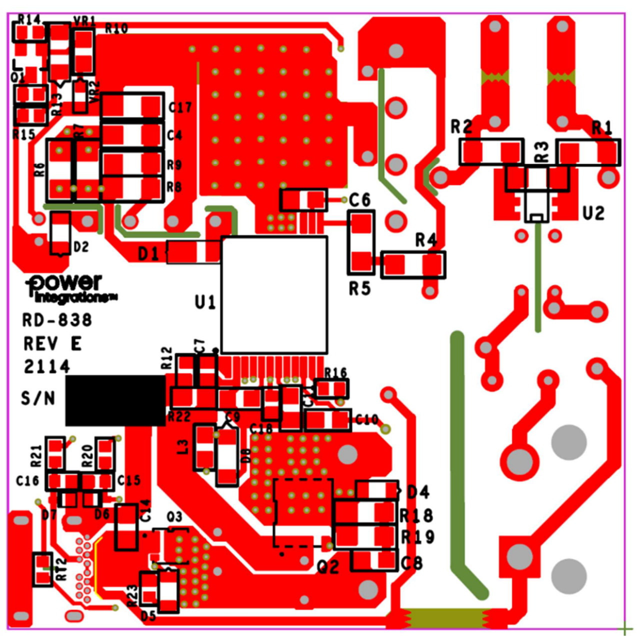


Figure 6 – Printed Circuit Layout, Bottom.

Note: Component references R3, C18, and D8, although present in the layout, should not be populated.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	DIODE BRIDGE 600 V 4A GB	GBL06	Genesic Semi
2	1	C1	330 nF, 310 VAC, Film, X2	B32922C3334M	Epcos
3	1	C2	100 μF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
4	1	C3	470 pF, ±10%, 250VAC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
5	2	C4 C17	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
6	1	C5	22 μF, ±20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
7	1	C6	4.7 μF ±10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
8	1	C7	4.7 μF, ±10%, 10V, Ceramic, X7S, 0603, -55°C ~ 125°C, Low ESL	C1608X7S1A475K080AC	TDK
9	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
10	3	C9 C10 C11	2.2 μF ±10% ,25V, Ceramic, X7R, 0805, -55°C ~ 125°C	CGA4J3X7R1E225K125AB	TDK
11	2	C12 C13	330 μF ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105°C, (8 mm x 13 mm	A750KS337M1EAAE018	KEMET
12	1	C14	1 μF ±20% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805	CGA4J3X7R1H105M125AE	TDK
13	2	C15 C16	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60mm x 0.80mm)	CC0603KRX7R9BB561	Yageo
14	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
15	1	D2	Diode, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD-323	BAV3004WS-7	Diodes, Inc.
16	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
17	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	2	D6 D7	Diode, ZENER, 24V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
19	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
20	1	J1	Power Entry Connector Receptacle, Male Pins, IEC 320-C8, Non-Polarized, Panel Mount, Snap-In; Through Hole, Right Angle	RAPC322X	Switchcraft
21	1	J2	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material, Superspeed+, Receptacle Connector, 24 Position, SMT, Right Angle, Through Hole	632723300011	Wurth
22	1	L1	250 μH, Toroidal Common Mode Choke, custom, DER-538, wound on 32-00275-00 core.	32-00367-00 TSD-4500	Power Integrations Premier Magnetics
23	1	L2	CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231 TSD-4501	Sumida Premier Magnetics
24	1	L3	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
25	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
26	1	Q2	MOSFET, N-CH, 120 V, 85 A (at VGS = 10 V), Trench Power AlphaSGT 120 V TM technology, DFN5X6	AONS62922	Alpha & Omega Semi
27	1	Q3	MOSFET, N-CH, 30 V, 48A (Ta), 50A (Tc), 6.2W (Ta), 83.3W (Tc) SMT, 8-DFN-EP (3.3x3.3)	AON7520C	Alpha & Omega Semi
28	2	R1 R2	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
29	1	R4	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
30	1	R5	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
31	2	R6 R7	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
32	2	R8 R9	RES, 680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
33	1	R10	RES, 11.8 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
34	1	R12	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
35	1	R13	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
36	1	R14	RES, 3.65 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3651V	Panasonic
37	2	R15 R16	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
38	2	R18 R19	RES, 20 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF20R0V	Panasonic
39	2	R20 R21	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
40	1	R22	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns

41	1	R23	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
42	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
43	1	RT2	NTC Thermistor, 100 kΩ, 1%, 4250 K, 0603	NCU18WF104F60RB	Murata
44	1	RV1	275 VAC, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
45	1	T1	Custom, DER-838 Transformer, EQ25, Lp = 469 μH Transformer	POL-INN047	Power Integrations Premier Magnetics
46	1	U1	InnoSwitch3-PD, InSOP24D	INN3879C-H801	Power Integrations
47	1	U2	CAPZero-2, SO-8C	CAP200DG	Power Integrations
48	1	VR1	DIODE, ZENER, 56 V, 500 mW, SOD123	MMSZ5263BT1G	ON Semi
49	1	VR2	Zener Diode 10 V 350 mW ±2% SMT SOD-523	BZT585B10T-7	Diodes, Inc.

7 Transformer Specification

7.1 *Electrical Diagram*

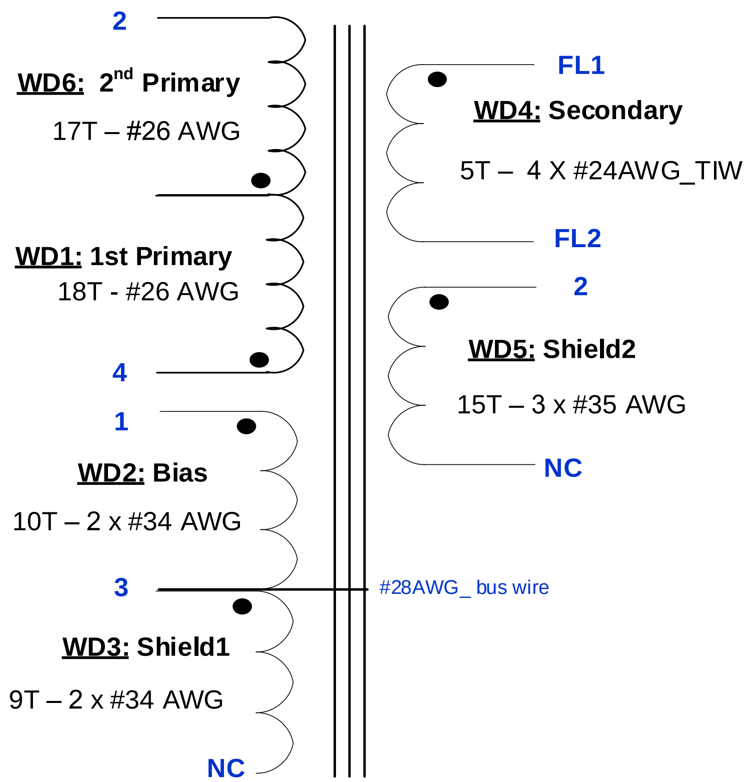


Figure 7 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Electrical Strength	60 secs, 10 mA, from pins 1-4 to FL1 and FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 2 and 4, with all other windings open.	469 μH ±5%
Resonant Frequency	Between pin 2 and 4, other windings open.	1,500 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and 4, with pins FL1-FL2 shorted.	4.5 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EQ25-3C95, Ferroxcube.
[2]	Bobbin: EQ25-Vertical, 4pins (4/0), PI custom, P/N: 25-01141-00.
[3]	Magnet Wire: **#**26 AWG, Double Coated.
[4]	Magnet Wire: **#**34 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Magnet Wire: **#**35 AWG, Double Coated.
[7]	Bus wire: #28AWG, Alpha Wire, Tinned Copper.
[8]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 8.2 mm Width.
[9]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 14 mm x 14 mm.
[10]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 30 mm x 55 mm.
[11]	Glue: Loctite, 409, Gel, Mf #:40904; or Equivalent.
[12]	Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or Equivalent.
[13]	Varnish: Dolph BC-359.
[14]	Heat Shrink Tube: FIT-221, 3/16”, Blk, PI#: 62-00003-00; or Equivalent.

7.4 *Transformer Build Diagram*

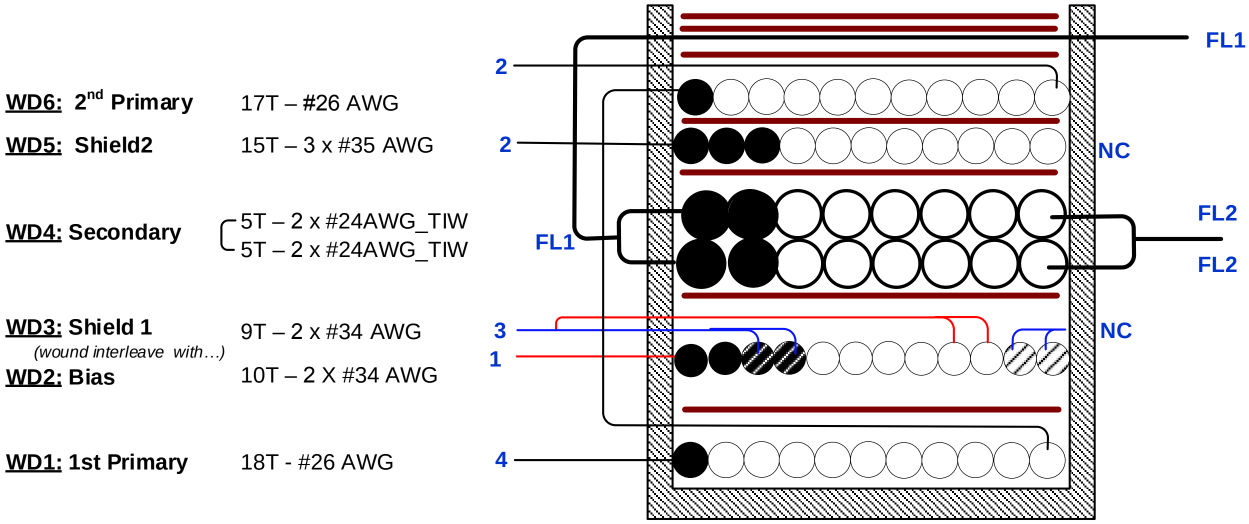
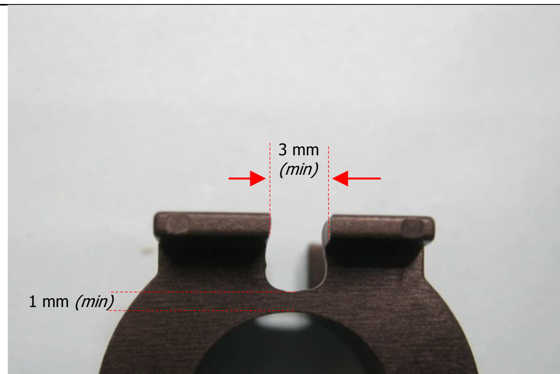
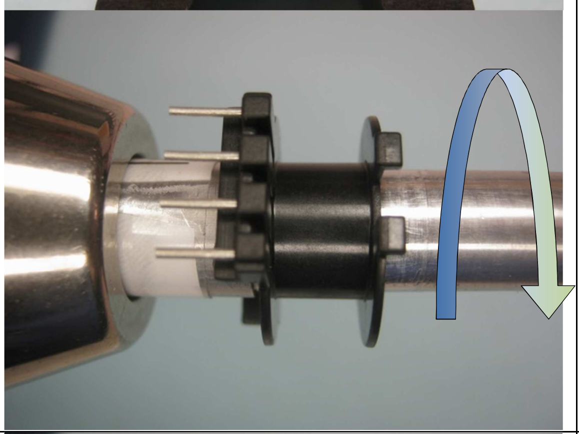
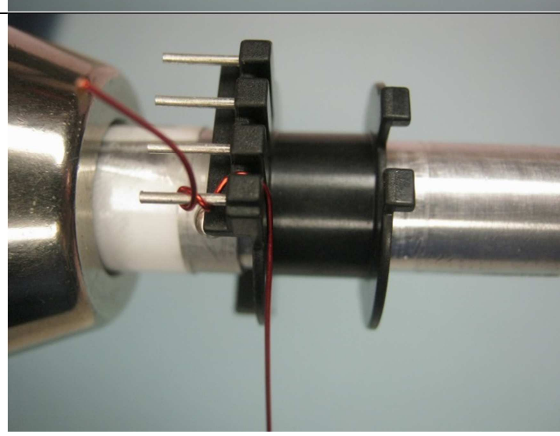


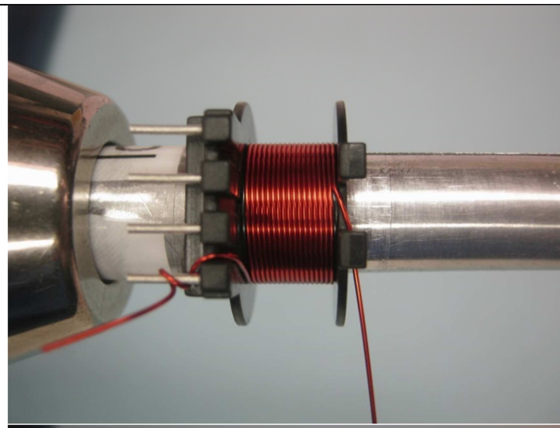
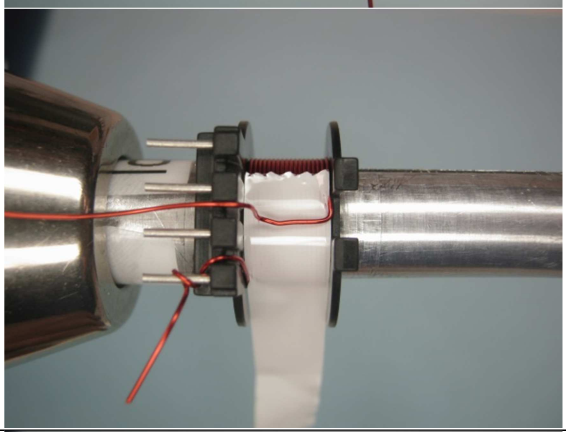
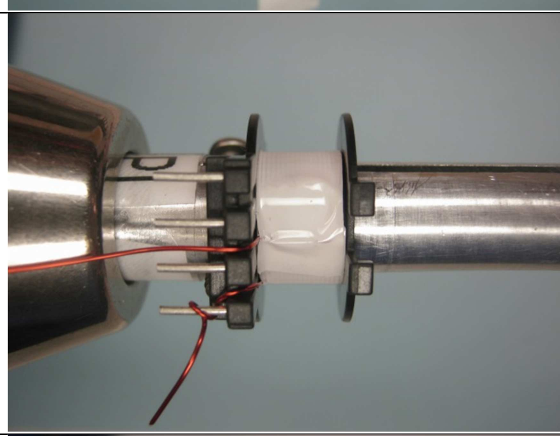
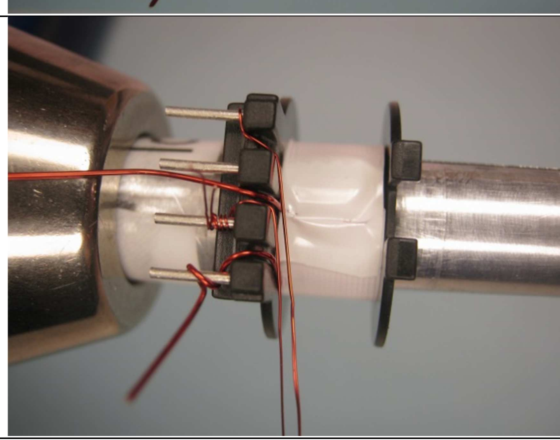
Figure 8 – Transformer Build Diagram.

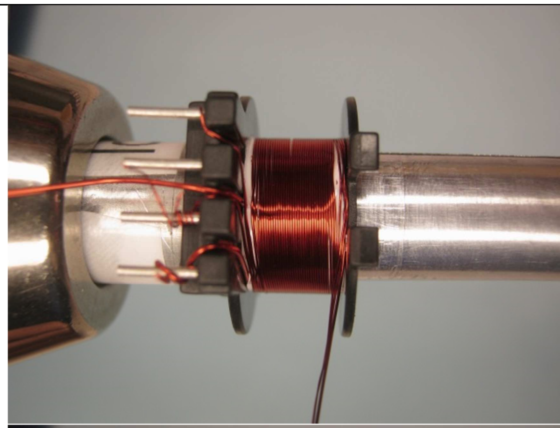
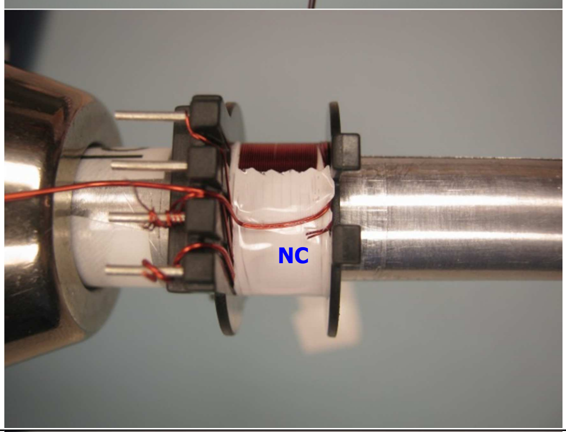
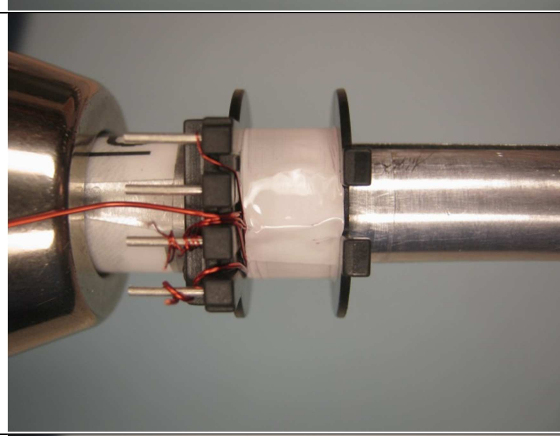
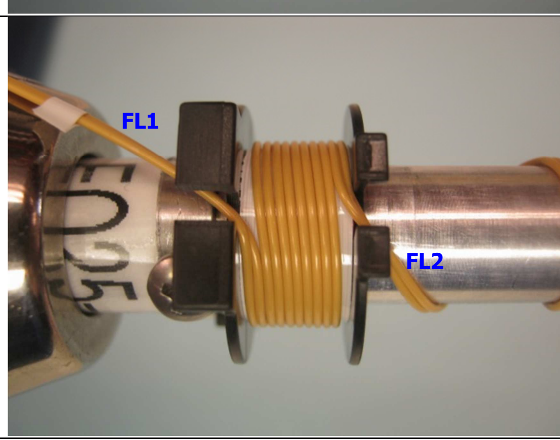
7.5 *Transformer Construction*

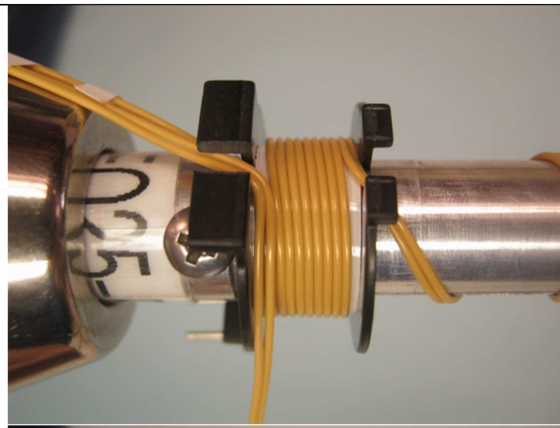
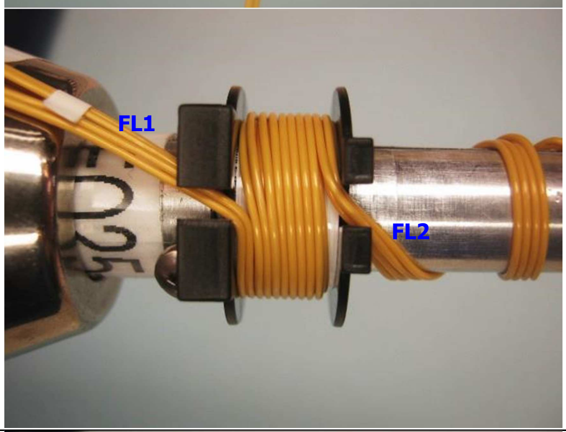
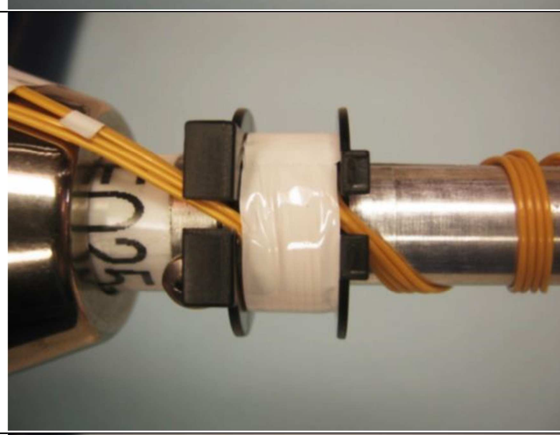
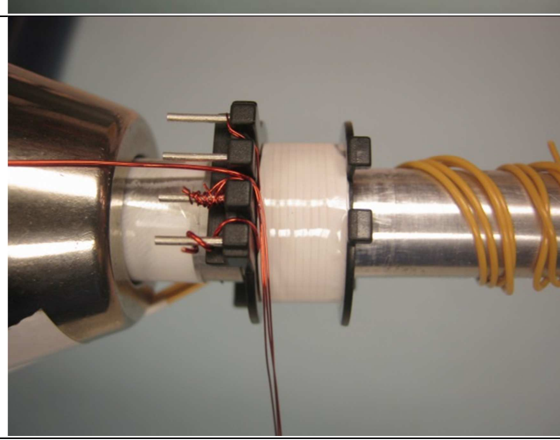
Winding preparation	Make slot 3.0 mm width (minimum) on bottom secondary flange of the bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 4, wind 18 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.
Insulation	1 layer of tape Item [8].
WD2: Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 1 for Bias winding, also use 2 wires same Item [4] start at pin 3 for Shield1 winding. Wind all these 4 wires in parallel, at the 9th turn, cut short 2 wires as No-Connect for Shield 1 winding, and wind another turn -10th turn for Bias winding then bring wires back to the left to terminate at pin 3.
Insulation	1 layer of tape Item [8].
WD4 Secondary	Start at left slot of secondary side, use 2 wires Item [5], leaving ~ 40.0mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2. *Attn: When enter or exit these wires should be gently to void wire insulation get scratches or cuts by sharp edges of slots.*
Insulation	1 layer of tape Item [8].
WD5 Shield2	Start at pin 2, wind 15 tri-filar turns of wire Item [6], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [8].
WD6 2nd Primary	Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.
Insulation	1 layer of tape Item [8]. Bring 4 wires marked as FL1 to the right and secure with 2 layers of` tape Item [8].
Finish	Gap core halves to get 469 µH. Place 1 tape Item [9] on one side and double layers on other side of each core halve for both core halves *(see pictures below).* Apply glue Item [11] at center legs and insert core halves to bobbin with secondary wire outputs on the sides which have double layers of tape (see pictures below). Solder pin 3 with bus-wire Item [6] then lean along core halves and secure with tape. Apply epoxy Item [12] between cores to body of the transformer. Varnish with Item [13]. *(Attn: Do steps below after varnishing).* Place 2 layers of tape Item [10] at the bottom then wrap up also place 1 layer on top and wrap down to the body of transformer as shown in pictures below. Tape around 1 turn of tape Item [8]. Insert heat shrinks Item [14] to secondary leads and apply heat to shrink. Hi-Pot test: follow specs of "Electrical strength" in table "Electrical specifications" above, (should pass).

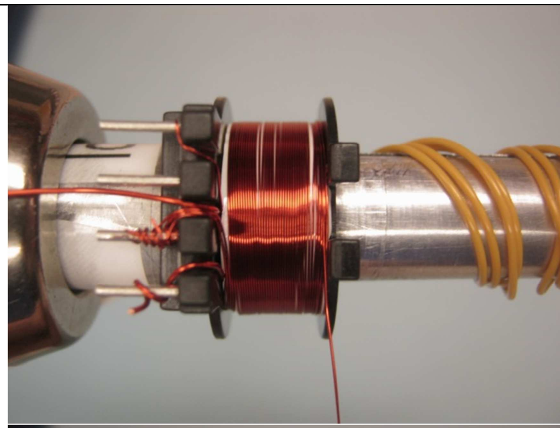
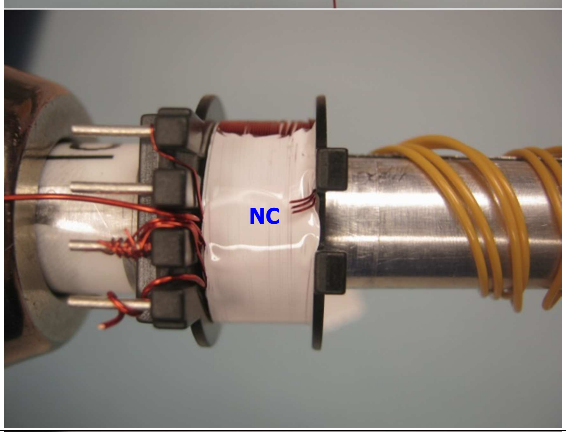
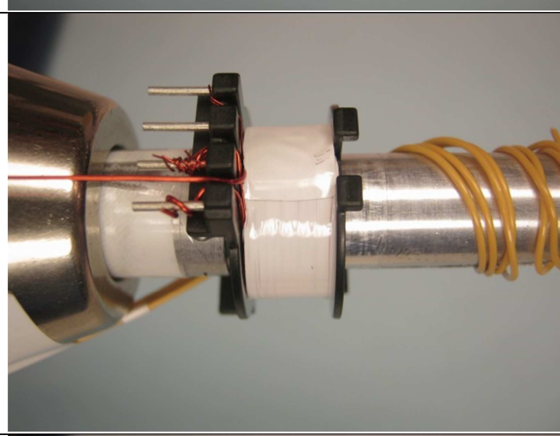
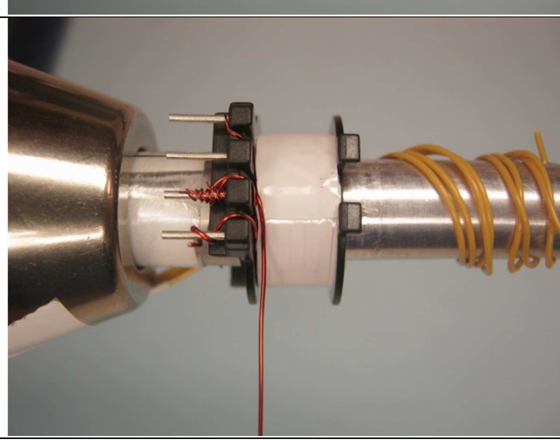
7.6 *Winding Illustrations*

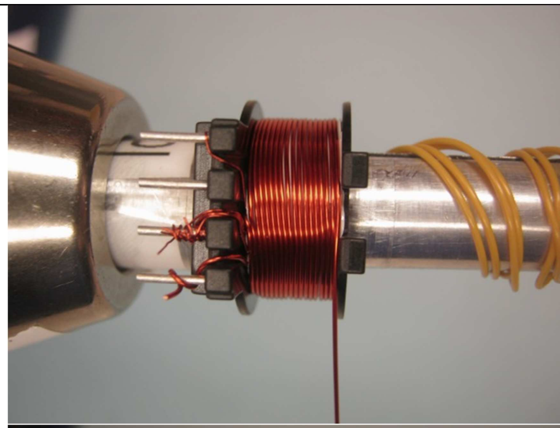
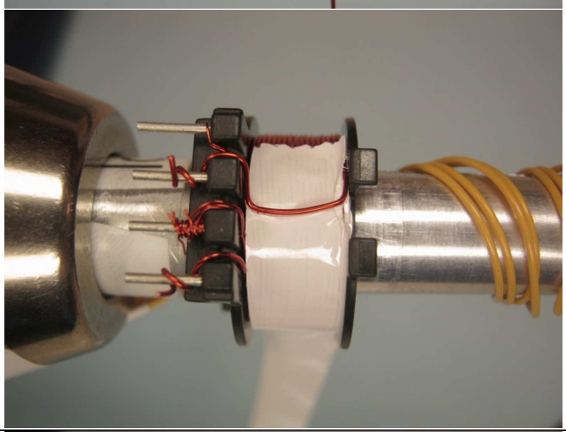
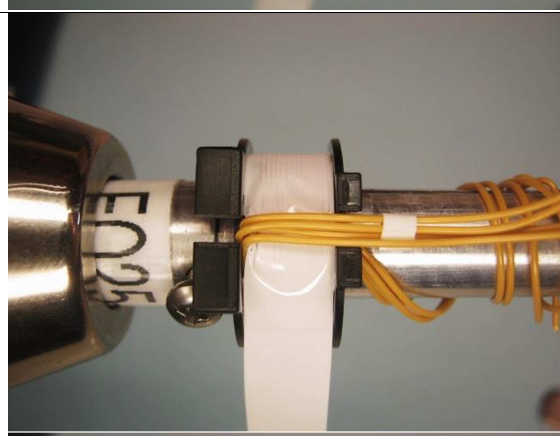
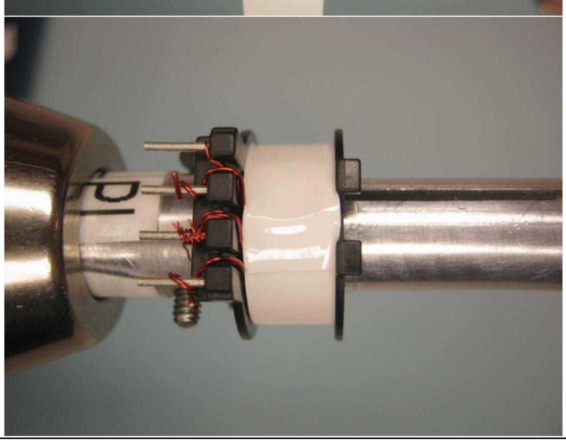
Winding preparation		Make slot with <u>3.0 mm width (minimum)</u> on bottom secondary flange of the bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 **1^{st} Primary**		Start at pin 4, wind 18 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2^{nd} Primary.

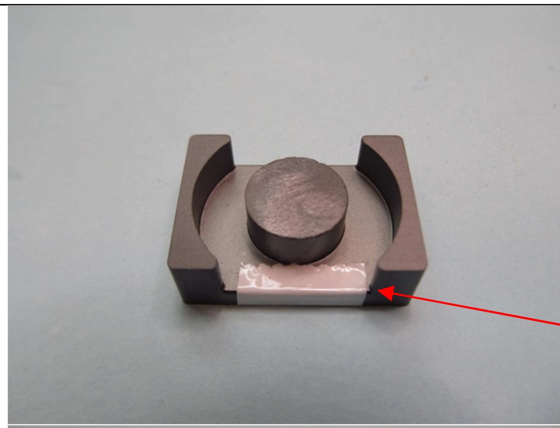
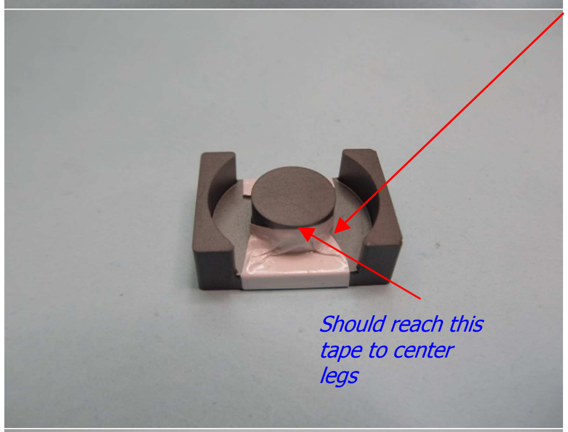
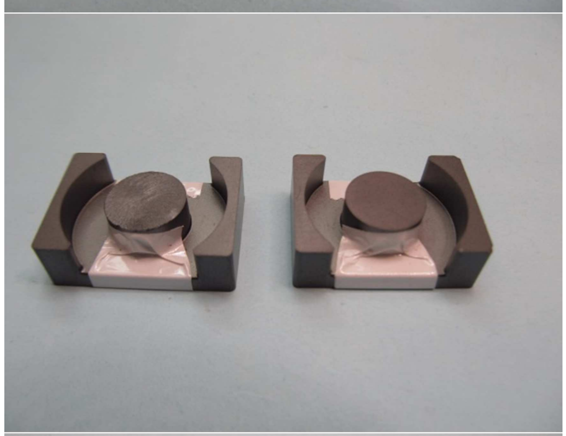
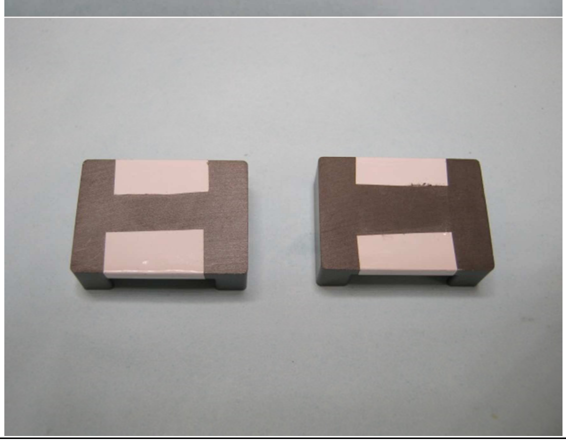
	 	
Insulation		1 layer of tape Item [8].
WD2: Bias & WD3: Shield1		Use 2 wires Item [4] start at pin 1 for Bias winding, also use 2 wires same Item [4] start at pin 3 for Shield1 winding. Wind all these 4 wires in parallel, at the 9th turn, cut short 2 wires as No-Connect for Shield 1 winding, and wind another turn -10th turn for Bias winding then bring wires back to the left to terminate at pin 3.

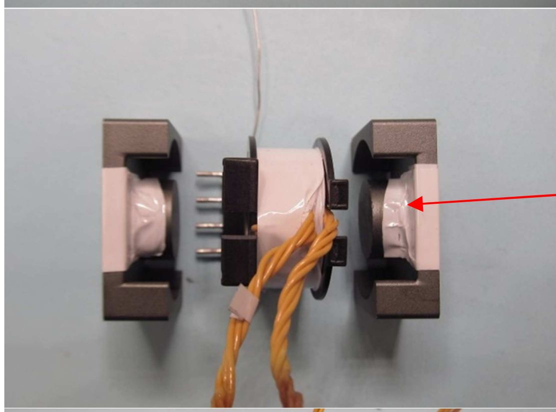
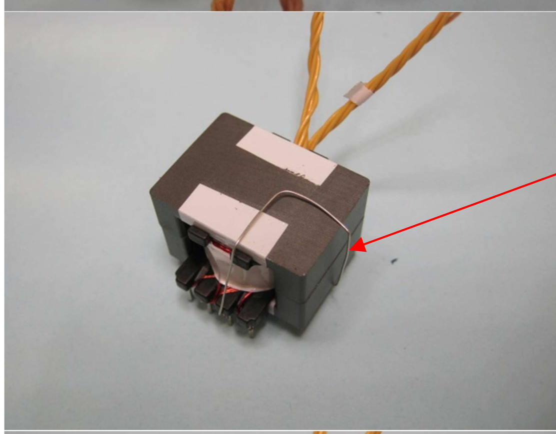
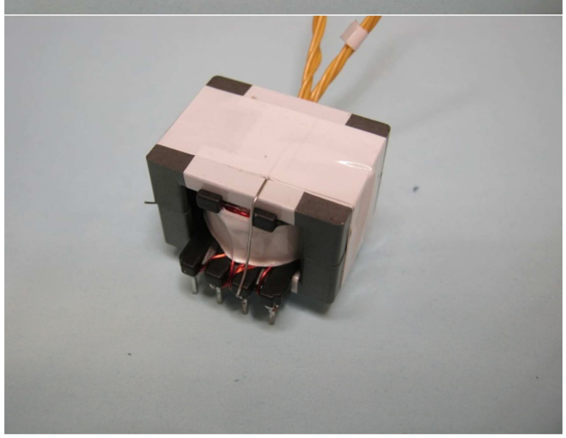
	 	
Insulation		1 layer of tape Item [8].
WD4 Secondary		Start at left slot of secondary side, use 2 wires Item [5], leaving ~ 40.0mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start

	 	and finish ends as FL1 and FL2. *Attn: When enter or exit these wires should be gently to void wire insulation get scratches or cuts by sharp edges of slots.*
Insulation		1 layer of tape Item [8].
WD5 Shield2		Start at pin 2, wind 15 tri-filar turns of wire Item [6], from left to right. At the last turn, cut short to leave as No-Connect.

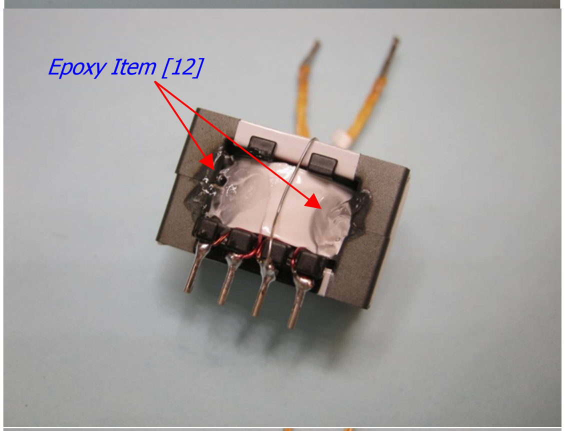
	 	
Insulation		1 layer of tape Item [8].
WD6 **2nd Primary**		Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.

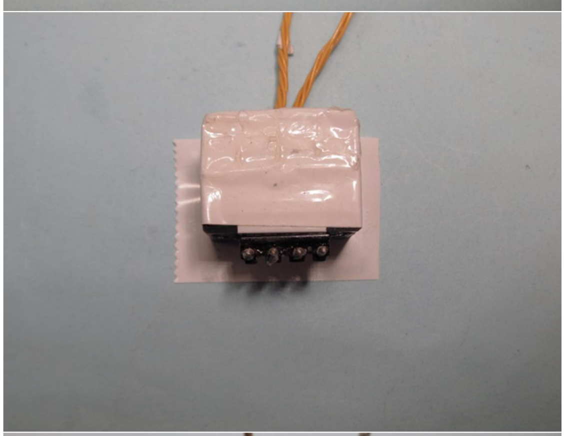
	 	
Insulation	 	1 layer of tape Item [8]. Bring 4 wires marked as FL1 to the right and secure with 2 layers of` tape Item [8].

Finish	   	Gap core halves to get 469 µH. <u>Place 1 tape Item [9] on one side</u> and <u>double layers on other side</u> of each core halve for both core halves *(see pictures below).*

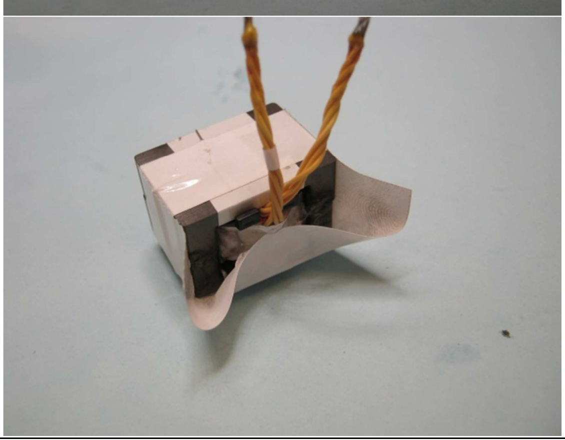
	 	Apply glue Item [11] at center legs and insert core halves to bobbin with secondary wire outputs on the sides which have double layers of tape (see pictures beside).
	 	Solder pin 3 with bus-wire Item [7] then lean along core halves and secure with tape.

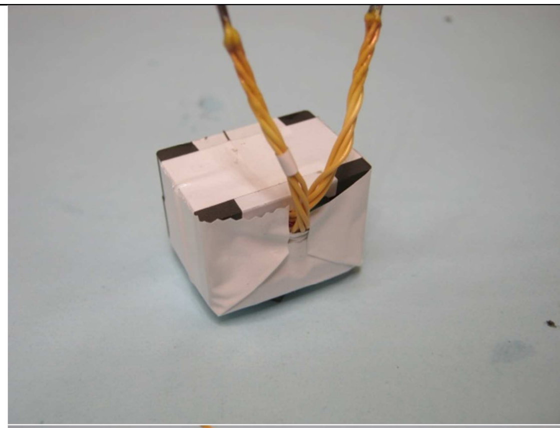
Apply epoxy Item [12] between cores to body of the transformer.
Varnish with Item [13].

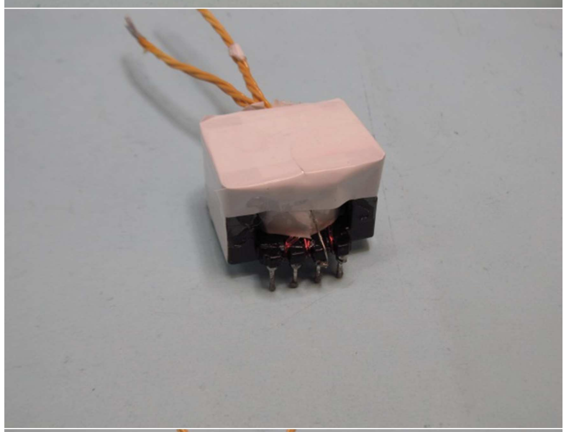


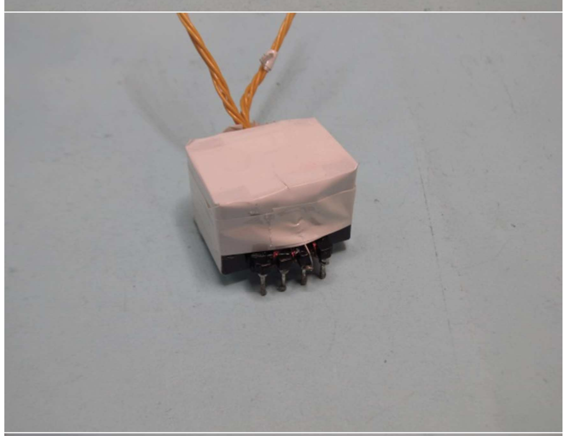


(<u>Attn:</u> Do steps below after varnishing).
Place 2 layers of tape Item [10] at the bottom

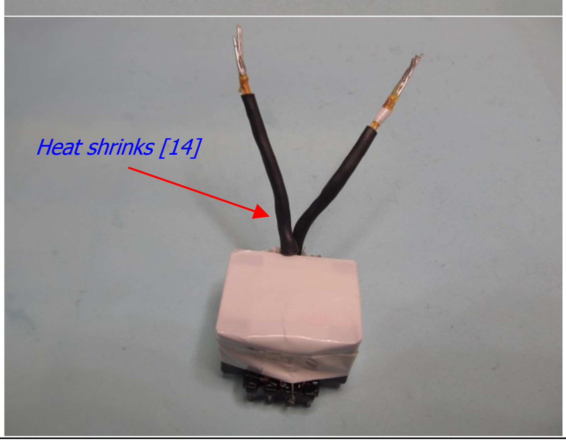








then wrap up also place 1 layer on top and wrap down to the body of transformer as shown in pictures beside.
Tape around 1turn of tape Item [8].



Insert heat shrinks Item [14] to secondary leads and apply heat to shrink.

Hi-Pot test: follow specs of "Electrical strength" in table "Electrical specifications" above, (should pass).
Finish

8 Common Mode Choke Specifications

8.1 *250 µH Common Mode Choke (L1)*

8.1.1 Electrical Diagram

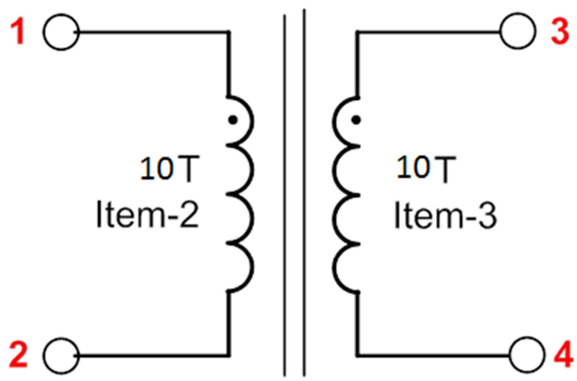


Figure 9 – Inductor Electrical Diagram.

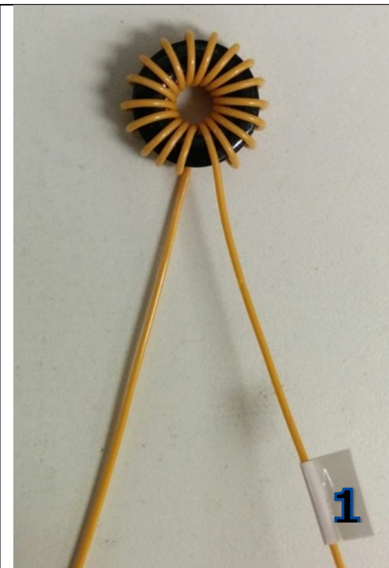
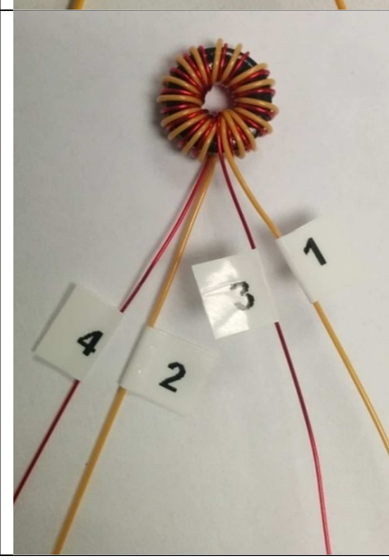
8.1.2 Electrical Specifications

Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	250 µH ±20%

8.1.3 Material List

Item	Description
[1]	Toroidal Core: 35T0375-10H, PI#: 32-00275-00.
[2]	Triple Insulated Wire: #26 AWG, Triple Coated.
[3]	Magnet Wire: #26 AWG, Double Coated.

8.1.4 Winding Instructions

<table>
<tr><td>Mark the start end of the winding as 1 and wind 10 turns of Item [2] on Item [1]. Mark the end of this winding as 2</td><td>
</td></tr>
<tr><td>Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding.
Varnish using Item [4]. Mark the start of this winding as 3 and the end as 4.</td><td>
</td></tr>
</table>

8.2 *18 mH Common Mode Choke (L2)*

8.2.1 Electrical Diagram

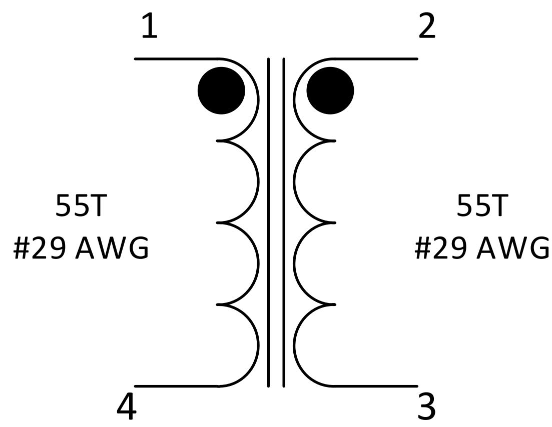


Figure 10 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	18 mH ±25%
Core effective Inductance Index		5950 nH/N^2
Leakage Inductance	Pins 1-4, with pins 2-3 shorted.	80 µH ±10%

8.2.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID T14 x 8 x 5.5, PI#: 32-00286-00.
[2]	Divider: Cable Tie, Panduit - Fish Paper, Insulating Cotton Rag, 0.010” Thick, PI#: 66-00042-00.
[3]	Magnet Wire: #29 AWG Heavy Nyleze.
[4]	Epoxy: Devon, 5mins Epoxy; or Equivalent.

8.2.4 Winding Instructions

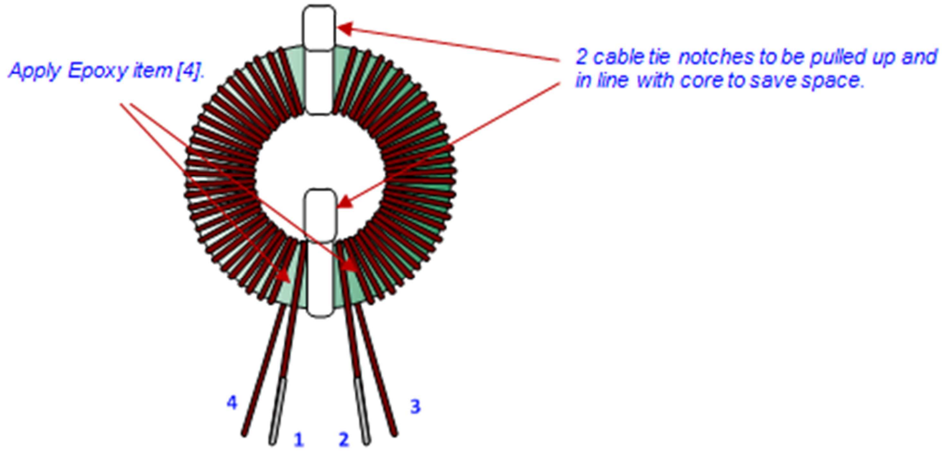


Figure 11 – 18 mH CMC Illustration Image.

- Place 2 pieces of cable tie Item [2] on to toroid Item [1] to divide 2 equal sections.
- Use 4 ft of wire Item [3], start as 1, wind 55 turns in 2 layers in a half section of toroid, and end as 4.
- Do the same for another half of Toroid, start as 2 and end as 3.
- Pull up 2 notches of cable ties to be in line with toroid body (to save space) and apply Epoxy Item [4] where leads floating.

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-PD Flyback_021521; Rev.0.4; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-PD Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX	265		265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9	SET-POINT 1					
10	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	3.000		3.000	A	Output current 1
12	POUT1			63.00	W	Output power 1
13	EFFICIENCY1	0.89		0.89		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
15	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
17	SET-POINT 2					
18	VOUT2	20.00		20.00	V	Output voltage 2
19	IOUT2	3.000		3.000	A	Output current 2
20	POUT2			60.00	W	Output power 2
21	EFFICIENCY2	0.88		0.88		Converter efficiency for output 2
22	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
25	SET-POINT 3					
26	VOUT3	15.00		15.00	V	Output voltage 3
27	IOUT3	3.000		3.000	A	Output current 3
28	POUT3			45.00	W	Output power 3
29	EFFICIENCY3	0.88		0.88		Converter efficiency for output 3
30	Z_FACTOR3	0.50		0.50		Z-factor for output 3
31	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
33	SET-POINT 4					
34	VOUT4	9.00		9.00	V	Output voltage 4
35	IOUT4	3.000		3.000	A	Output current 4
36	POUT4			27.00	W	Output power 4
37	EFFICIENCY4	0.88		0.88		Converter efficiency for output 4
38	Z_FACTOR4	0.50		0.50		Z-factor for output 4
39	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
41	SET-POINT 5					
42	VOUT5	5.00		5.00	V	Output voltage 5
43	IOUT5	3.000		3.000	A	Output current 5
44	POUT5			15.00	W	Output power 5
45	EFFICIENCY5	0.88		0.88		Converter efficiency for output 5
46	Z_FACTOR5	0.50		0.50		Z-factor for output 5
47	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery

						Object)
81	VOLTAGE_CDC				V	Cable drop compensation implemented in firmware
85	**PRIMARY CONTROLLER SELECTION**					
86	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
87	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
88	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
89	DEVICE_GENERIC	INN38X9		INN38X9		Device selection
90	DEVICE_CODE			INN3879C		Device code
91	PDEVICE_MAX			65	W	Device maximum power capability
92	RDSON_25DEG			0.44	Ω	Primary switch on-time resistance at 25°C
93	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.980	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.130	A	Primary switch typical current limit
96	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.48	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			588.31	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	85300	Info	85300	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
104	VOR	145.0		145.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			86.76	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.719		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.627		Primary switch duty cycle
109	TIME_ON			11.28	us	Primary switch on-time
110	TIME_OFF			4.37	us	Primary switch off-time
111	LPRIMARY_MIN			445.7	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			469.2	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			492.6	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.775	A	Primary switch average current
118	IPEAK_PRIMARY			2.164	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.543	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.066	A	Primary switch ripple current
121	IRMS_PRIMARY			1.067	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			15.151	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			3.798	A	Secondary winding pedestal current
126	IRMS_SECONDARY			5.762	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			4.919	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	CUSTOM		CUSTOM		Core selection
134	CORE NAME	EQ25		EQ25		Core code

135	AE	95.0		95.0	mm^2	Core cross sectional area
136	LE	41.4		41.4	mm	Core magnetic path length
137	AL	5710		5710	nH	Ungapped core effective inductance per turns squared
138	VE	4145		4145	mm^3	Core volume
139	BOBBIN NAME	EQ25-Custom		EQ25-Custom		Bobbin name
140	AW	44.0		44.0	mm^2	Bobbin window area
141	BW	8.00		8.00	mm	Bobbin width
142	MARGIN	0.0		0.0	mm	Bobbin safety margin
144	**PRIMARY WINDING**					
145	NPRIMARY			35		Primary winding number of turns
146	BPEAK			3456	Gauss	Peak flux density
147	BMAX			3170	Gauss	Maximum flux density
148	BAC			1508	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			383	nH	Typical gapped core effective inductance per turns squared
150	LG			0.291	mm	Core gap length
151	LAYERS_PRIMARY	2		2		Primary winding number of layers
152	AWG_PRIMARY	26		26		Primary wire gauge
153	OD_PRIMARY_INSULATED			0.465	mm	Primary wire insulated outer diameter
154	OD_PRIMARY_BARE			0.405	mm	Primary wire bare outer diameter
155	CMA_PRIMARY			238.1	Cmils/A	Primary winding wire CMA
157	**SECONDARY WINDING**					
158	NSECONDARY	5		5		Secondary winding number of turns
159	AWG_SECONDARY			19		Secondary wire gauge
160	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
161	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
162	CMA_SECONDARY			223.6	Cmils/A	Secondary winding wire CMA
164	**BIAS WINDING**					
165	NBIAS			8		Bias winding number of turns
169	**PRIMARY COMPONENTS SELECTION**					
170	**LINE UNDERVOLTAGE**					
171	BROWN-IN REQURED	76.00		76.00	V	Required line brown-in threshold
172	RLS			4.00	MΩ	Connect two 2 MOhm resistors to the V-pin for the required UV/OV threshold
173	BROWN-IN ACTUAL			75.98	V	Actual brown-in threshold using standard resistors
174	BROWN-OUT ACTUAL			66.93	V	Actual brown-out threshold using standard resistors
176	**LINE OVERVOLTAGE**					
177	OVERVOLTAGE_LINE		Warning	334.21	V	The device voltage stress will be higher than 650V when overvoltage is triggered
179	**BIAS WINDING**					
180	VBIAS	7.00		7.00	V	Rectified bias voltage at the cable disconnect (5V) set-point
181	VF_BIAS			0.70	V	Bias winding diode forward drop
182	VREVERSE_BIASDIODE			92.33	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS			22	uF	Bias winding rectification capacitor
184	CBPP			4.70	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					
190	VDRAIN_OFF_SRFET			74.33	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AUTO		AO4294		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown

						voltage
193	RDSON_SRFET			15.5	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
197	**SET-POINTS ANALYSIS**					
198	**TOLERANCE CORNER**					
199	USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
200	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
201	USER_LPRIMARY	TYP		469.2	uH	Primary inductance corner to be evaluated
203	**SET-POINT SELECTION**					
204	SET-POINT	1		1		Select the set-point which needs to be evaluated
205	FSWITCHING			68672.3	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
206	VOR			145.0	V	Voltage reflected to the primary winding when the primary switch turns off
207	VMIN			131.23	V	Valley of the minimum input AC voltage
208	KP			1.101		Measure of continuous/discontinuous mode of operation
209	MODE_OPERATION			DCM		Mode of operation
210	DUTYCYCLE			0.502		Primary switch duty cycle
211	TIME_ON			7.30	us	Primary switch on-time
212	TIME_OFF			7.26	us	Primary switch off-time
214	**PRIMARY CURRENT**					
215	IAVG_PRIMARY			0.511	A	Primary switch average current
216	IPEAK_PRIMARY			2.038	A	Primary switch peak current
217	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
218	IRIPPLE_PRIMARY			2.038	A	Primary switch ripple current
219	IRMS_PRIMARY			0.833	A	Primary switch RMS current
221	**SECONDARY CURRENT**					
222	IPEAK_SECONDARY			14.264	A	Secondary winding peak current
223	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
224	IRMS_SECONDARY			5.542	A	Secondary winding RMS current
225	IRIPPLE_CAP_OUT			4.659	A	Output capacitor ripple current
227	**MAGNETIC FLUX DENSITY**					
228	BPEAK			3076	Gauss	Peak flux density
229	BMAX			2875	Gauss	Maximum flux density
230	BAC			1438	Gauss	AC flux density (0.5 x Peak to Peak)

Note that the warning information above has been verified not an issue for this design (INN3879C is a 750V rating device).

10 Performance Data

Note 1: Output voltages measured at the end of cable
2: Measurements taken at room temperature (approximately 24 °C)

10.1 *No-Load Input Power at 5 V_{OUT}*

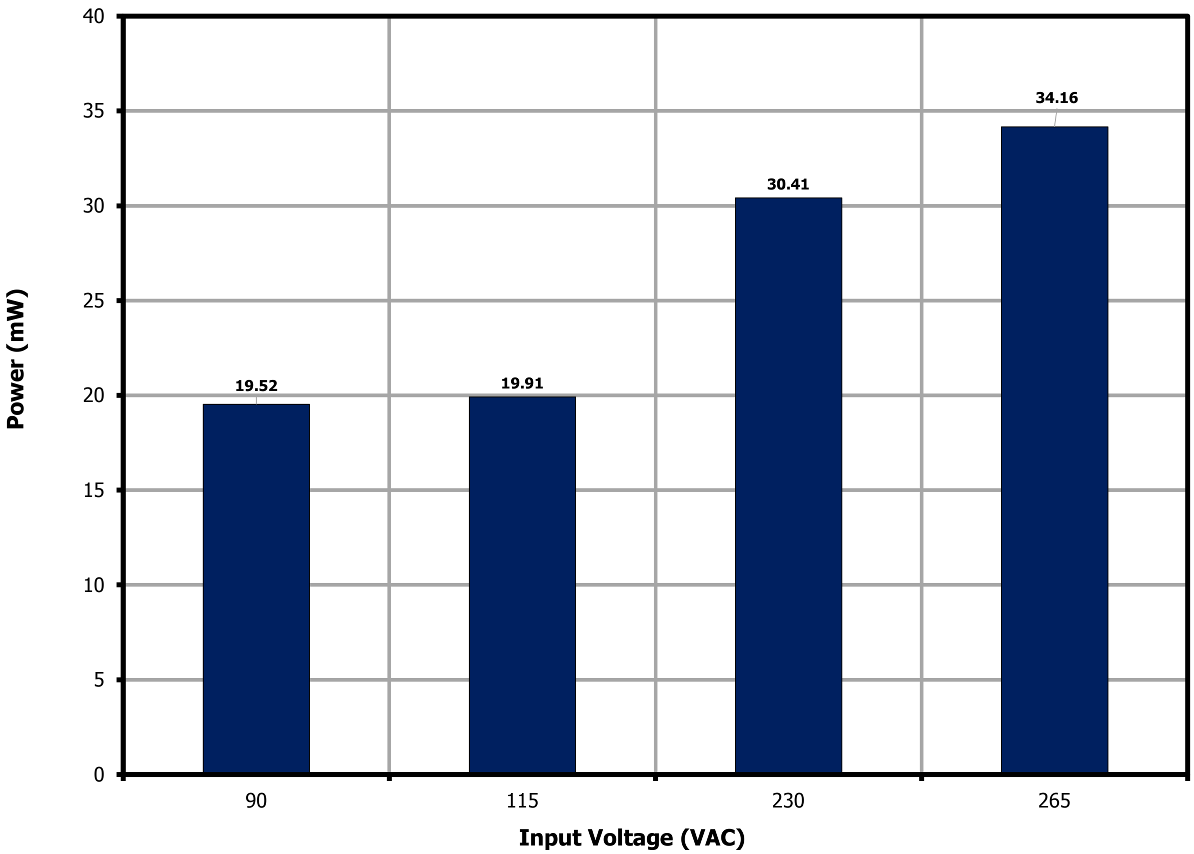


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.2 *Full Load Efficiency*

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	**115 VAC**	**230 VAC**	**265 VAC**
5	3	15	84.83	85.32	85.37	85.16
9	3	29	87.88	88.35	89.25	89.14
15	3	45	89.15	89.81	91.06	91.05
20	3	60	88.53	90.26	91.63	91.68

10.3 *Average and 10% Load Efficiency (End of cable)*

10.3.1 Efficiency Requirements

		Test Effective Power (W)	Average 2016 New EISA2007	Average Jan-16 CoC v5 Tier 2	10% Load Jan-16 CoC v5 Tier 2
V_{OUT} (V)	Model (V)				
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6 %	87.3%	77.3%
15	>6	45	87.7%	88.9%	78.9%
20	>6	60	88.0%	89.0%	79.0%

10.3.2 Efficiency Performance Summary (End of Cable with CDC Enabled)

V_{OUT} (V)	Current (A)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	3	87.88	86.94	89.49	86.23
9	3	90.04	89.99	89.82	87.35
15	3	90.79	91.38	88.96	87.28
20	3	90.92	91.72	88.48	87.06

10.3.3 Average and 10% Load Efficiency at 115 VAC (End of Cable)

10.3.3.1 Output: 5 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	4.89	2.992	85.32	**87.88**
75	4.92	2.243	87.17	
50	4.95	1.490	88.91	
25	4.96	0.740	90.11	
10	4.98	0.291	**89.49**	

10.3.3.2 Output: 9 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	8.89	2.993	88.35	**90.04**
75	8.93	2.243	89.56	
50	8.95	1.491	90.80	
25	8.97	0.741	91.47	
10	8.98	0.291	**89.82**	

10.3.3.3 Output: 15 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	14.92	2.993	89.81	**90.79**
75	14.96	2.243	90.60	
50	15.00	1.490	91.35	
25	15.02	0.740	91.39	
10	15.02	0.291	**88.96**	

10.3.3.4 Output: 20 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	19.93	2.991	90.26	**90.92**
75	19.98	2.242	90.81	
50	20.03	1.490	91.31	
25	20.05	0.740	91.29	
10	20.04	0.291	**88.48**	

10.3.4 Average and 10% Load Efficiency at 230 VAC (End of Cable)

10.3.4.1 Output: 5 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	4.90	2.992	85.37	**86.94**
75	4.93	2.243	86.79	
50	4.95	1.491	87.73	
25	4.97	0.740	87.87	
10	4.98	0.291	**86.23**	

10.3.4.2 Output: 9 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	8.92	2.993	89.25	**89.99**
75	8.95	2.243	90.09	
50	8.97	1.491	90.65	
25	8.98	0.741	89.97	
10	8.99	0.291	**87.35**	

10.3.4.3 Output: 15 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	14.96	2.993	91.06	**91.38**
75	15.00	2.243	91.54	
50	15.03	1.491	91.87	
25	15.04	0.741	91.06	
10	15.05	0.291	**87.28**	

10.3.4.4 Output: 20 V / 3 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	19.99	2.992	91.63	**91.72**
75	20.03	2.243	92.01	
50	20.06	1.490	92.08	
25	20.07	0.740	91.16	
10	20.07	0.291	**87.06**	

10.4 *Efficiency Across Line (End of cable)*

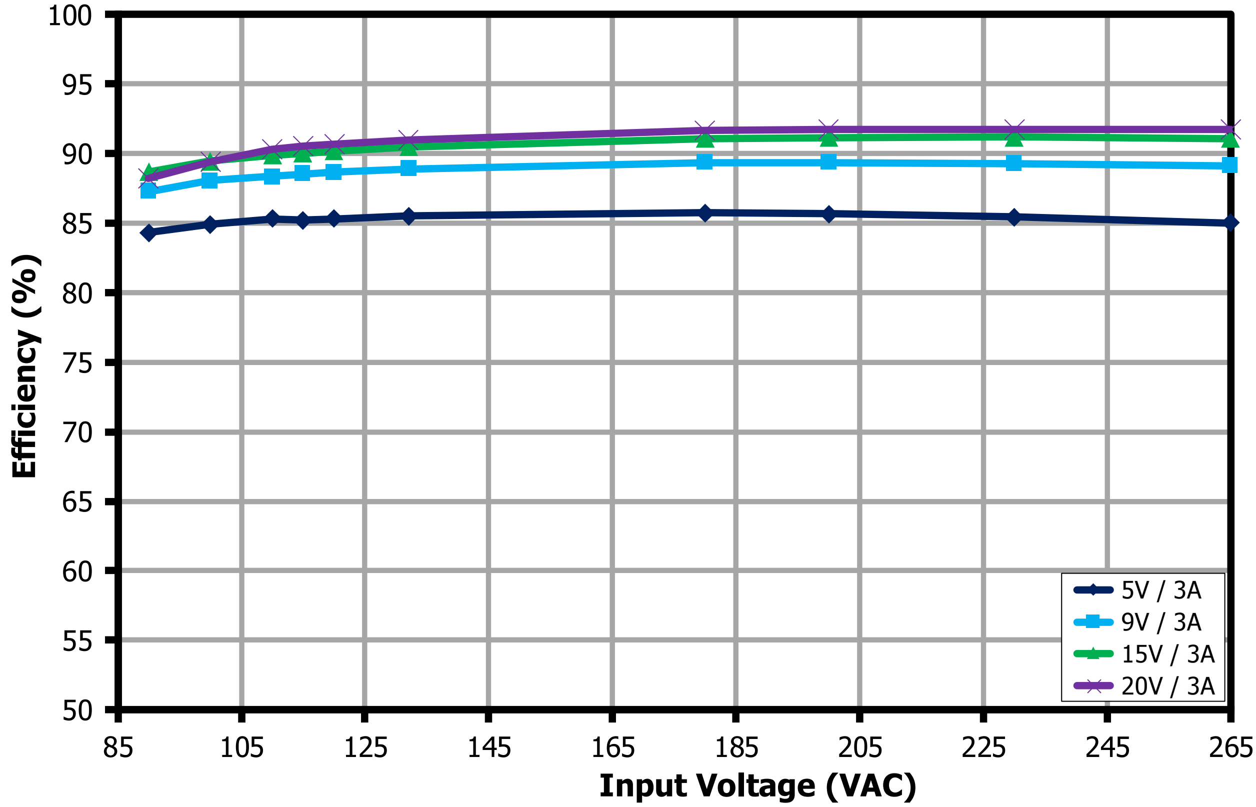


Figure 13 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

10.5 *Line Regulation (End of Cable)*

10.5.1 Output: 5 V / 3 A

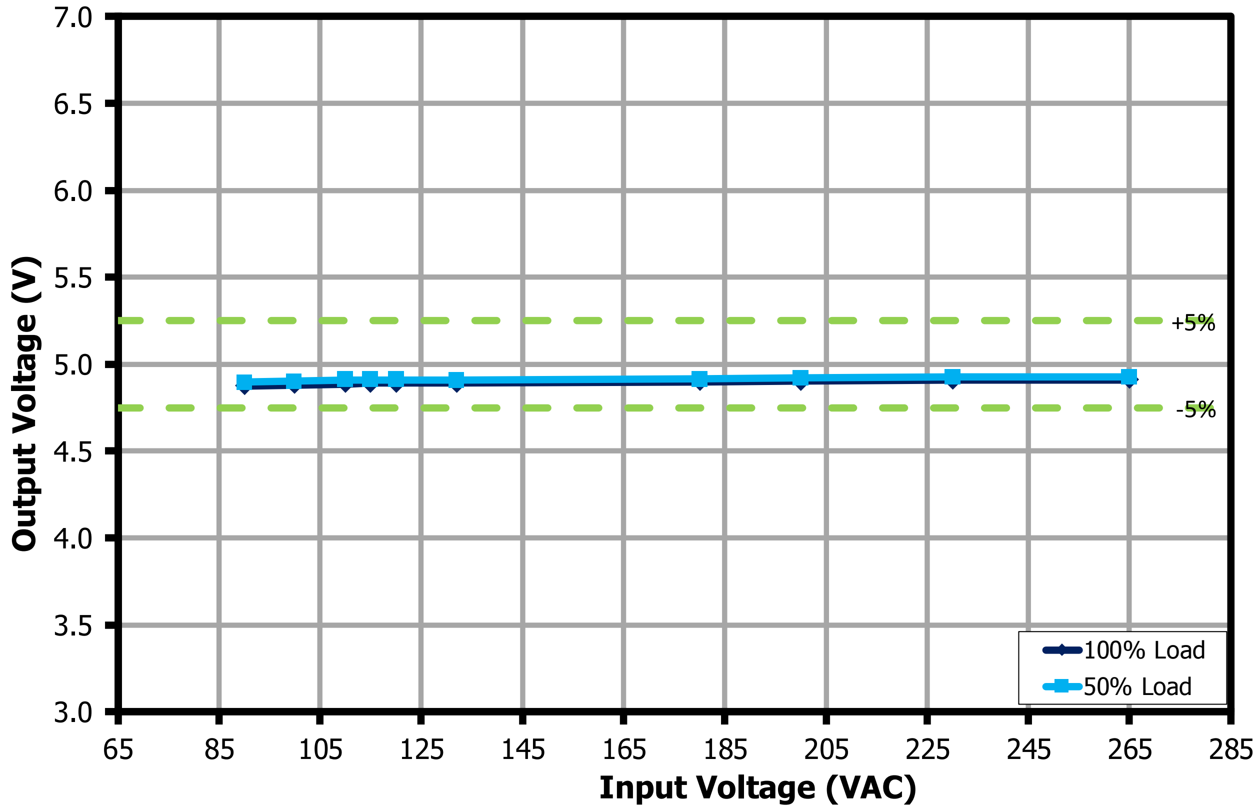


Figure 14 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

10.5.2 Output: 9 V / 3 A

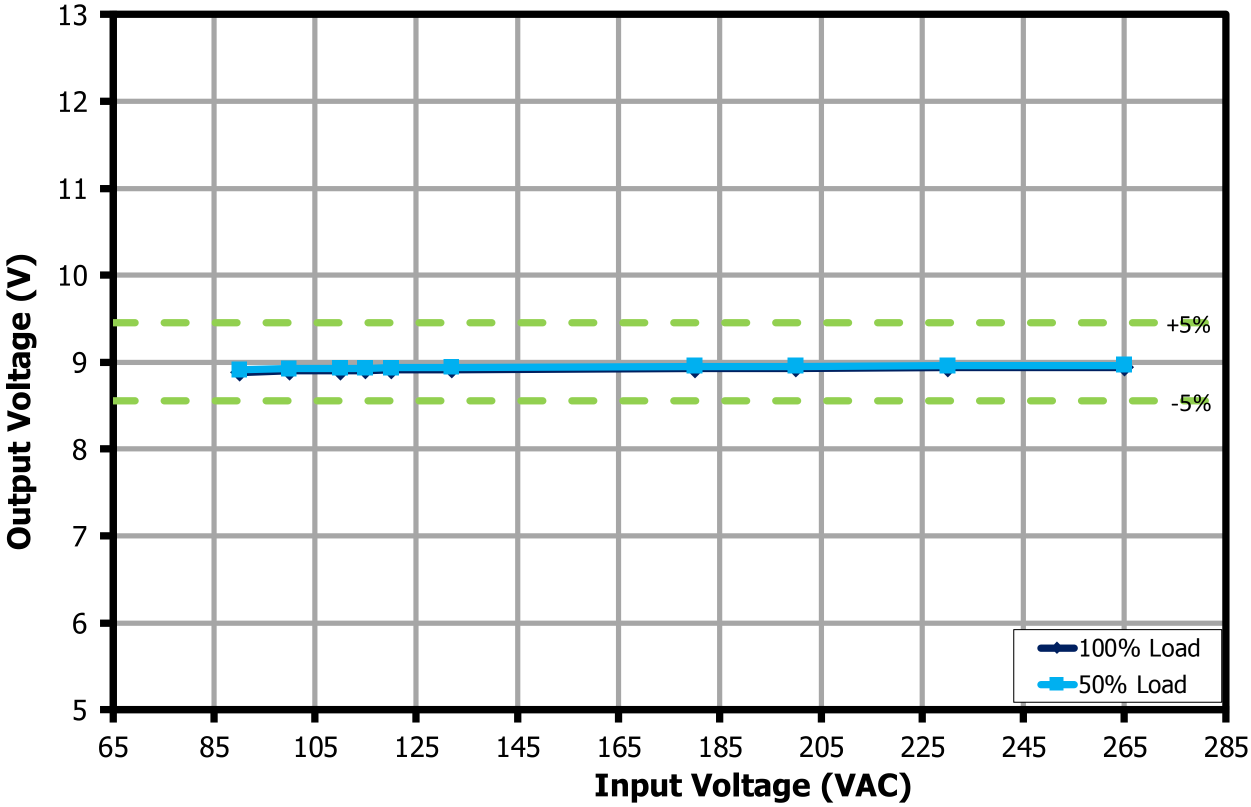


Figure 15 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.5.3 Output: 15 V / 3 A

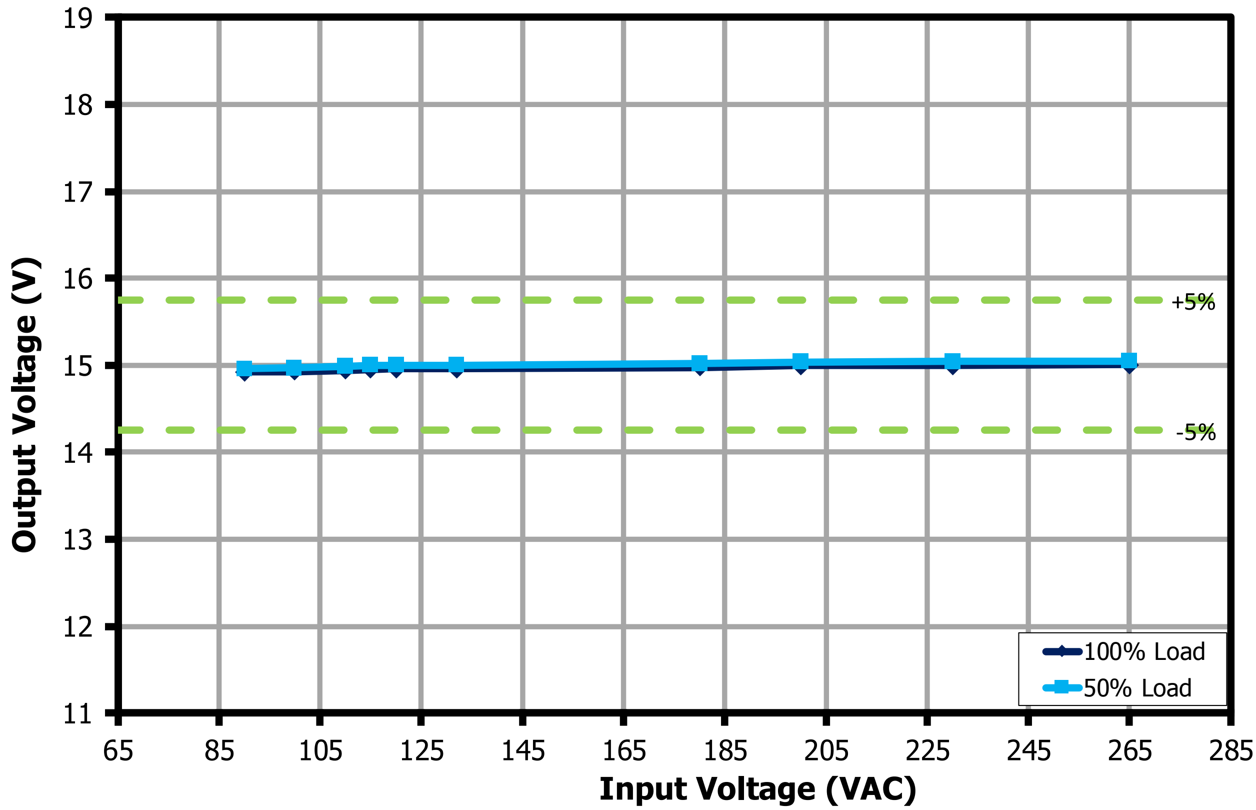


Figure 16 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

10.5.4 Output: 20 V / 3 A

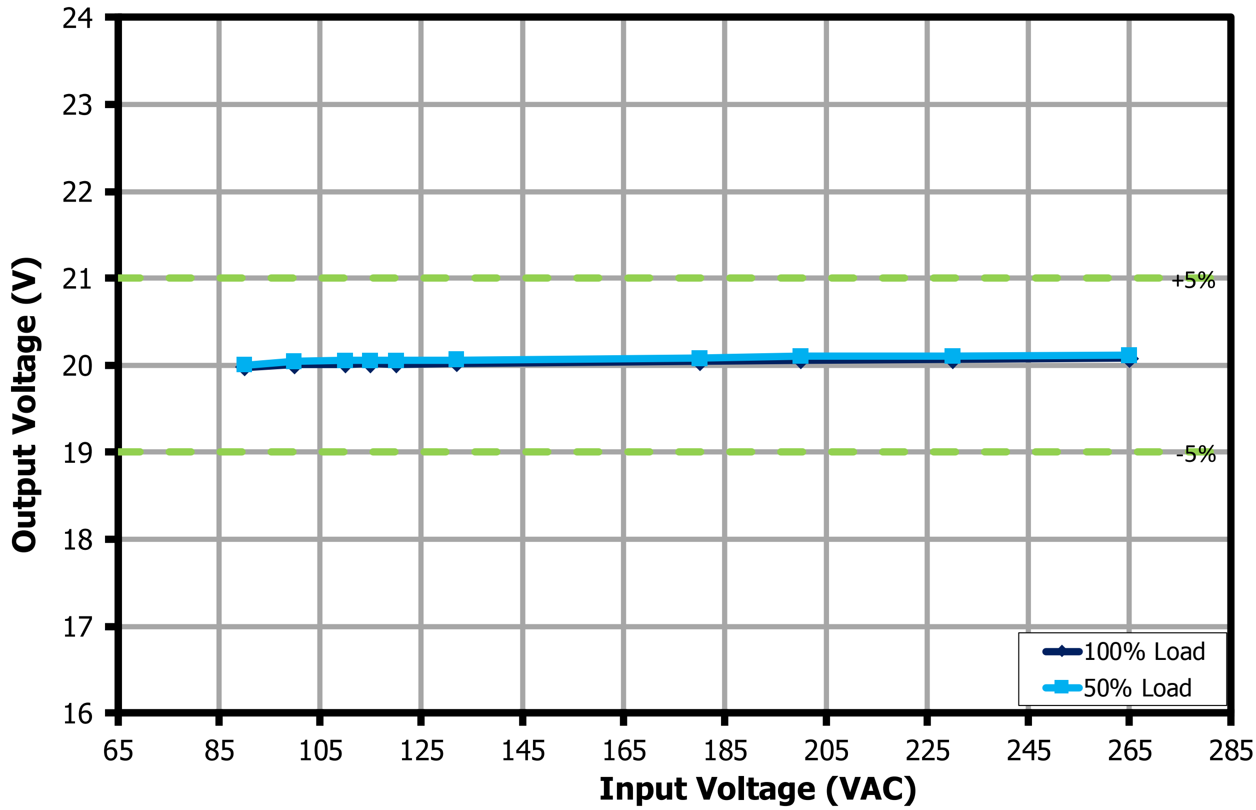


Figure 17 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

10.6 *Load Regulation (End of Cable)*

10.6.1 Output: 5 V / 3 A

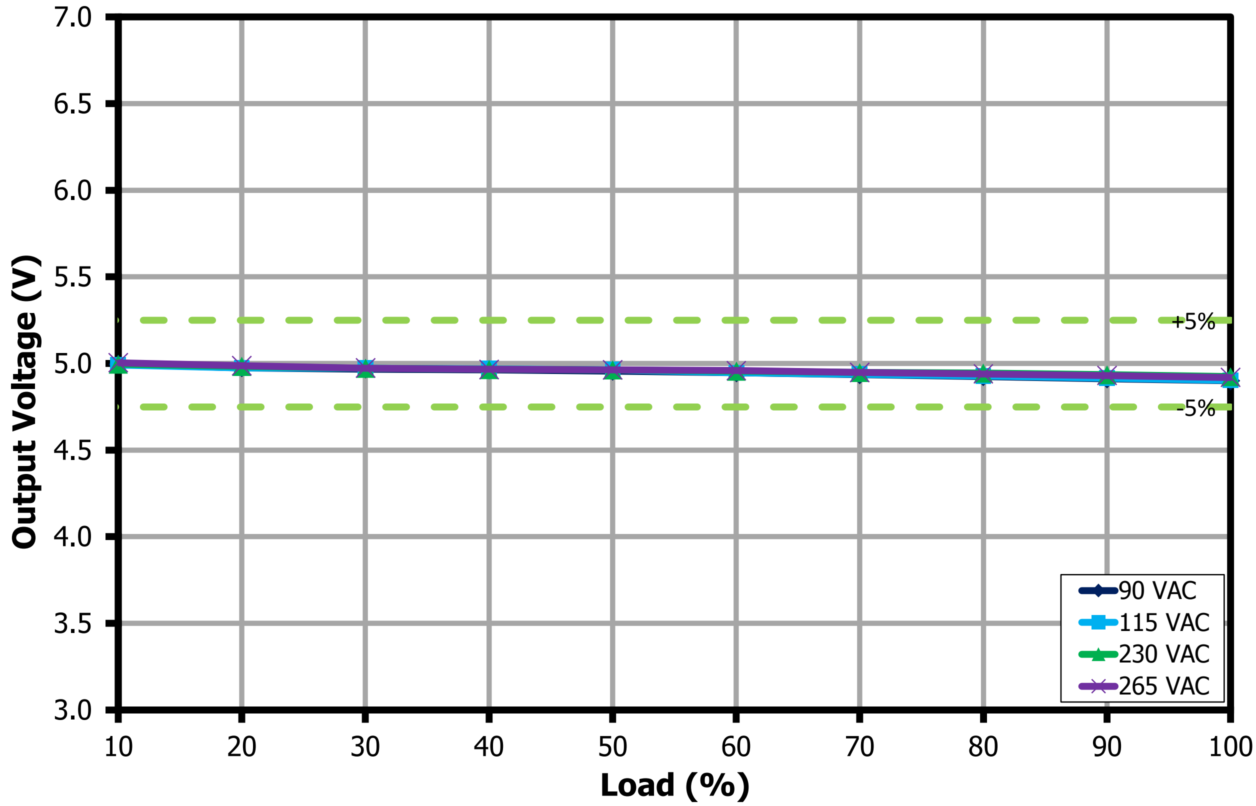


Figure 18 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

10.6.2 Output: 9 V / 3 A

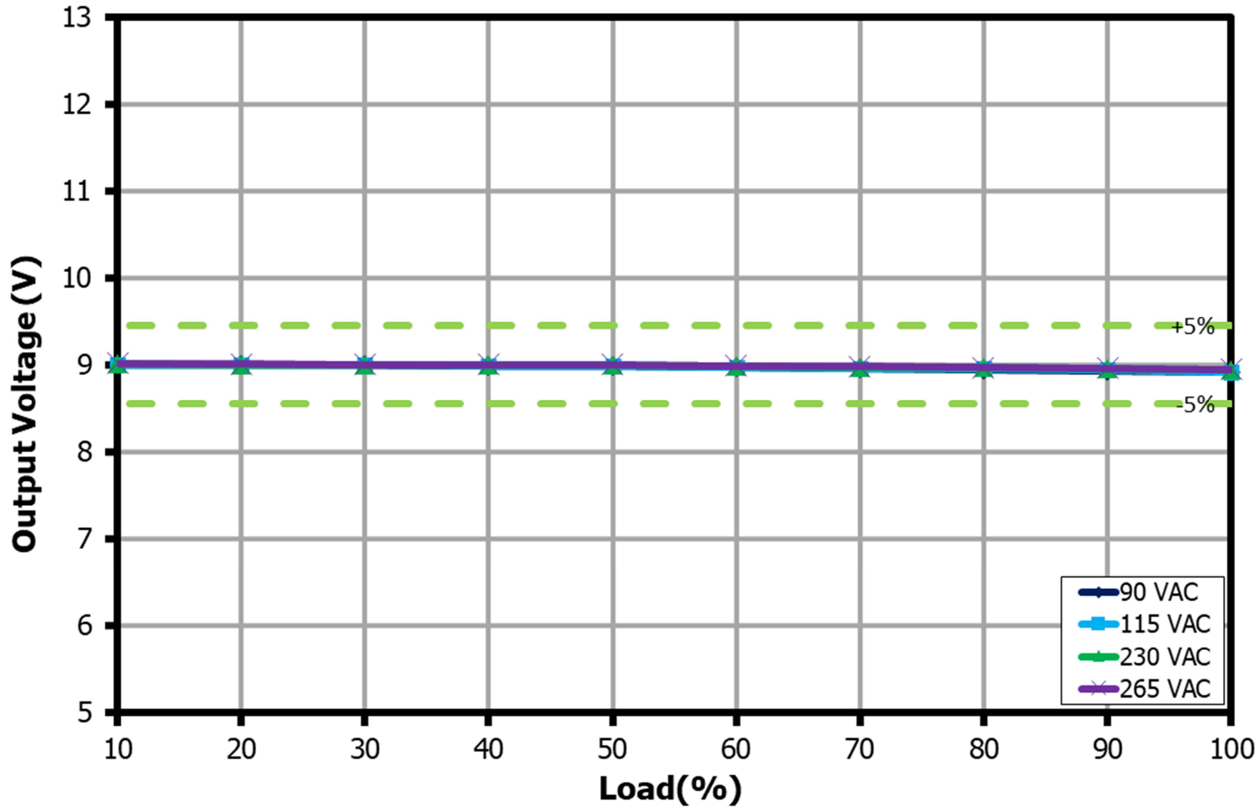


Figure 19 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

10.6.3 Output: 15 V / 3 A

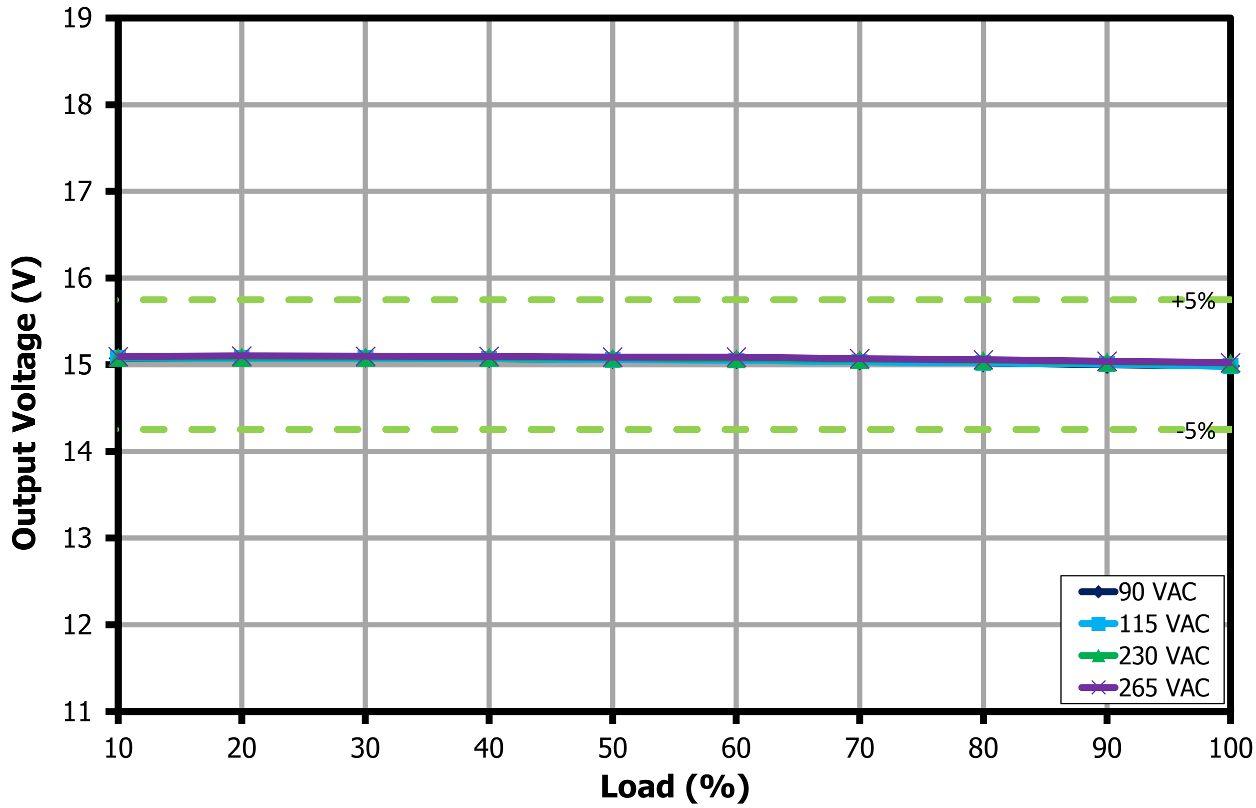


Figure 20 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

10.6.4 Output: 20 V / 3 A

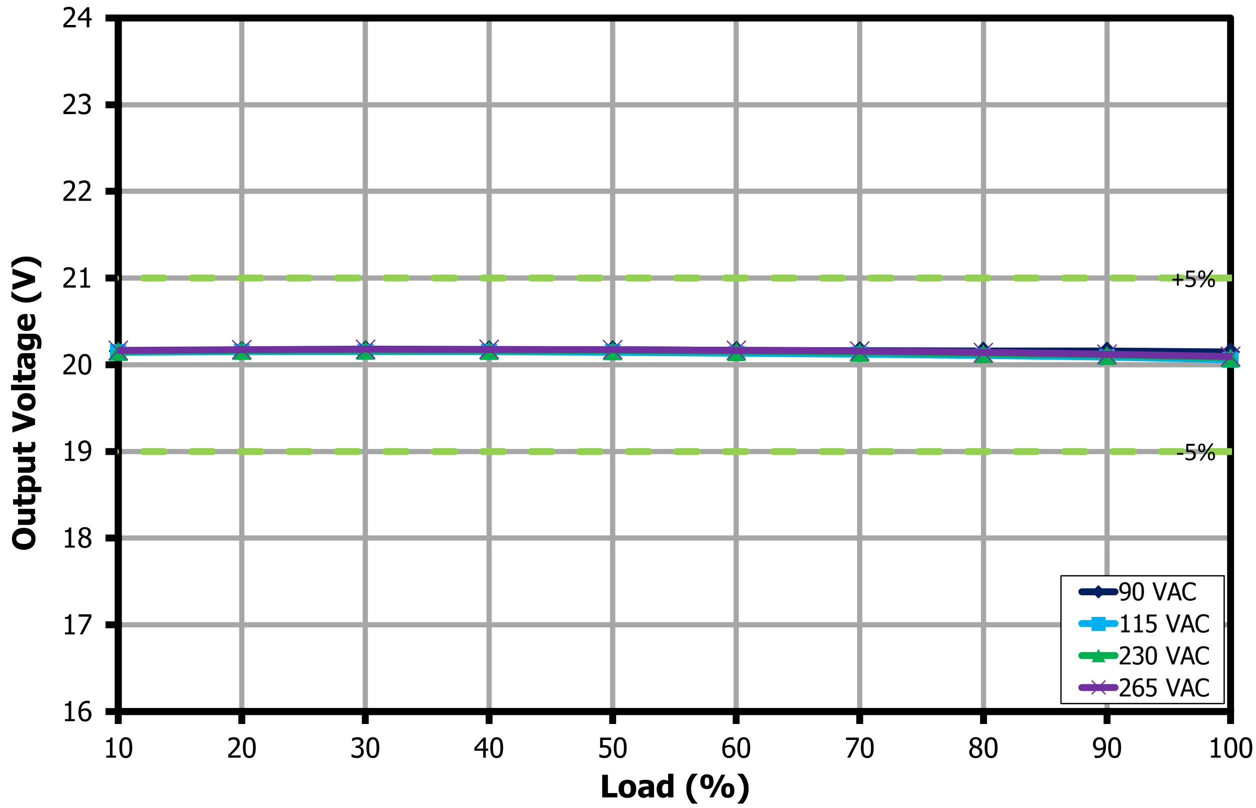


Figure 21 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

11 Thermal Performance in Open Case

Note: The performance data below is for open case operation under room temperature with one-hour soak for each condition

11.1 *Output: 5 V / 3 A (90 VAC)*

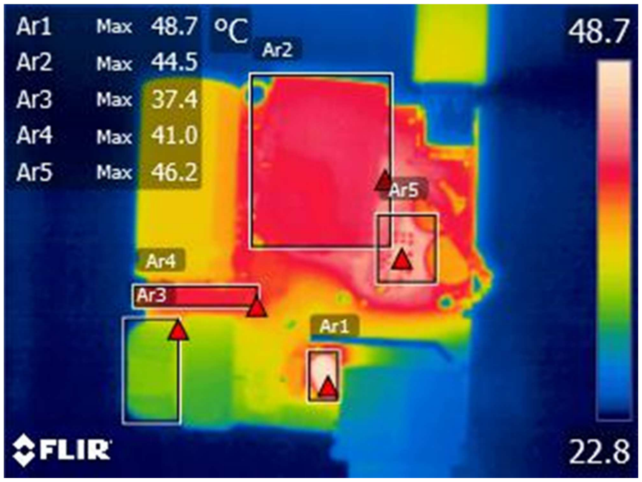


Figure 22 – Top Thermal Image.
Ar1: Thermistor, RT1 = 48.7 ºC.
Ar2: Transformer, T1 = 44.5 ºC.
Ar3: CMC, L2 = 37.4 ºC.
Ar4: Bridge Diode, BR1 = 41.0 ºC.
Ar5: PCB Near Transformer = 46.2 ºC.

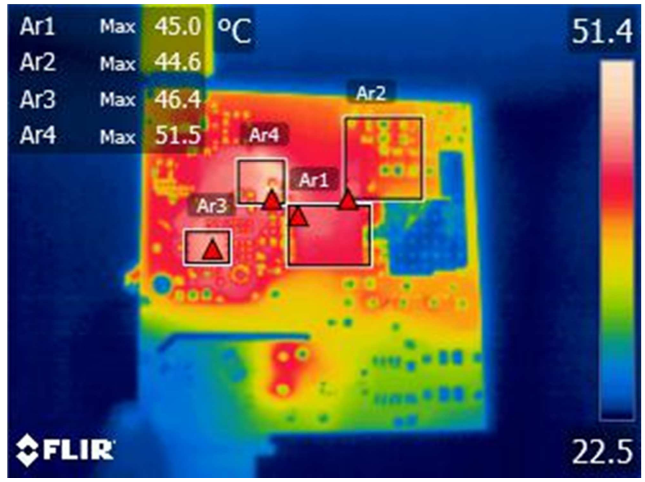


Figure 23 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 45.0 ºC.
Ar2: Primary Snubber = 44.6 ºC.
Ar3: SR FET, Q2 = 46.4 ºC.
Ar4: PCB Under Transformer = 51.5 ºC.
Ambient: = 22.5 ºC.

11.2 *Output: 5 V / 3 A (265 VAC)*

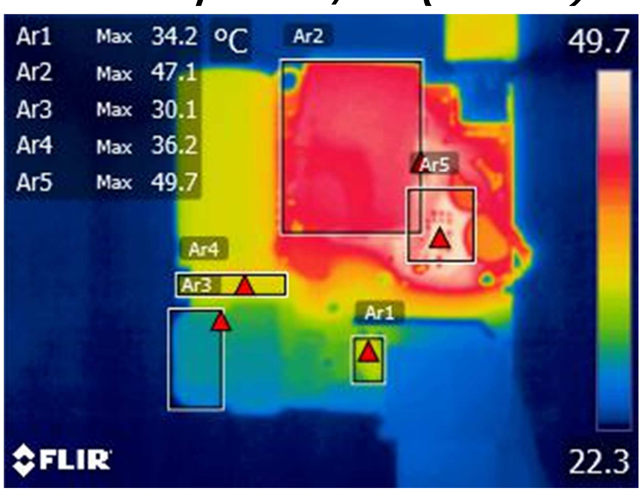


Figure 24 – Top Thermal Image.
Ar1: Thermistor, RT1 = 34.2 ºC.
Ar2: Transformer, T1 = 47.1 ºC.
Ar3: CMC, L2 = 30.1 ºC.
Ar4: Bridge Diode, BR1 = 36.2 ºC.
Ar5: PCB Near Transformer = 49.7 ºC.

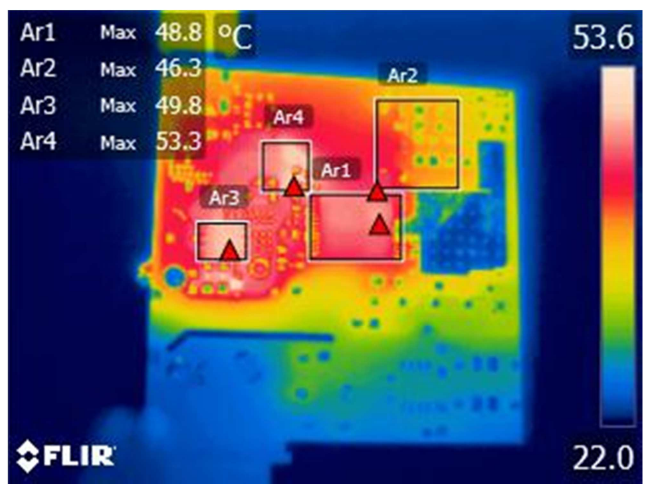


Figure 25 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 48.8 ºC.
Ar2: Primary Snubber = 46.3 ºC.
Ar3: SR FET, Q2 = 49.8 ºC.
Ar4: PCB Under Transformer = 53.3 ºC.
Ambient: = 22.2 ºC.

11.3 *Output: 9V / 3 A (90 VAC)*

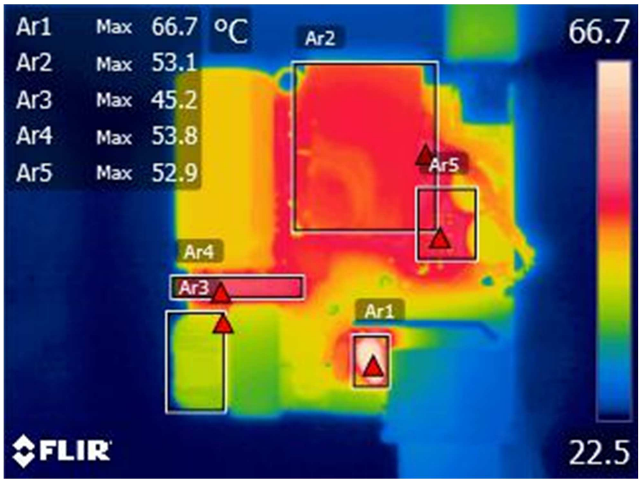


Figure 26 – Top Thermal Image.
Ar1: Thermistor, RT1 = 66.7 ºC.
Ar2: Transformer, T1 = 53.1 ºC.
Ar3: CMC, L2 = 45.2 ºC.
Ar4: Bridge Diode, BR1 = 53.8 ºC.
Ar5: PCB Near Transformer = 52.9 ºC.

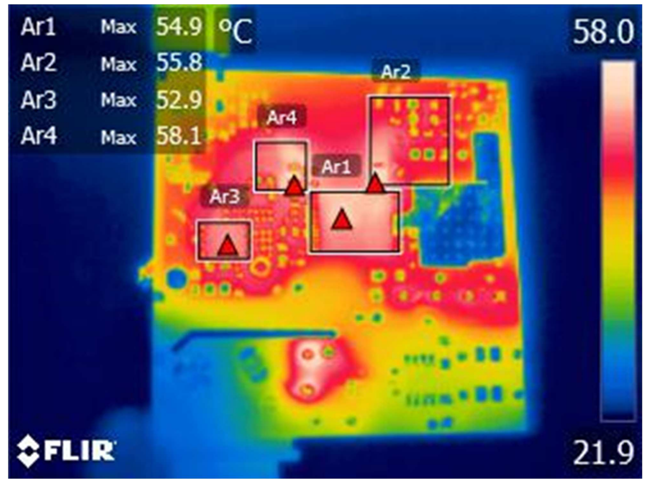


Figure 27 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 54.9 ºC.
Ar2: Primary Snubber = 55.8 ºC.
Ar3: SR FET, Q2 = 52.9 ºC.
Ar4: PCB Under Transformer = 58.1 ºC.
Ambient: = 23.1 ºC.

11.4 *Output: 9 V / 3 A (265 VAC)*

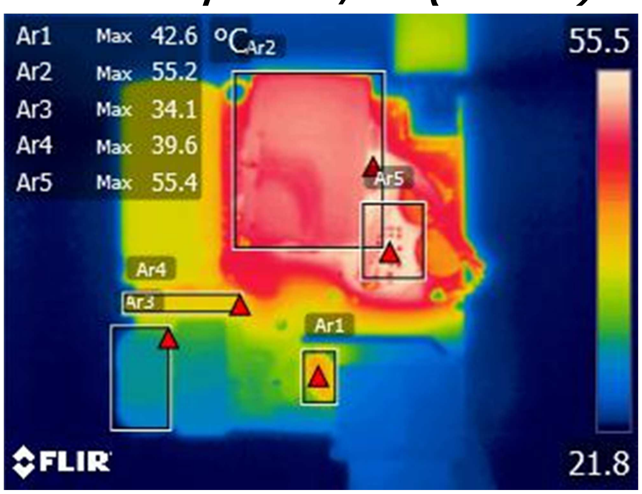


Figure 28 – Top Thermal Image.
Ar1: Thermistor, RT1 = 42.6 ºC.
Ar2: Transformer, T1 = 55.2 ºC.
Ar3: CMC, L2 = 34.1 ºC.
Ar4: Bridge Diode, BR1 = 39.6 ºC.
Ar5: PCB Near Transformer = 55.4 ºC.

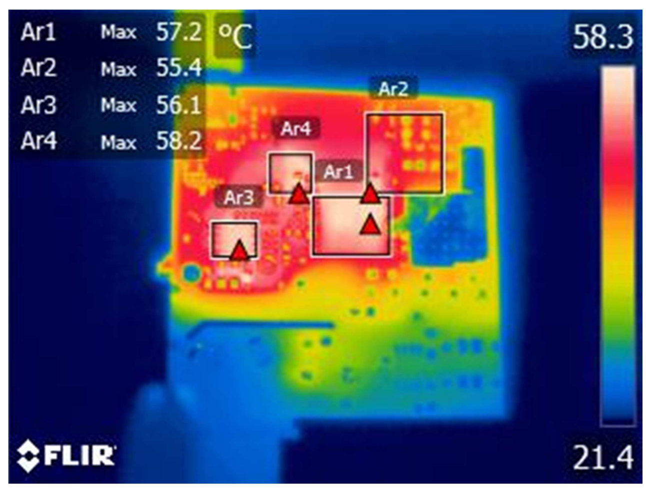


Figure 29 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 57.2 ºC.
Ar2: Primary Snubber = 55.4 ºC.
Ar3: SR FET, Q2 = 56.1 ºC.
Ar4: PCB Under Transformer = 58.2 ºC.
Ambient: = 22.6 ºC.

11.5 ***Output: 15 V / 3 A (90 VAC)***

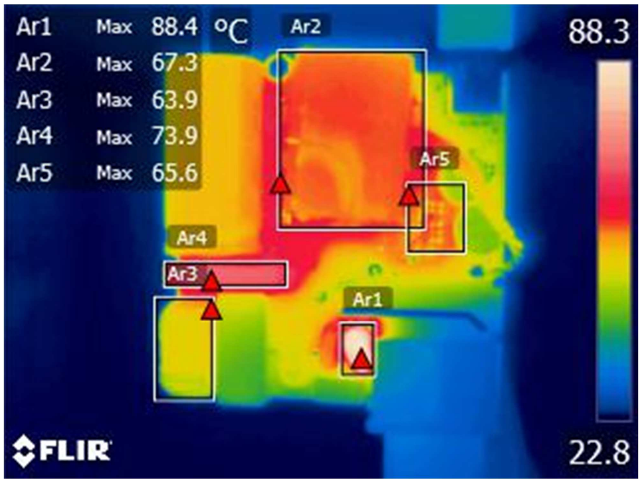


Figure 30 – Top Thermal Image.
Ar1: Thermistor, RT1 = 88.4 ºC.
Ar2: Transformer, T1 = 67.3 ºC.
Ar3: CMC, L2 = 63.9 ºC.
Ar4: Bridge Diode, BR1 = 73.9 ºC.
Ar5: PCB Near Transformer = 65.6 ºC.

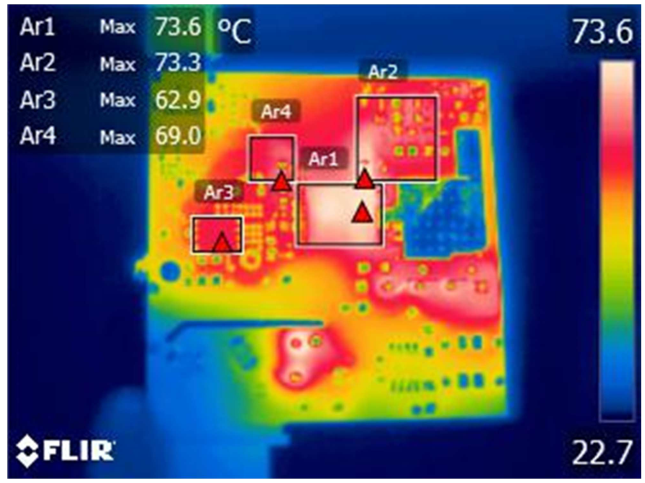


Figure 31 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 73.6 ºC.
Ar2: Primary Snubber = 73.3 ºC.
Ar3: SR FET, Q2 = 62.9 ºC.
Ar4: PCB Under Transformer = 69.0 ºC.
Ambient: = 24.0 ºC.

11.6 ***Output: 15 V / 3 A (265 VAC)***

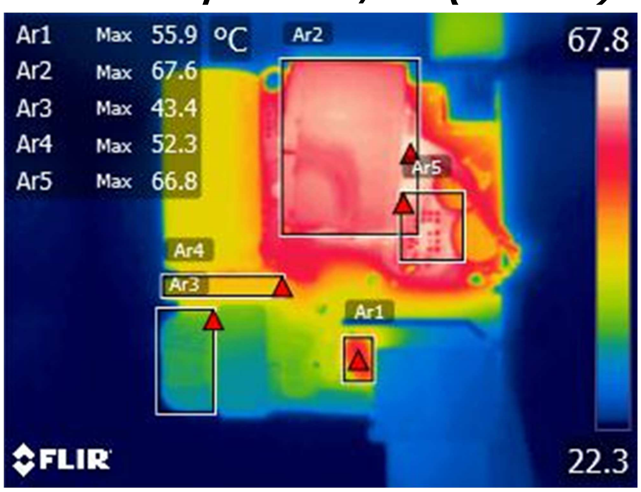


Figure 32 – Top Thermal Image.
Ar1: Thermistor, RT1 = 55.9 ºC.
Ar2: Transformer, T1 = 67.6 ºC.
Ar3: CMC, L2 = 43.4 ºC.
Ar4: Bridge Diode, BR1 = 52.3 ºC.
Ar5: PCB Near Transformer = 66.8 ºC.

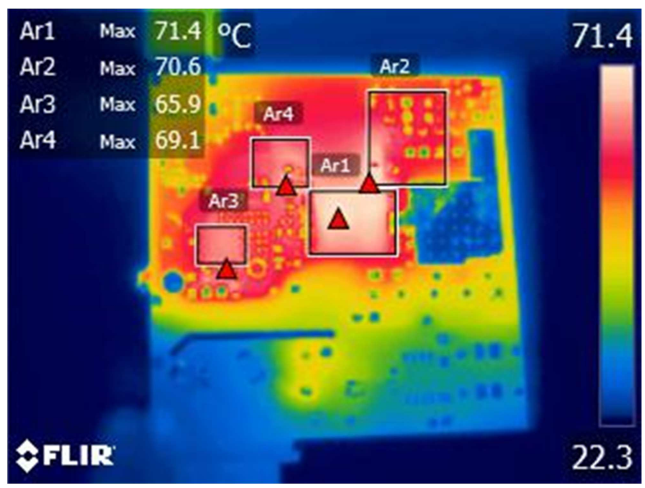


Figure 33 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 71.4 ºC.
Ar2: Primary Snubber = 70.6 ºC.
Ar3: SR FET, Q2 = 65.9 ºC.
Ar4: PCB Under Transformer = 69.1 ºC.
Ambient: = 23.3 ºC.

11.7 *Output: 20 V / 3 A (90 VAC)*

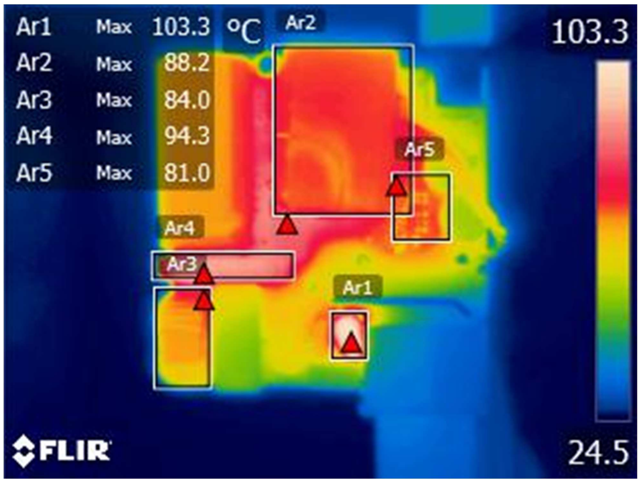


Figure 34 – Top Thermal Image.
Ar1: Thermistor, RT1 = 103.3 ºC.
Ar2: Transformer, T1 = 88.2 ºC.
Ar3: CMC, L2 = 84.0 ºC.
Ar4: Bridge Diode, BR1 = 94.3 ºC.
Ar5: PCB Near Transformer = 81.0 ºC.

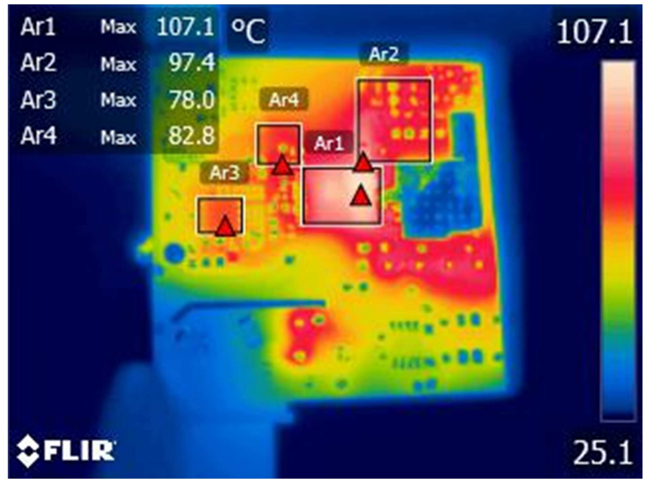


Figure 35 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 107.1 ºC.
Ar2: Primary Snubber = 97.4 ºC.
Ar3: SR FET, Q2 = 78.0 ºC.
Ar4: PCB Under Transformer = 82.8 ºC.
Ambient: = 24.5 ºC.

Note: For adapter design, a thermal insulator pad and a heat spreader are needed. The InnoSwitch3-PD and SR FET ICs could be cooled down below 100 ºC with a heat spreader. Please refer to Chapter 12 of DER-802 report or Chapter 10 of DER-601.

11.8 *Output: 20 V / 3 A (265 VAC)*

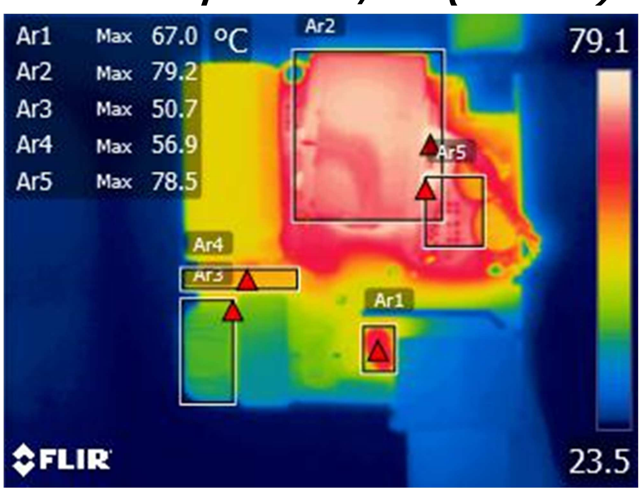


Figure 36 – Top Thermal Image.
Ar1: Thermistor, RT1 = 67.0 ºC.
Ar2: Transformer, T1 = 79.2 ºC.
Ar3: CMC, L2 = 50.7 ºC.
Ar4: Bridge Diode, BR1 = 56.9 ºC.
Ar5: PCB Near Transformer = 78.5 ºC.

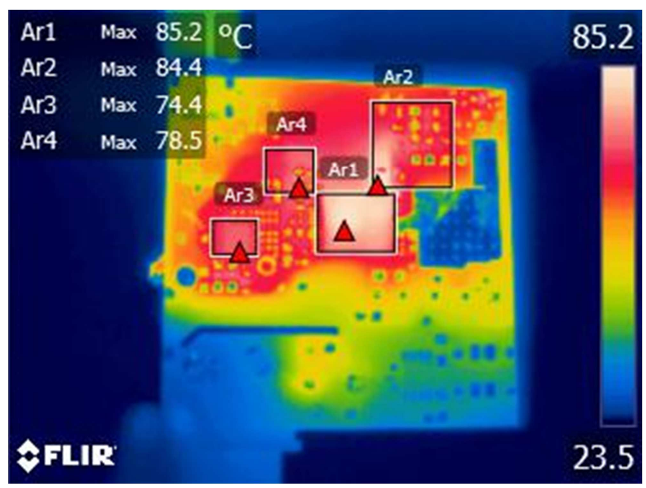


Figure 37 – Bottom Thermal Image.
Ar1: InnoSwitch3-PD, U1 = 85.2 ºC.
Ar2: Primary Snubber = 84.4 ºC.
Ar3: SR FET, Q2 = 74.4 ºC.
Ar4: PCB Under Transformer = 78.5 ºC.
Ambient: = 24.0 ºC.

12 Waveforms

12.1 *Load Transient Response*

Note 1: Output voltages captured at the end of cable
2: Measurements taken at room temperature

12.1.1 Output: 5 V / 3 A

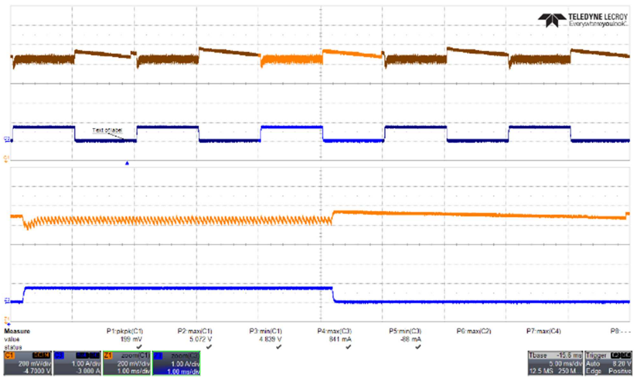


Figure 38 – Transient Response.
90 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 4.839 V, V_{MAX}: 5.072 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

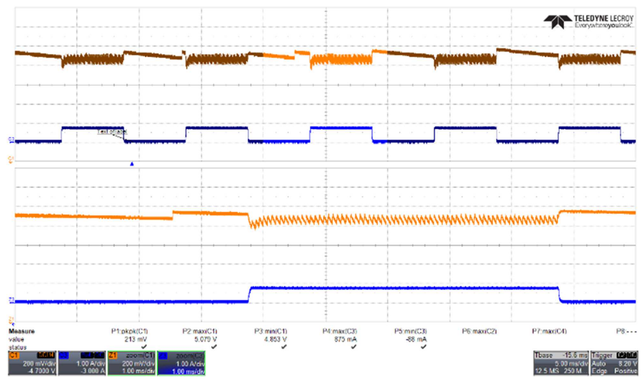


Figure 39 – Transient Response.
265 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN} : 4.853 V, V_{MAX}: 5.079 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

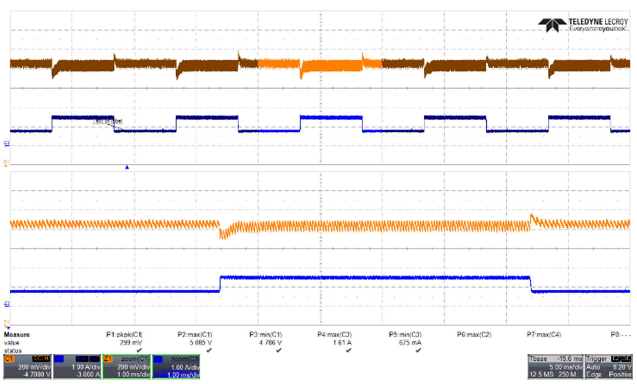


Figure 40 – Transient Response.
90 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.786 V, V_{MAX}: 5.085 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

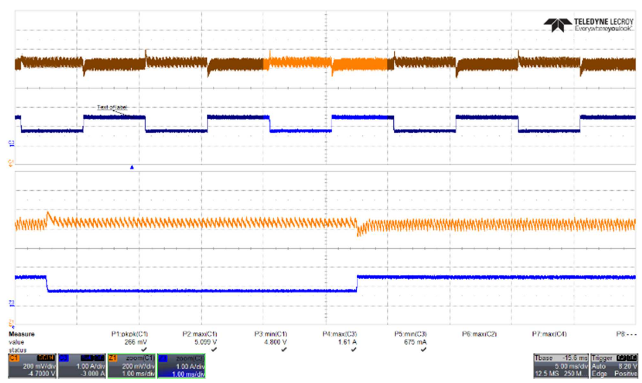


Figure 41 – Transient Response.
265 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.800 V, V_{MAX}: 5.099 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

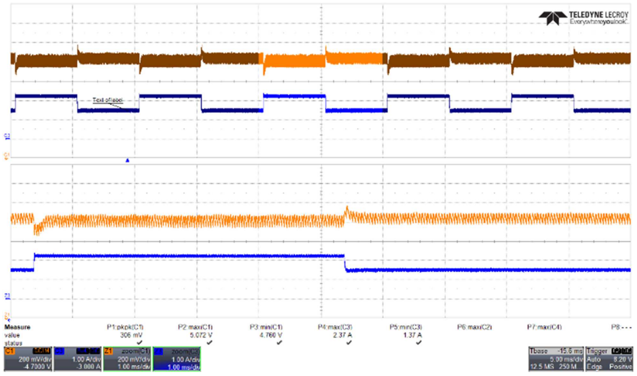


Figure 42 – Transient Response.
90 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.760 V, V_{MAX}: 5.072 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

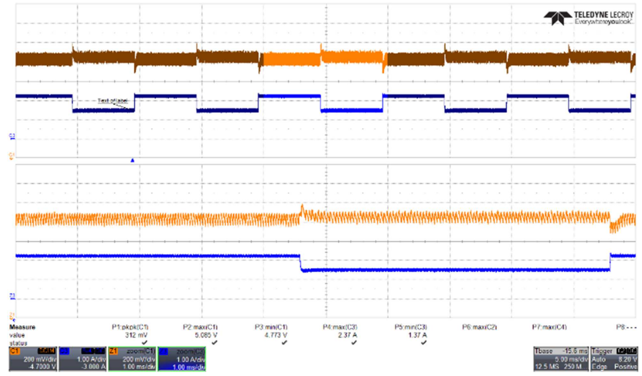


Figure 43 – Transient Response.
265 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.773 V, V_{MAX}: 5.085 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

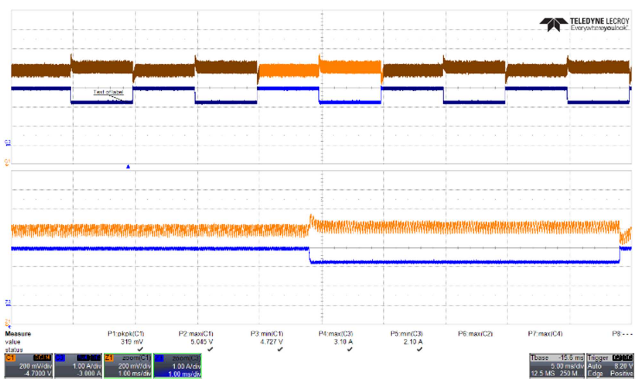


Figure 44 – Transient Response.
90 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 4.727 V, V_{MAX}: 5.045 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

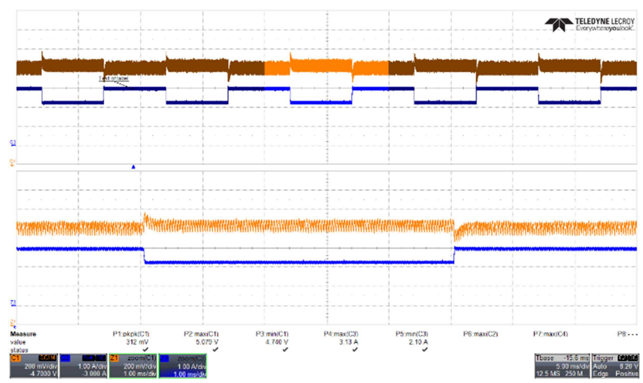


Figure 45 – Transient Response.
265 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 4.740 V, V_{MAX}: 5.079 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

12.1.2 Output: 9 V / 3 A

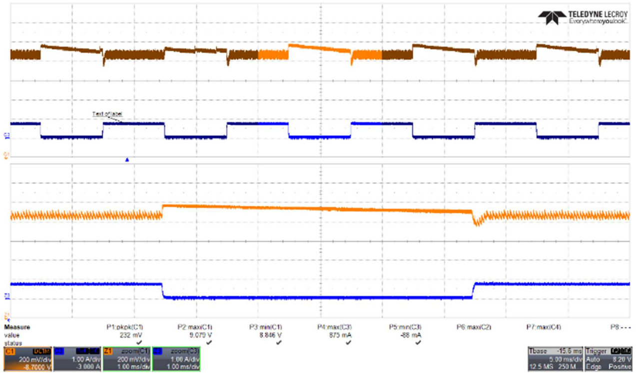


Figure 46 – Transient Response.
90 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.846 V, V_{MAX}: 9.079 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

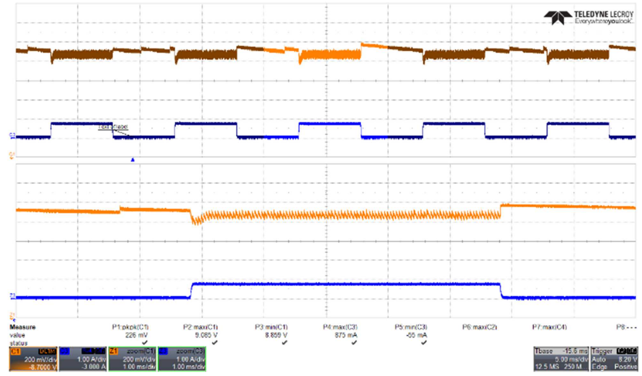


Figure 47 – Transient Response.
265 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN} 8.859 V, V_{MAX}: 9.085 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

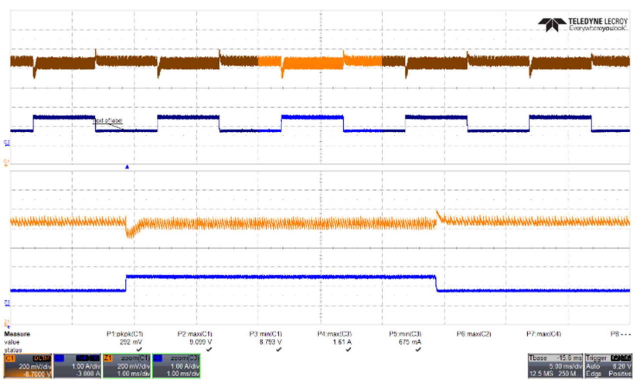


Figure 48 – Transient Response.
90 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.793 V, V_{MAX}: 9.099 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

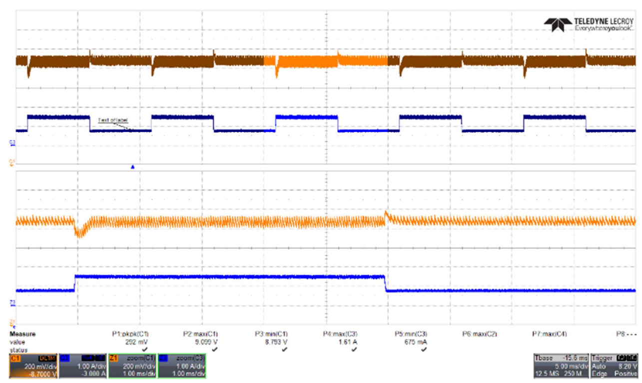


Figure 49 – Transient Response.
265 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.793 V, V_{MAX}: 9.099 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

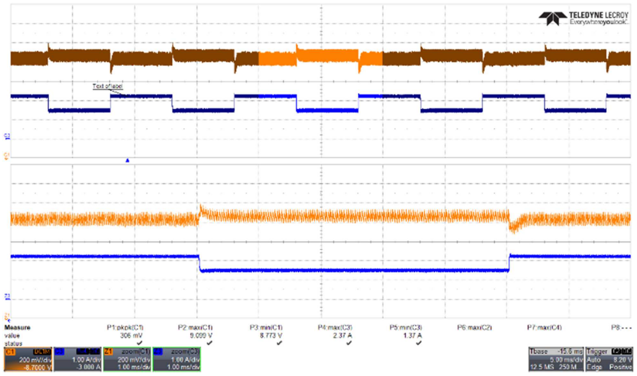


Figure 50 – Transient Response.
90 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.773 V, V_{MAX}: 9.099V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

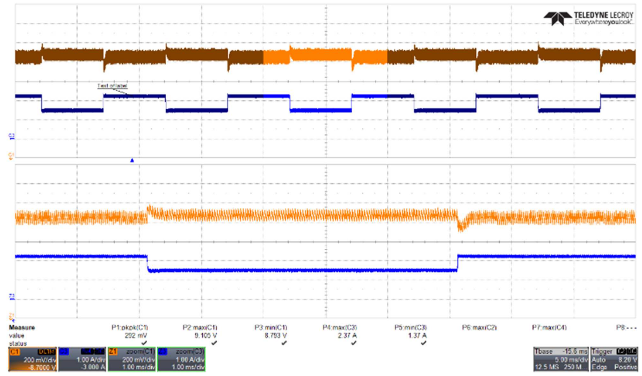


Figure 51 – Transient Response.
265 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.793 V, V_{MAX}: 9.105 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

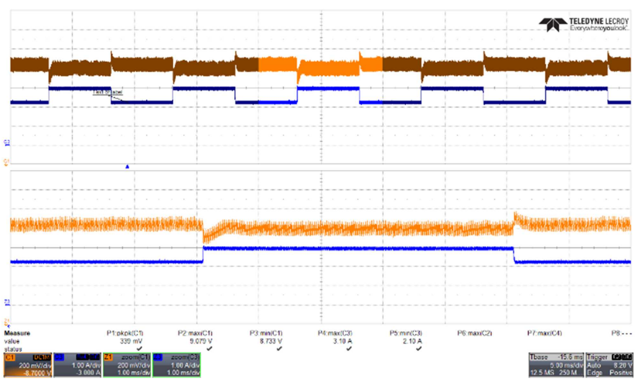


Figure 52 – Transient Response.
90 VAC, 9.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 8.733 V, V_{MAX}: 9.079 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

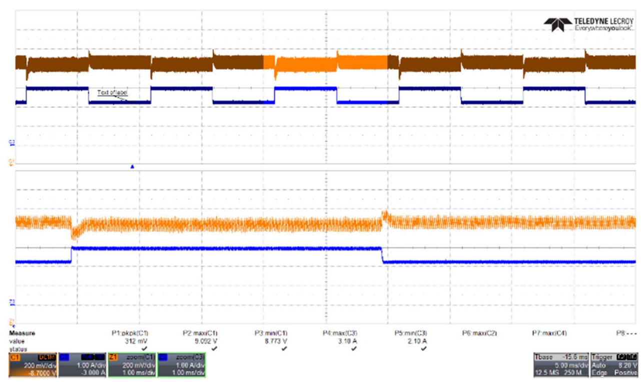


Figure 53 – Transient Response.
265 VAC, 9.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 8.773 V, V_{MAX}: 9.092 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

12.1.3 Output: 15 V / 3 A

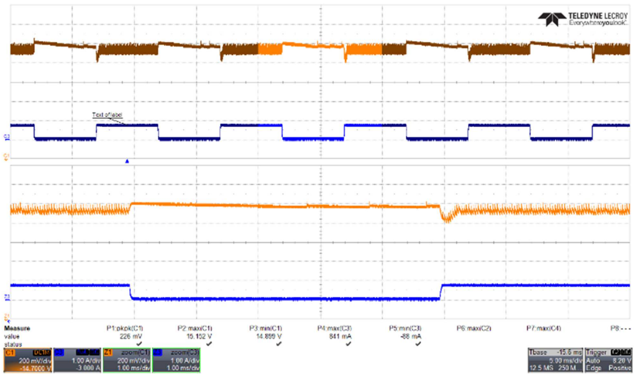


Figure 54 – Transient Response.
90 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.899 V, V_{MAX}: 15.152 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

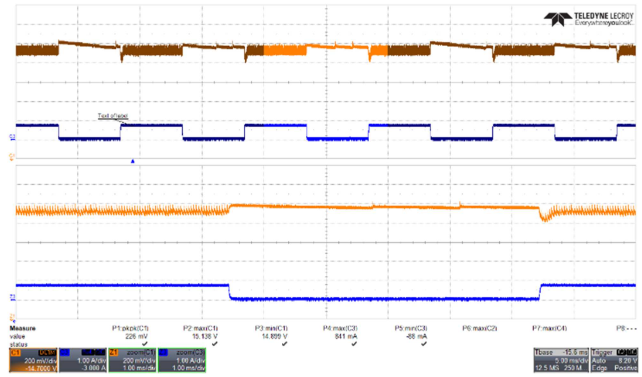


Figure 55 – Transient Response.
265 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.899 V, V_{MAX}: 15.138 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

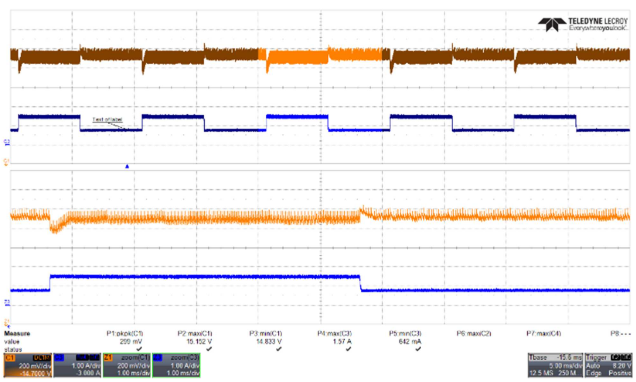


Figure 56 – Transient Response.
90 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.833 V, V_{MAX}: 15.152 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

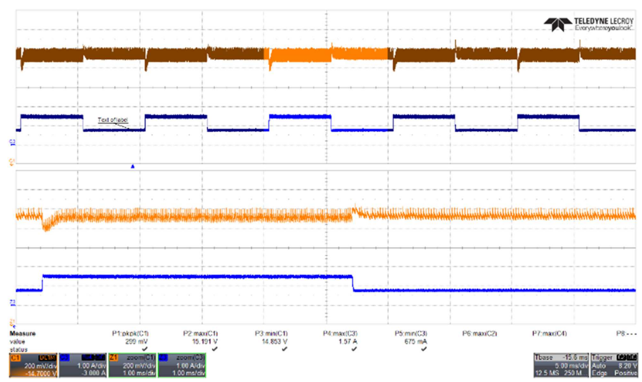


Figure 57 – Transient Response.
265 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.853V, V_{MAX}: 15.191 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

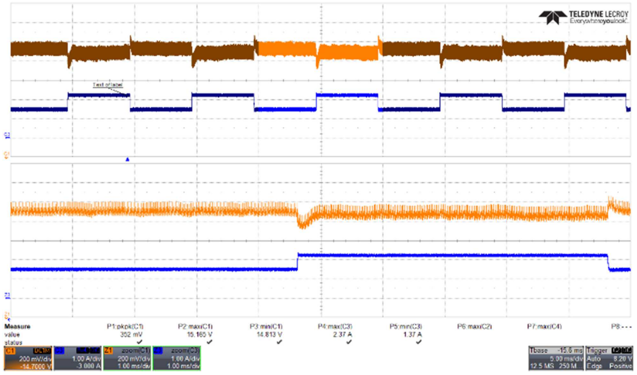


Figure 58 – Transient Response.
90 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.813 V, V_{MAX}: 15.165 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

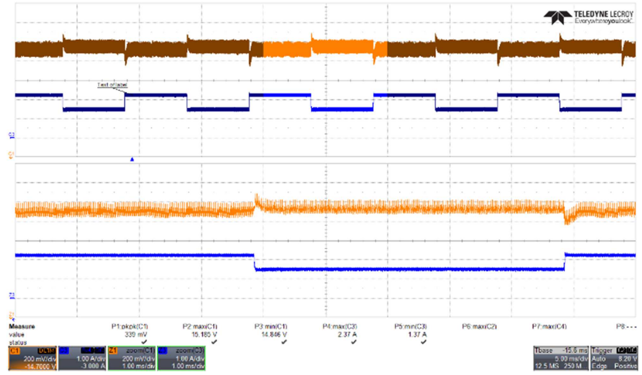


Figure 59 – Transient Response.
265 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.846 V, V_{MAX}: 15.185 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

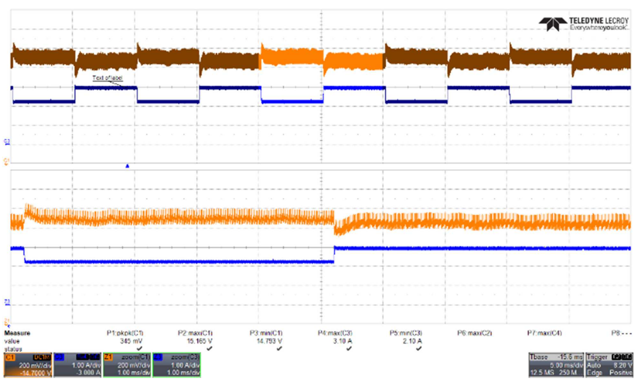


Figure 60 – Transient Response.
90 VAC, 15 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 14.793 V, V_{MAX}: 15.165 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

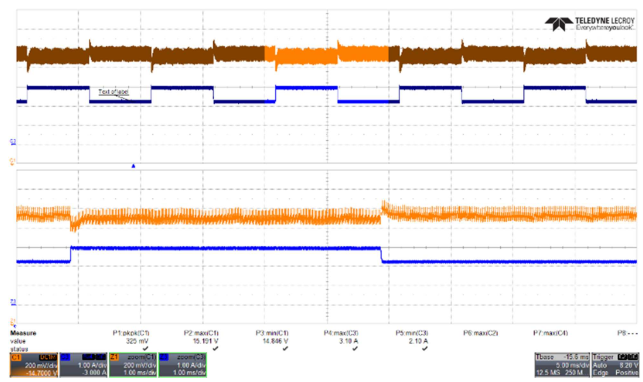


Figure 61 – Transient Response.
265 VAC, 15 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 14.846 V, V_{MAX}: 15.191 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

12.1.4 Output: 20 V / 3 A

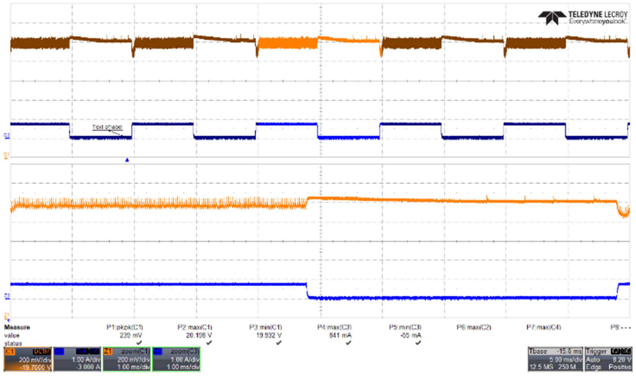


Figure 62 – Transient Response.
90 VAC, 20 V, 0 – 0.75 A Load Step.
V_{MIN}: 19.932 V, V_{MAX}: 20.198 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

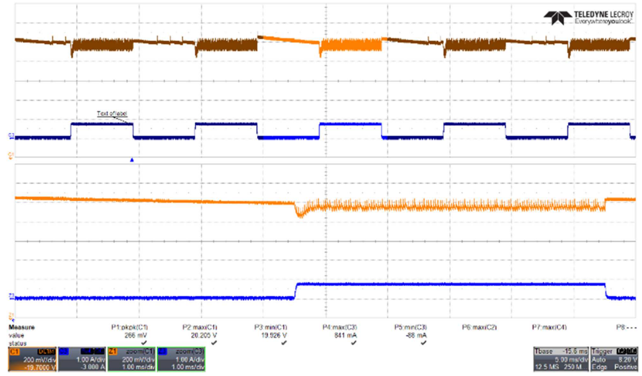


Figure 63 – Transient Response.
265 VAC, 20 V, 0 – 0.75A Load Step.
V_{MIN}: 19.926 V, V_{MAX}: 20.205 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

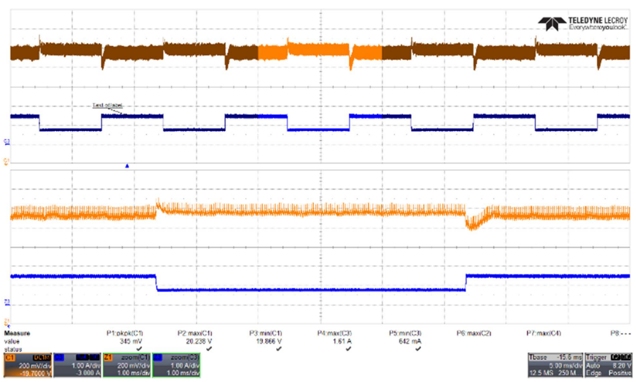


Figure 64 – Transient Response.
90 VAC, 20 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 19.866 V, V_{MAX}: 20.238 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

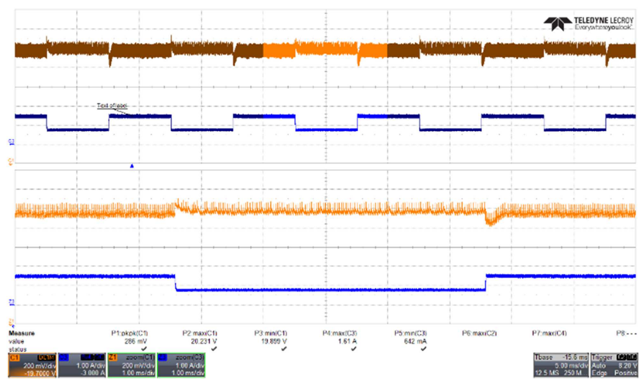


Figure 65 – Transient Response.
265 VAC, 20 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 19.899 V, V_{MAX}: 20.231 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

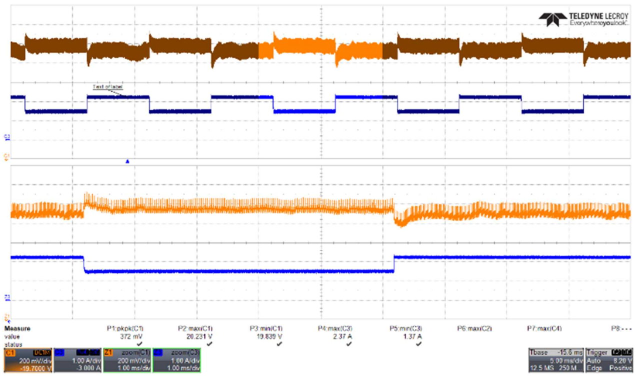


Figure 66 – Transient Response.
90 VAC, 20 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 19.839 V, V_{MAX}: 20.231 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

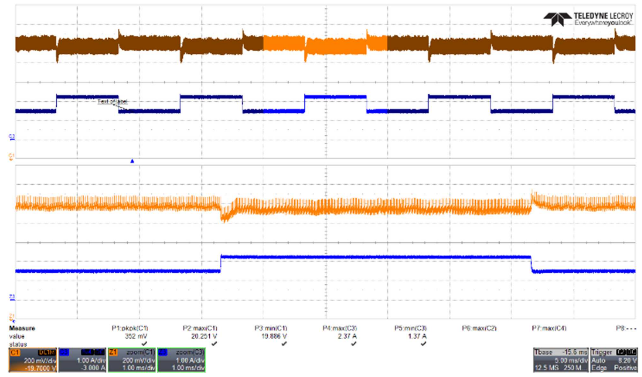


Figure 67 – Transient Response.
265 VAC, 20 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 19.886 V, V_{MAX}: 20.251 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

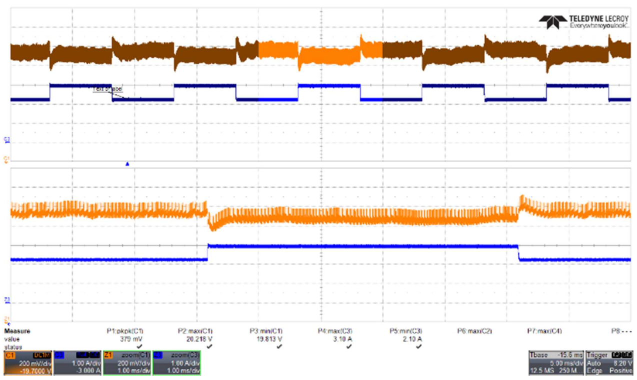


Figure 68 – Transient Response.
90 VAC, 20 V, 2.25 – 3 A Load Step.
V_{MIN}: 19.813 V, V_{MAX}: 20.218 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

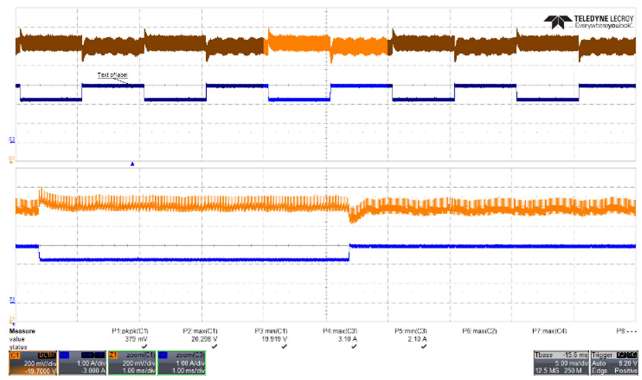


Figure 69 – Transient Response.
265 VAC, 20 V, 2.25 – 3 A Load Step.
V_{MIN}: 19.919 V, V_{MAX}: 20.298 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.
Zoom: 1 ms / div.

12.2 ***Switching Waveforms***

Note: Measurements taken at room temperature

12.2.1 Primary Drain Voltage

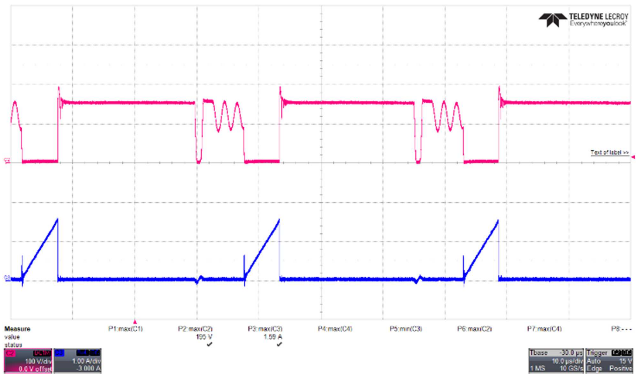


Figure 70 – Drain Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (195 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

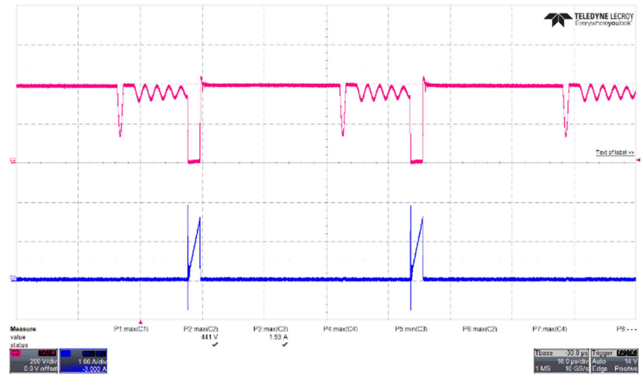


Figure 71 – Drain Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (441 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

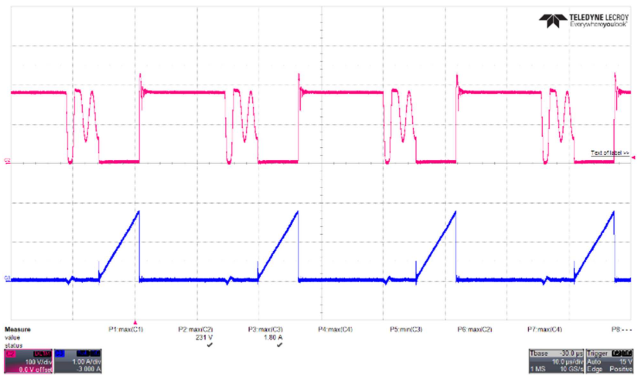


Figure 72 – Drain Voltage Waveforms.
90 VAC, 9.0 V, 3 A Load (231 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

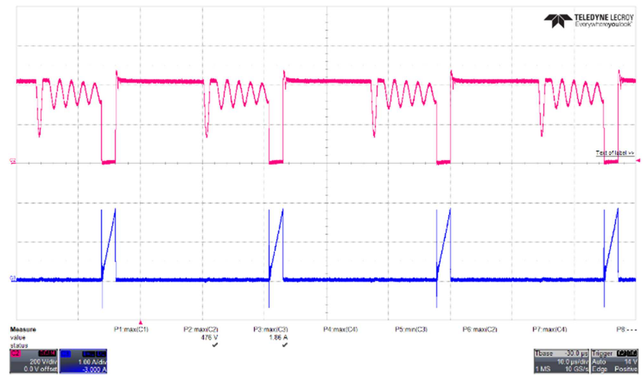


Figure 73 – Drain Voltage Waveforms.
265 VAC, 9 V, 3 A Load (476 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

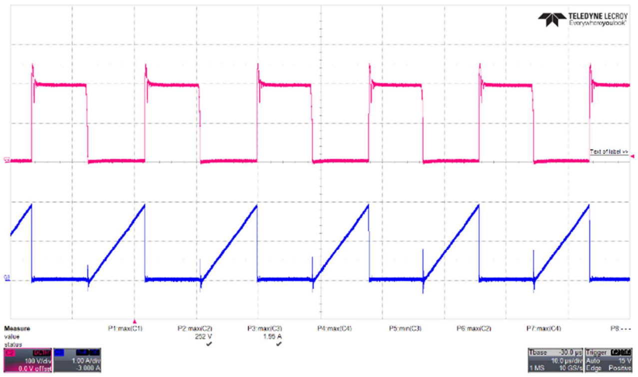


Figure 74 – Drain Voltage Waveforms.
90 VAC, 15.0 V, 3 A Load (252 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

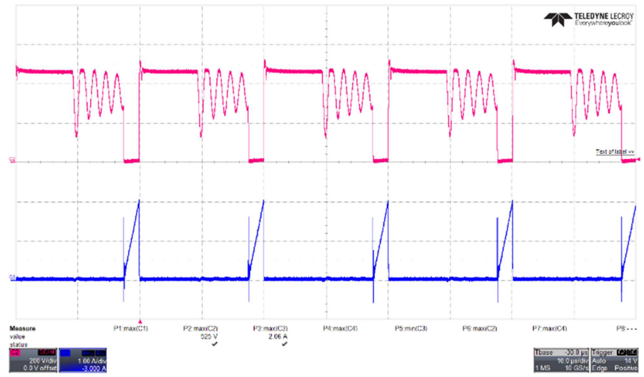


Figure 75 – Drain Voltage Waveforms.
265 VAC, 15.0 V, 3 A Load (525 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

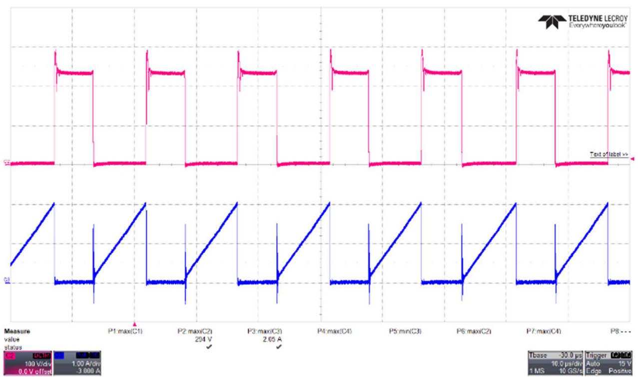


Figure 76 – Drain Voltage Waveforms.
90 VAC, 20 V, 3 A Load (294 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

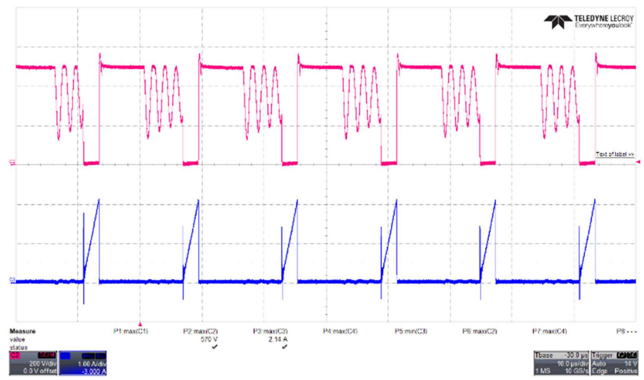


Figure 77 – Drain Voltage Waveforms.
265 VAC, 20 V, 3 A Load (570 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

12.2.2 SR FET Voltage

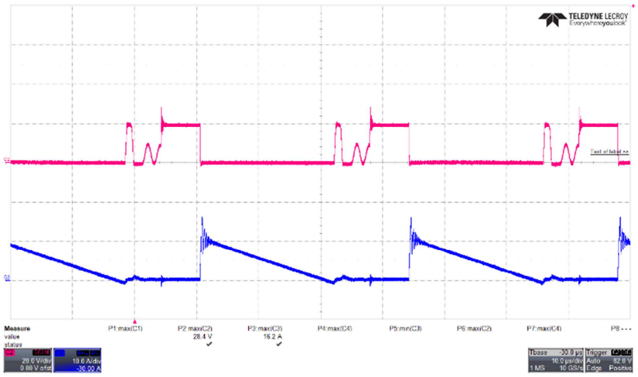


Figure 78 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (28.4 V_{MAX}).
Upper: V_{DRAIN}, 20 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 µs / div.

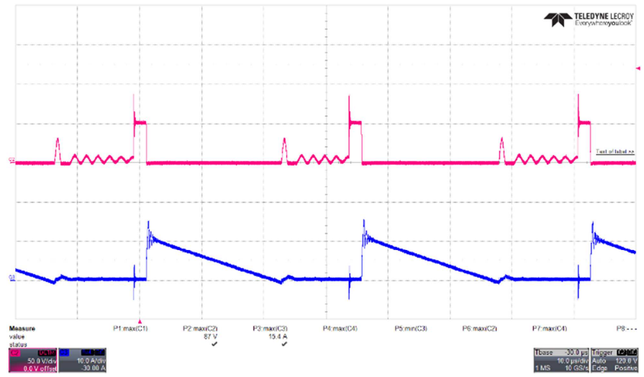


Figure 79 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (87 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 µs / div.

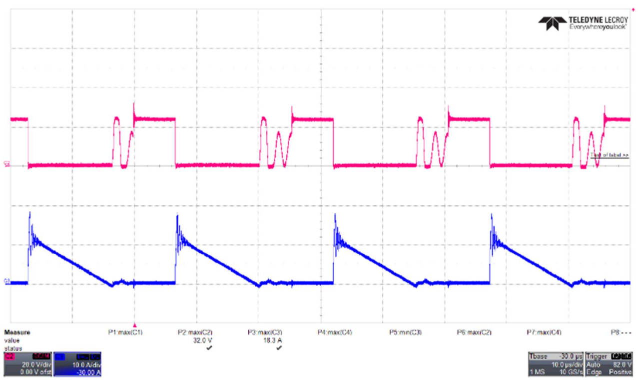


Figure 80 – SR FET Voltage Waveforms.
90 VAC, 9.0 V, 3 A Load (32.0 V_{MAX}).
Upper: V_{DRAIN}, 20 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 µs / div.

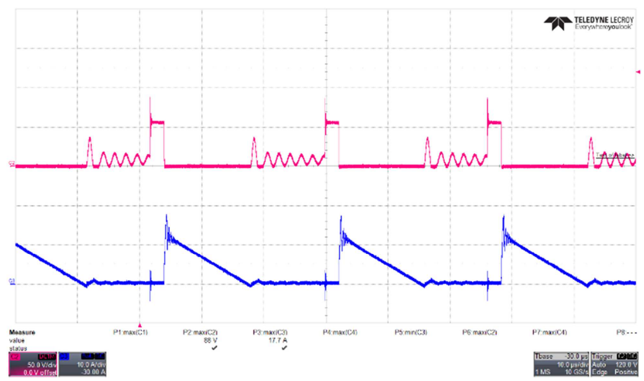


Figure 81 – SR FET Voltage Waveforms.
265 VAC, 9.0 V, 3 A Load (88 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 µs / div.

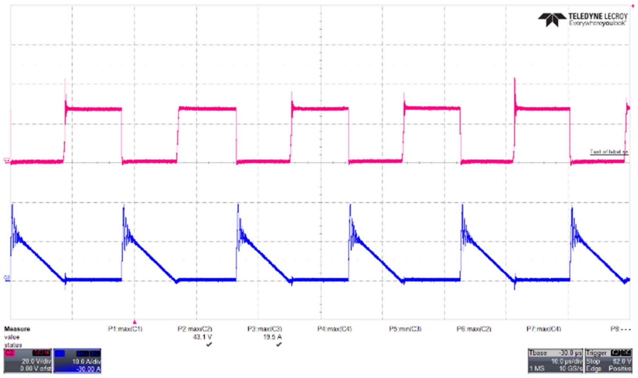


Figure 82 – SR FET Voltage Waveforms.
90 VAC, 15.0 V, 3 A Load(43.1 V_{MAX}).
Upper: V_{DRAIN}, 20 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 μs / div.

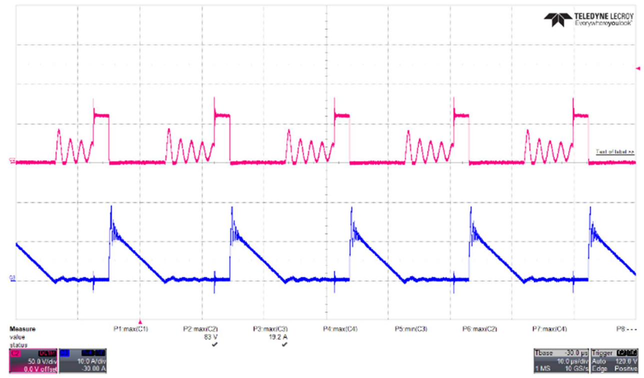


Figure 83 – SR FET Voltage Waveforms.
265 VAC, 15.0 V,3 A Load (83 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 μs / div.

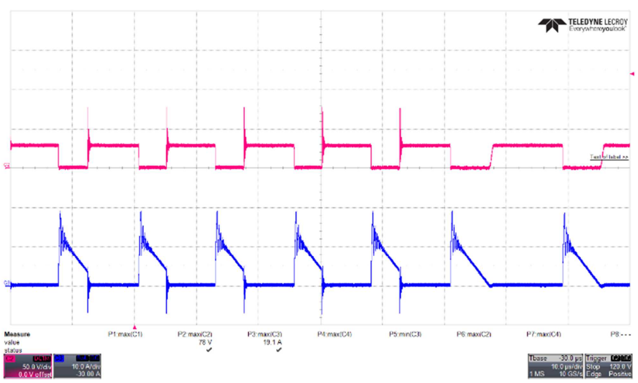


Figure 84 – SR FET Voltage Waveforms.
90 VAC, 20 V, 3 A Load (78 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 μs / div.

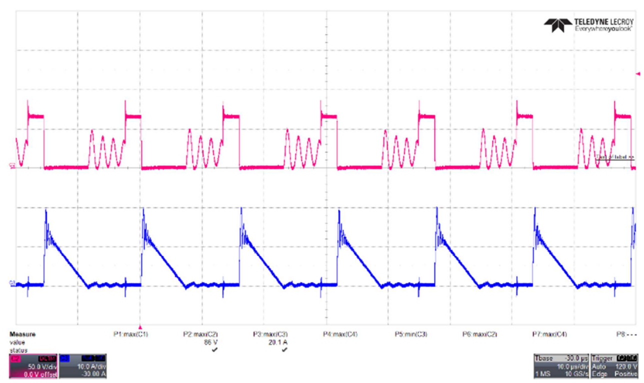


Figure 85 – SR FET Voltage Waveforms.
265 VAC, 20 V, 3 A Load (86 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 10 μs / div.

12.3 *Start-up*

Note: Measurements taken at room temperature

12.3.1 Primary FET

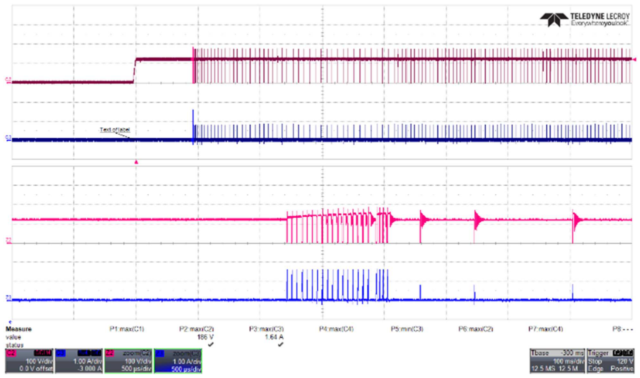


Figure 86 – Drain Voltage Waveforms.
90 VAC, 5.0 V, 0 A Load (186 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 100 ms / div. (Zoom: 500 µs / div.)

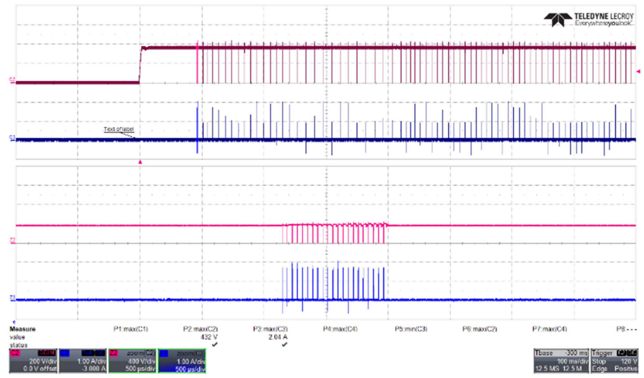


Figure 87 – Drain Voltage Waveforms.
265 VAC, 5.0 V, 0 A Load (432 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 100 ms / div. (Zoom: 500 µs / div.)

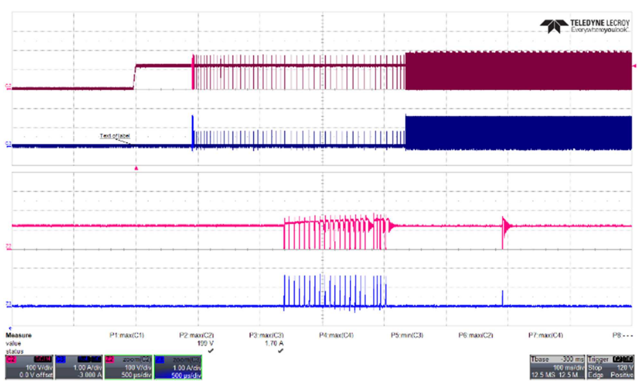


Figure 88 – Drain Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (199 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 100 ms / div. (Zoom: 500 µs / div.)

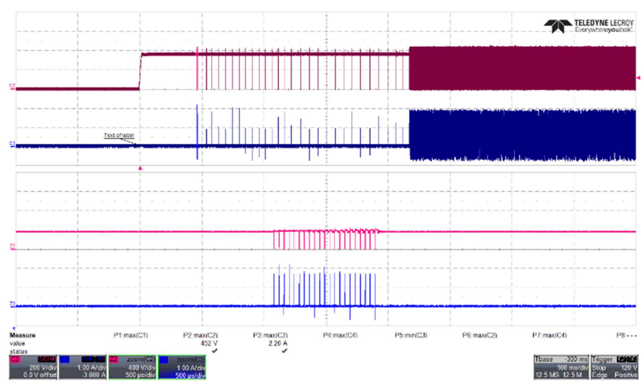


Figure 89 – Drain Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (452 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div.
Time: 100 ms / div. (Zoom: 500 µs / div.)

12.3.2 SR FET

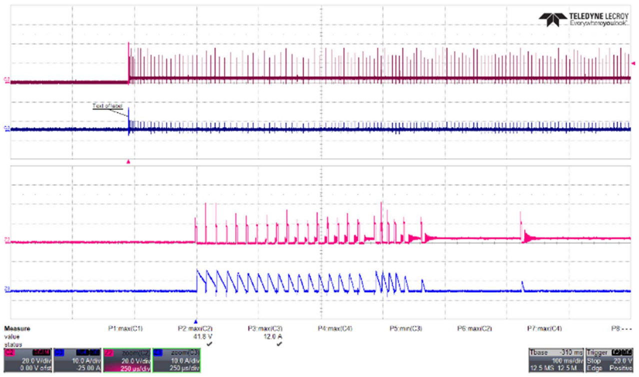


Figure 90 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 0 A Load (41.8 V_{MAX}).
Upper: V_{DRAIN}, 20 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 100 ms / div. (Zoom: 250 µs / div.)

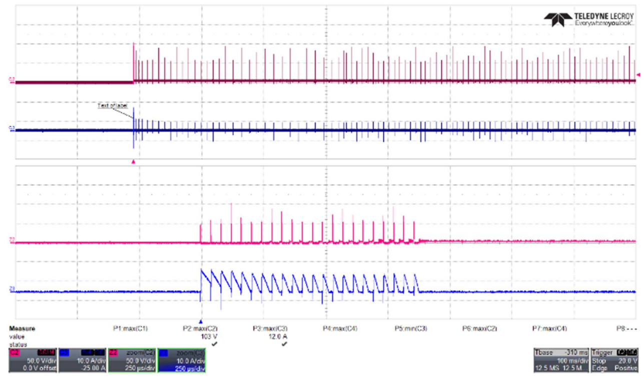


Figure 91 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 0 A Load (103 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 100 ms / div. (Zoom: 250 µs / div.)

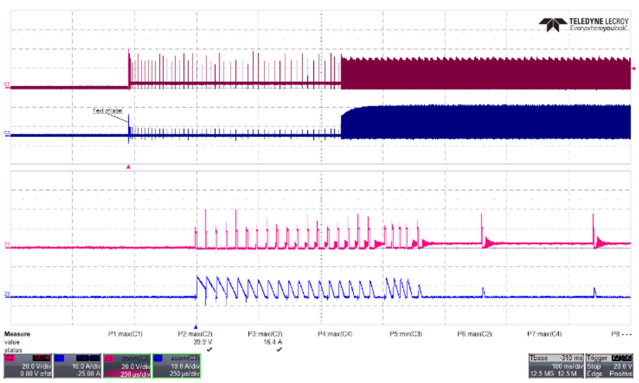


Figure 92 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 3 A Load (39.9 V_{MAX}).
Upper: V_{DRAIN}, 20 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 100 ms / div. (Zoom: 250 µs / div.)

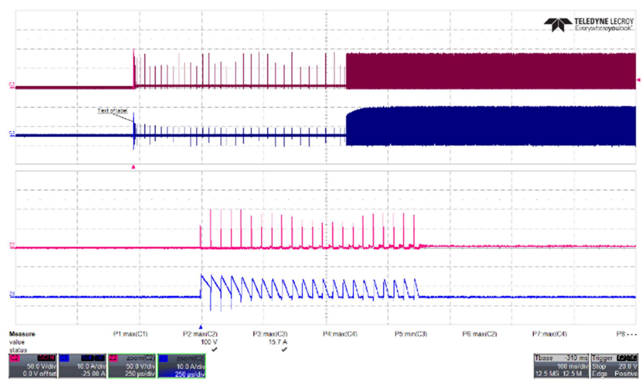


Figure 93 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 3 A Load (100 V_{MAX}).
Upper: V_{DRAIN}, 50 V / div.
Lower: I_{DRAIN}, 10 A / div.
Time: 100 ms / div. (Zoom: 250 µs / div.)

13 Output Ripple Measurements

13.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

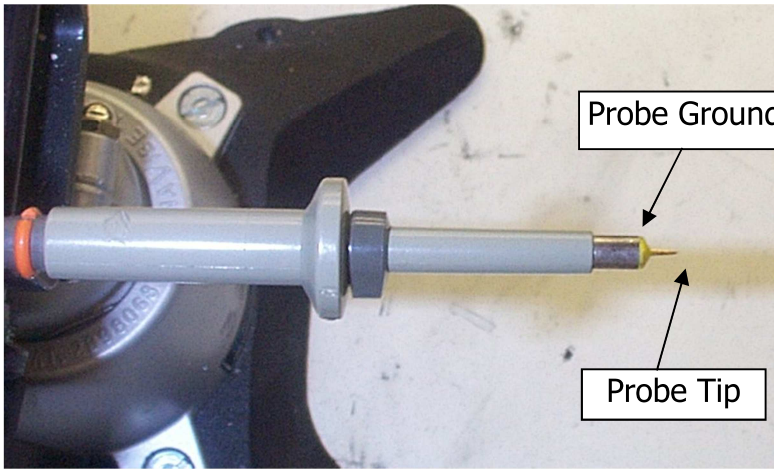


Figure 94 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

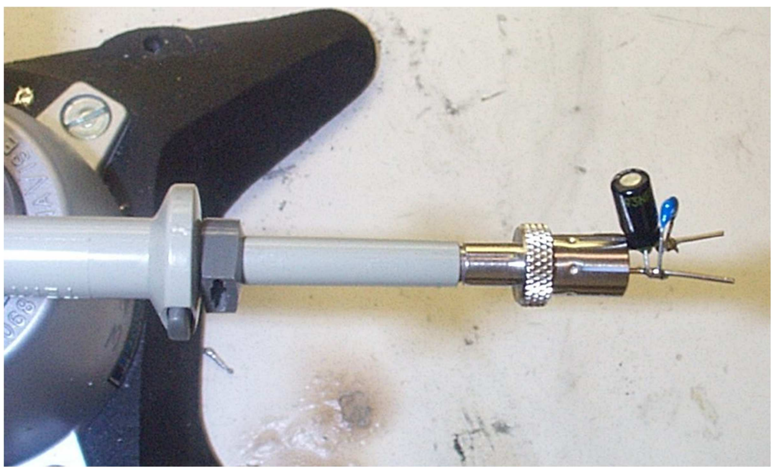


Figure 95 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.2 ***Output Voltage Ripple Waveforms***

Note 1: Output voltages captured at the end of cable
2: Measurements taken at room temperature

13.2.1 Output: 5 V / 3 A

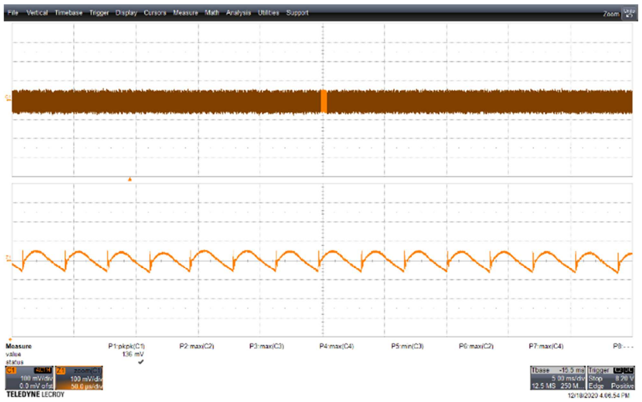


Figure 96 – Output Ripple. PK-PK = 136 mV.
90 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

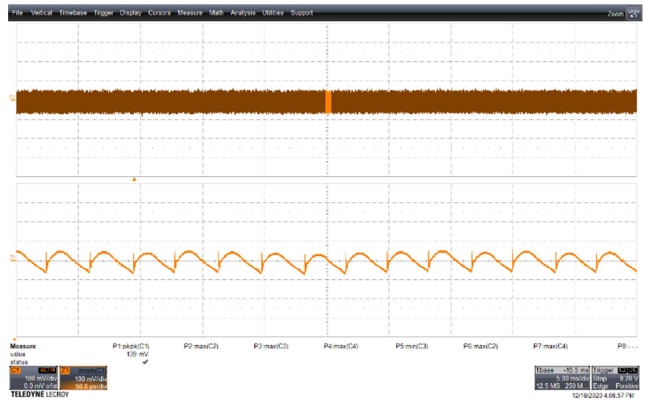


Figure 97 – Output Ripple. PK-PK = 139 mV.
115 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

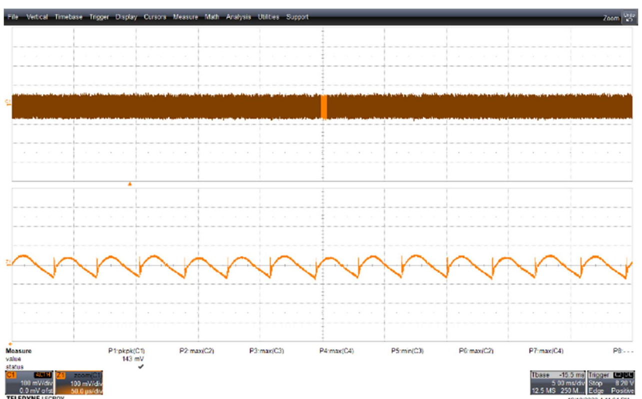


Figure 98 – Output Ripple. PK-PK = 143 mV.
230 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

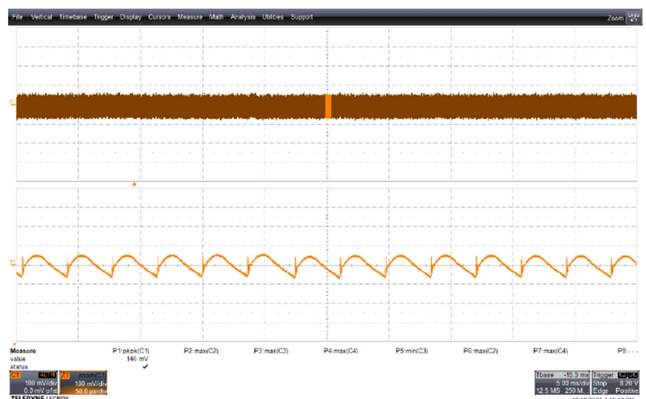


Figure 99 – Output Ripple. PK-PK = 146 mV.
265 VAC_{IN} 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

13.2.2 Output: 9 V / 3 A

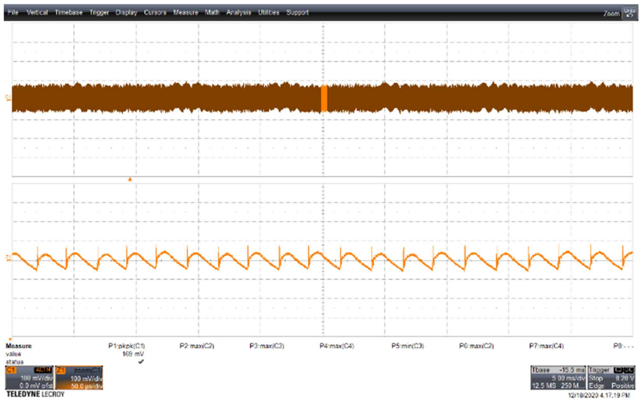


Figure 100 – Output Ripple. PK-PK = 169 mV
90 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

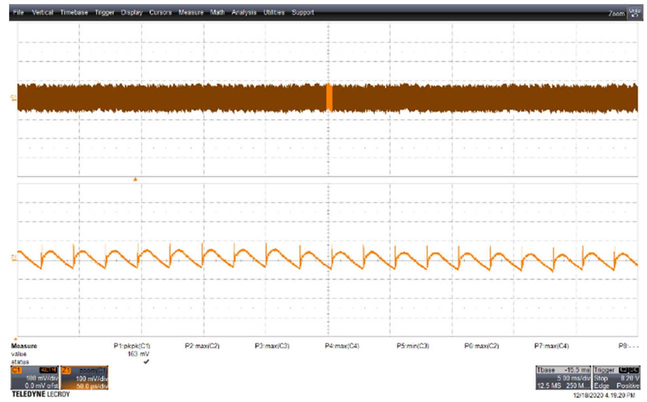


Figure 101 – Output Ripple. PK-PK = 163 mV
115 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

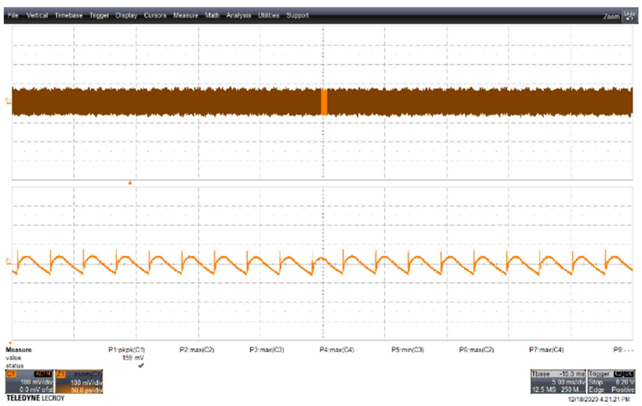


Figure 102 – Output Ripple. PK-PK = 159 mV
230 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

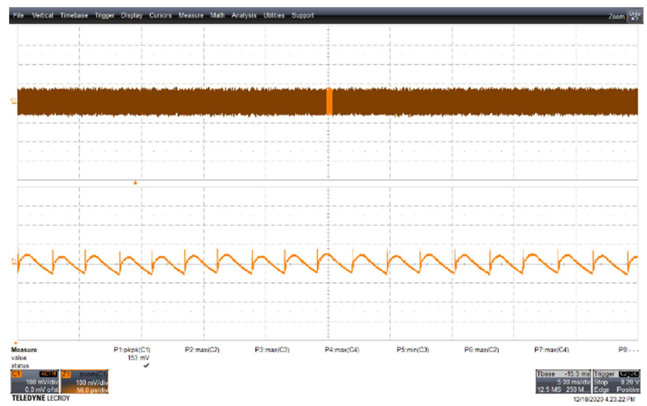


Figure 103 – Output Ripple. PK-PK = 153 mV
265 VAC_{IN} 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

13.2.3 Output: 15 V / 3 A

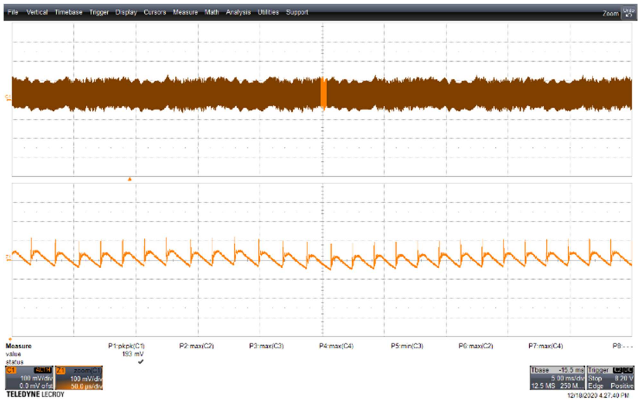


Figure 104 – Output Ripple. PK-PK = 193 mV.
90 VAC_{IN}, 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

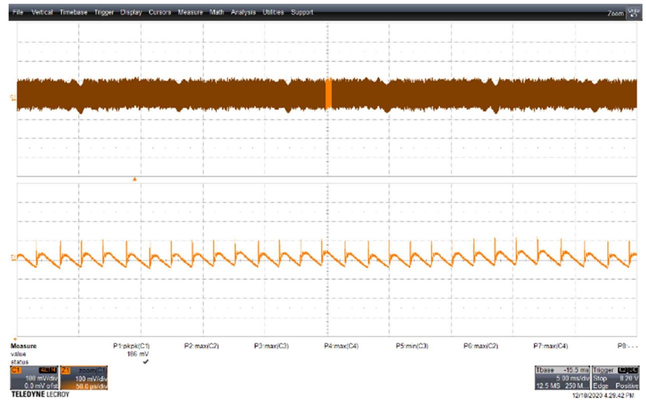


Figure 105 – Output Ripple. PK-PK = 186 mV.
115 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

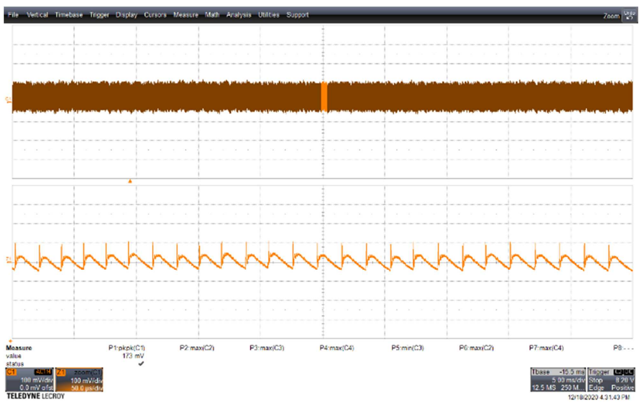


Figure 106 – Output Ripple. PK-PK = 173 mV.
230 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

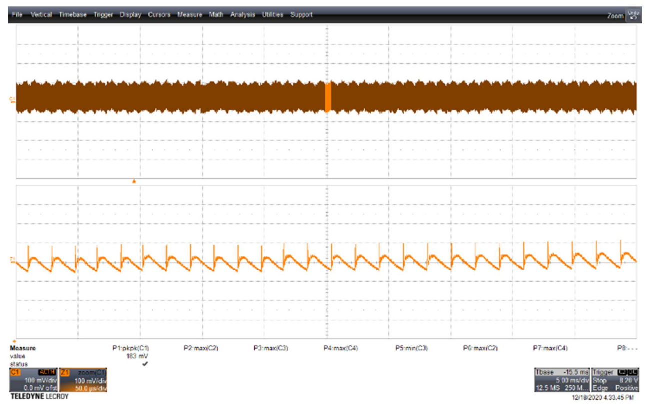


Figure 107 – Output Ripple. PK-PK = 183 mV.
265 VAC_{IN} 15.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

13.2.4 Output: 20 V / 3 A

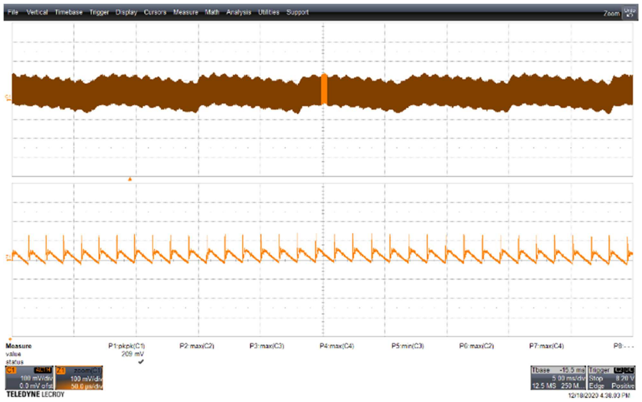


Figure 108 – Output Ripple. PK-PK = 209 mV.
90 VAC_{IN}, 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

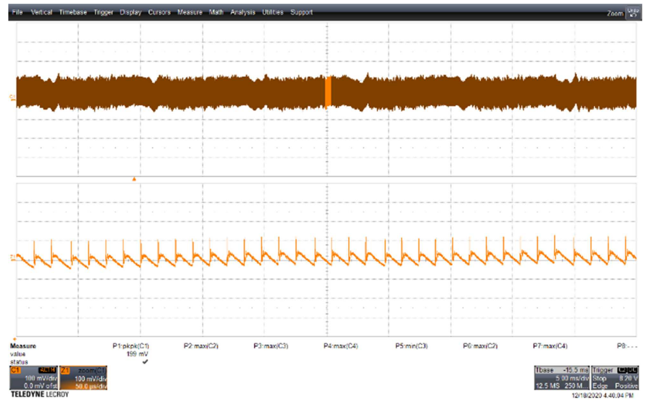


Figure 109 – Output Ripple. PK-PK = 199 mV.
115 VAC_{IN}, 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

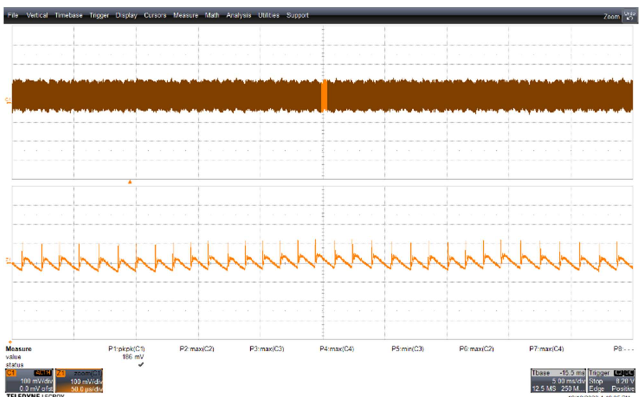


Figure 110 – Output Ripple. PK-PK = 186 mV.
230 VAC_{IN} 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

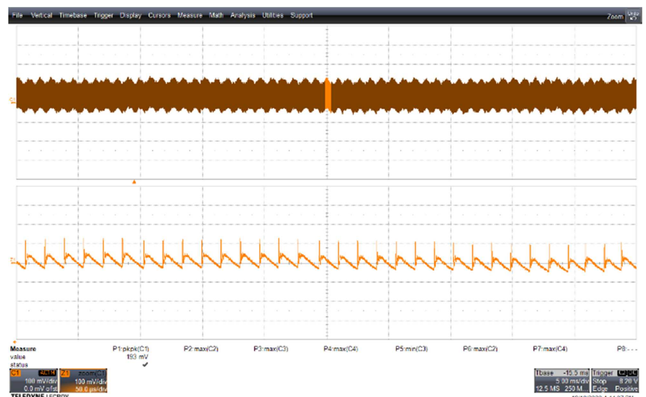


Figure 111 – Output Ripple. PK-PK = 193 mV.
265 VAC_{IN} 20 V, 3 A Load.
V_{OUT}, 100 mV / div., 5 ms / div.
Zoom: 50 µs / div.

13.3 *Output Voltage Ripple Amplitude*

Note 1: Output voltages captured at the end of cable
2: Measurements taken at room temperature

13.3.1 Output: 5 V / 3 A

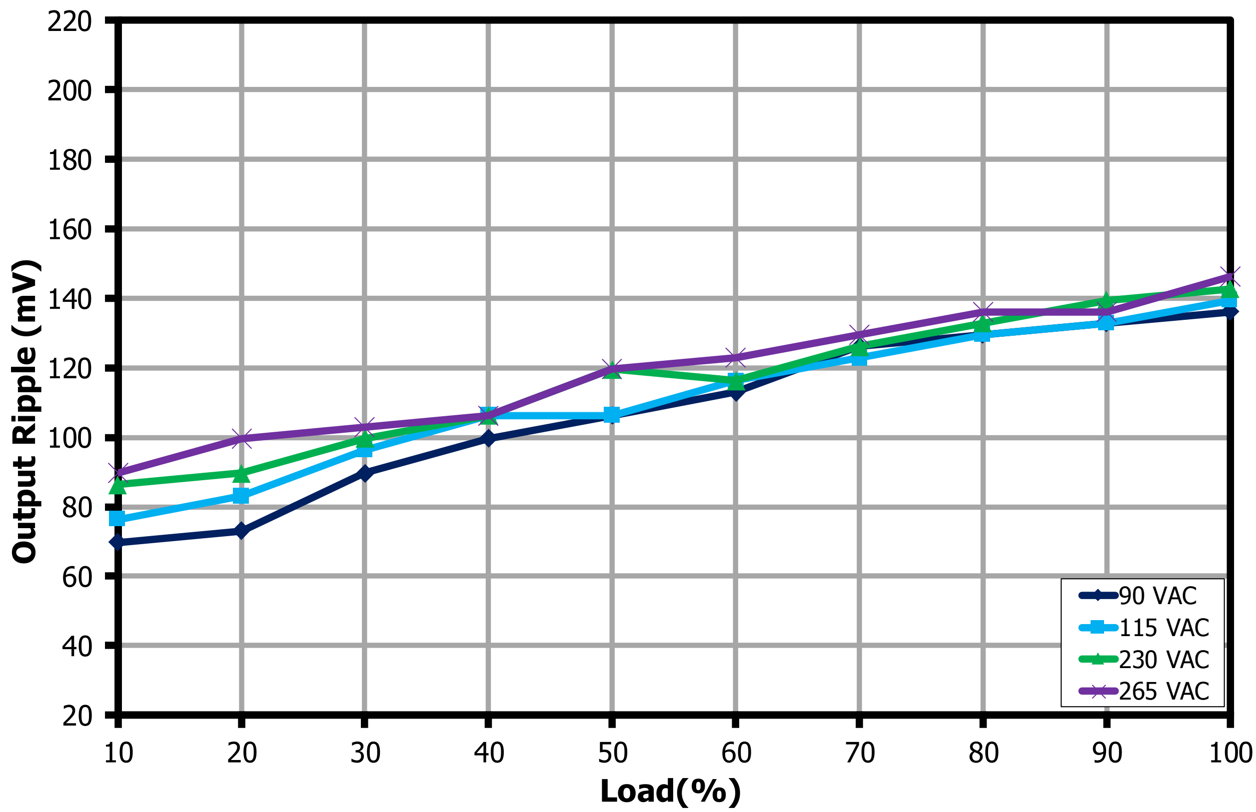


Figure 112 – 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.2 Output: 9 V / 3 A

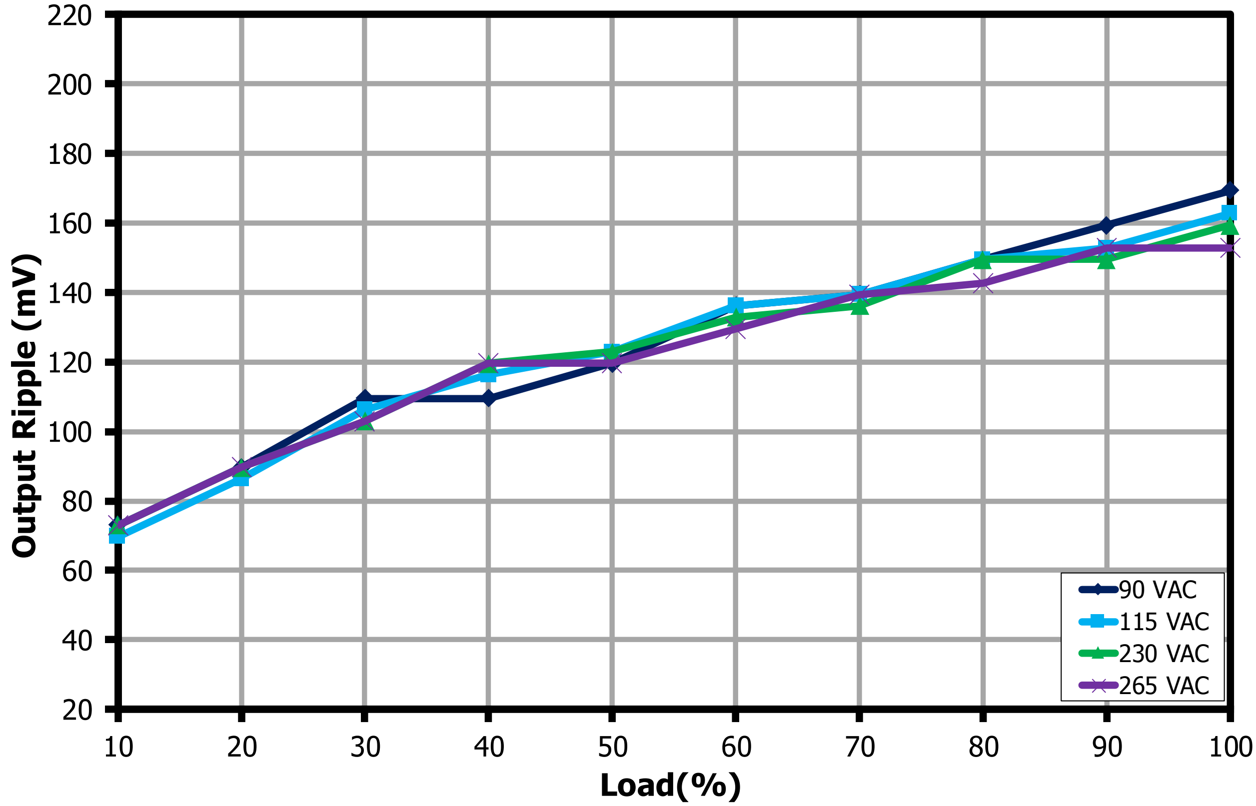


Figure 113 – 9 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.3 Output: 15 V / 3 A

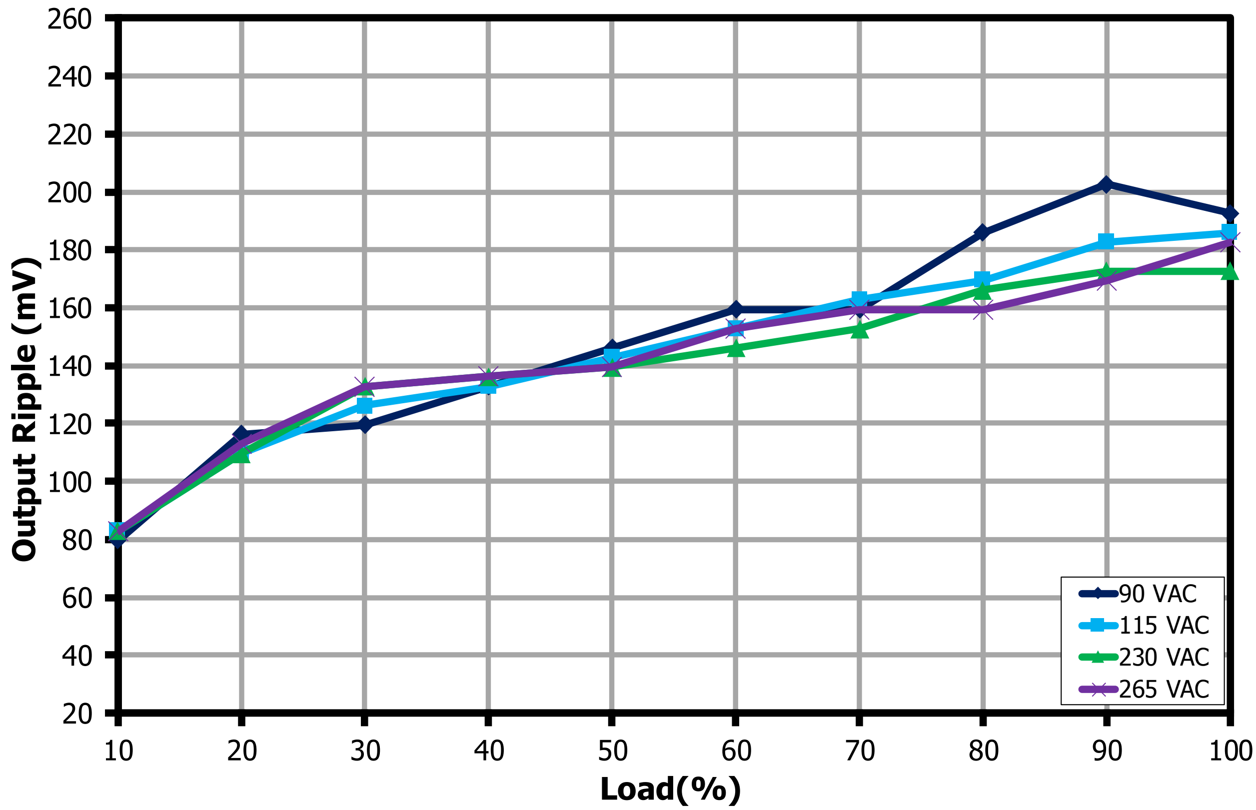


Figure 114 – 15 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.4 Output: 20 V / 3 A

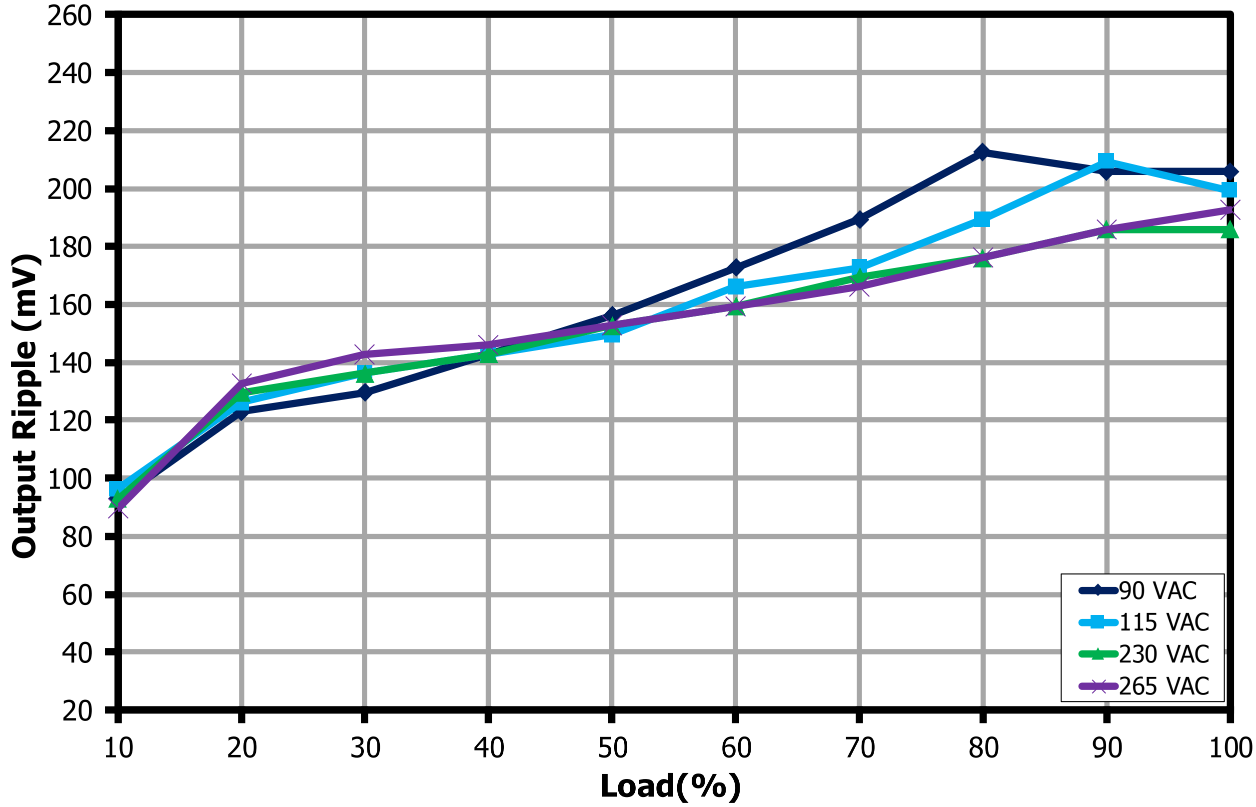


Figure 115 – 20 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

14 CV/CC Profile

One Programmable Power Supply (PPS) Augmented Power Data Objects (APDO) is supported in this design:

- PDO5: 3.3 V – 21 V / 3 A PPS

CVCC profiles were taken with the output voltage measured on the board at room temperature.

14.1 *Output: 20 V / 3 A PPS Request, PDO5*

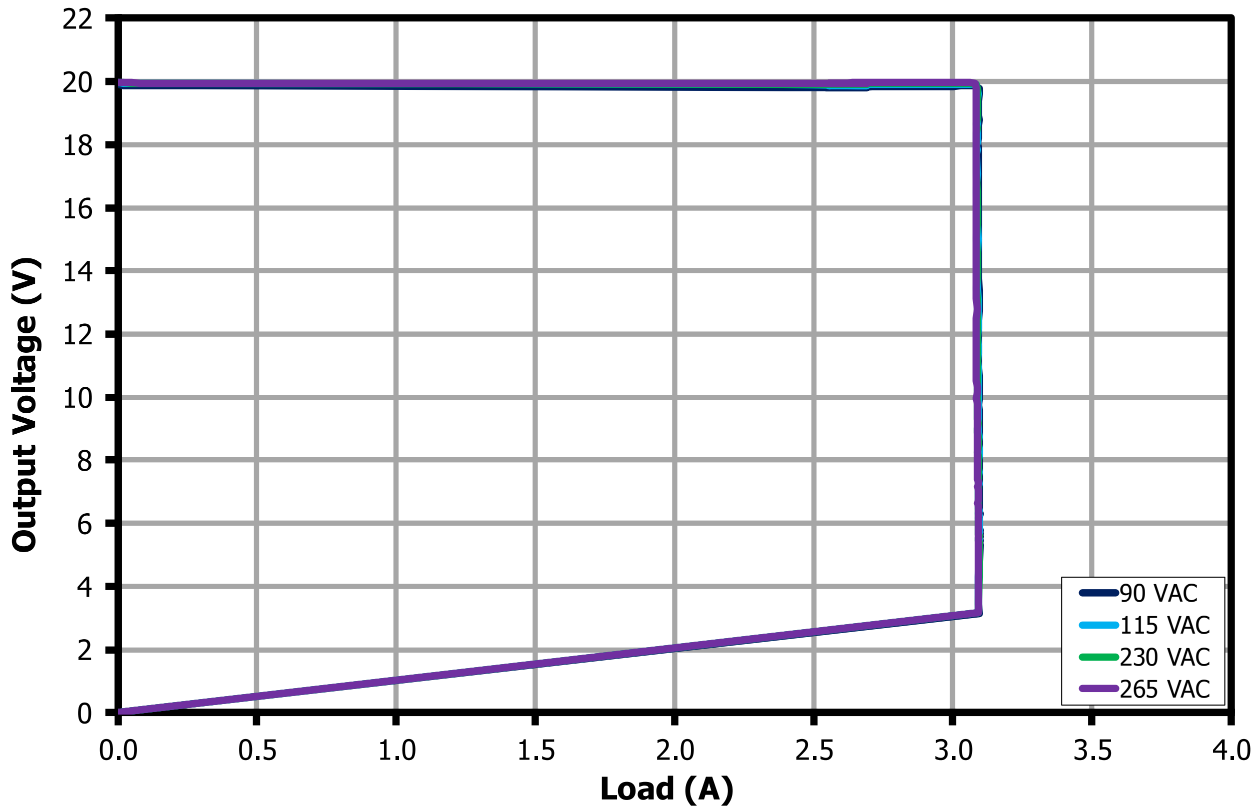


Figure 116 – CV/CC Profile with Output 20 V, 3 A.

14.2 *Output: 15 V / 3 A PPS Request, PDO5*

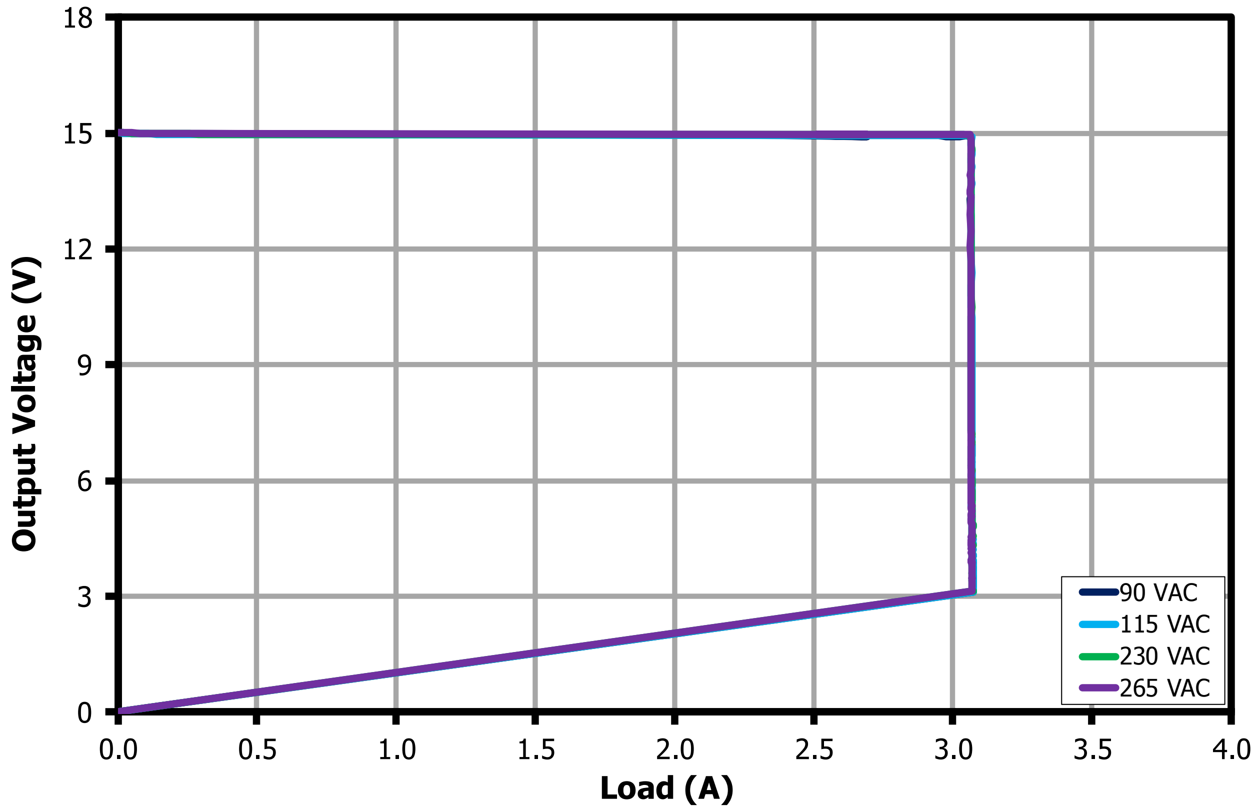


Figure 117 – CV/CC Profile with Output 15 V, 3 A.

14.3 *Output: 9 V / 3 A PPS Request, PDO5*

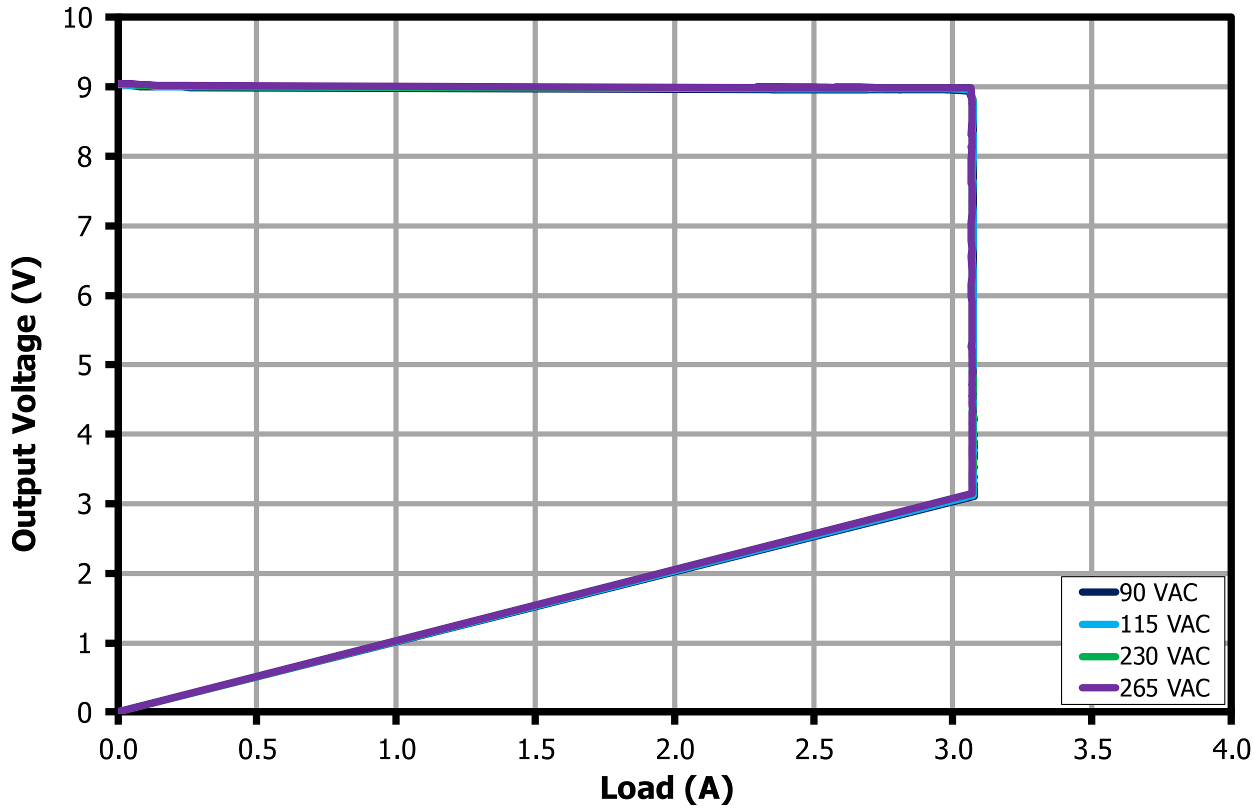


Figure 118 – CV/CC Profile with Output 9 V, 3 A.

14.4 *Output: 5 V / 3 A PPS Request, PDO5*

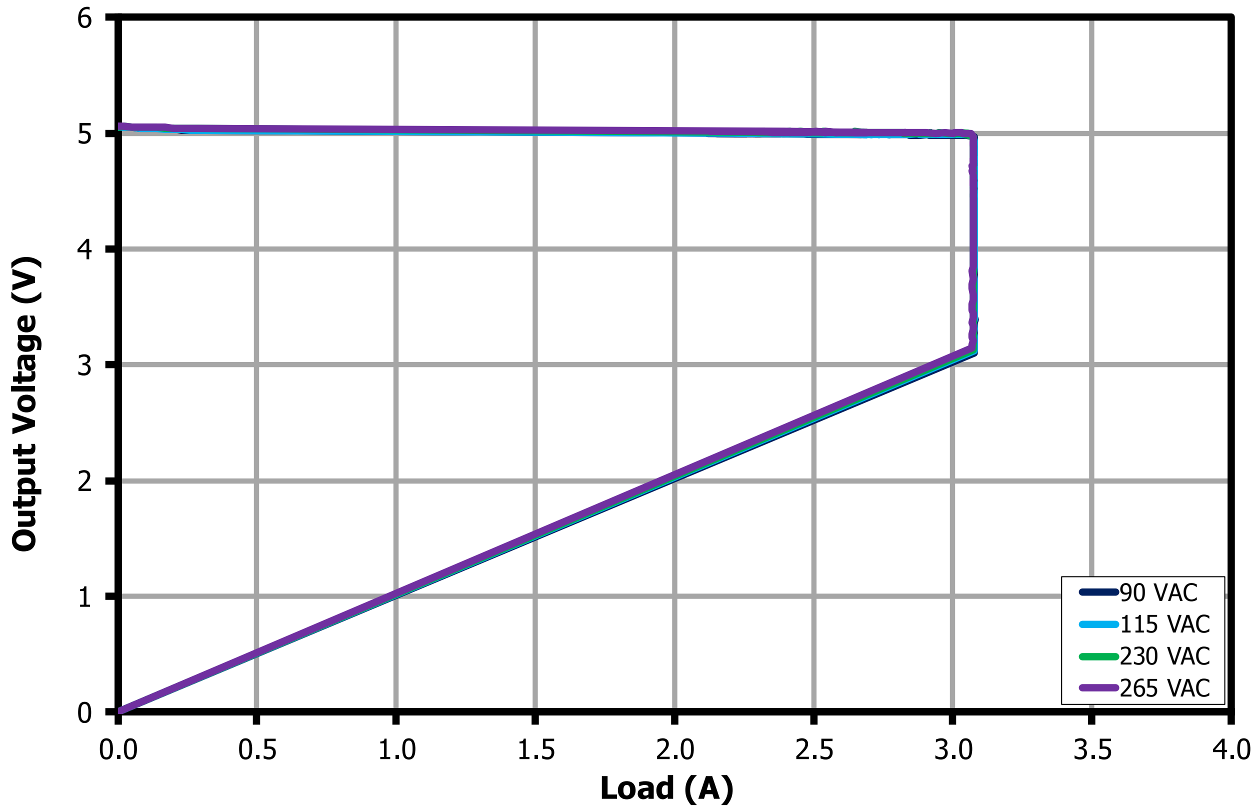
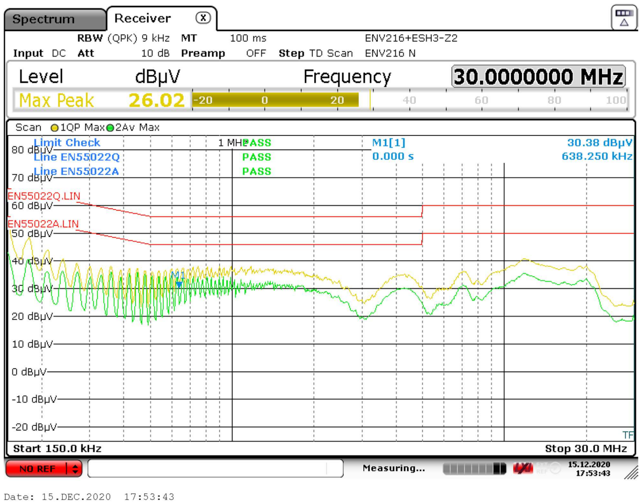


Figure 119 – CV/CC Profile with Output 5 V, 3 A.

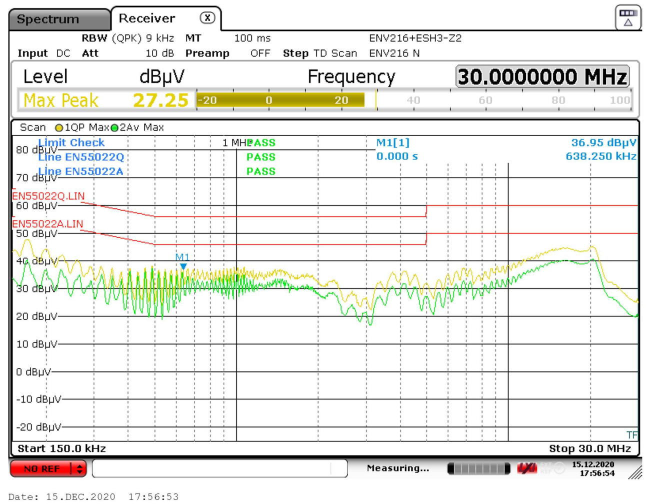
15 Conducted EMI

15.1 *Earth Floating (QPK / AV)*

15.1.1 Output: 5 V / 3 A



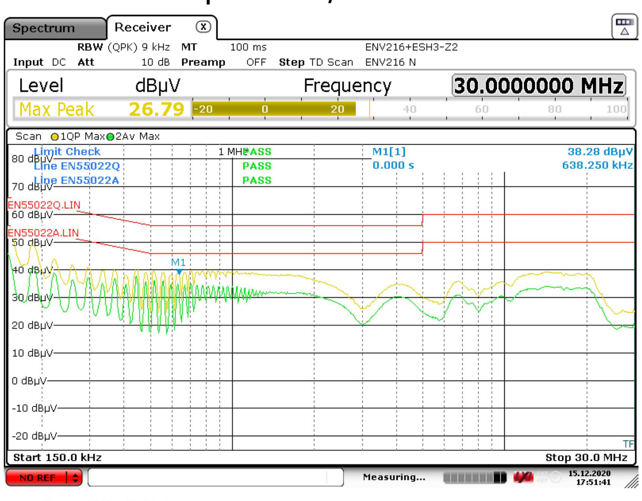
115 VAC_{IN}.



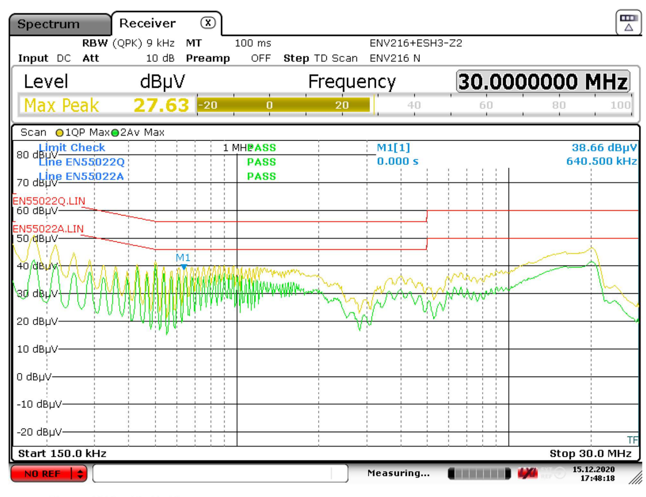
230 VAC_{IN}.

Figure 120 – Earth Floating EMI, 5 V / 3 A Load.

15.1.2 Output: 9 V / 3 A



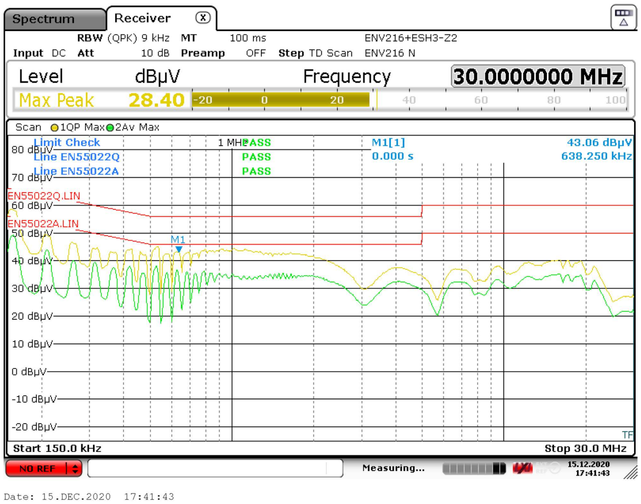
115 VAC_{IN}.



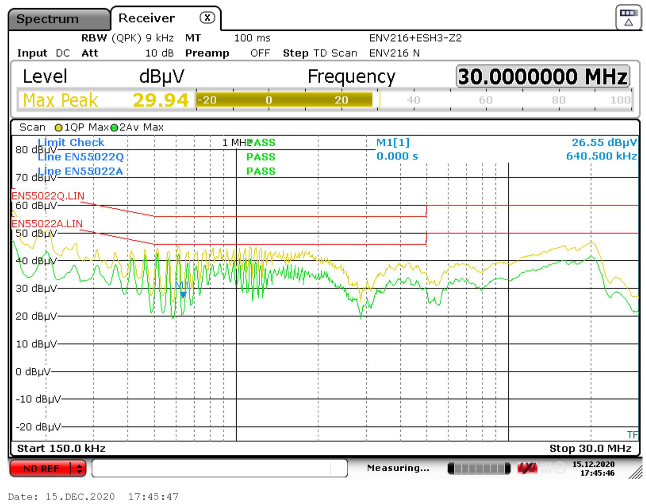
230 VAC_{IN}.

Figure 121 – Earth Floating EMI, 9 V / 3 A Load.

15.1.3 Output: 15 V / 3 A



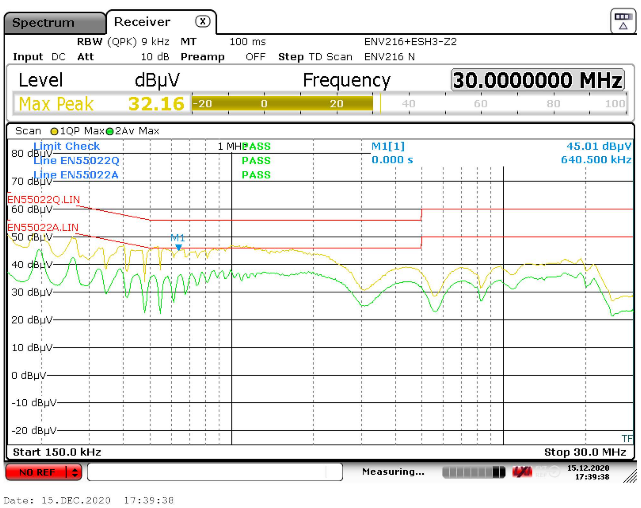
115 VAC_{IN}.



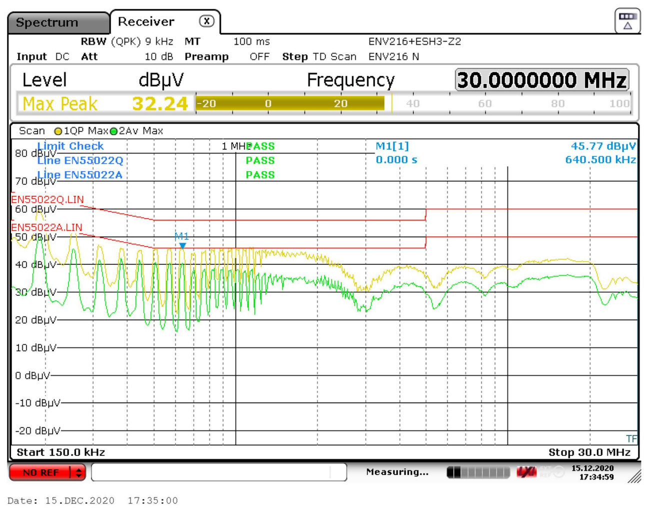
230 VAC_{IN}.

Figure 122 – Earth Floating EMI, 15 V / 3 A Load.

15.1.4 Output: 20 V / 3 A



115 VAC_{IN}.

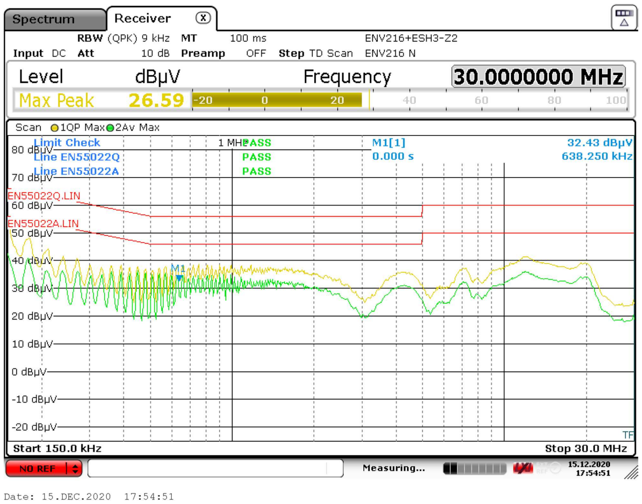


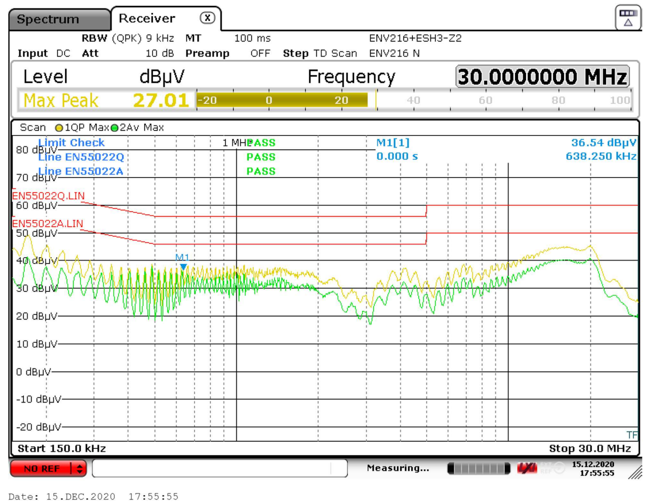
230 VAC_{IN}.

Figure 123 – Earth Floating EMI, 20 V / 3 A Load.

15.2 *Earth Grounded (QPK / AV)*

15.2.1 Output: 5 V / 3 A

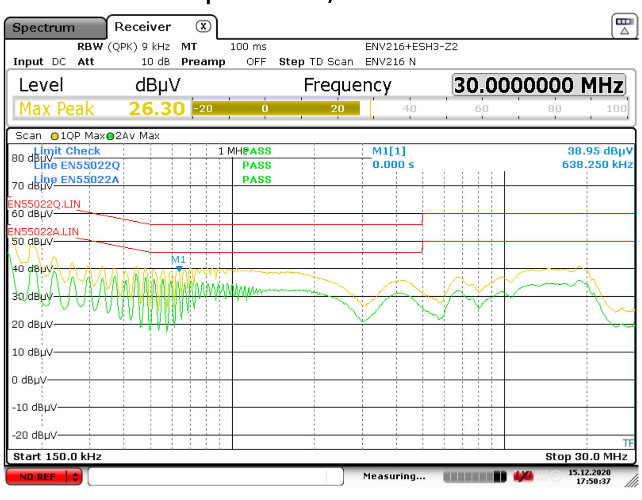


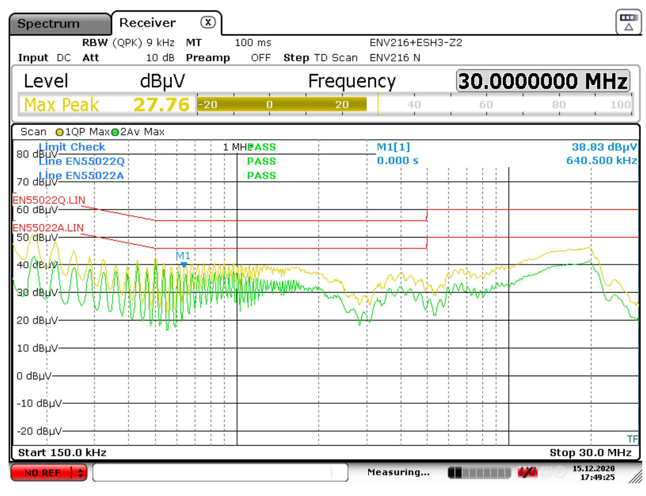


115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 124 – Earth Grounded EMI, 5 V / 3 A Load

15.2.2 Output: 9 V / 3 A

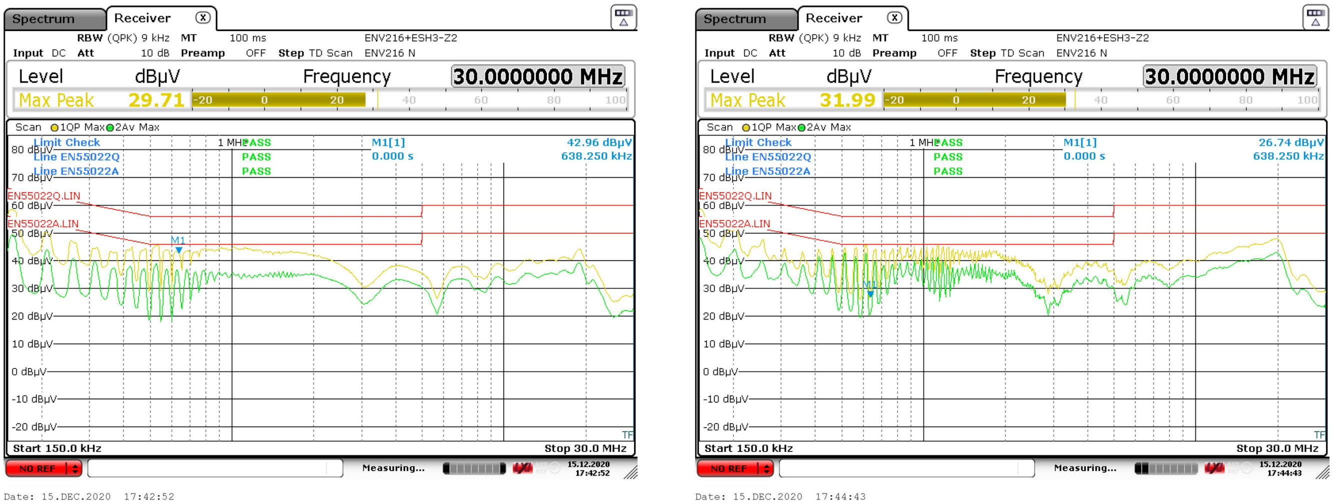




115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 125 – Earth Grounded EMI, 9 V / 3 A Load.

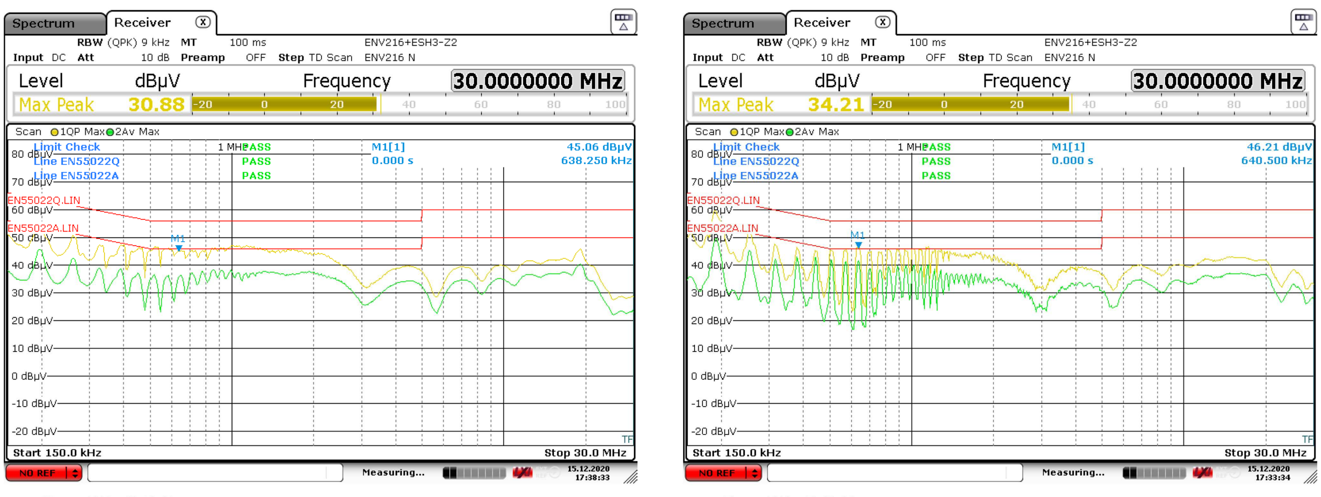
15.2.3 Output: 15 V / 3 A



115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 126 – Earth Grounded EMI, 15 V / 3 A Load.

15.2.4 Output: 20 V / 3 A



115 VAC$_{IN}$. 230 VAC$_{IN}$.

Figure 127 – Earth Grounded EMI, 20 V / 3 A Load.

16 Combination Wave Surge

The unit was subjected to ±1500 V differential mode and ±3500 V common mode combination wave surge at several line phase angles with 10 strikes for each condition. Note that InnoSwitch3-PD AR might be observed due to line OV/UV protection mechanism triggered during the test, which is a normal protection feature of the InnoSwitch3-PD IC.

16.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+1500	L1 to L2	0	Pass	Pass
-1500	L1 to L2	0	Pass	Pass
+1500	L1 to L2	90	Pass	Pass
-1500	L1 to L2	90	Pass	Pass
+1500	L1 to L2	180	Pass	Pass
-1500	L1 to L2	180	Pass	Pass
+1500	L1 to L2	270	Pass	Pass
-1500	L1 to L2	270	Pass	Pass

16.2 *Common Mode Surge (L1 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+3500	L1 to PE	0	Pass	Pass
-3500	L1 to PE	0	Pass	Pass
+3500	L1 to PE	90	Pass	Pass
-3500	L1 to PE	90	Pass	Pass
+3500	L1 to PE	180	Pass	Pass
-3500	L1 to PE	180	Pass	Pass
+3500	L1 to PE	270	Pass	Pass
-3500	L1 to PE	270	Pass	Pass

16.3 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+3500	L2 to PE	0	Pass	Pass
-3500	L2 to PE	0	Pass	Pass
+3500	L2 to PE	90	Pass	Pass
-3500	L2 to PE	90	Pass	Pass
+3500	L2 to PE	180	Pass	Pass
-3500	L2 to PE	180	Pass	Pass
+3500	L2 to PE	270	Pass	Pass
-3500	L2 to PE	270	Pass	Pass

16.4 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+3500	L1, L2 to PE	0	Pass	Pass
-3500	L1, L2 to PE	0	Pass	Pass
+3500	L1, L2 to PE	90	Pass	Pass
-3500	L1, L2 to PE	90	Pass	Pass
+3500	L1, L2 to PE	180	Pass	Pass
-3500	L1, L2 to PE	180	Pass	Pass
+3500	L1, L2 to PE	270	Pass	Pass
-3500	L1, L2 to PE	270	Pass	Pass

17 Electrostatic Discharge

The unit was tested with ±8.8 kV contact discharge and ±16.5 kV air discharge at the output VBUS, output GND, CC1 and CC2 nodes, at the end of Type-C cable and on-board, with 10 strikes for each condition. A test failure was defined as an interruption of output (latch-off) that needs operator intervention to recover, or a complete loss of function which is not recoverable.

17.1 *Contact Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location	Test Result 5 V / 0 A	Test Result 5 V / 3 A
+8.8	Output VBUS (End of Type-C cable)	Pass	Pass
	Output GND (End of Type-C cable)	Pass	Pass
	CC1 (End of Type-C cable)	Pass	Pass
	CC2 (End of Type-C cable)	Pass	Pass
-8.8	Output VBUS (End of Type-C cable)	Pass	Pass
	Output GND (End of Type-C cable)	Pass	Pass
	CC1 (End of Type-C cable)	Pass	Pass
	CC2 (End of Type-C cable)	Pass	Pass

17.2 *Air Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 5 V / 0 A	Test Result 5 V / 3 A
+16.5	Output VBUS (End of Type-C cable)	Pass	Pass
	Output GND (End of Type-C cable)	Pass	Pass
	CC1 (End of Type-C cable)	Pass	Pass
	CC2 (End of Type-C cable)	Pass	Pass
	Output GND (On-board)	Pass	Pass
	Output VBUS (On-board, no Type-C cable connection)	Pass	NA
	Output GND (On-board, no Type-C cable connection)	Pass	NA
-16.5	Output VBUS (End of Type-C cable)	Pass	Pass
	Output GND (End of Type-C cable)	Pass	Pass
	CC1 (End of Type-C cable)	Pass	Pass
	CC2 (End of Type-C cable)	Pass	Pass
	Output GND (On-board)	Pass	Pass
	Output VBUS (On-board, no Type-C cable connection)	Pass	NA
	Output GND (On-board, no Type-C cable connection)	Pass	NA

18 Voltage and Current Step Test using Quadramax and Total Phase Analyzer

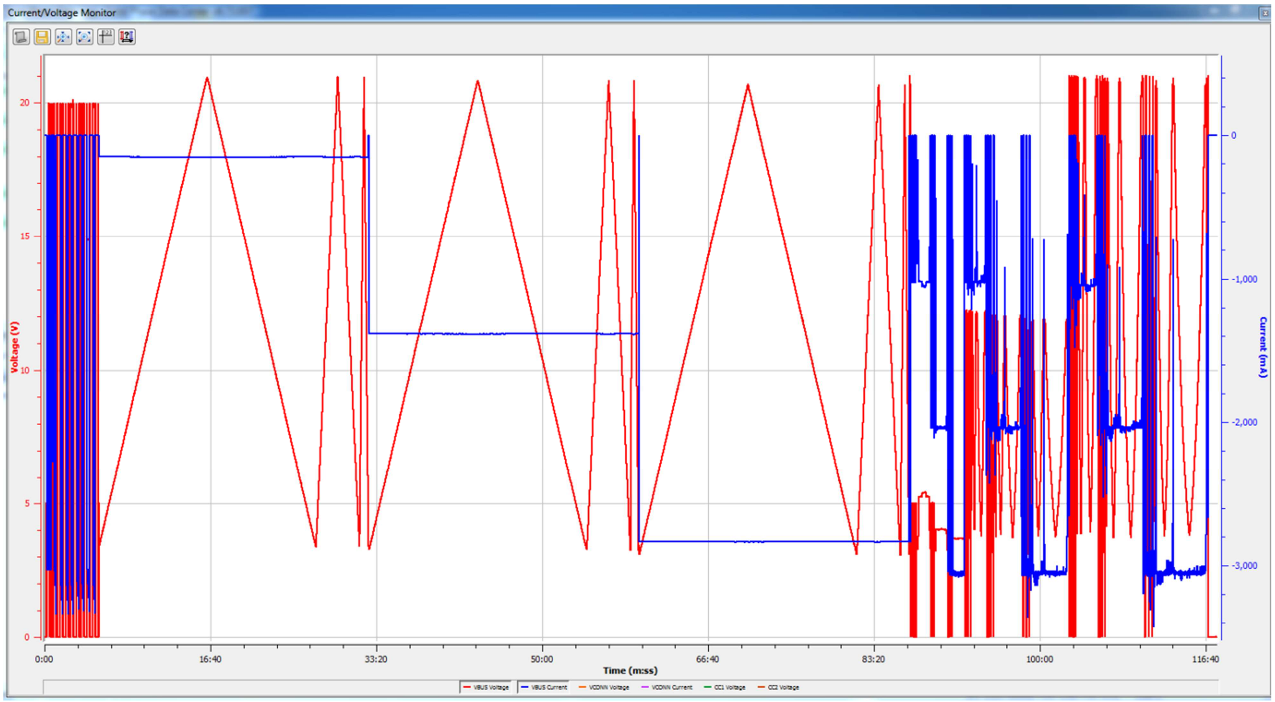


Figure 128 – Total Phase Plot for a Passing Result for VST and CLT Test in Quadramax.

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
03-Mar-11	HL/JW	3.1	Initial Release.	Apps & Mktg
21-Apr-21	JW	3.2	Corrected PCB Images.	Apps & Mktg
14-Sep-21	KM	3.3	Updated Formatting	Apps & Mktg
16-Nov-21	KM	3.4	Added Magnetics Supplier	Apps & Mktg

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