InnoMux2-BL Family

Isolated Flyback Switcher IC with One Accurate CV and up to Four Accurate CC Outputs

Product Highlights

Highly Integrated, Compact Footprint

- Accurate constant voltage and constant current outputs using a single transformer, eliminating multiple post regulators
- Pairs with the IML204DG IC to implement up to 4 accurate CC channels
- Incorporates a multi-mode quasi-resonant discontinuous conduction mode (DCM) and continuous conduction mode (CCM) flyback controller with high-voltage switch, secondary-side control and synchronous rectification driver
- Integrated FluxLink™ feedback link eliminates optocouplers
- Excellent transient response: <±5% CV with 0%-100% load step
- Constant voltage (CV) output up to 24 V and up to 150 V for constant current (CC) LED drive output

EcoSmart™ – Energy Efficient

- Design readily meets TV and monitor energy efficiency regulations
- Proprietary switching algorithm ensures high efficiency across load
- Low dissipation allows PCB cooling – no heat sinks required

Advanced Protection / Safety Features

- Primary sensed output OVP
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Overload protection for each output
- LED short / open protection

Full Safety and Regulatory Compliance

- Reinforced isolation
- Isolation voltage >4000 VAC
- 100% production HIPOT tested
- UL1577 isolation voltage 4000 VAC (max) and TUV (EN62368)
- Enables designs that have "A" performance criteria for EN61000-4 suite of test standards, including EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- Ideal for computer monitors and appliances with display panel

Description

The InnoMux™2-BL IC provides accurate, isolated, offline CV and CC regulation using a single transformer, dramatically reducing power sub-system component count and board area. The single-stage, multiple output, architecture eliminates DC/DC post regulators, providing regulated outputs. InnoMux2-BL IC-based designs have low BOM count and small size. The family incorporates both primary and secondary-side controllers, with protection, sense elements and a safety-rated feedback mechanism (FluxLink) into a single IC. The InnoMux2-BL IC also includes a multi-mode LED backlight controller making it ideal for monitors, TVs and appliances with lighting or display requirements, and partners with the IML204DG IC to implement up to four CC strings for high-end displays.

The InnoMux2-BL IC contains enhanced features for maximizing conversion efficiency including quasi-resonant switching in DCM operation, accurate SR control and minimum-threshold-regulation for the LED driver.

Figure 2. InnoMux2-BL IC in InSOP-24D Package.

Output Power Table

Product	230 VAC ±15%[1]	85-265 VAC[1]
IMX2065C[2]	25 W	22 W
IMX2066C[2]	35 W	27 W

Table 1. InnoMux2-BL Controller Part Numbers.

1. Continuous power using nominal primary current limit in a typical open frame application at +50 °C ambient with adequate PCB thermal design to ensure junction temperature <125 °C.
2. InSOP-24D.

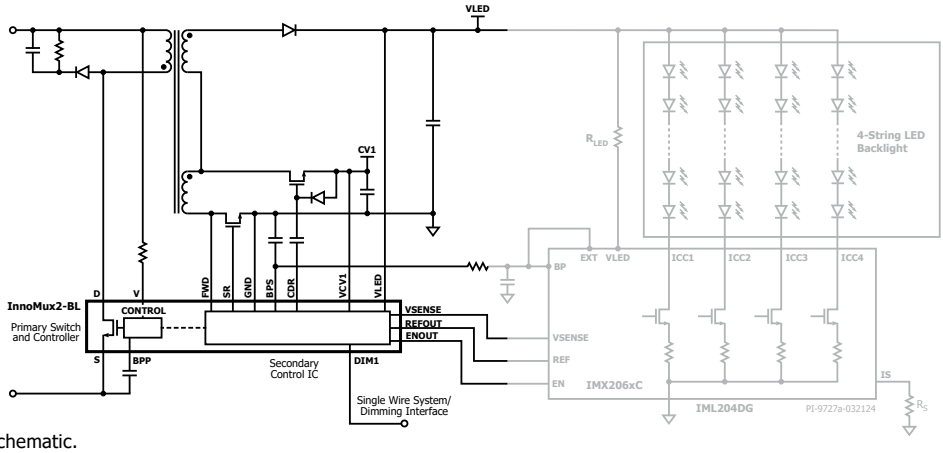


Figure 1. Typical Application Schematic.

Configuration Options

Part Number	BV Rating	Continuous Power[1]	Output with IML204DG	CV1	Maximum V_{LED}	V_{SENSE} Voltage	SR MOSFET Driver	Dimming Interface	Package
IMX2065C	650 V	22 W	1 CV, 4 CC	5 V	60 V	0.3 V	Yes	1-Pin Filtered PWM Dimming	InSOP-24D
IMX2066C	650 V	27 W	1 CV, 4 CC	5 V	60 V	0.3 V	Yes	1-Pin Filtered PWM Dimming	InSOP-24D

Table 2. Configuration Options.
1. 85 – 265 VAC.

Block Diagram

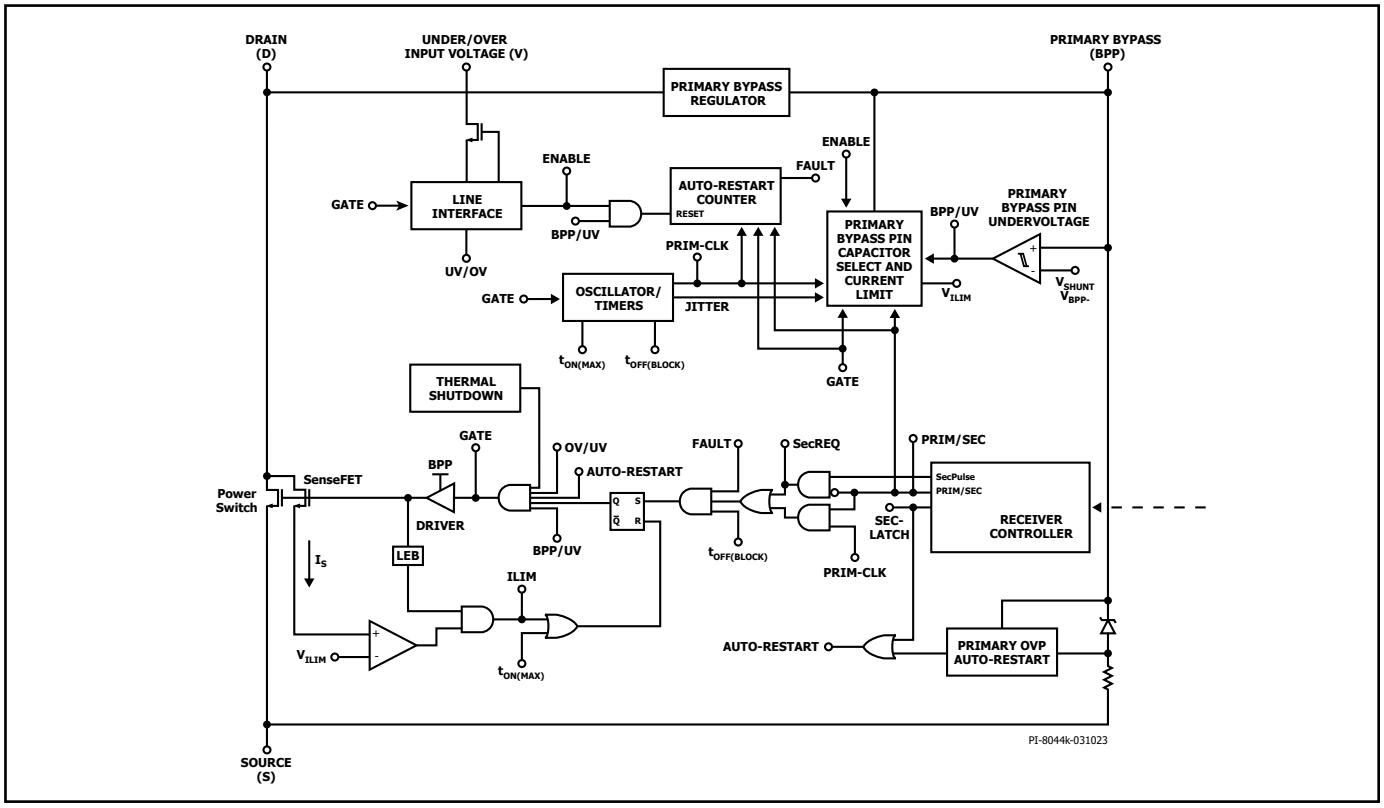


Figure 3. InnoMux2-BL Primary Block Diagram.

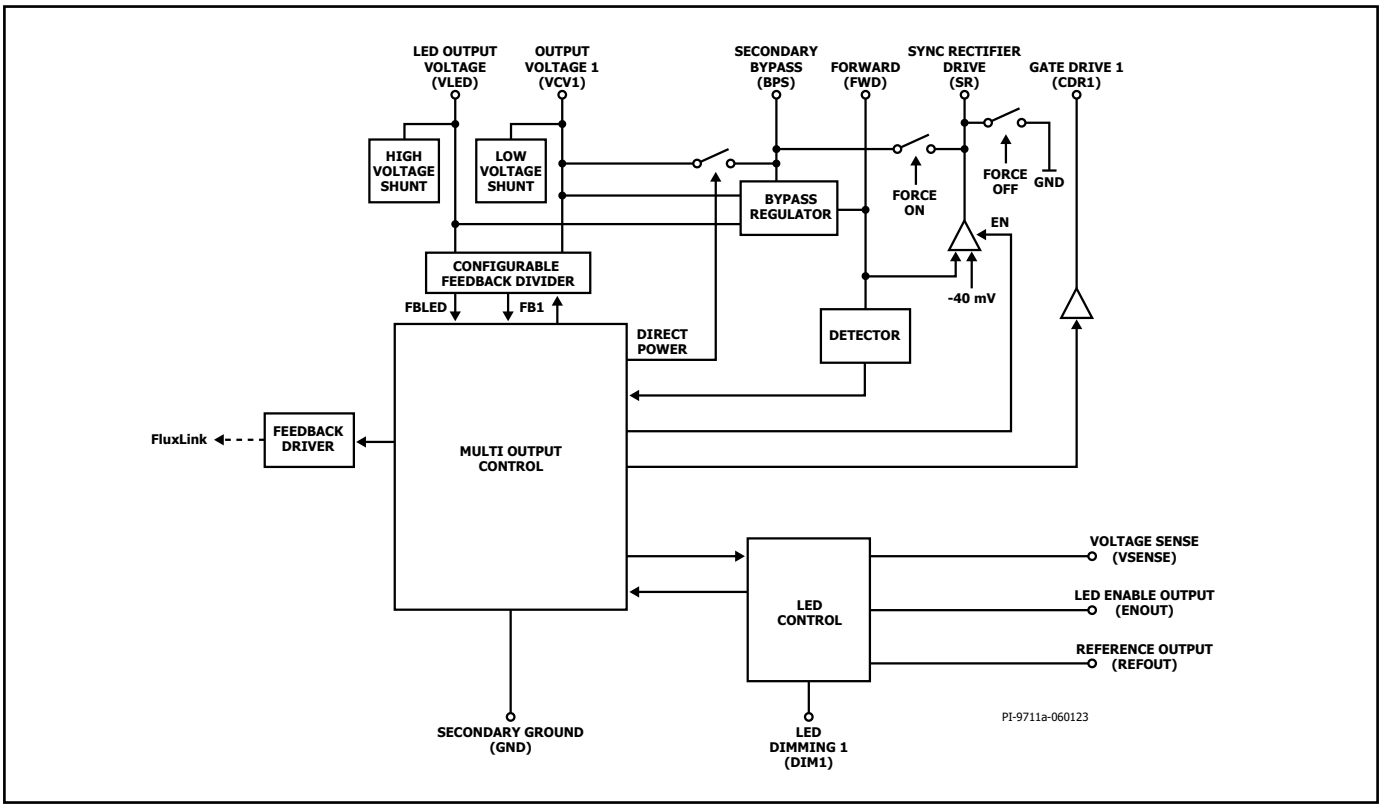


Figure 4. InnoMux2-BL Secondary Block Diagram LED Configuration.

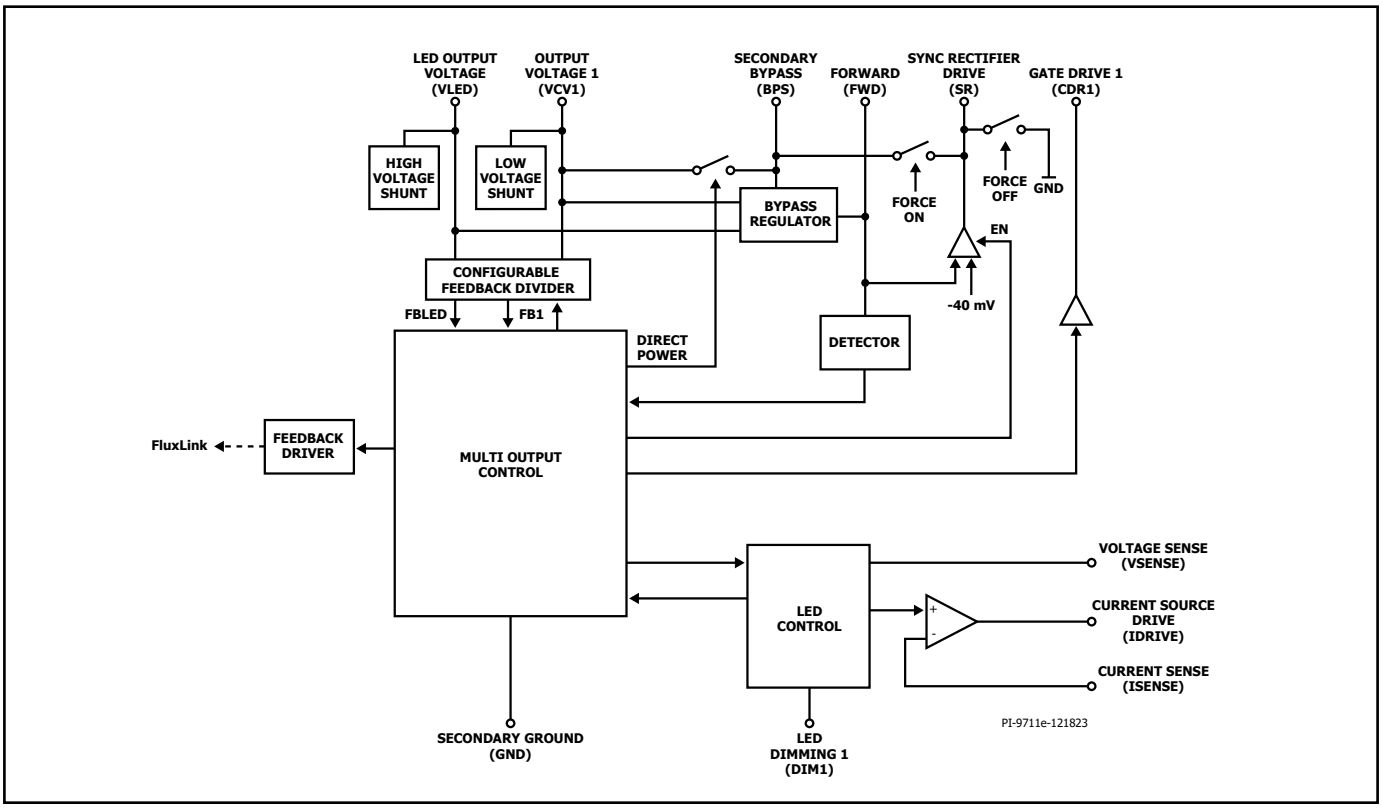


Figure 5. InnoMux2-BL Secondary Block Diagram for H411 Trim Code.

Pin Functional Description

InnoMux2-BL InSOP-24D 1CV+4LED Single Dimming with SR Pin Configuration

REFERENCED OUTPUT (REFOUT) Pin (Pin 1)
Connection to IML204DG driver for the analog dimming reference. Should be connected to REF pin on the IML204DG IC.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

LED ENABLE OUTPUT (ENOUT) Pin (Pin 3)
Connection to IML204DG driver to enable / disable the LEDs. Should be connected to EN pin on the IML204DG IC.

VOLTAGE SENSE (VSENSE) Pin (Pin 4)
Connection to IML204DG to observe the current source drain voltage. This signal is used by the InnoMux2-BL IC for regulation of the LED voltage to minimise power dissipation in the IML204DG IC. Should be connected to VSENSE pin on the IML204DG IC.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for V_{CV1} output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor for the secondary IC supply.

LED DIMMING 1 (DIM1) Pin (Pin 7)
LED dimming control input.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 8)
Gate driver for external SR MOSFET.

FORWARD (FWD) Pin (Pin 9)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 10)
Connected directly to the V_{CV1} output voltage, to provide current for the controller on the secondary-side and provide sensing for output voltage regulation and protection.

LED OUTPUT VOLTAGE (VLED) Pin (Pin 11)
Connected directly to the LED output voltage, to provide current for the controller on the secondary side and provide sensing for LED voltage regulation and protection.

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor of the primary-side supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

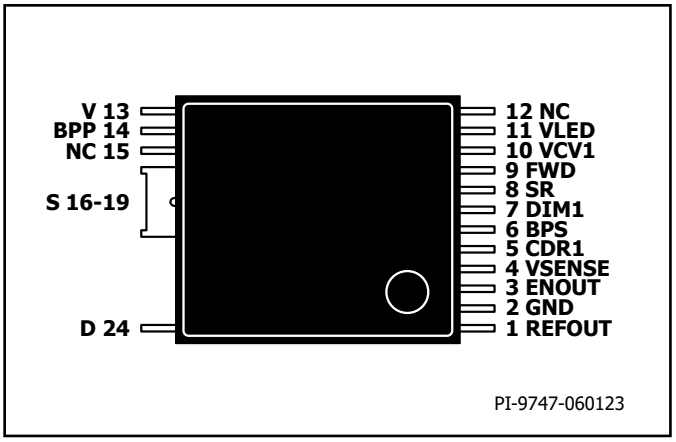


Figure 6. InnoMux2-BL InSOP-24D 1CV+4LED Single Dimming with SR Pin Configuration.

Pin Functional Description for H411 Trim Code

InnoMux2-BL InSOP-24D 1CV+1LED Single Dimming with SR Pin Configuration

CURRENT SENSE (ISENSE) Pin (Pin 1)
Connection to external LED driver MOSFET source terminal for sensing LED current. An external current sense resistor should be connected between this and the GND pin.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

CURRENT SOURCE DRIVE (IDRIVE) Pin (Pin 3)
Connection to external LED driver MOSFET gate terminal for controlling LED current.

VOLTAGE SENSE (VSENSE) Pin (Pin 4)
Connection to external LED driver MOSFET drain terminal for regulation of voltage to minimize MOSFET power dissipation.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for V_{CV1} output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor for the secondary IC supply.

LED DIMMING 1 (DIM1) Pin (Pin 7)
LED dimming control input.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 8)
Gate driver for external SR MOSFET.

FORWARD (FWD) Pin (Pin 9)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 10)
Connected directly to the V_{CV1} output voltage, to provide current for the controller on the secondary-side and provide sensing for output voltage regulation and protection.

LED OUTPUT VOLTAGE (VLED) Pin (Pin 11)
Connected directly to the LED output voltage, to provide current for the controller on the secondary side and provide sensing for LED voltage regulation and protection.

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor of the primary-side supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

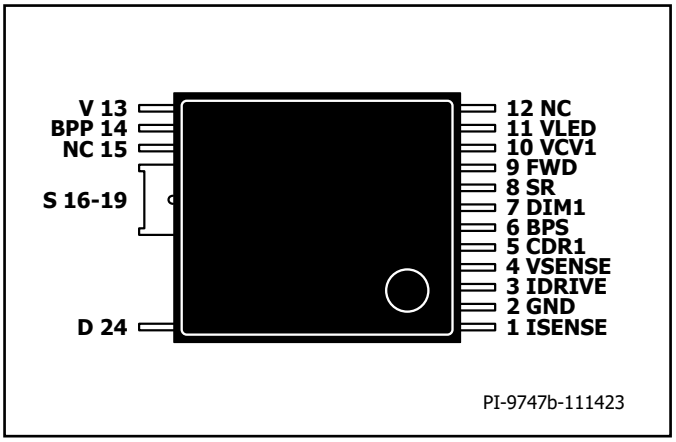


Figure 7. InnoMux2-BL InSOP-24D 1CV+1LED Single Dimming with SR Pin Configuration.

InnoMux2-BL Functional Description

The InnoMux2-BL IC combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device. The InnoMux2-BL architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to accurately communicate power requests from the secondary controller to the primary controller.

The primary controller on InnoMux2-BL IC is a quasi-resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses a variable current control scheme. The primary consists of a jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, overvoltage protection, leading edge blanking, secondary output diode / SR MOSFET short protection circuit and a 650 V power switch.

The secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, multi-output controller for regulating up to three outputs independently, 5 V regulator on the SECONDARY BYPASS pin, synchronous rectifier (SR) MOSFET driver, high-side MOSFET drivers, shunts to prevent individual outputs from rising in abnormal loading conditions, single string LED driver, timing functions and a host of integrated protection features.

Figures 3, 4 and 5 show the functional block diagrams of the primary and secondary controllers with the most important features.

Primary Controller

InnoMux2-BL IC has variable frequency CCM / CrM / DCM controller plus ZVS operation in DCM for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoMux2-BL IC to be powered externally through a bias winding, decreasing the no-load consumption and enhancing low-standby-power operation.

Primary Bypass I_{LIM} Programming

InnoMux2-BL ICs allow the user to adjust primary current limit (I_{LIM}) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used. There are 2 selectable capacitor sizes – 0.47 μF and 4.7 μF for setting standard and increased I_{LIM} settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (= $V_{BPP} – V_{BPP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to $V_{BPP(SHUNT)}$ to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has an OV protection feature with either a latching or an auto-reset response. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

Output OV protection is also included as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin $UV_{(IUV-)}$ threshold.

Over-temperature protection is also included as an integrated feature on the secondary controller.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle) to the next switching request.

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current per cycle approaches 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to prevent audible noise). The time between switching cycles will continue to increase as load reduces.

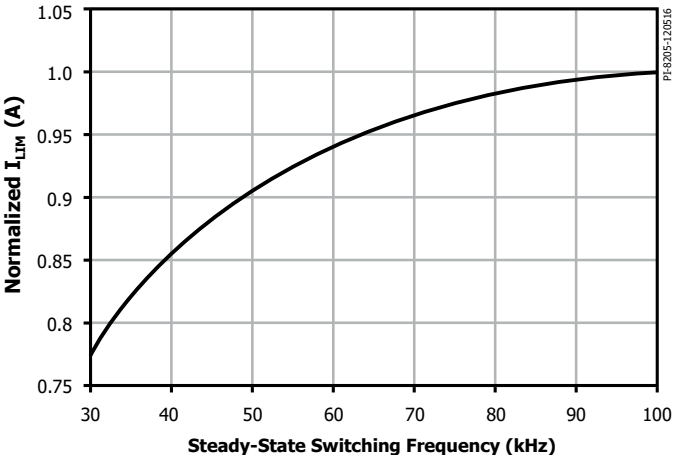


Figure 8. Normalized Primary Current vs. Switching Frequency.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M; this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoMux2-BL IC enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~3 V or by going below the UNDER/OVER INPUT VOLTAGE pin $UV_{(IUV-)}$ threshold.

In auto-restart, switching of the power MOSFET is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests received at a rate that is above the overload detection frequency (f_{OVL}) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for $>t_{AR(SK)}$.

The secondary controller can initiate an auto-restart by not sending switching request cycles to the primary controller. The primary controller will then restart.

It is also possible that communication is lost, in which case the primary will also try to restart. Although this should never be the case in normal operation, it can be useful when system ESD events(for example) cause a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where the I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs. This provides sufficient time for the transformer to reset when operating with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the I_{LIM} state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-out for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of an internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage MOSFET will disconnect the external sense resistor from the internal sense circuits to eliminate current drawn through the sense resistor. The line sensing function will reactivate at the beginning of the next switching cycle.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™, LinkSwitch™ and other InnoSwitch™ controllers).

If no feedback signals are received during the auto-restart time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up from the FORWARD pin or output voltage and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests, or if the secondary detects that the primary is switching without cycle requests, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoMux2-BL IC features an active audible noise reduction mode where by the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz – 142 µs and 83 µs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

The secondary controller includes an audible-noise-reduction engine.

Frequency Soft-Start

At start-up (before handshake) the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

Secondary Controller

The IC is powered by the 5 V (V_{BPS}) regulator which is supplied by either an output or FORWARD pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the detection block used for both handshaking and timing circuit to turn on and regulate the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation.

In continuous conduction mode (CCM) the SR FET is turned off when a feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The FORWARD detector also measures the FORWARD pin voltage during the primary on time, this feeds into the SR zero voltage switching control function.

BPS Regulator

The regulator limits the BPS pin to V_{BPS}. The source is automatically selected as follows:

- V_{CV1} is used if VCV1 pin > V_{BPS_VCV1}, otherwise
- V_{LED} is used.

V_{LED} can only be used as a source for BPS during start-up.

During start-up, the FORWARD pin is also used as a source for BPS. This is provided to support start-up into heavy load and is not intended for continuous operation. The FORWARD pin needs to be a minimum of ≈8 V when the primary is on in order for this to function correctly.

A 2.2 µF or 4.7 µF ceramic capacitor on the BPS pin is required. There are no stability requirements on the capacitor; the BPS regulator is unconditionally stable.

BPS Regulator – Direct Power

When V_{CV1} is 5 V (V_{CV5V_BPS}) the BPS pin is automatically connected internally to the VCV1 pin, directly powering BPS instead of using the BPS linear regulator. This reduces power loss in the secondary controller and reduces standby power. This is automatically selected when V_{CV1} is V_{CV5V_BPS}.

High-Side MOSFET Drive

The high-side selection MOSFETs are driven with a drive voltage that is 5 V above the given output using a capacitive drive approach. The capacitive drive approach benefits from easy level translation by use of a capacitor CDR Capacitor-Drive (CDR) . A regular refresh cycle to top up the charge on the CDR is needed when one of the switches has been on for a long time, as the charge on the CDR will otherwise slowly leak away. Refresh is also needed during start-up to allow the CDR to follow the output voltage when the output is being pulled up. The controller will perform refresh cycles when necessary by turning the selection MOSFET off and then back on.

The default refresh time is $T_{REFRESH}$, which is doubled to 2 × $T_{REFRESH}$ during start-up. The longer the refresh time the better, but the MOSFET needs to be turned back on before the end of the primary on time. Once the CV outputs are in regulation the refresh time is reduced to $T_{REFRESH}$. Because the output is no longer changing, the refresh is only needed to top up CDR and by reducing the refresh time the risk of the primary on time finishing before the refresh is reduced.

A diode is required to be placed between the gate-source of each selection MOSFET to provide a path for charging the capacitor. A low forward voltage diode such as a Schottky diode should be used.

The optimal capacitor value for CDR depends on the gate charge of the selection MOSFET. The selection MOSFET on-level gate voltage is determined by $V_{BPS} \times (C_{DR}/(C_G + C_{DR})$, so it is essential that the gate charge (at 5 V gate voltage) is much smaller than the charge in the CDR capacitor. A typical value for the CDR capacitor is 100 nF. For higher CDR capacitor values, the refresh time might be insufficient and the capacitor will not be able to follow the output during start-up. It is therefore important to select low gate-charge devices for the selection MOSFETs to minimise the required CDR capacitor value as well as to minimise energy required to drive the MOSFETs.

High-Side MOSFET Static Pull-Down

To ensure that the selection MOSFET gates are held low when the secondary is not in control, the CDR1 pin has an internal pull down circuit "ON" feature to pull the pin low and reduce any voltage on the gate due to capacitive coupling.

Synchronous Rectifier Driver

The SR driver on InnoMux2-BL IC is not an "on/off" driver. The SR MOSFET's gate-source voltage is modulated to regulate the FORWARD pin voltage to roughly -40 mV while the discharge current is flowing in the SR MOSFET. The regulated approach allows for improved noise immunity, removing the possibility of the MOSFET being turned off too early causing increased power loss.

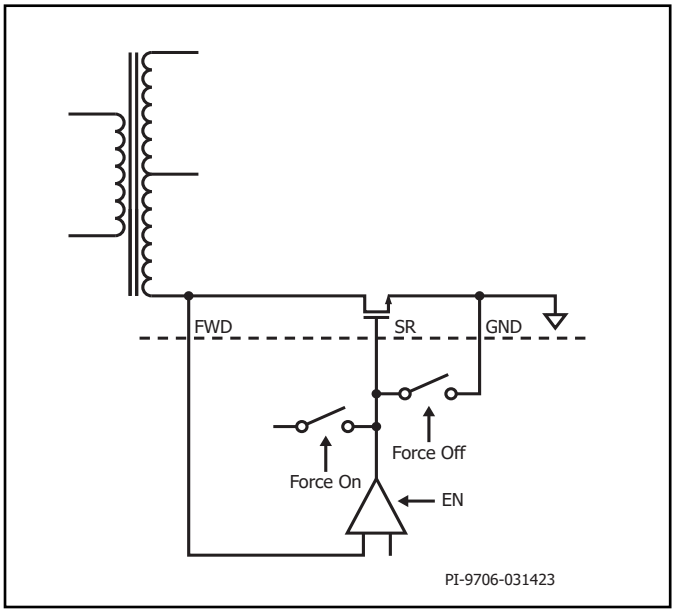


Figure 9. Synchronous Rectifier Driver Diagram.

A force-on signal provides a boost when turning on the SR MOSFET to charge the gate-source capacitance quickly. A force off signal is used to quickly discharge the gate-source capacitance when operating in CCM and also ensure the MOSFET is held off when the secondary is not conducting.

For optimum performance, an SR MOSFET with a gate-source capacitance of less than 10 nF is recommended.

SR Disable Protection

In each cycle the SR is only engaged if a new cycle is requested by the secondary controller and the negative edge is detected on the FORWARD pin.

SR Static Pull-Down

To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has internal pull down circuit "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Short/Open SR Protection

In order to protect against the SYNCHRONOUS RECTIFIER DRIVE pin system faults, (an SR pin short to ground or SR pin open), the secondary controller has a protection mode that ensures that the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is less than 200 pF, the device will assume that the SYNCHRONOUS RECTIFIER DRIVE pin is "open". If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is above 20 nF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "short". In either of these two cases a fault is detected otherwise the controller will assume an SR FET is connected.

In the event an SYNCHRONOUS RECTIFIER DRIVE pin fault is detected the secondary controller will stop requesting pulses from the primary and initiate auto-restart.

Multi-Output Control

The multi-output control regulates each output independently by requesting pulses from the primary based on the FB pin voltages of each output. The transformer energy is then directed to the output that needs the energy on a cycle-by-cycle basis. This is accomplished by turning on the selection MOSFET in series with the CV1 output. The transformer shall be designed such that the V_{OR} increases between V_{CV1} and between V_{LED}. This guarantees that the current through the V_{LED} diode is negligible when the selection MOSFET for V_{CV1} is turned on, disabling the selection MOSFET will direct the energy delivery to the LED output.

Enhanced Audible Noise Reduction

The InnoMux2-BL IC has enhanced features for audible noise reduction. Multi-output control can create sub-harmonic frequencies of the switching frequency in the flux of the transformer. These sub-harmonics can fall in the audible range. The InnoMux2-BL IC avoids such conditions by sharing fractions of discharge pulses between outputs.

This is achieved by allowing the first part of the discharge pulse to the V_{LED} output and then turning on the selection MOSFET part way through the discharge and allowing the second part of the discharge to flow via the V_{CV1} output. The point at which the MOSFET is turned on to switch over from the LED output to the CV1 output is dependent on the relative loading of the outputs.

This provides an added benefit of reducing the RMS currents in the secondary windings, reducing power loss. The operating frequency of each output is increased (while the power switch frequency remains the same) reducing the output ripple for a given filter capacitance.

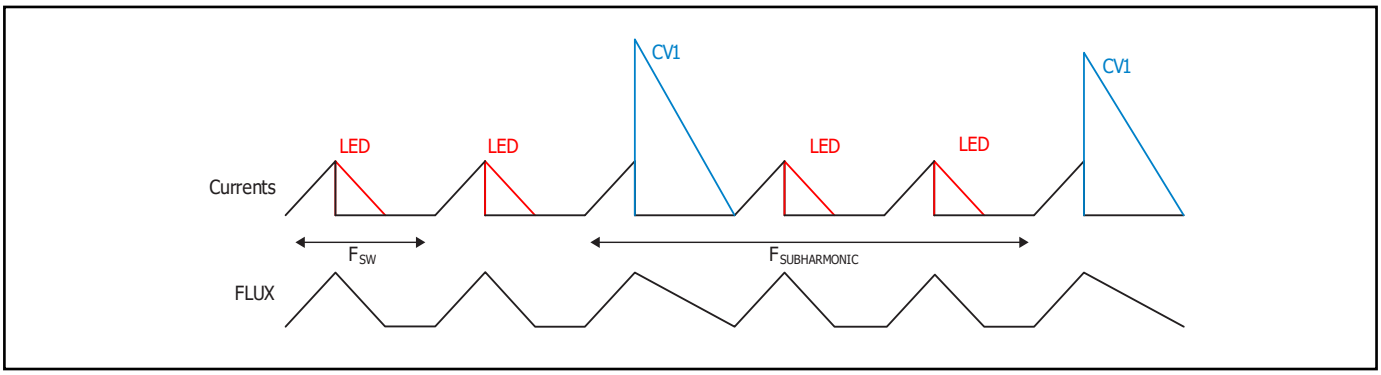


Figure 10. Multi-Output Control Switching Pattern.

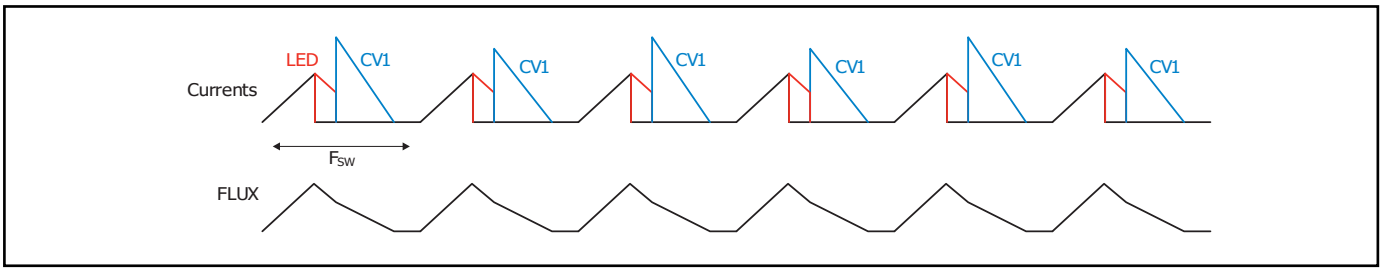


Figure 11. InnoMux2-BL Switching Pattern.

Output Capacitance Requirement

The InnoMux2-BL IC has a minimum output capacitance requirement for each output to ensure optimum operation. This is given by the following equation:

$$C_{OUT_{MIN}} = \frac{L_{PRI} \times I_{LIMIT}^2}{4 \times \frac{V_{OUT}^2}{V_{FB(REG)}} \times V_{SHTHR}}$$

Where:

L_{PRI} is the primary inductance
I_{LIMIT} is the primary peak current
V_{OUT} is the output voltage for the given output
V_{SHTHR} is 10 mV for CV outputs and 5 mV for VLED output
$V_{FB(REG)}$ internal voltage comparator reference voltage

Minimum Off-Time

The secondary controller initiates a cycle request using the FluxLink magneto-inductive connection to the primary. The maximum frequency of secondary cycle requests is limited by the minimum cycle off-time of $t_{OFF(MIN)}$. This ensures that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency

The maximum switch-request frequency from the secondary controller is f_{SREQ}.

Maximum Secondary Inhibit Period

Secondary requests to initiate primary switching are inhibited when necessary to maintain operation below maximum frequency and ensure minimum off-time. Secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle request is ~30 µs.

Output Voltage Protection

If the output voltage is 12% higher than the regulation threshold for V_{CV1} or 16% higher than the regulation threshold for V_{LED} a command is sent to the primary to either latch-off or begin an auto-restart sequence. This integrated output OVP can be used in conjunction or independently to the primary sensed OVP.

Shunts

The LV shunt is designed to limit the voltage lift on the V_{CV1} output. Voltage lift on the V_{CV1} output will typically occur due to its lower V_{OR}. At turn-on of the V_{CV1} selection MOSFET after delivery of a pulse to one of the other outputs, a small amount of energy is delivered to the V_{CV1} output from the higher idle ring voltage. The LV shunt is turned on when the sensed voltage exceeds $V_{LV(SHUNT)}$.

In practical applications it is unlikely that the V_{CV1} output will lift; V_{CV1} output lift typically only occurs when the V_{CV1} output is unloaded while the other outputs are running at high load. It is likely V_{CV1} is powering the secondary controller and this alone is sufficent to prevent lift.

The HV shunt is used to limit the voltage on the V_{LED} rail to the maximum allowed voltage in case of peak-charging of the V_{LED} output when the V_{LED} output is not loaded. This peak charging is predominantly caused by leakage in the transformer; the V_{LED} output typically has lowest leakage and thus will receive a small amount of energy from switching cycles that are destined for V_{CV1}. The HV shunt is turned on when the sensed voltage exceeds $V_{HV(SHUNT)}$.

Overload / Short-Circuit Protection

The V_{CV1} and V_{LED} outputs have a maximum power protection feature. The controller determines whether the output is more than 10% (CV outputs) or more than 1% (V_{LED} output) below the set point. If this condition persists for multiple switching cycles, then the output is assumed to be overloaded – either the output has a short-circuit, or the output power capability of the power supply has been exceeded and it cannot maintain regulation.

Power Limit

Short-circuit fault protection acts as system power limit but it would allow the full output power to be drawn from a single output. The power limit function therefore also includes an average frequency limit that has a configurable level.

The power limit threshold for each of the three outputs is set by controller configuration (default is disabled). Several setting levels for each output are available.

The power limit measures the average frequency of switching pulses to a specific output. If this frequency is above a preset threshold for a certain amount of time, then a fault is flagged and the controller will auto restart or latch-off.

Power Limit Options
30 kHz
38 kHz
47 kHz
59 kHz
73 kHz
92 kHz
115 kHz

Table 3. Power Limit Options.

Over-Temperature Latch-Off

The thermal shutdown circuitry senses the secondary die temperature. The threshold is set to $T_{SD(SEC)}$.

Primary control over-temperature is the main temperature protection feature and includes hysteresis. The secondary controller also has over temperature protection but once reached creates a latch-off condition as hysteresis is not available.

DCM ZVS Mode Switching

The InnoMux2-BL IC features Zero Voltage Switching (ZVS) in the primary switch while the converter is operating in discontinuous conduction mode (DCM). This is achieved using the synchronous rectifier (SR) MOSFET. This mode of operation is disabled in continuous conduction mode (CCM).

Before turning on the primary switch, the SR MOSFET is turned on at the valley of the idle ring on the FORWARD pin. The SR MOSFET is kept on to charge the transformer's magnetizing inductance. The SR MOSFET is turned off and the voltage on the primary is allowed to ring down to near zero volts at which point the primary switch is turned on.

The SR MOSFET on-time for achieving ZVS is automatically calculated by the InnoMux2-BL controller. This corrects for design parameters, input voltage and output voltage. The calculation is based on the FORWARD pin voltage during the primary on-time. To sample the FORWARD pin voltage correctly the primary on-time needs to be at least 500 ns and FORWARD pin voltage needs to be less than 100 V.

ZVS is not available when the LED is disabled when operating below 15 kHz, or when the FORWARD pin is out of range. In this case quasi-resonant switching is used.

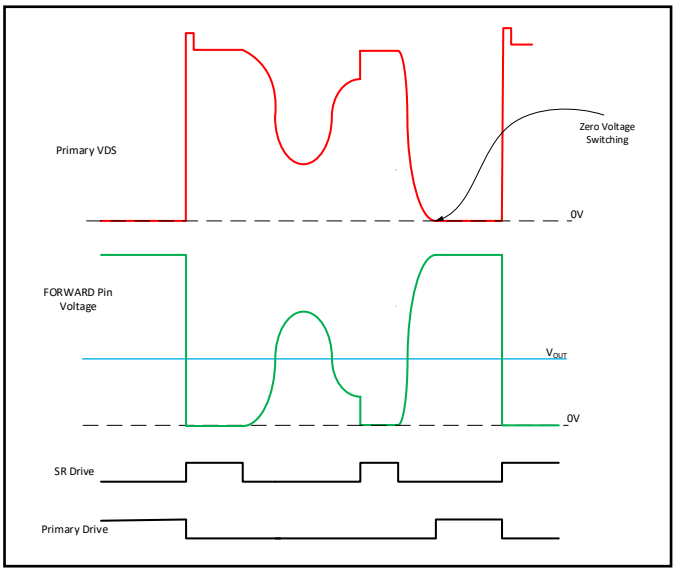


Figure 12. DCM ZVS Mode Switching.

DCM Only Mode

With PFC input or for a high-line (only) input design, DCM is always preferred due to the lower SR voltage spike when the primary turns on. The InnoMux2-BL IC has an option to only allow DCM switching. To ensure power delivery in a corner case condition, a $K_P > 1.2$ is recommended to enable this feature.

Four LED Strings Operation

The InnoMux2-BL IC is paired with the IML204DG companion controller for driving a 4-string backlight. The InnoMux2-BL IC will minimize the voltage drop over the current sources in the IML204DG companion controller by regulating the output voltage driving the LED strings (V_{LED}).

The interface between the InnoMux2-BL IC and IML204DG IC is described in the IML204DG data sheet.

Output Voltage Regulation for VLED Output

To maximize efficiency the InnoMux2-BL IC keeps the voltage drop across the current source as low as possible. The output voltage for driving the LED string (V_{LED}) is therefore regulated according to the minimum required voltage drop across the current source. The low voltage drop across the current source is maintained for any LED current by changing the V_{LED} output voltage set point.

The minimum voltage setting is configurable to accommodate a range of LED requirements and MOSFET characteristics.

To ensure stability of the LED voltage regulation a maximum V_{LED} output capacitance is recommended which depends on the maximum LED voltage and the maximum LED current.

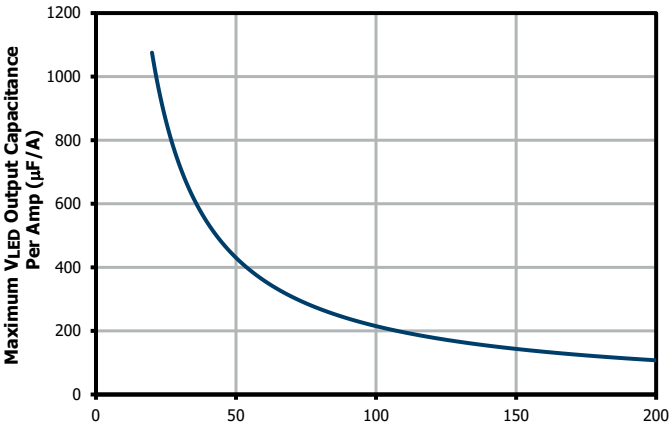


Figure 13. Maximum LED Output Capacitance.

LED Dimming

The current through the LED strings can be varied to change the LED brightness.

The InnoMux2-BL IC supports multiple dimming modes. The dimming mode is also configurable.

Figure 14 provides an overview of the available dimming modes in the InnoMux2-BL IC.

PWM Dimming

In this mode, the LED current steps from zero to $I_{LED(MAX)}$ at a frequency given by the PWM input. The LED average current is controlled by the duty cycle of the PWM input.

PWM dimming is supported by applying a PWM signal with desired duty cycle to the DIM1 pin. The allowed PWM frequency range is given by $PWM_{F(RANGE)}$. Pulling the DIM1 pin low disables the LEDs.

Pulling DIM1 low is intended to disable the LEDs during a 'screen-off' mode. Disabling the LED regulator will reduce the InnoMux2-BL IC current consumption.

The LED driver is limited to a minimum on-time ($t_{LED(ON)MIN}$) which limits the minimum duty cycle and a minimum off time $t_{LED(OFF)MIN}$ which limits the maximum duty cycle before reaching 100%. 100% duty is achievable.

Analog Dimming

In this mode, the LED current is continuous and is proportional to the DIM1 pin voltage. $V_{ADIM(MAX)}$ on DIM1 pin corresponds to $I_{LED(MAX)}$, reducing the DIM1 pin voltage reduces the LED current in a linear fashion. Pulling DIM1 pin below $V_{ADIM(DISABLE)}$ disables the LEDs and they remain disabled until DIM1 pin is above $V_{ADIM(ENABLE)}$.

Filtered PWM Dimming

In this mode, the LED current is continuous (as in Analog Dimming). The LED current level is proportional to the DIM1 pin duty cycle. This avoids the need for generating an accurate analog voltage, instead a regular PWM signal can be used and the controller converts the duty cycle to an analog current level.

100% duty cycle on the DIM1 pin corresponds to $I_{LED(MAX)}$, reducing the DIM1 pin duty cycle reduces the LED current in a linear fashion from 100% down to 3%. The allowed PWM frequency range is $FPWM_{F(RANGE)}$. Pulling DIM1 pin low disables the LEDs.

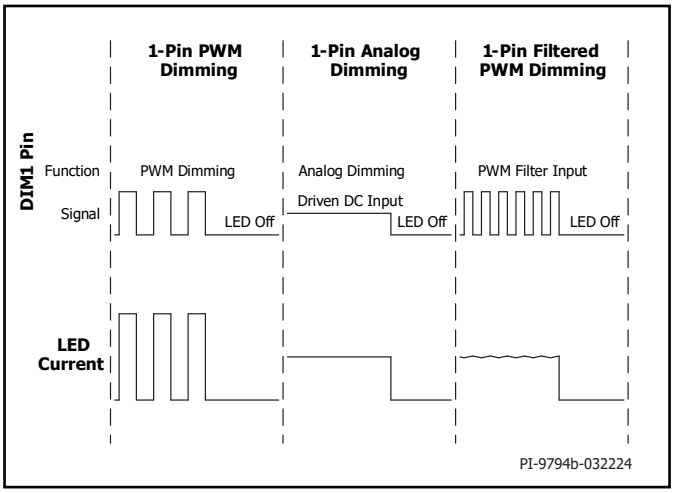


Figure 14. InnoMux2-BL Dimming Modes.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage ..... -0.3 to 650 V
DRAIN Pin Peak Current: IMX2065 ..... 3.87 A
IMX2066 ..... 4.88 A
V Pin Voltage ..... -0.3 V to 650 V
BPP/BPS Pin Voltage ..... -0.3 V to 6 V
BPP Pin Current ..... 100 mA
FWD Pin Voltage ..... -1.5 V to 250 V
SR Pin Voltage ..... -0.3 V to 6 V
VCV1 Pin Voltage ..... -0.3 V to 30 V
VLED Pin Voltage ..... -0.3 V to 250 V
CDR1 Pin Voltage ..... -0.3 V to 6 V
DIM1 Pin Voltage ..... -0.3 V to 6 V
ENOUT Pin Voltage ..... -0.3 V to 6 V
REFOUT Pin Voltage ..... -0.3 V to 6 V
ISENSE Pin Voltage ..... -0.3 V to 6 V
IDRIVE Pin Voltage ..... -0.3 V to 6 V
VSENSE Pin Voltage ..... -0.3 V to 250 V

Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3] ..... -40 to 150 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16” from case for 5 seconds.

Thermal Resistance

Thermal Resistance: IMX2065C
(θ_{JA}) ..... 58 °C/W[2], 54 °C/W[3]
(θ_{JC}) ..... 7 °C/W[2]
IMX2066C
(θ_{JA}) ..... 51 °C/W[2], 46 °C/W[3]
(θ_{JC}) ..... 5 °C/W[2]

Notes:
1. The case temperature is measured on the top of the package.
2. Soldered to 0.36 sq. inch (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1.0 sq. inch (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz		0.8	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (MOSFET not Switching) T_J = 25 °C		145	200	300	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (MOSFET Switching at f_{OSC}) T_J = 25 °C	IMX2065		0.65	1.03	mA
			IMX2066		0.86	1.21	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	T_J = 25 °C V_{BP} = 0 V		4.65	4.90	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.80	3.15	3.50	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.6	25.8	28	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		20.0	23	24.5	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		106	115	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			7		µA
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100			µA
Line Fault Protection							
UV/OV Pin Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C			3		µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT}	di/dt = 238 mA/µs T_J = 25 °C	IMX2065	0.88	0.95	1.02	A
		di/dt = 313 mA/µs T_J = 25 °C	IMX2066	1.16	1.25	1.34	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$	di/dt = 288 mA/µs T_J = 25 °C	IMX2065	1.05	1.15	1.25	A
		di/dt = 363 mA/µs T_J = 25 °C	IMX2066	1.32	1.45	1.58	
Overload Frequency	f_{OVL}	T_J = 25 °C		102	110	118	kHz
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6	7.5	11.3	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7	2	2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note B		0.17	0.2	0.23	sec
Output							
On-State Resistance	$R_{DS(ON)}$	IMX2065 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	Ω
			T_J = 100 °C		3.02	3.47	
		IMX2066 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.30	1.50	
			T_J = 100 °C		2.02	2.32	
Off-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$				70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	118	130	145	kHz
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C		3.2		mA
BPS Pin Voltage	V_{BPS}		4.9	5.0	5.15	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)}$			3.0	3.3	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(HYS)}$	T_J = 25 °C		1.0		V
Start-Up Ramp Time	$t_{SS(RAMP)}$			76		ms
Minimum Off-Time	$t_{OFF(MIN)}$			3.2		µs
BPS Direct Power V_{CV1} Range	$V_{CV5V(BPS)}$		4.65	5.0	5.45	V
BPS Source Threshold V_{CV1}	$V_{BPS(VCV1)}$		7.4	7.9	9.3	V
Minimum Voltage V_{LED}	$V_{STAYALIVE}$		6.55	8.0	9	V
Threshold Shutdown	$T_{SD(SEC)}$	See Note B		140		°C
Recommended Output Voltage Range						
V_{CV1} Recommended Voltage Range	V_{CV1}		5		25	V
V_{LED} Recommended Voltage Range	V_{LED}		9		150	V
Feedback						
FEEDBACK Pin Regulation Voltage	$V_{FB(REG)}$	T_J = 25 °C	1.208	1.220	1.234	V
Overvoltage Threshold V_{CV1}	$V_{FB(OVP)}$	T_J = 25 °C		112% of $V_{FB(REG)}$		V
Overvoltage Threshold V_{LED}	$V_{FB(OVP)VLED}$	T_J = 25 °C		116% of $V_{FB(REG)}$		V
LV Shunt Threshold	$V_{LV(SHUNT)}$	T_J = 25 °C		104% of $V_{FB(REG)}$		V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Feedback (cont.)							
Maximum LV Shunt Current	$I_{LV(SHUNT)}$			20	30		mA
HV Shunt Threshold	$V_{HV(SHUNT)}$		V_{LED}		108% of $V_{FB(REG)}$		
Maximum HV Shunt Current	$I_{HV(SHUNT)}$		V_{LED} < 50 V		8		mA
			V_{LED} < 100 V		4.1		mA
			V_{LED} < 150 V		3.3		mA
			V_{LED} > 150 V		2.1		mA
Led Control							
Frequency Range PWM Dimming	$PWM_{F(RANGE)}$			90		30,000	Hz
Frequency Range Filtered PWM Dimming	$FPWM_{F(RANGE)}$			90		30,000	HZ
Minimum On-Time PWM Dimming	$t_{LED(ON)MIN}$				5		µs
Frequency Range PWM Dimming	$PWM_{F(RANGE)}$	H411 variant only		90		1,000	Hz
Frequency Range Filtered PWM Dimming	$FPWM_{F(RANGE)}$	H411 variant only		90		30,000	Hz
Minimum On-Time PWM Dimming	$t_{LED(ON)MIN}$	H411 variant only			12		µs
Minimum Off-Time PWM Dimming	$t_{LED(OFF)MIN}$	Limits the maximum duty cycle before reach 100%			1		µs
DIM1 Pin Digital Input Thresholds	V_{IL}					0.8	V
	V_{IH}			2.0			V
DIM1 Pin Maximum Analog Dimming Voltage	$V_{ADIM(MAX)}$				3.0		V
DIM1 Pin Analog Dimming Enable Threshold	$V_{ADIM(ENABLE)}$				100	120	mV
DIM1 Pin Analog Dimming Disable Threshold	$V_{ADIM(DISABLE)}$			40	50		mV
VSENSE Pin Short to VLED Pin Detection Threshold	$V_{SENSE(FAULT)}$	T_J = 25 °C			97% of V_{LED}		V
ISENSE Pin Voltage	V_{SENSE}	DIM1 Pin = $V_{ADIM(MAX)}$ (ADIM) DIM1 Pin = 100% Duty (FPWM) T_J = 25 °C		98	100	102	mV
		DIM1 Pin = 10% of $V_{ADIM(MAX)}$ (ADIM) DIM1 Pin = 10% Duty (FPWM) T_J = 25 °C		8	10	12	
IDRIVE Pin Saturation Detection	$V_{IDRIVE(SAT)}$	T_J = 25 °C			85% of BPS		V

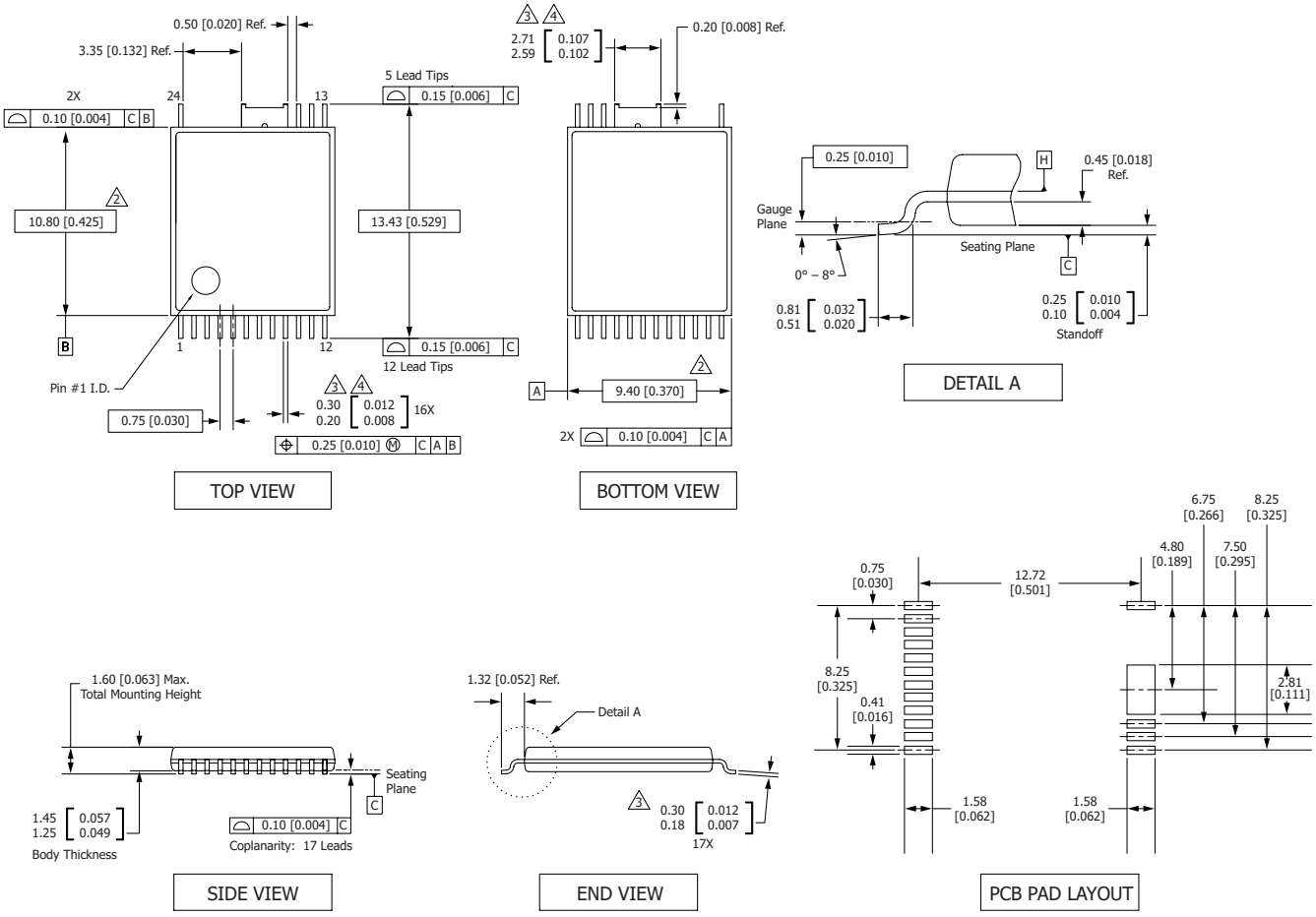
Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Selection MOSFET						
CDR1 Pin Drive Voltage	V_{CDR}			BPS		V
CDR1 Pin Pull-Up Resistance		T_J = 25 °C	4.75	5.4	5.8	Ω
CDR1 Pin Pull-Down Resistance		T_J = 25 °C	4.75	5.4	6.5	Ω
Refresh Pulse Width	$T_{REFRESH}$	Note: Doubled during start-up		500		ns
Synchronous Rectifier[1]						
SR Pin Drive Voltage	V_{SR}			BPS		V
SR FWD Pin Regulation Target	$V_{FWD(REG)}$			-40	-85	mV
SR Pin Pull-Up Speed	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF $V_{FWD(REG)}$ - V_{FWD} = +40 mV		10		V/µs
SR Pin Pull-Down Speed	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF $V_{FWD(REG)}$ - V_{FWD} = -30 mV		-10		V/µs
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2nF 10-90%		50		ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2nF 10-90%		25		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 5.0 V I_{SR} = 5 mA	6	7.9	9	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 5.0 V I_{SR} = 5 mA	6	7.8	9	Ω

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Minimum	Value Tolerance Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

InSOP-24D



Notes:

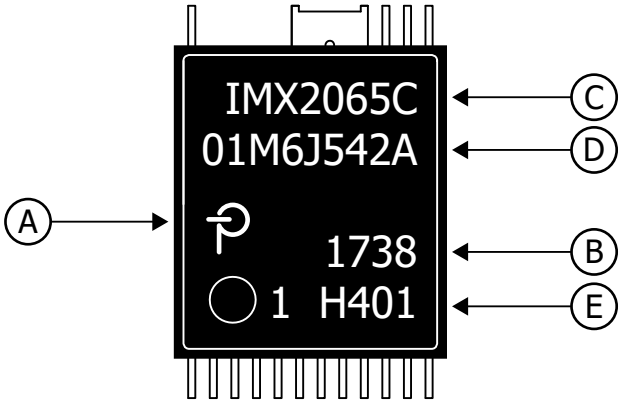
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

PI-8106-052620
POD-inSOP-24D Rev C

POD-inSOP-24D_C_052920

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8727r-110923

Feature Code Option

Part Number	Feature Code	Feature
IMX2065C	H411	1 CV and 1 CC Output
IMX2066C	H411	1 CV and 1 CC output

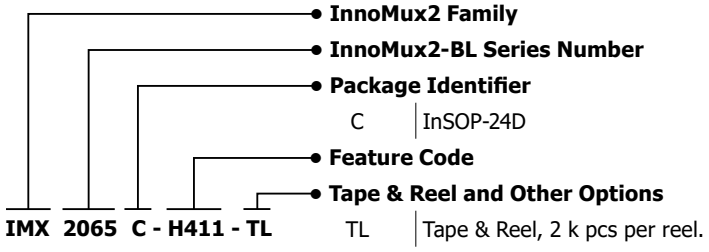
MSL Table

Part Number	MSL Rating
IMX2065C	3
IMX2066C	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
B	Production release.	03/24
C	Figure description update on page 6.	09/24

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany
(AC-DC/LED/Motor Control Sales)
Einsteinring 37
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
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