PANJIT SEMI CONDUCTOR

CHAMPION

Dr. Flyback™ for Optimal Efficiency (95% to 96%) & Power Density

Resonant Flyback

Almost Always ZVS for both switches to reduce EMI filters size and to reduce transformer size

f_{sw} V_{EAO}-clamped=2.0V: Laser Trim for Switching Frequency Selection in Light Load Mode

Ready for GaN or SiC

GENERAL DESCRIPTION

Dr. Flyback™ is the industry first **Resonant Flyback** controller with integrated Super Junction Mosfet (SJMOS):

TSSOP package:
High Side integrates a 650V/4A 1.2Ω Power Mosfet

Dr. Flyback™ system's both switches (High Side Mosfet and Low Side Mosfet) are **Almost Always Zero Voltage Switching (ZVS)**. As the results, its efficiency is ~2% higher than the traditional Quasi-Resonant (QR) Flyback topology.

Dr. Flyback™ unique Input Power and Switching Frequency one to one mapping, **Dr. Flyback™** efficiency is optimized for 100%, 75%, 50%, 25%, 10%, light load and no load consumption.

APPLICATIONS

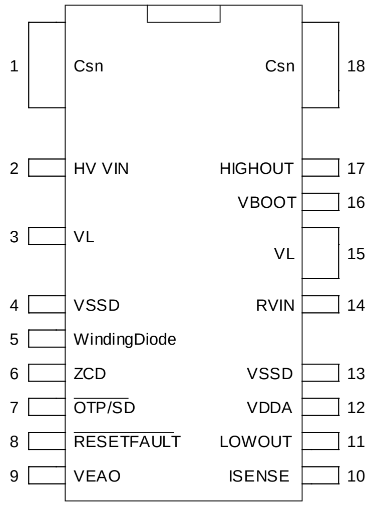
- Output Power < 150W Flyback Converter
- Optimal Power Density AC Adapter/Charger (uncased) ➔ 32.8W/in³ (2W/cc)
- Cool Mos or GaN or SiC Device in AC Adapter

FEATURES

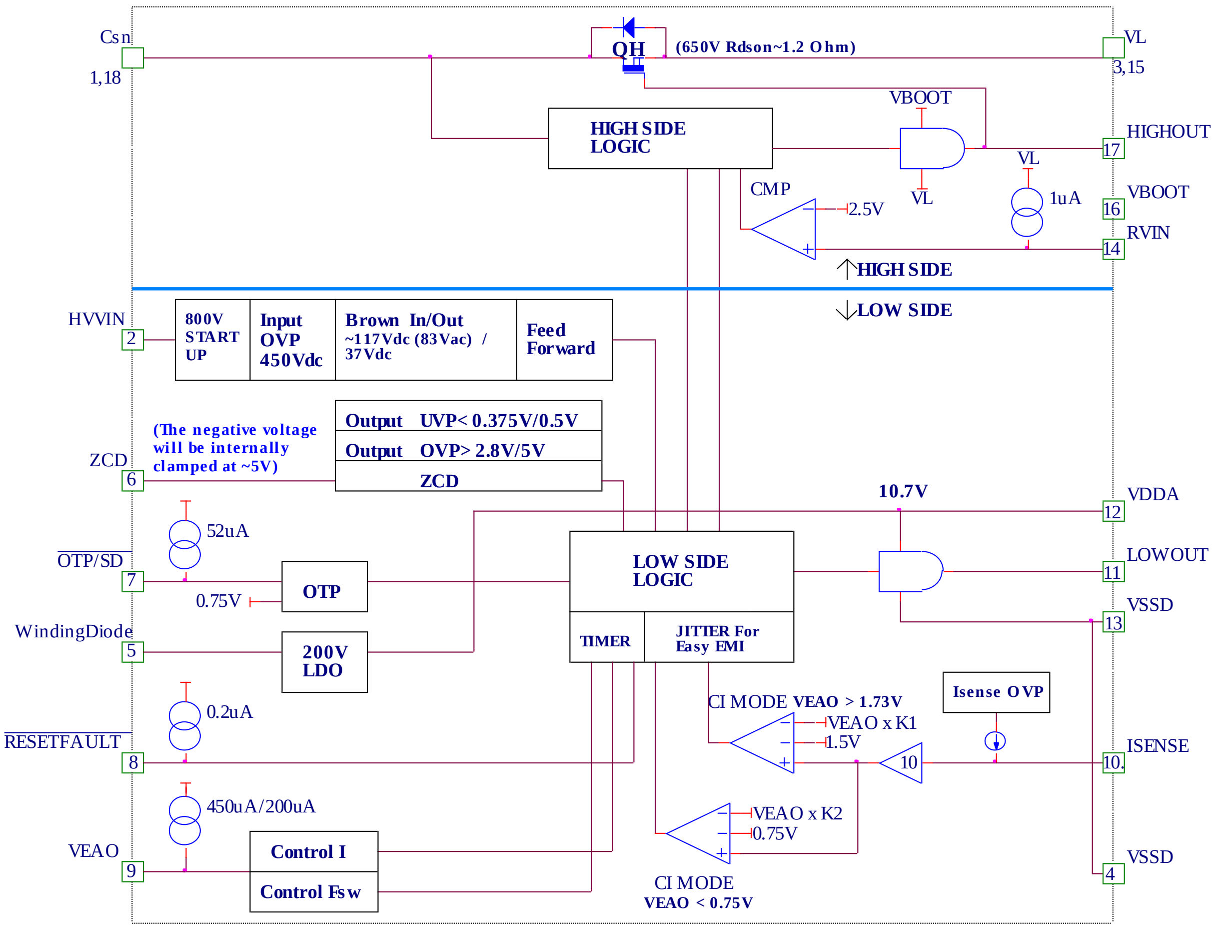
1. Patented (Both China and USA)
2. **Industry First Resonant Flyback**
3. **Almost Always ZVS** for both switches
4. f_{sw} V_{EAO}-clamped Options (@V_{EAO}=2.0V): for switching frequency optimization in light load mode (default: 89kHz). **For other frequency selection or adjustment, please consult with Champion FAEs**
5. **Optimal Efficiency and Power Density** for Flyback power system with minimum components (~60 total components for USB Type-C PD AC Adapter)
6. ~2% Additional Efficiency Improvement: (Efficiency of **Dr. Flyback™** system − Efficiency of QR Flyback system) ~2% @ same test condition
7. η ~> **95%⁺**, the highest Efficiency Flyback Power Supply with **Dr. Flyback™**, Dr. Bridge, Dr. SR and CM02
8. Lossless Snubber without snubber resistor; only $C_{snubber}$ (C_{sn}): Typical C_{sn} < 2nF
9. **Kick Mode** when V_{EAO} < 0.5V/0.75V for super light load
10. Power Supply Application Range from 10W to 150W
11. Typical No Load Input Power Consumption < **30mW @Vin = 230Vac @Vo=5V**
12. Internal Jitter for easy EMI design
13. Internal 200V LDO with ~10.7V VDDA, LDO output
14. Protections:
    A. **Input-O.V.P** ~450Vdc (318Vac):
    When Input > 450Vdc, Dr. Flyback™ stops and when Input < 450Vdc, Dr. Flyback™ runs immediately.
    B. **Brown In/Out** ~117Vdc(83Vac)/37Vdc(bulk cap voltage)
    C. **Output-O.V.P with ZCD pin :**
    ZCD pin > 5V : Latch Mode
    ZCD pin >2.8V : Retry Mode(Default)
    D. **Output-U.V.P with ZCD pin**: Retry Mode
    After V_{EAO} > 2.75V and Internal Timer > 4~10mS ($1/f_{sw}$) (~900 cycles) timer delay for **Output-U.V.P**: Retry Mode
    ZCDSHORT threshold = 0.375V, when VDDA < ~13.0V
    ZCDSHORT threshold = 0.50V, when VDDA > ~13.0V
    E. After V_{EAO} > 3.65V and internal Timer > ~30mS for **Peak Load protection**: Retry Mode
    F. VDDA: **VDDA O.V.P** = 27.5V: Retry Mode
    G. VDDA: **UVLO-on** ~21V, **UVLO-off** ~7.5V
    H. $\overline{\text{OTP/SD}}$ with 0.75V threshold and internal pull up 52uA with external thermistor: Retry Mode;
    Type-C PD IC or Secondary-Side any protections can use a Photocoupler to pull down $\overline{\text{OTP/SD}}$ pin
    I. **Second Internal OTP** ~150°C/130°C: Retry Mode
    J. **Isense OVP : Isense pin > 0.5V :** Latch Mode
15. Regulation:
    SSR, Secondary Side Regulation: with TL431 and with Photocoupler: **Dr. Flyback™** provides 450uA at V_{EAO} pin. Redundant OVP is possible through $\overline{\text{OTP/SD}}$ pin
16. Typical R_{SENSE} can be a 0.25W power dissipation resistor for AC Adapter

PIN CONFIGURATION

High Voltage 18-pin (TSSOP) TOP View
Q_H : 650V/4A SJMOS, $R_{DS(on)}$ typ. =1.2Ω



SIMPLIFIED BLOCK DIAGRAM



Note: Q_H: 650V/4A SJMOS, $R_{DS(on)}$ typ.=1.2Ω

Product and Packing Information

Part No.	Protection Function	Package Type	Packing Type	Marking
DRFLYBACK-A	All Retry	TSSOP-18L	2500 pcs / 13" reel	Dr.Flyback JPSAxxx
DRFLYBACK-B	All Latch	TSSOP-18L	2500 pcs / 13" reel	Dr.Flyback JPSBxxx

Note :

Clamped Frequency LL: Low Line HL: High Line		
LL	Heavy Load CRM	no clamping
	Light Load DCM	89kHz@V_{EAO}=2V
HL	Heavy Load CRM	no clamping
	Light Load DCM	89kHz@V_{EAO}=2V

PIN DESCRIPTION

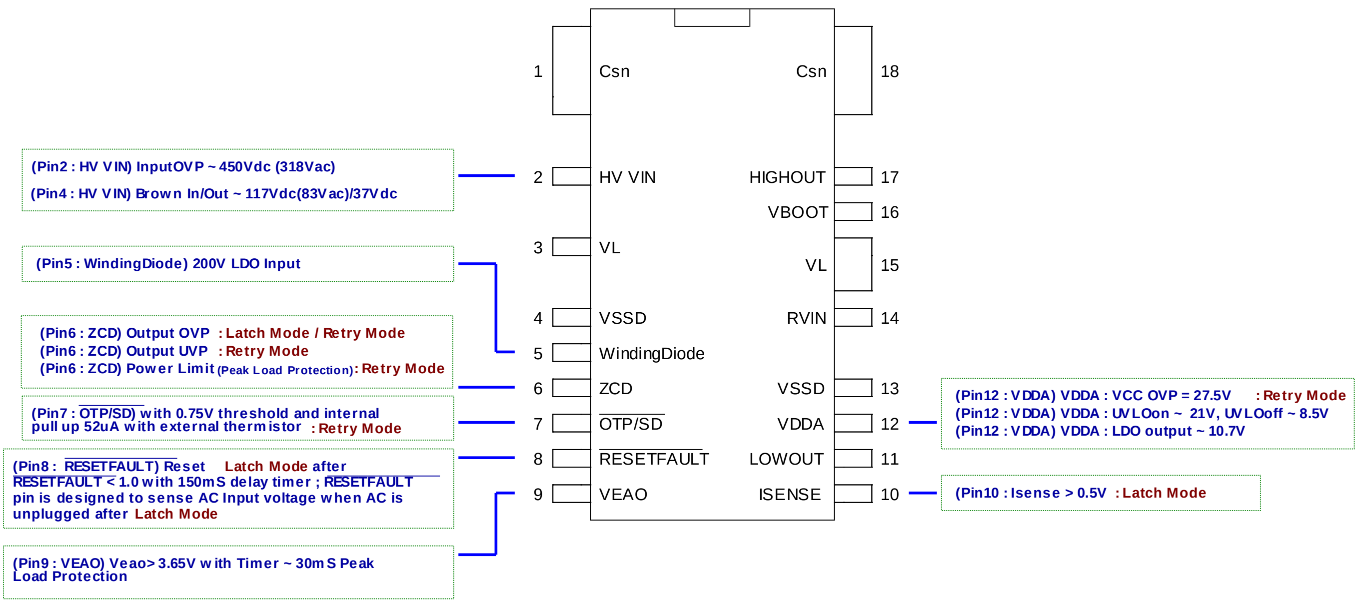
Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1, 18	C_{sn}	C_{sn} pin, High Side 650V/4A 1.2Ω SJMOS Drain and it needs to connected to the external C_{sn}	-0.5+V_L	-	650+V_L	V
2	HV VIN	Input Startup, Input OVP (V_{th}~450V), Brown In/Out (V_{th}=117Vdc(83Vac)/37Vdc), Feed forward	0	-	550	V
3, 15	V_L	High Side IC GND pin and Low Side Power Mosfet Drain pin	-0.5	-	650	V
4, 13	VSSD	Low Side IC GND pin				V
5	WindingDiode	LDO Input pin	-	-	200	V
6	ZCD	ZCD; Valley Detect; Output OVP (V_{th}=2.75V), Output UVP (V_{th}=0.375V or 0.75V determined by VDDA)	-5	-	5	V
7	$\overline{\text{OTP/SD}}$	It can source 52uA; $\overline{\text{OTP/SD}}$ voltage level <0.75V, it goes to RetryMode	0	-	5	V
8	$\overline{\text{RESETFAULT}}$	After going LatchMode, by letting $\overline{\text{RESETFAULT}}$ <1.0V, it resets Fault state and the system restarts itself again (from AC remove).	0	-	5	V
9	V_{EAO}	Either PSR/SSR, V_{EAO} is the compensation location and it is an error amplifier output and it is like a GM, transconductance amplifier output.	0	-	5	V
10	ISENSE	It sense R_{SENSE} voltage peak	-0.3	-	1	V
11	LOWOUT	Low Side Gate Drive Output pin	-0.3	-	VDDA+0.3	V
12	VDDA	Low Side IC supply pin	7	-	27.5	V
14	R_{VIN}	An external resistor connected between R_{VIN} and Vin (// C_{RVIN} option)	-0.3+V_L	-	6+V_L	V
16	V_{BOOT}	High Side IC supply pin	7+V_L	-	27+V_L	V
17	HIGHOUT	High Side Gate Drive Output pin	-0.3+V_L	-	0.3+V_{BOOT}+V_L	V

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

TSSOP Parameter	Min.	Max.	Units
C_{sn}, $C_{snubber}$ (pin 1, 18)	-1+V_L	650+V_L	V
HV VIN (pin 2)	-	800	V
V_L (pin 3, 15)	-	650	V
ZCD (pin 6)	-5	7	V
$\overline{\text{OTP/SD}}$ (pin 7), $\overline{\text{RESETFAULT}}$ (pin 8), V_{EAO} (pin 9), ISENSE (pin 10)	-	6	V
LOWOUT (pin 11)	VSSD-0.3	VDDA+0.3	V
LOWOUT (pin 11) (duration less than 25nS)	VSSD-3.0	VDDA+0.3	V
Peak LOWOUT (pin 11) Current Source or Sink	-	0.25	A
Peak LOWOUT (pin 11) Current Source or Sink (duration less than 5uS)	-	0.5	A
LOWOUT (pin 11), Energy Per Cycle	-	1.5	uJ
VDDA (pin 12)	-	29	V
R_{VIN} (pin 14)	-0.3+V_L	6+V_L	V
V_{BOOT} (pin 16)	-0.3+V_L	27+V_L	V
HIGHOUT (pin 17)	V_L-0.3	V_L+V_{BOOT}+0.3	V
Junction Temperature	-	150	°C
Storage Temperature Range	-65	150	°C
Operating Temperature Range	-40	125	°C
Lead Temperature (Soldering, 10 sec)	-	260	°C
Thermal Resistance (θ_{JA}) / Plastic 18 Pin (TSSOP)	-	33	°C/W
Case Temperature (θ_{JC}) / Plastic 18 Pin (TSSOP)	-	10	°C/W

TSSOP Protections (Fault State): RetryMode, LatchMode and $\overline{\text{RESETFAULT}}$ pins



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, T_A= 25°C (Note 1)

Symbol	Parameter	Test Conditions	Dr. Flyback™			Unit
			Min.	Typ.	Max.	
HIGHOUT						
PMOS	HIGHOUT is pulled high	-	-	-	60	Ω
NMOS	HIGHOUT is pulled low	-	-	-	10	Ω
C_{sn}						
$C_{sn,max}$	External Maximum C_{sn} value	Requirement to User 2nF	-	2	-	nF
R_{VIN} with external resistor						
$RVIN_H$	R_{VIN} Input Logic High	-	-	4-V_L	-	V
$RVIN_L$	R_{VIN} Input Logic Low	-	-	3-V_L	-	V
ZCD						
ZCD_{th}	Zero Crossing Detector	-	-	80	-	mV
O.V.P (Vo)	Output Over Voltage Protection	-	2.65	2.8	2.95	V
U.V.P (Vo)	Output Under Voltage Protection	when VDDA < ~13.0V	0.25	0.375	0.5	V
		when VDDA > ~13.0V	0.4	0.5	0.6	V
$\overline{\text{OTP/SD}}$						
I_{OTP}	OTP pin source current	-	49	52	55	uA
OTP	Over Temperature Threshold	-	0.6	0.75	0.9	V
$\overline{\text{RESETFAULT}}$						
RESETtime	Time to reset after Resetfaultb pin <1V	-	-	150	-	mS
$V_{Resetfaultb}$	-	-	-	1	-	V
V_{EAO}						
$V_{EAO,max}$	Maximum Effective V_{EAO}	-	3.75	-	4.25	V
At HIGHLINE 20V/15V mode, when VDDA > ~13.1V						
I_{veao} source 2.75V	Source Current	V_{EAO} > 2.75V	300	450	600	uA
I_{veao} source 1.73V	Source Current	V_{EAO} < 1.73V	100	200	300	uA
Power Limit	Peak Load Protection threshold	-	3.5	3.65	3.8	V
Mode Selection V_{th} (High)	Light Load threshold/ Fixed Current Mode	Sweep V_{EAO} from 0V to high until become High f_{sw}	2.6	2.75	2.9	V
Mode Selection V_{th} (Low)	Light Load threshold/ Fixed Current Mode	Sweep V_{EAO} from high to 0V until become Low f_{sw}	1.58	1.73	1.88	V
At HIGHLINE 3.3V/5V/9V/12V mode, when VDDA < ~13.0V						
I_{veao} source	Source Current	Veao < 1.75V	100	200	300	uA
Power Limit	Peak Load Protection threshold	-	2.35	2.5	2.65	V
Mode Selection (Kick) (High)	Voltage difference between two V_{EAO} voltage levels when Mode changed	Kick and change mode define (sweep V_{EAO} from 0V to high)	0.35	0.5	0.65	V
Mode Selection (Kick) (Low)	Voltage difference between two V_{EAO} voltage levels when Mode changed	Kick and change mode define (sweep V_{EAO} from high to 0V)	0.35	0.5	0.65	V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, T_A= 25°C (Note 1)

Symbol	Parameter	Test Conditions	Dr. Flyback™			Unit
			Min.	Typ.	Max.	
At LOWLINE						
I_{veao} source	Source Current	-	300	450	600	uA
Power Limit	Peak Load Protection threshold	-	3.5	3.65	3.8	V
LOWOUT						
PMOS	LOWOUT is pulled high	-	-	-	60	Ω
NMOS	LOWOUT is pulled low	-	-	-	10	Ω
VDDA						
UVLO-on	IC on threshold	-	19	20	21	V
UVLO-off	IC off threshold	-	6.5	7.5	8.5	V
VBOOT						
UVLO-on	IC on threshold	-	8.5	9.5	10.5	V
UVLO-off	IC off threshold	-	7	8	9	V
ISENSE						
Current Limit	At LOWLINE with VEAO=3.5V	-	0.20	-	0.25	V

Note 1: Limits are guaranteed by testing, or sampling with the test conditions above.

Part/N	Brand Name	Type	VDS (V)	VGS (V)	ID_TC (A)	RDS(ON) _Max. (Ω)	VGS(th)_Max. (V)	Ciss_Typ. (pF)	Coss_Typ. (pF)	Qg_Typ. (nC)	Qgs_Typ. (nC)	Qgd_Typ. (nC)	Trr_Typ. (ns)	Rg_Typ. (Ω)
					25℃	10V								(V)
CMS6504AN	Champion	N	650	20	4	1.25	4	333	20	11.6	6.72	1.16	191.9	24.45
CMS6515AN	Champion	N	650	20	15	0.33	4	698	36	16.4	6.0	4.3	308.0	3.56

Our Goals

Flyback Converter is the lowest-cost-offline power supply for power <150W application. **Dr. Flyback™** is designed to maintain the lowest cost while squeezing all possible energy to achieve the highest possible efficiency. By proper design with CM02, Dr. Bridge, **Dr. Flyback™**, and Dr. SR, **the total efficiency is approaching 95%** for a 15V/20V output 45W/65W AC Adapter (from our lab bench result with our demo board). By appropriating system design and operating switching frequency ~150KHz@High Line (~120KHz@Low Line) under full load, the power density is approaching 32.8W/in^3 (2W/cc).

Dr. Flyback™ is a Resonant Flyback

Dr. Flyback™ is a Resonant Flyback. Let us observe this equation: $0.5 \times L_m \times I_{Lm}^2 = 0.5 \times C_{vds(QL)} \times V_{ds}^2$ …… Eq1.
By observing the equation 1, if the initial energy of $0.5 \times C_{vds(QL)} \times V_{ds}^2$ is finite value, by switching $C_{vds(QL)}$ with different value of Capacitor, V_{ds} value can be different. As the results, the three switches in **Dr. Flyback™** system can be ZVS switching. The three switches of **Dr. Flyback™** are:

1. Main Flyback Switch at Bottom (Low Side), let us call it, Q_L
2. Change the snubber diode and let it become an integrated High Side Mosfet, let us call it, Q_H
3. Change the output diode and let it using Dr. SR, it is the third switch, and let us call it, Q_{SR}

Above three switches can be Almost Always ZVS in the system of **Dr. Flyback™**.

In the system of **Dr. Flyback™**, we recycle the energy of snubber capacitor (external capacitor), C_{sn} to achieve ZVS. **C_{sn} should be < 2nF for high switching frequency application.**

C_{sn} value is selected so $0.5 \times C_{sn} \times (N \times V_{OUT})^2 = 0.5 \times C_{vds(QL)} \times (380V)^2$ …… Eq2.
Typical C_{sn} =1nF~2nF for majority application. C_{sn} <2.4nF should be sufficient to cover majority application. If C_{sn} >2.4nF, it may limit the switching frequency of application.

Switching highest switching frequency f_{sw} with either Silicon Mosfet or GaN or SiC

Almost Always ZVS allows much higher switching frequency. When operating in heavy load mode, the maximum switching frequency of **Dr. Flyback™** is not clamped. The switching frequency depends entirely on the transformer design and overall system performance considerations. In addition, in order to optimize light load efficiency and system operation, **Dr. Flyback™** can be customized trimmed to the desired frequency (@V_{EAO}=2.0V) in light load mode (default is 89kHz). For other switching frequency selection or adjustment, please consult with Champion FAEs. On our demo board, the power Mosfets (High Side and Low Side) are Super Junction Mosfets (SJMOS). Therefore, if the application wants to use GaN or SiC, **Dr. Flyback™** is ready.

Almost Always ZVS

Almost Always ZVS is achieved by two independent controllers inside of **Dr. Flyback™**. As the results, the three switches of **Dr. Flyback™** System are Almost Always ZVS. The following pins allow you to tweak the sensibility of High Side On/Off edges:

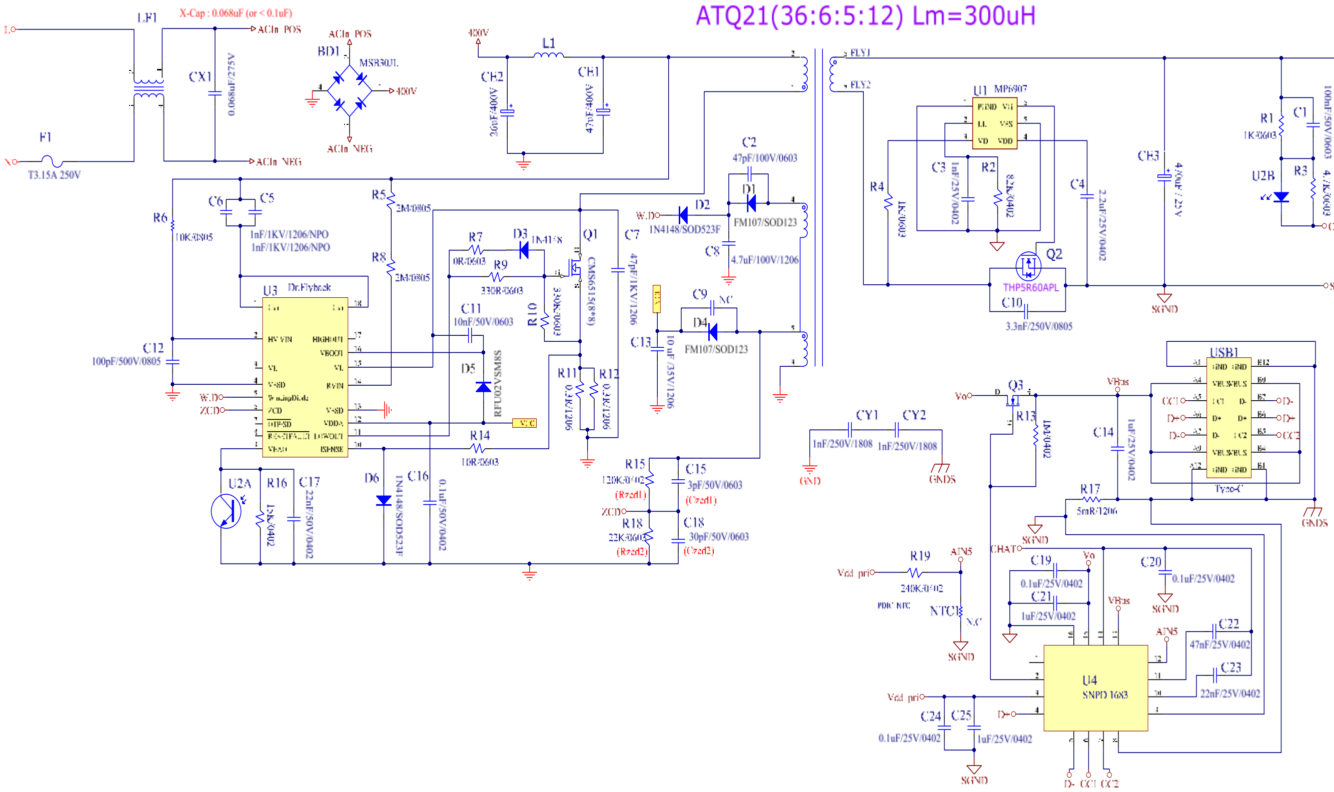
- **R_{VIN} : Sense V_L= Input Voltage: A R_{VIN} resistor with 1MΩ~10MΩ (tuning High Side Off edge)**
- **High Side Switch, Q_H Off Edge to squeeze out C_{sn} Energy:** R_{VIN} resistor, typical value should be 1MΩ~10MΩ. If R_{VIN} resistor value is higher, Q_H will be turned off at higher V_L voltage level. If R_{VIN} resistor value is lower, Q_H will be turned off at lower V_L voltage level

2. **ZCD : Delay Low Side Switch, Q_L On Edge: Naturally, V_L swings down, if Q_L is turned on too early, by adding a C_{zcd} around 10pF (option) it can shift Q_L on when V_L voltage level is near Zero voltage.**

   Rzcd2 and Czcd2 location must be near ZCD pin. Therefore, ZCD network layout is very important. ZCD pin waveforms must be in phase with V_L waveform. ZCD phase and V_L phase must be the same. ZCD is following V_L. ZCD is V_L/constant.

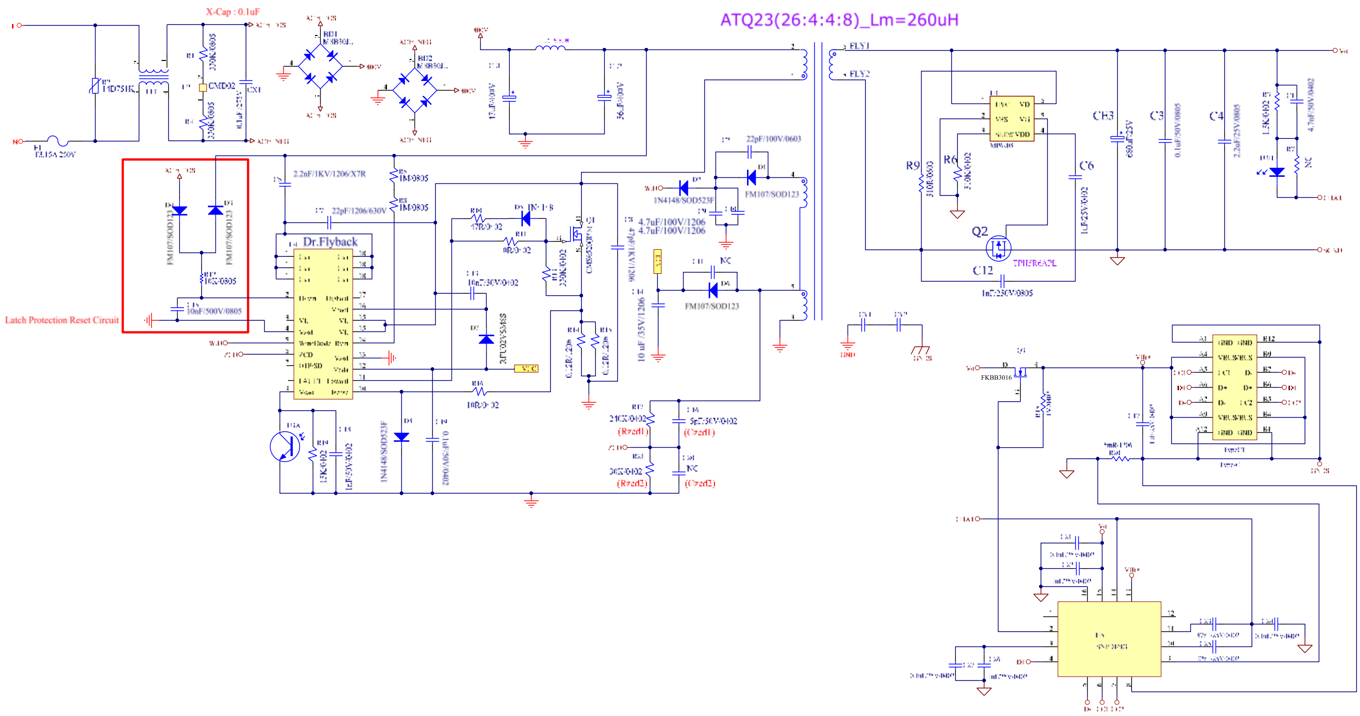
   ZCD flat region target voltage = 2.2V~2.5V

Dr. Flyback™ 45W USB-C PD APPLICATION CIRCUIT



Dr. Flyback™ 65W USB-C PD APPLICATION CIRCUIT

(with Latch Protection Reset Circuit)



Performance Data (45W PD Application)

115Vac/60Hz

115VAC/60Hz	20V	Efficiency					
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	20.22	0.225	5.301	85.82%	33-36
DCM	25%	20.24	0.563	12.5	91.08%	45-49
DCM	50%	20.25	1.125	24.6	92.61%	64-73
CRM	75%	20.26	1.688	36.75	93.03%	138-160
CRM	100%	20.32	2.250	49.03	93.25%	112-132
Avg 4 point Eff					92.49%	

115VAC/60Hz	15V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	15.18	0.3	5.19	87.75%	32-34
DCM	25%	15.2	0.750	12.42	91.79%	44-49
DCM	50%	15.23	1.500	24.56	93.02%	65-75
CRM	75%	15.27	2.250	36.77	93.44%	107-120
CRM	100%	15.3	3.000	49.2	93.29%	84-105
Avg 4 point Eff					92.88%	

115VAC/60Hz	9V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	9.07	0.3	3.125	87.07%	13
DCM	25%	9.1	0.750	7.53	90.64%	40
DCM	50%	9.13	1.500	14.83	92.35%	49-54
DCM	75%	9.16	2.250	22.22	92.75%	60-70
CRM/DCM	100%	9.2	3.000	29.7	92.93%	84/68
Avg 4 point Eff					92.17%	

115VAC/60Hz	5V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	5.04	0.3	1.747	86.55%	8
KICK	25%	5.07	0.750	4.243	89.62%	13
DCM	50%	5.12	1.500	8.437	91.03%	37-46
CRM/DCM	75%	5.15	2.250	12.64	91.67%	59/39-54
CRM/DCM	100%	5.2	3.000	16.935	92.12%	56/52
Avg 4 point Eff					91.11%	

230Vac/50Hz

230VAC/50Hz	20V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
DCM	10%	20.22	0.225	5.632	80.78%	30-34
DCM	25%	20.23	0.563	12.88	88.35%	48-52
DCM	50%	20.22	1.125	24.923	91.27%	62-71
CRM	75%	20.19	1.688	36.95	92.21%	167-177
CRM	100%	20.18	2.250	48.83	92.99%	148-155
Avg 4 point Eff					91.20%	

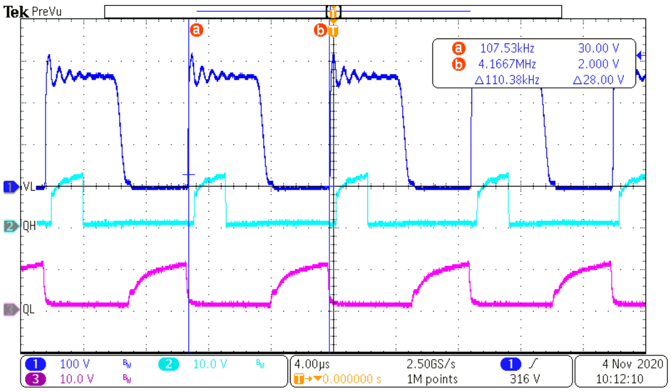
230VAC/50Hz	15V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	15.18	0.3	5.44	83.71%	11k/34
DCM	25%	15.2	0.750	12.822	88.91%	42-47
DCM	50%	15.21	1.500	24.96	91.41%	62-73
CRM	75%	15.14	2.250	36.77	92.64%	137
CRM	100%	15.08	3.000	48.76	92.78%	107-125
Avg 4 point Eff					91.44%	

230VAC/50Hz	9V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	9.07	0.3	3.285	82.83%	10-11
DCM	25%	9.1	0.750	7.938	85.98%	34-38
DCM	50%	9.13	1.500	15.29	89.57%	47-52
DCM	75%	9.16	2.250	22.68	90.87%	58-67
CRM/DCM	100%	9.2	3.000	30.15	91.54%	85/64
Avg 4 point Eff					89.49%	

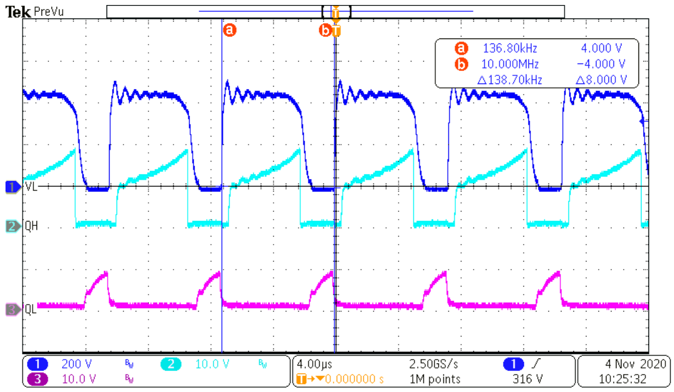
230VAC/50Hz	5V	Efficiency				
Mode	Load	Vout (Board end)	Iout	Pin	EFF (Board End)	Fsw(KHz)
KICK	10%	5.04	0.3	1.865	81.07%	6
KICK	25%	5.08	0.750	4.454	85.54%	12
KICK	50%	5.12	1.500	8.718	88.09%	12k/58
DCM	75%	5.15	2.250	13.12	88.32%	43
CRM/DCM	100%	5.2	3.000	17.46	89.35%	61/41-51
Avg 4 point Eff					87.83%	

No Load Consumption

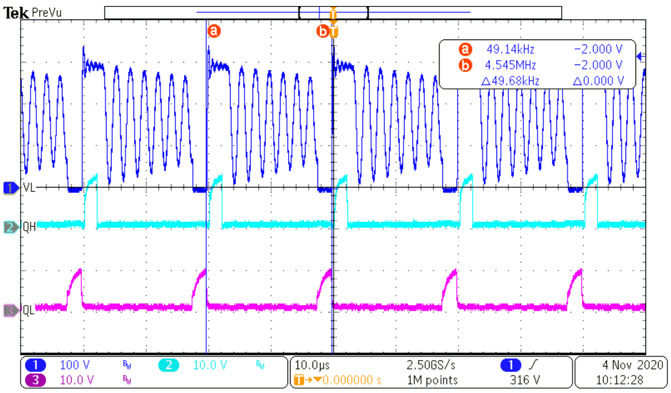
115Vac/60Hz @5Vout	230Vac/50Hz @5Vout
30mW	32mW



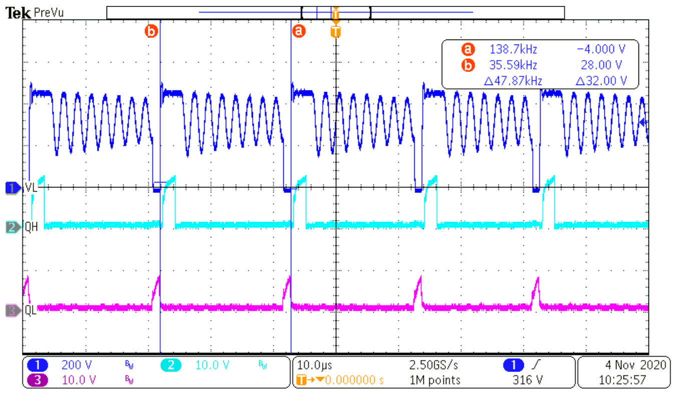
V_{in} = 115Vac/60Hz, 100% Load



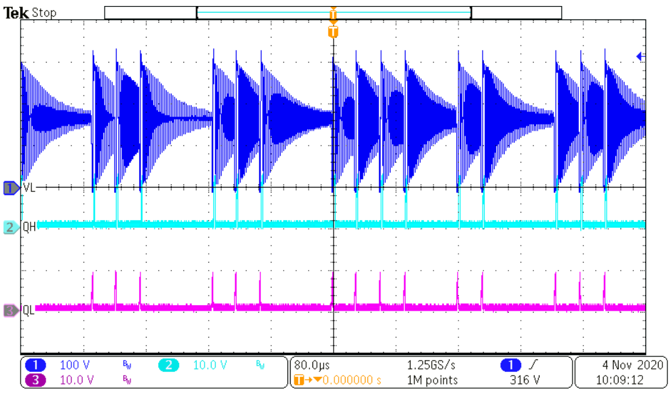
V_{in} = 230Vac/50Hz, 100% Load



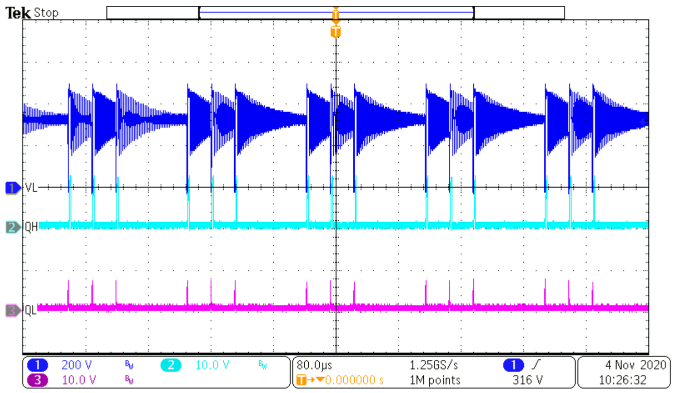
V_{in} = 115Vac/60Hz, 25% Load



V_{in} = 230Vac/50Hz, 25% Load



V_{in} = 115Vac/60Hz, 5% Load



V_{in} = 230Vac/50Hz, 5% Load

Performance Data (65W PD Application)

115Vac/60Hz

115Vac	20V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
DCM	10%	20.22	0.325	6.57	7.5	87.62%	44
DCM	25%	20.23	0.8125	16.44	17.88	91.93%	62
CRM/DCM	50%	20.22	1.625	32.86	35.34	92.98%	178/63
CRM	75%	20.24	2.438	49.34	52.78	93.47%	145
CRM	100%	20.28	3.250	65.91	70.53	93.45%	120
Avg 4 point Eff						92.96%	89.000%

115Vac	15V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
DCM	10%	15.18	0.3	4.55	5.225	87.16%	37
DCM	25%	15.21	0.75	11.41	12.45	91.63%	53
DCM	50%	15.23	1.5	22.85	24.6	92.87%	72
CRM	75%	15.24	2.250	34.29	36.78	93.23%	147
CRM	100%	15.3	3.000	45.90	49.09	93.50%	117
Avg 4 point Eff						92.81%	88.852%

115Vac	9V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
DCM	10%	9.14	0.3	2.74	3.182	86.17%	28
DCM	25%	9.17	0.75	6.88	7.572	90.83%	40
DCM	50%	9.2	1.5	13.80	14.93	92.43%	53
DCM	75%	9.26	2.250	20.84	22.42	92.93%	63
DCM	100%	9.27	3.000	27.81	29.9	93.01%	77
Avg 4 point Eff						92.30%	87.295%

115Vac	5V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
KICK	10%	5.05	0.3	1.52	1.765	85.84%	2.88/37
DCM	25%	5.08	0.75	3.81	4.3	88.60%	32
DCM	50%	5.12	1.5	7.68	8.465	90.73%	42
DCM	75%	5.17	2.250	11.63	12.71	91.52%	48
DCM	100%	5.22	3.000	15.66	17.05	91.85%	52
Avg 4 point Eff						90.68%	81.835%

230Vac/50Hz

230Vac	20V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
DCM	10%	20.22	0.325	6.57	7.806	84.19%	44
DCM	25%	20.18	0.8125	16.40	18.12	90.49%	76
CRM	50%	20.23	1.625	32.87	35.8	91.83%	226
CRM	75%	20.17	2.438	49.16	52.72	93.26%	192
CRM	100%	20.11	3.250	65.36	69.83	93.60%	156
Avg 4 point Eff						92.29%	89.000%

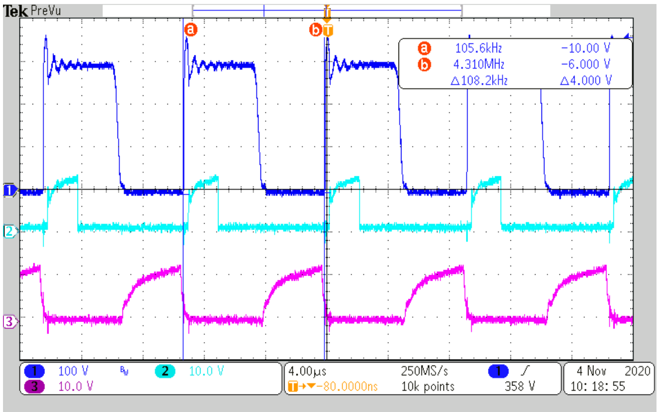
230Vac	15V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
DCM	10%	15.19	0.3	4.56	5.575	81.74%	43
DCM	25%	15.19	0.75	11.39	12.79	89.07%	52
DCM	50%	15.1	1.5	22.65	24.75	91.52%	89
CRM	75%	15.19	2.250	34.18	36.92	92.57%	178
CRM	100%	15.14	3.000	45.42	48.69	93.28%	150
Avg 4 point Eff						91.61%	88.852%

230Vac	9V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
KICK	10%	9.15	0.3	2.75	3.18	86.32%	KICK
KICK	25%	9.17	0.75	6.88	7.683	89.52%	KICK
DCM	50%	9.22	1.5	13.83	15.18	91.11%	31
DCM	75%	9.26	2.250	20.84	22.65	91.99%	38
DCM	100%	9.29	3.000	27.87	30.18	92.35%	50
Avg 4 point Eff						91.24%	87.295%

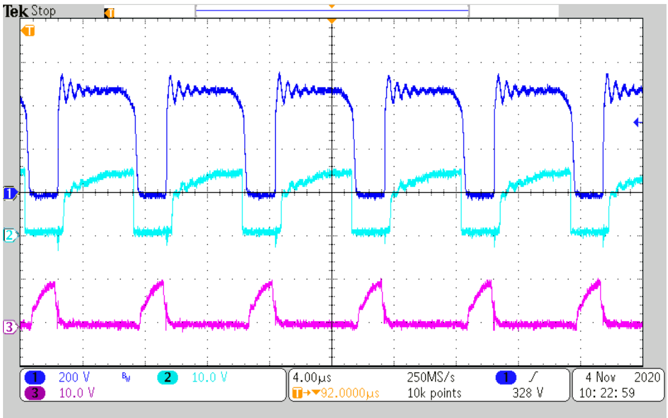
230Vac	5V	Efficiency					
Mode	Load	Vout	Iout	Pout	Pin	EFF	Fsw(KHz)
KICK	10%	5.061	0.3	1.52	1.84	82.52%	KICK
KICK	25%	5.091	0.75	3.82	4.351	87.76%	KICK
KICK	50%	5.133	1.5	7.70	8.63	89.22%	KICK
KICK	75%	5.164	2.250	11.62	12.95	89.72%	KICK
DCM	100%	5.22	3.000	15.66	17.38	90.10%	35
Avg 4 point Eff						89.20%	81.835%

No Load Consumption

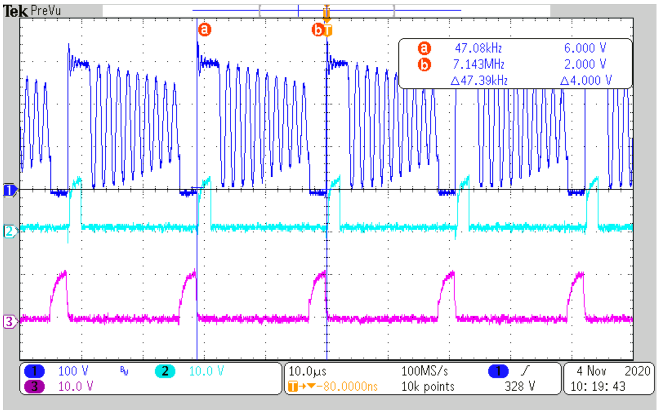
115Vac/60Hz @5Vout	230Vac/50Hz @5Vout
27mW	29mW



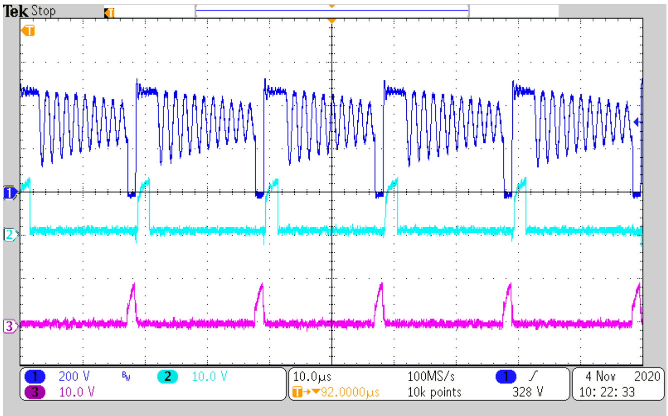
V_{in} = 115Vac/60Hz, 100% Load



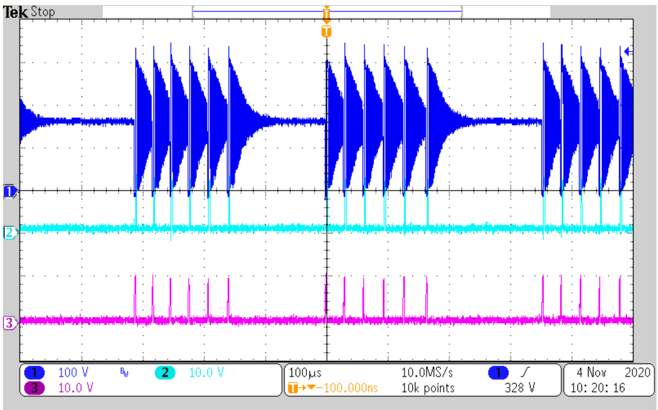
V_{in} = 230Vac/50Hz, 100% Load



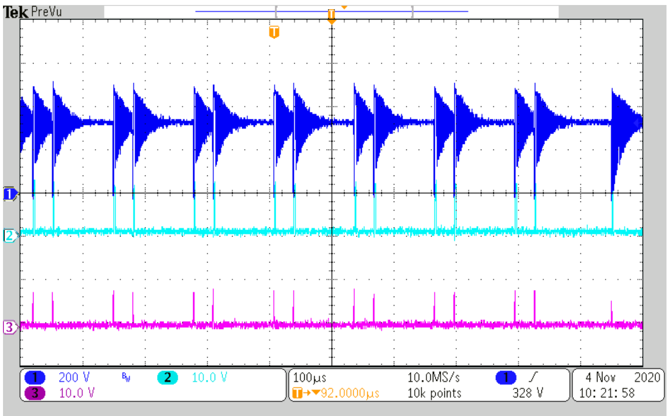
V_{in} = 115Vac/60Hz, 25% Load



V_{in} = 230Vac/50Hz, 25% Load

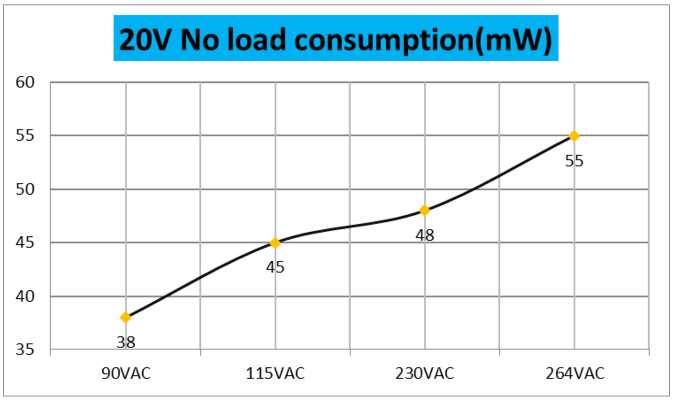


V_{in} = 115Vac/60Hz, 5% Load

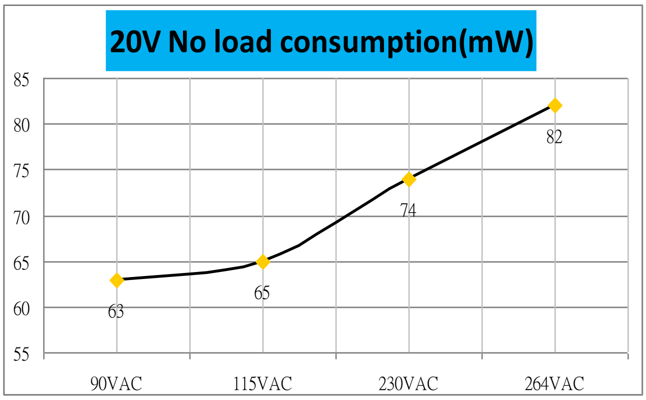


V_{in} = 230Vac/50Hz, 5% Load

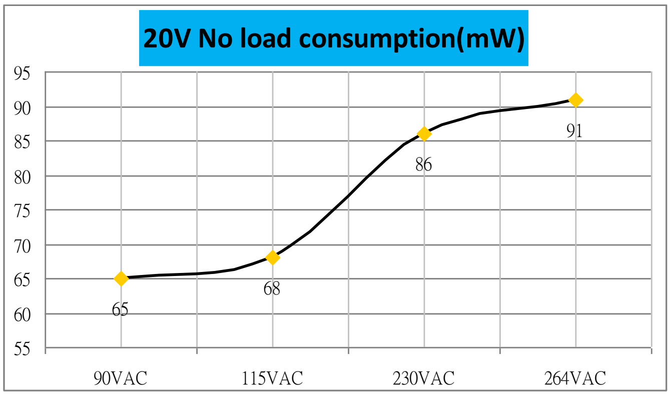
Dr. Flyback™ with SR_NO Load Power Consumption
(65W/20V Single Output without USB Type-C PD circuit)



Dr. Flyback™ with SR_NO Load Power Consumption (20V with USB Type-C PD circuit)

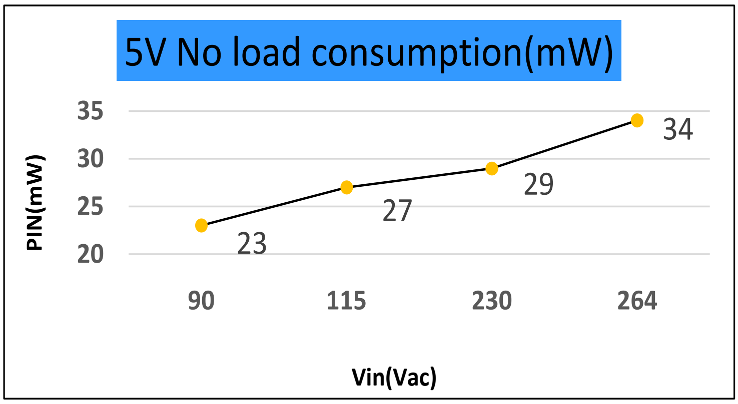


65W PD



45W PD

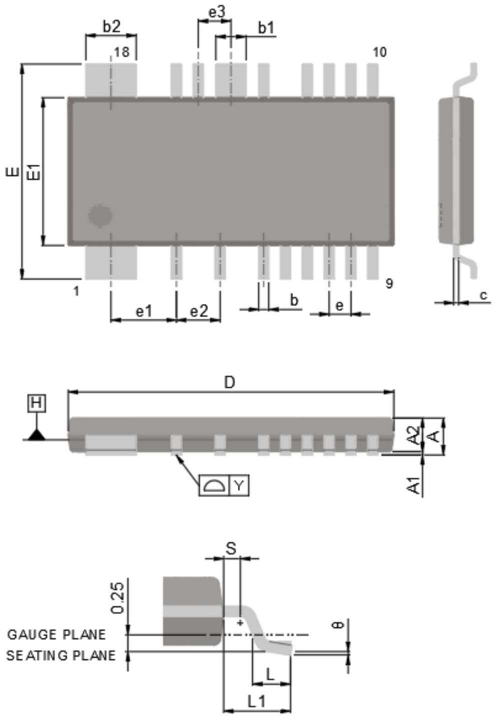
Dr. Flyback™ with SR _NO Load Power Consumption (65W/5V with USB Type-C PD circuit)



PACKAGE DIMENSION

TSSOP-18L Dimension

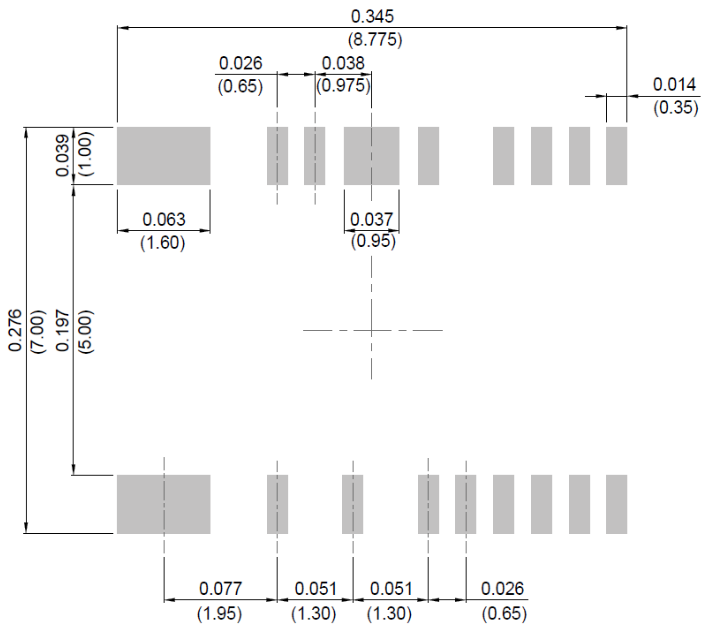
Unit: inch(mm)



TSSOP-18L Dimension.Unit:Inch (mm)				
Dim	Unit (inch)		Unit (mm)	
	Min	Max	Min	Max
A	-	0.047	-	1.20
A1	-	0.006	-	0.15
A2	0.031	0.041	0.80	1.05
b	0.007	0.012	0.19	0.30
b1	0.033	0.037	0.84	0.95
b2	0.059	0.063	1.49	1.60
c	0.004	0.008	0.09	0.20
D	0.378	0.386	9.60	9.80
E1	0.169	0.177	4.30	4.50
E	0.252 BSC.		6.40 BSC.	
e	0.026 BSC.		0.65 BSC.	
e1	0.077 BSC.		1.95 BSC.	
e2	0.051 BSC.		1.30 BSC.	
e3	0.038 BSC.		0.975 BSC.	
L1	0.039 BSC.		1.00 REF.	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
θ	0°	8°	0°	8°
Y	-		0.10	

TSSOP-18L Pad Layout

Unit: inch(mm)



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