

# MOSFET - Power, Single N-Channel, STD Gate, $\mu$ 8FL 40 V, 1.43 m $\Omega$ , 178 A

## NVTFWS1D3N04XM

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	40	V
Gate-to-Source Voltage	DC	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C = 25^{\circ}\text{C}$	$I_D$	178	A
	$T_C = 100^{\circ}\text{C}$		126	
Power Dissipation	$T_A = 25^{\circ}\text{C}$	$P_D$	83	W
Pulsed Drain Current	$T_C = 25^{\circ}\text{C}$ , $t_p = 10\text{ }\mu\text{s}$	$I_{DM}$	895	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)		$I_S$	71	A
Single Pulse Avalanche Energy ( $I_{LPK} = 17.2\text{ A}$ )		$E_{AS}$	281	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

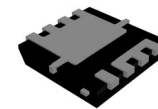
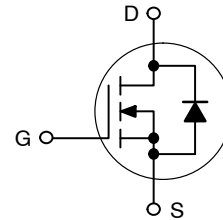
### THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	46.4	

1. Surface mounted on FR4 board using 650 mm<sup>2</sup>, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

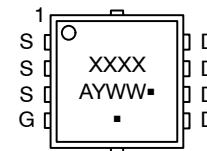
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
40 V	1.43 m $\Omega$ @ 10 V	178 A

### N-CHANNEL MOSFET



WDFNW8  
( $\mu$ 8FL)  
CASE 515AP

### MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NVTFWS1D3N04XM

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	40	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	I <sub>D</sub> = 1 mA, Referenced to 25°C	–	15	–	mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 25°C	–	–	1	μA
		V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125°C	–	–	100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	–	–	100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 25°C	–	1.24	1.43	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 90 μA, T <sub>J</sub> = 25°C	2.5	3	3.5	V
Gate Threshold Voltage Temperature Coefficient	ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 90 μA	–	–7.34	–	mV/°C
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 20 A	–	103	–	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz	–	2288	–	pF
Output Capacitance	C <sub>OSS</sub>		–	1449	–	
Reverse Transfer Capacitance	C <sub>RSS</sub>		–	22	–	
Total Gate Charge	Q <sub>G(tot)</sub>	V <sub>DD</sub> = 32 V, I <sub>D</sub> = 50 A, V <sub>GS</sub> = 10 V	–	36	–	nC
Threshold Gate Charge	Q <sub>G(th)</sub>		–	7	–	
Gate-to-Source Charge	Q <sub>GS</sub>		–	11	–	
Gate-to-Drain Charge	Q <sub>GD</sub>		–	7	–	
Gate Resistance	R <sub>G</sub>	f = 1 MHz	–	0.7	–	Ω

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 0/10 V, I <sub>D</sub> = 50 A, V <sub>DD</sub> = 32 V, R <sub>G</sub> = 0 Ω	–	21	–	ns
Rise Time	t <sub>r</sub>		–	8	–	
Turn-Off Delay Time	t <sub>d(off)</sub>		–	34	–	
Fall Time	t <sub>f</sub>		–	8	–	

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C	–	0.79	1.2	V
		I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C	–	0.64	–	
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A, di/dt = 100 A/μs, V <sub>DD</sub> = 32 V	–	48	–	ns
Charge Time	t <sub>a</sub>		–	20	–	
Discharge Time	t <sub>b</sub>		–	28	–	
Reverse Recovery Charge	Q <sub>RR</sub>		–	48	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

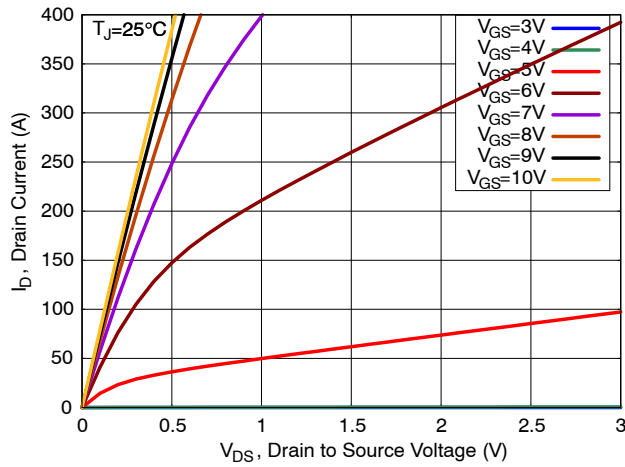


Figure 1. On-Region Characteristics

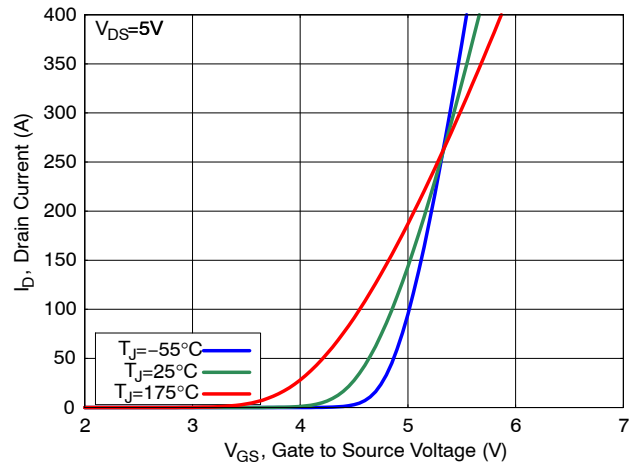


Figure 2. Transfer Characteristics

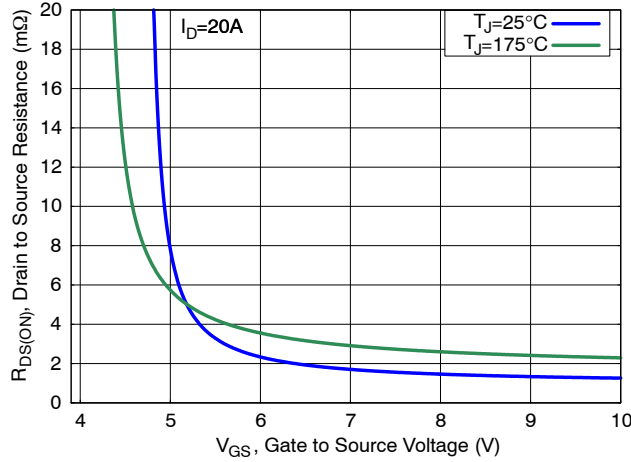


Figure 3. On-Resistance vs. Gate Voltage

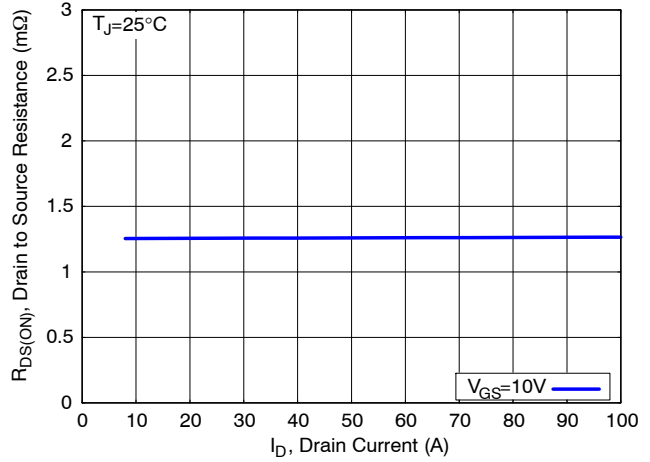


Figure 4. On-Resistance vs. Drain Current

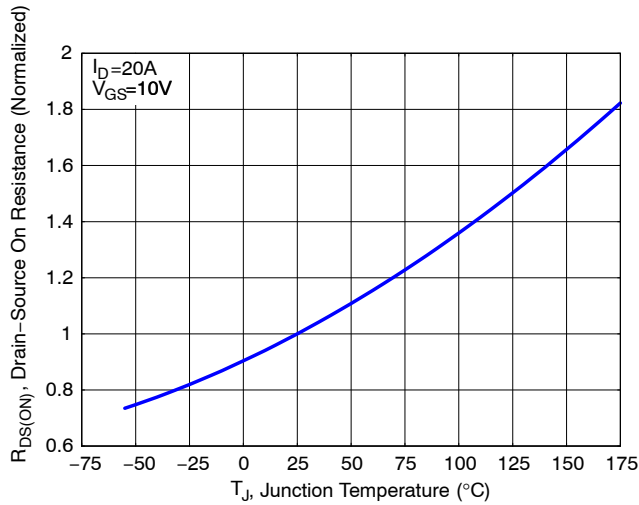


Figure 5. Normalized ON Resistance vs. Junction Temperature

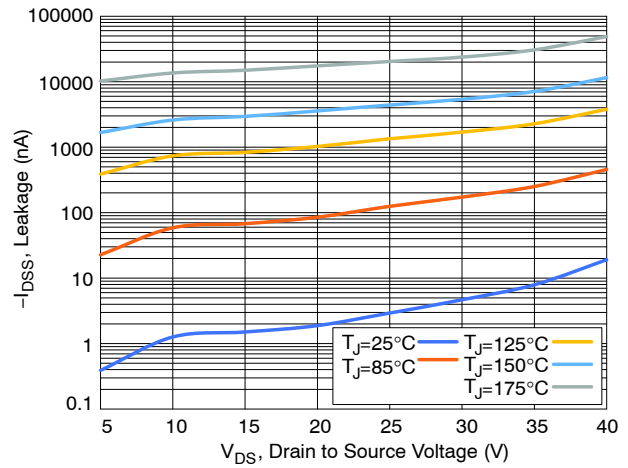


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

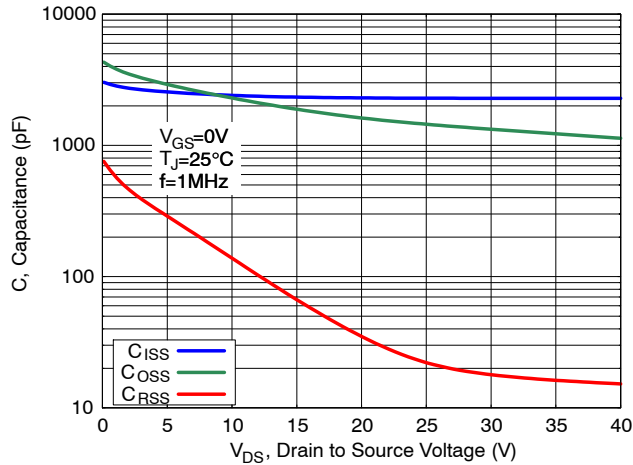


Figure 7. Capacitance Characteristics

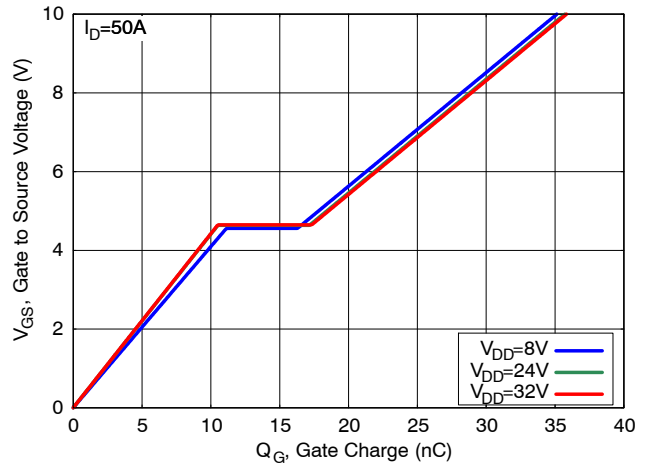


Figure 8. Gate Charge Characteristics

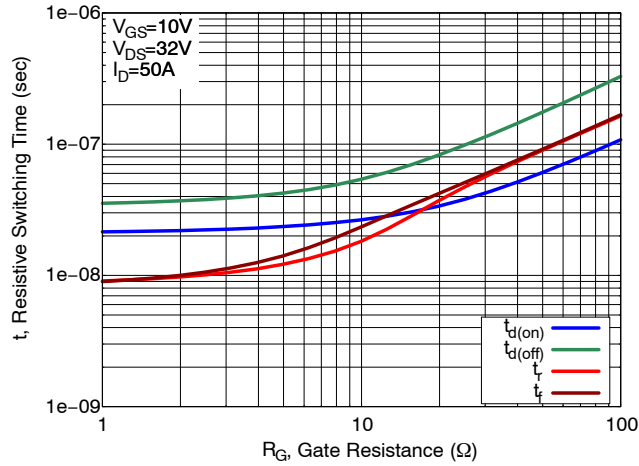


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

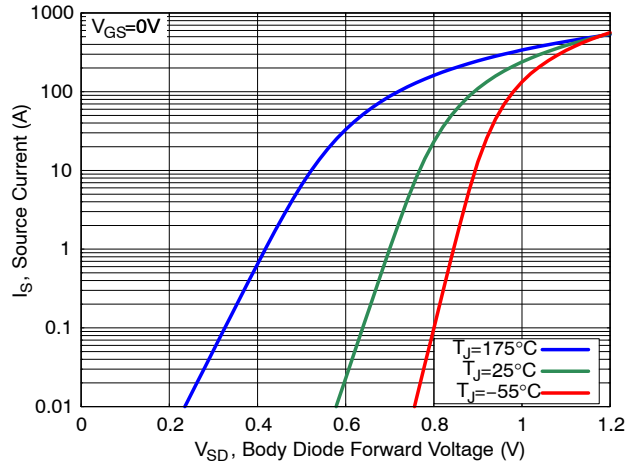


Figure 10. Diode Forward Characteristics

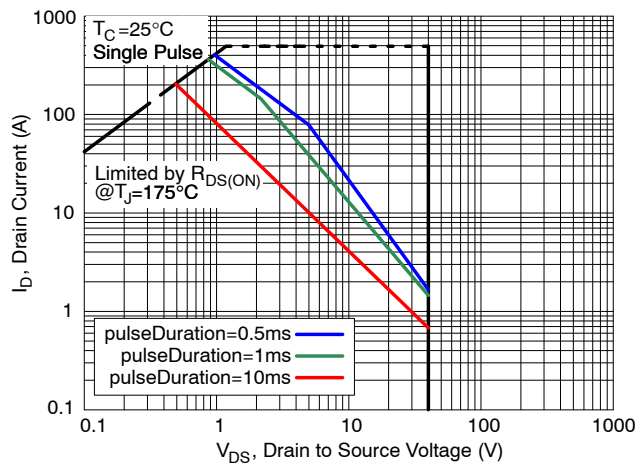


Figure 11. Safe Operating Area (SOA)

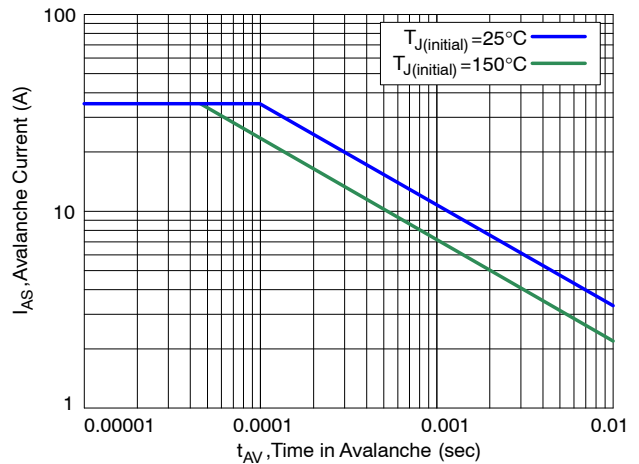


Figure 12. Avalanche Current vs. Pulse Time (UIS)

# NVTFWS1D3N04XM

## TYPICAL PERFORMANCE CHARACTERISTICS

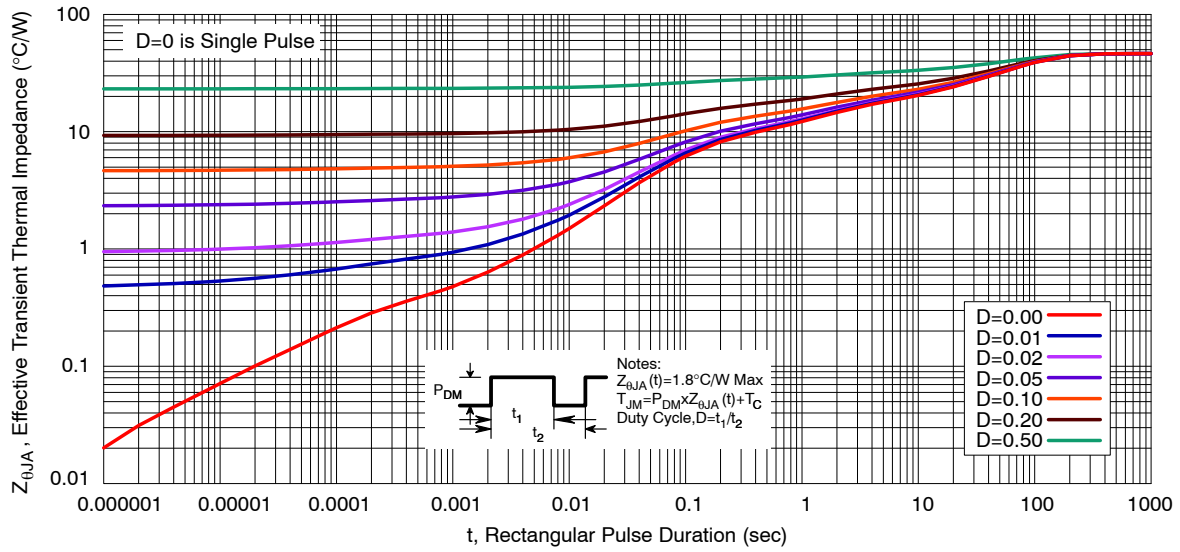
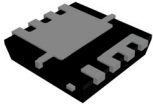


Figure 13. Transient Thermal Response

## PACKAGE MARKING AND ORDERING INFORMATION

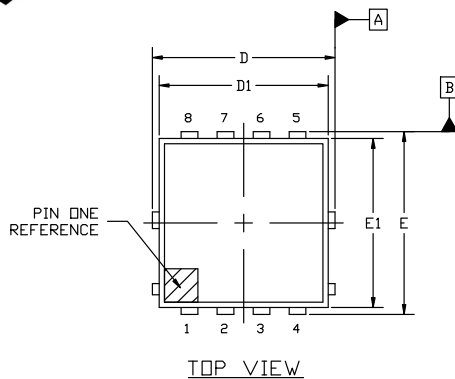
Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVTFWS1D3N04XMTAG	1D3W	WDFNW8	Tape & Reel	N/A	N/A	1500 Units


**WDFNW8 3.30x3.30x0.75, 0.65P**
**CASE 515AP**  
**ISSUE A**

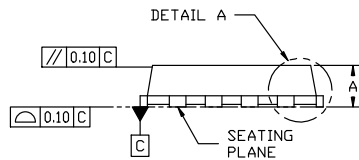
DATE 07 NOV 2023

## NOTES:

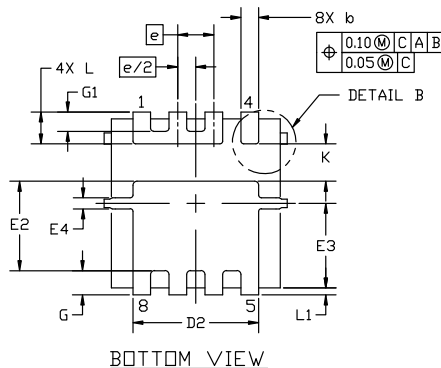
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. FULL-CUT u8FL FUSED WF.



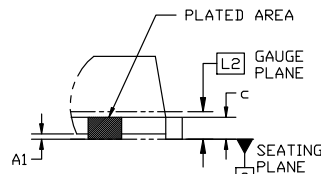
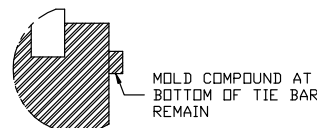
TOP VIEW



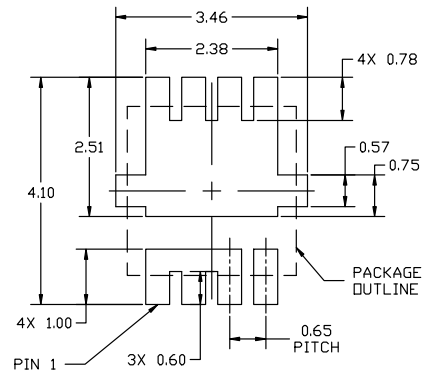
SIDE VIEW



BOTTOM VIEW

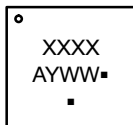

DETAIL "A"  
SCALE 2:1

DETAIL "B"  
SCALE 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	1.35	1.50	1.60
E4	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
L2	0.25 BSC		



## RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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