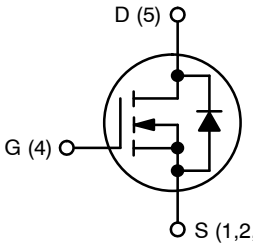
MOSFET - Power, Single N-Channel, STD Gate, SO8FL

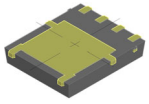
40 V, 3.9 mΩ, 80 A

NVMFWS4D0N04XM

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	3.9 mΩ @ 10 V	80 A



N−CHANNEL MOSFET



DFNW5 (SO−8FL)
CASE 507BA

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	40	V
Gate−to−Source Voltage	DC	V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	80	A
	T_C = 100°C		57	
Power Dissipation	T_C = 25°C	P_D	43	W
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs	I_D	450	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	59	A
Single Pulse Avalanche Energy (I_{PK} = 3.6 A)		E_{AS}	138	mJ
Lead Temperature for Soldering Purposes		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction−to−Ambient (Notes 1, 2)	$R_{\theta JA}$	42	

1. Surface−mounted on FR4 board using 650 mm^2, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA. Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, T_J = 25°C			1	μA
		V_{DS} = 40 V, T_J = 125°C			20	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 6 A, T_J = 25°C		3.4	3.9	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 30 μA, T_J = 25°C	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 30 μA		−7.36		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 6 A		32		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		784		pF
Output Capacitance	C_{OSS}			504		
Reverse Transfer Capacitance	C_{RSS}			10		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DD} = 32 V, I_D = 6 A		12		nC
Threshold Gate Charge	$Q_{G(TH)}$			2		
Gate−to−Source Charge	Q_{GS}			3		
Gate−to−Drain Charge	Q_{GD}			2		
Gate Resistance	R_G	f = 1 MHz		1.6		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 10 V, V_{DD} = 32 V, I_D = 6 A, R_G = 0 Ω		7		ns
Rise Time	t_r			8		
Turn−Off Delay Time	$t_{d(OFF)}$			10		
Fall Time	t_f			9		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 6 A, T_J = 25°C		0.78	1.2	V
		V_{GS} = 0 V, I_S = 6 A, T_J = 125°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 6 A, V_{DD} = 32 V		53		ns
Charge Time	t_a			9		
Discharge Time	t_b			44		
Reverse Recovery Charge	Q_{RR}			18		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

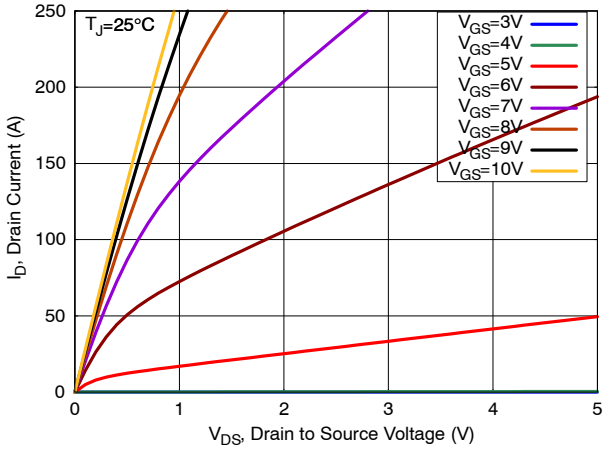


Figure 1. On−Region Characteristics

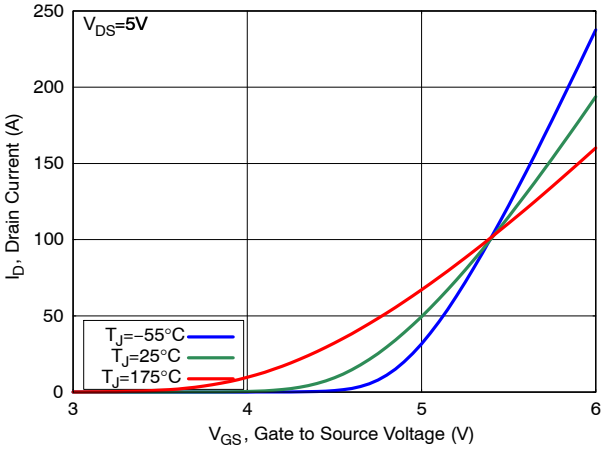


Figure 2. Transfer Characteristics

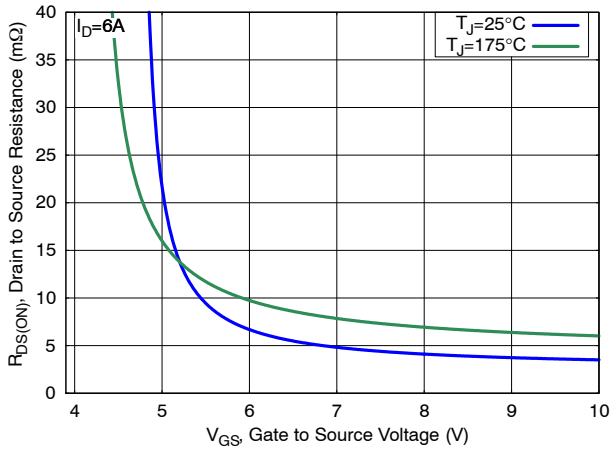


Figure 3. On−Resistance vs. Gate Voltage

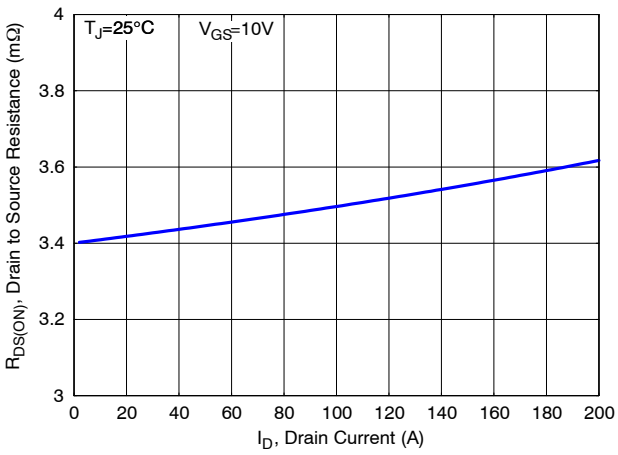


Figure 4. On−Resistance vs. Drain Current

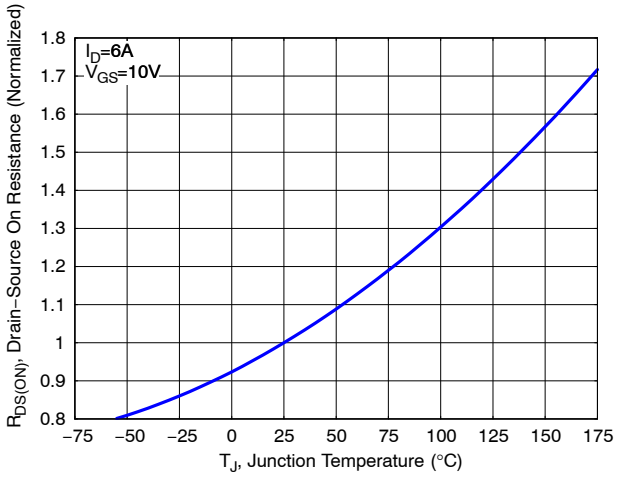


Figure 5. Normalized ON Resistance vs. Junction Temperature

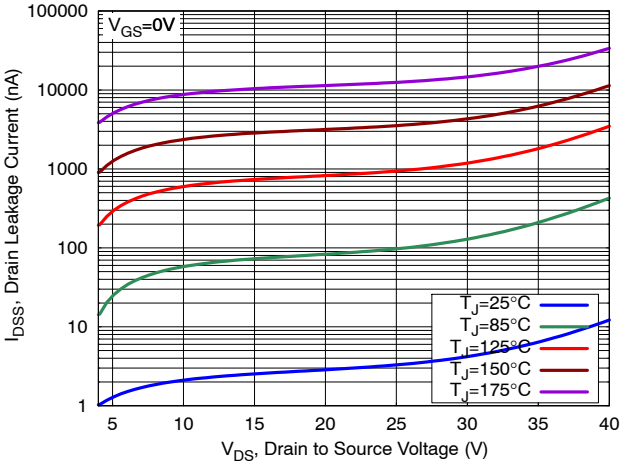


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS (continued)

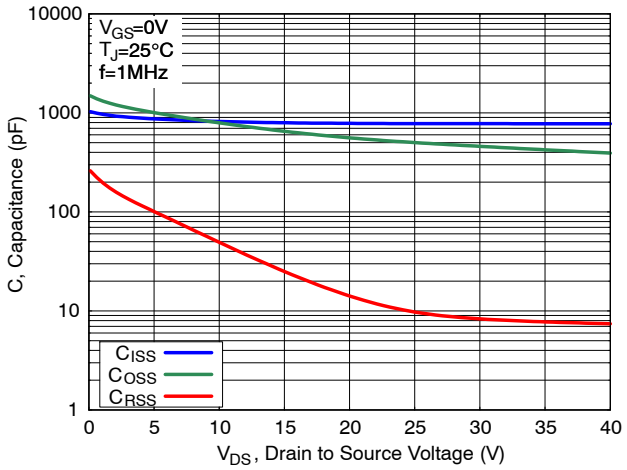


Figure 7. Capacitance Characteristics

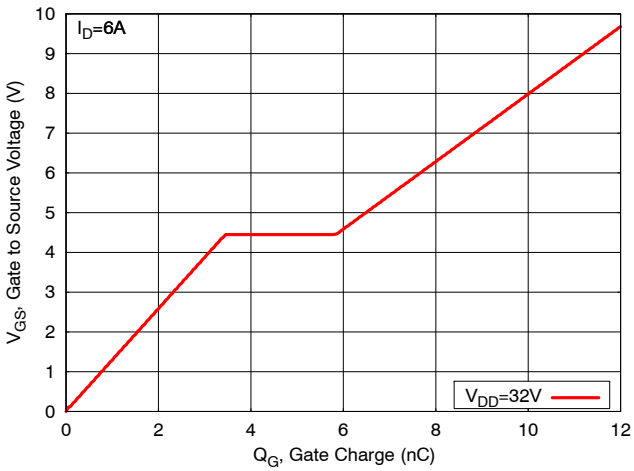


Figure 8. Gate Charge Characteristics

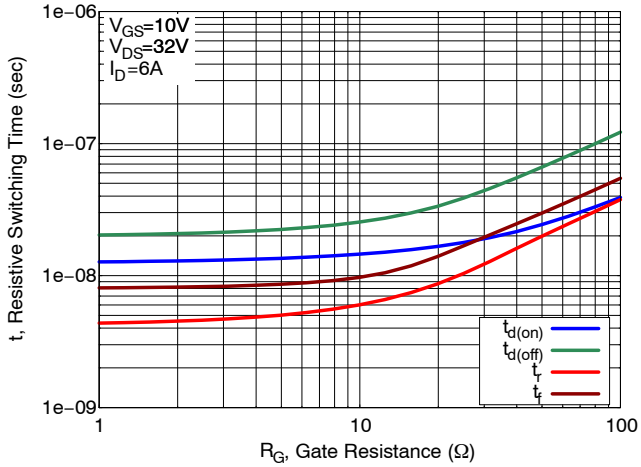


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

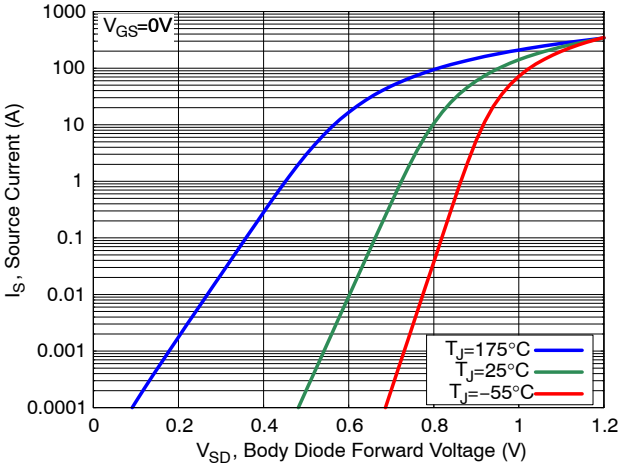


Figure 10. Diode Forward Characteristics

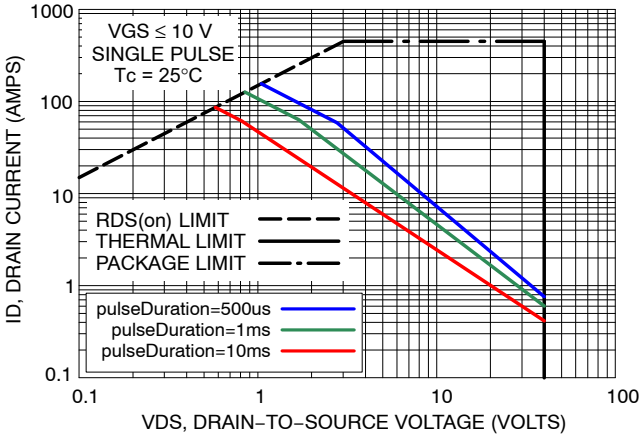


Figure 11. Maximum Rated Forward Biased Safe Operating Area

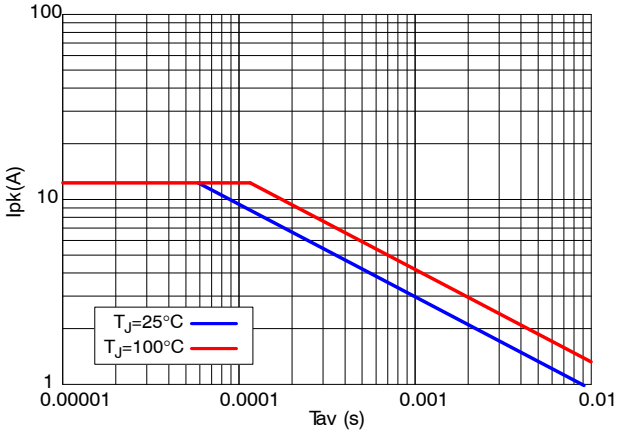


Figure 12. Ipeak vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

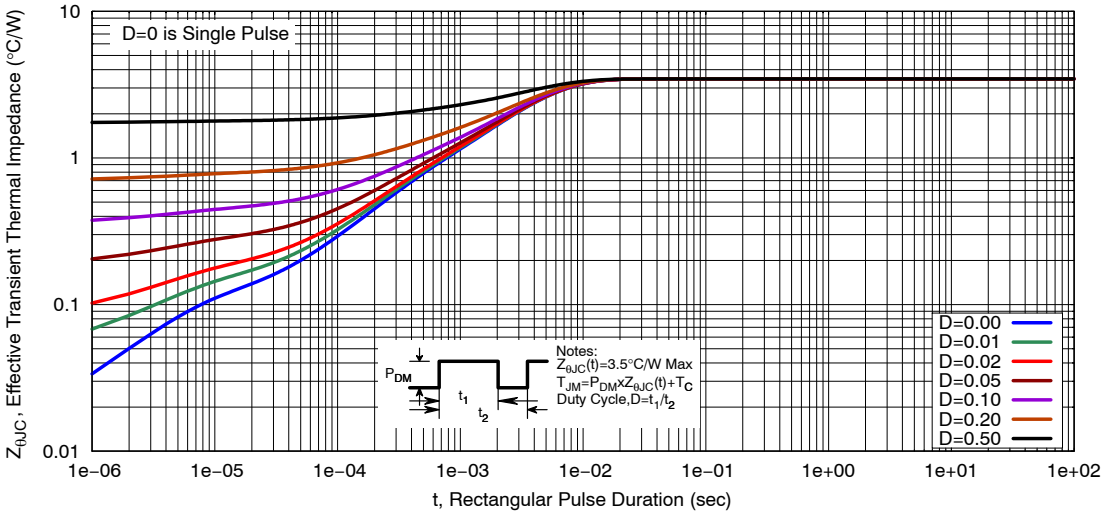


Figure 13. Transient Thermal Response

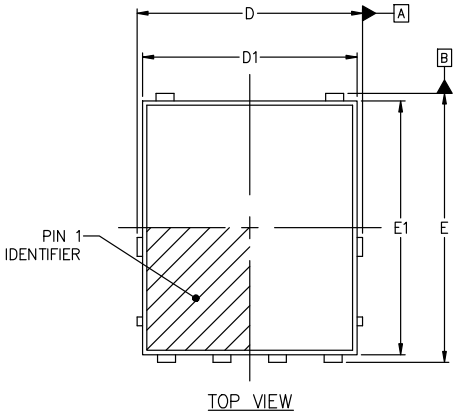
DEVICE ORDERING INFORMATION

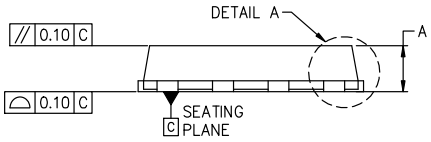
Device	Marking	Package	Shipping†
NVMFWS4D0N04XMT1G	4D0N4W	DFNW5 (Pb−Free)	1500 / Tape & Reel

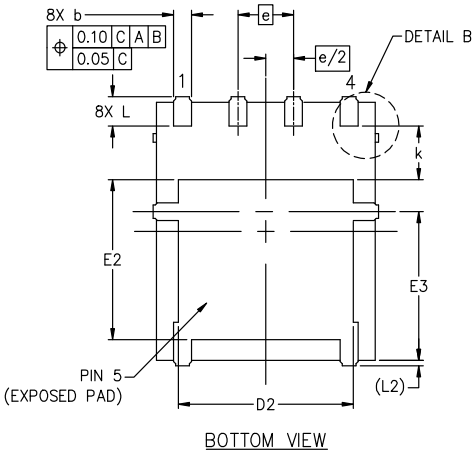
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

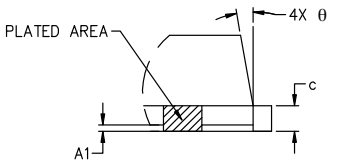


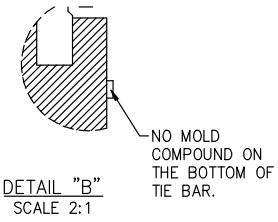




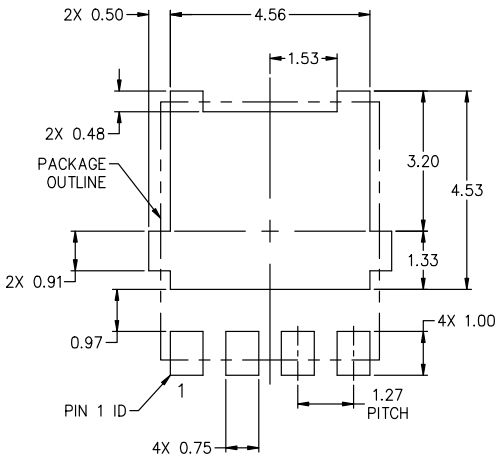
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.





DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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