

# MOSFET - Power, Single N-Channel STD Gate, SO8FL

## 80 V, 3 mΩ, 135 A **NVMFWS3D0N08X**

#### **Features**

- Low Q<sub>RR</sub>, Soft Recovery Body Diode
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	80	V
Gate-to-Source Voltage		$V_{GS}$	±20	V
Continuous Drain Current	T <sub>C</sub> = 25°C	I <sub>D</sub>	135	Α
(Note 1)	T <sub>C</sub> = 100°C		96	
Power Dissipation (Note 1)	T <sub>C</sub> = 25°C	$P_{D}$	119	W
Pulsed Drain Current	T <sub>C</sub> = 25°C,	I <sub>DM</sub>	543	Α
Pulsed Source Current (Body Diode)	t <sub>p</sub> = 100 μs	I <sub>SM</sub>	543	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +175	°C
Source Current (Body Diode)		I <sub>S</sub>	179	Α
Single Pulse Avalanche Energy (I <sub>PK</sub> = 47 A) (Note 2)		E <sub>AS</sub>	110	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C

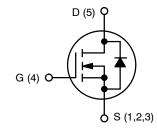
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.

1

3.  $E_{AS}$  of 110 mJ is based on started  $T_J$  = 25°C,  $I_{AS}$  = 55 A,  $V_{DD}$  = 64 V,  $V_{GS}$  =10 V, 100% avalanche tested.

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	3 mΩ @ 10 V	135 A



**N-CHANNEL MOSFET** 



DFNW5 (SO-8FL) CASE 507BA

3D0N8W AYWZZ

3D0N8W = Specific Device Code A = Assembly Location

Y = Year
W = Work Week
ZZ = Assembly Lot Code

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 3 of this data sheet.

#### THERMAL CHARACTERISTICS

Parameter		Value	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	1.26	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

<sup>4.</sup> Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz. Cu pad.
5. R<sub>thJA</sub> is determined by the user's board design.

#### **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•	•		
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/$ $\Delta T_J$	I <sub>D</sub> = 1 mA, Referenced to 25°C		31.6		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 25°C			1	μΑ
		V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 31 \text{ A}$		2.6	3.0	mΩ
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 153 \mu A$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/$ $\Delta T_J$	$V_{GS} = V_{DS}$ , $I_D = 153 \mu A$		-7.5		mV/°C
Forward Transconductance	9FS	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 31 A		97		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE				•	
Input Capacitance	C <sub>ISS</sub>			2680		pF
Output Capacitance	C <sub>OSS</sub>			780		
Reverse Transfer Capacitance	C <sub>RSS</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}, f = 1 \text{ MHz}$		12		•
Output Charge	Q <sub>OSS</sub>			56		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 6 V, V <sub>DD</sub> = 40 V, I <sub>D</sub> = 31 A		23		
				38		
Threshold Gate Charge	Q <sub>G(TH)</sub>			7		
Gate-to-Source Charge	$Q_GS$	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 40 V, I <sub>D</sub> = 31 A		13		
Gate-to-Drain Charge	$Q_{GD}$			6		
Gate Plateau Voltage	$V_{GP}$			4.7		V
Gate Resistance	$R_{G}$	f = 1 MHz		0.7		Ω
SWITCHING CHARACTERISTICS			•	•	•	•
Turn-On Delay Time	t <sub>d(ON)</sub>			22		ns
Rise Time	t <sub>r</sub>	t <sub>r</sub> Resistive Load,		8		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$V_{GS}$ = 0/10 V, $V_{DD}$ = 64 V, $I_{D}$ = 31 A, $R_{G}$ = 2.5 $\Omega$		33		1
Fall Time	t <sub>f</sub>			5		1
SOURCE-TO-DRAIN DIODE CHARACTE	ERISTICS		-	<u>-</u>	-	-
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = 31 \text{ A}, T_J = 25^{\circ}\text{C}$		0.82	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 31 A, T <sub>J</sub> = 125°C		0.66	† †	1

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERIS	TICS					
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dl/dt = 1000 A/us,		22		ns
Charge Time	t <sub>a</sub>			13		
Discharge Time	t <sub>b</sub>	$V_{GS} = 0 \text{ V, dI/dt} = 1000 \text{ A/}\mu\text{s,}$ $I_{S} = 31 \text{ A, V}_{DD} = 64 \text{ V}$		9		
Reverse Recovery Charge	$Q_{RR}$			150		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NVMFWS3D0N08XT1G	3D0N8W	DFNW5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **TYPICAL CHARACTERISTICS**

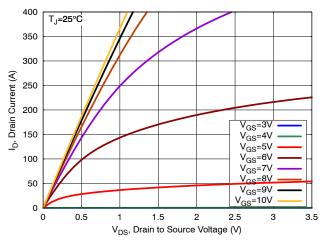


Figure 1. On-Region Characteristics

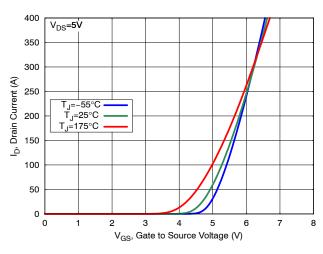


Figure 2. Transfer Characteristics

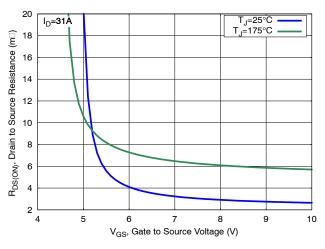


Figure 3. On-Resistance vs. Gate Voltage

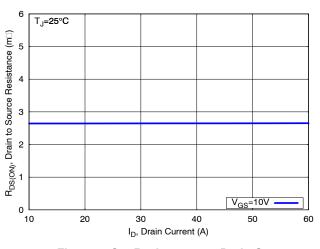


Figure 4. On-Resistance vs. Drain Current

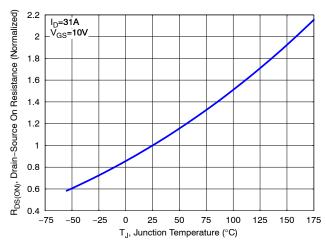


Figure 5. Normalized ON Resistance vs. Junction Temperature

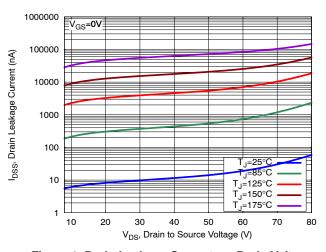


Figure 6. Drain Leakage Current vs. Drain Voltage

#### **TYPICAL CHARACTERISTICS**

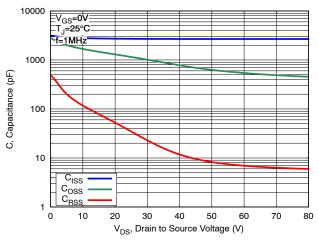


Figure 7. Capacitance Characteristics

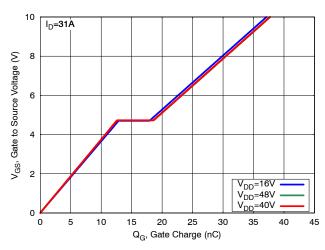


Figure 8. Gate Charge Characteristics

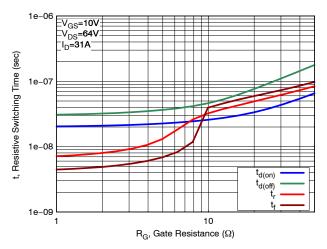


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

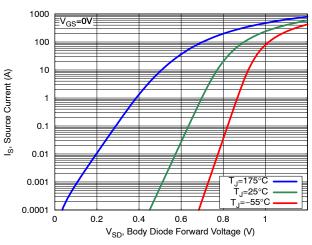


Figure 10. Diode Forward Characteristics

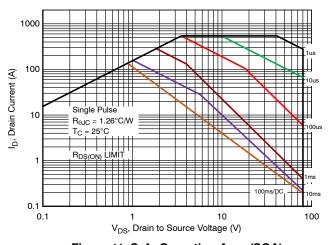


Figure 11. Safe Operating Area (SOA)

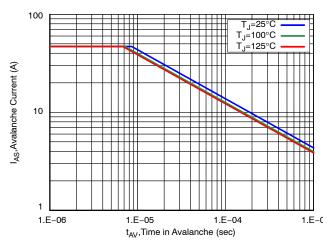
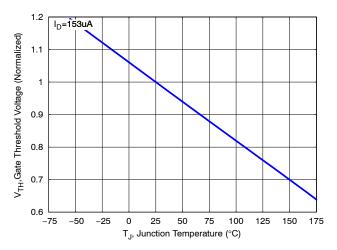


Figure 12. Avalanche Current vs Pulse Time (UIS)

#### **TYPICAL CHARACTERISTICS**



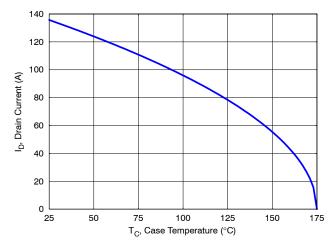


Figure 13. Gate Threshold Voltage vs Junction Temperature

Figure 14. Maximum Current vs. Case Temperature

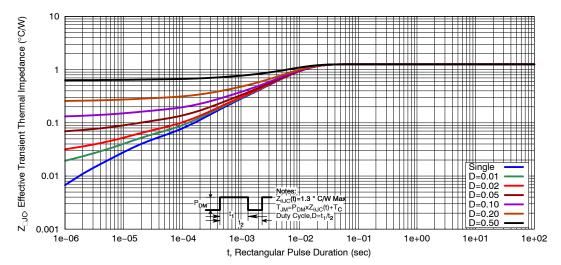
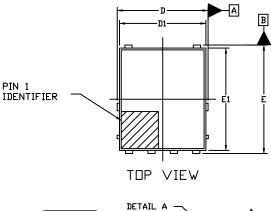


Figure 15. Transient Thermal Response

#### PACKAGE DIMENSIONS

#### DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA **ISSUE A** 

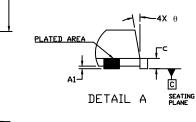


// 0.10 C

|△|0.10|C|

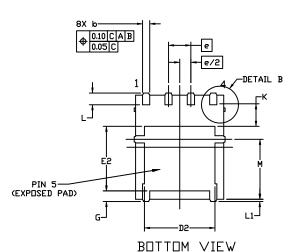


- TES:
  DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  CONTROLLING DIMENSION: MILLIMETERS
  DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR GATE BURRS.
  THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN
  FEATURES TO AID IN FILLET FORMATION ON THE LEADS
  DURING MOUNTING.



SEATING PLANE

	MILLIMETERS		
DIM	MIN.	N□M.	MAX.
Α	0.90	1.00	1.10
A1	0.00		0.05
b	0.33	0.41	0.51
С	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
К	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
М	3.00	3.40	3.80
А	0+		12*



SIDE VIEW



2X 0.4950—
PACKAGE 2X 0.475 3.20  2x 1.53 4.53  2x 0.905 1.33  4x 1.00 1 1.27  4X 0.75 4X 0.75

#### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

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